1 General Description

The AS5045 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.0879° = 4096 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

An internal voltage regulator allows the AS5045 to operate at either 3.3 V or 5 V supplies

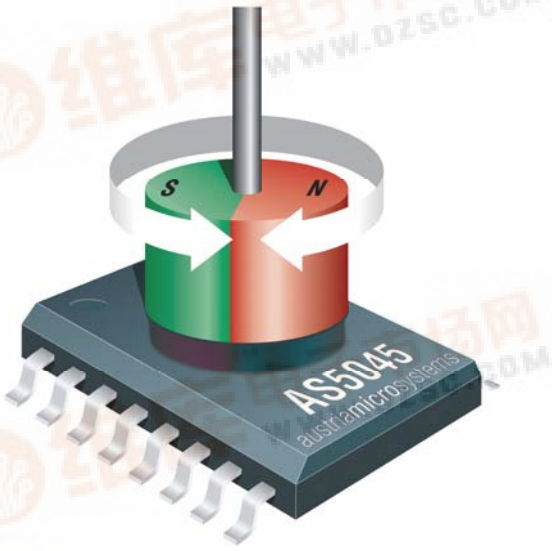


Figure 1: Typical arrangement of AS5045 and magnet

1.1 Benefits

- Complete system-on-chip
- Flexible system solution provides absolute and PWM outputs simultaneously
- Ideal for applications in harsh environments due to contactless position sensing
- No calibration required

1.2 Key Features

- Contactless high resolution rotational position encoding over a full turn of 360 degrees
- Two digital 12bit absolute outputs:
  - Serial interface and
  - Pulse width modulated (PWM) output
- User programmable zero position
- Failure detection mode for magnet placement monitoring and loss of power supply
- "red-yellow-green" indicators display placement of magnet in Z-axis
- Serial read-out of multiple interconnected AS5045 devices using Daisy Chain mode
- Tolerant to magnet misalignment and airgap variations
- Wide temperature range: - 40°C to + 125°C
- Small Pb-free package: SSOP 16 (5.3mm x 6.2mm)

1.3 Applications

- Industrial applications:
  - Contactless rotary position sensing
  - Robotics
- Automotive applications:
  - Steering wheel position sensing
  - Transmission gearbox encoder
  - Headlight position control
  - Torque sensing
  - Valve position sensing
- Replacement of high end potentiometers

2 Pin Configuration

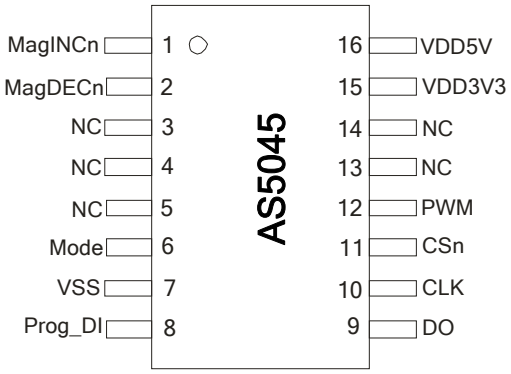


Figure 2: Pin configuration SSOP16

2.1 Pin Description

Table 1 shows the description of each pin of the standard SSOP16 package (Shrink Small Outline Package, 16 leads, body size: 5.3mm x 6.2mmm; see Figure 2).

Pins 7, 15 and 16 are supply pins, pins 3, 4, 5, 6, 13 and 14 are for internal use and must not be connected.

Pins 1 and 2 are the magnetic field change indicators, MagINCn and MagDECn (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range. Furthermore those indicators can also be used for contact-less push-button functionality.

Pin 6 Mode allows switching between filtered (slow) and unfiltered (fast mode). See section 4.

Pin	Symbol	Type	Description
1	MagINCn	DO_OD	Magnet Field Magnitude INCrease; active low, indicates a distance reduction between the magnet and the device surface. See Table 5
2	MagDECn	DO_OD	Magnet Field Magnitude DECrease; active low, indicates a distance increase between the device and the magnet. See Table 5
3	NC	-	Must be left unconnected
4	NC	-	Must be left unconnected
5	NC	-	Must be left unconnected
6	Mode	-	Select between slow (open, low: VSS) and fast (high) mode. Internal pull-down resistor.
7	VSS	S	Negative Supply Voltage (GND)
8	Prog_DI	DI_PD	OTP Programming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Connect to VSS if not used
9	DO	DO_T	Data Output of Synchronous Serial Interface
10	CLK	DI, ST	Clock Input of Synchronous Serial Interface; Schmitt-Trigger input
11	CSn	DI_PU, ST	Chip Select, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
12	PWM	DO	Pulse Width Modulation of approx. 244Hz; 1µs/step (opt. 122Hz; 2µs/step)
13	NC	-	Must be left unconnected
14	NC	-	Must be left unconnected
15	VDD3V3	S	3V-Regulator Output, internally regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V

Table 1: Pin description SSOP16

DO_OD	digital output open drain	S	supply pin
DO	digital output	DI	digital input
DI_PD	digital input pull-down	DO_T	digital output /tri-state
DI_PU	digital input pull-up	ST	Schmitt-Trigger input

Pin 8 (Prog) is used to program the zero-position into the OTP (see chapter 7.1).

This pin is also used as digital input to shift serial data through the device in Daisy Chain configuration, (see page 6).

Pin 11 Chip Select (CSn; active low) selects a device within a network of AS5045 encoders and initiates serial data transfer. A logic high at CSn puts the data output pin (DO) to tri-state and terminates serial data transfer. This pin is also used for alignment mode (Figure 13) and programming mode (Figure 9).

Pin 12 allows a single wire output of the 10-bit absolute position value. The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 4096µs over a full turn). By using an external low pass filter, the digital PWM signal is converted into an analog voltage, making a direct replacement of potentiometers possible.

3 Functional Description

The AS5045 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5045 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate

Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface.

A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 16).

The AS5045 senses the orientation of the magnetic field and calculates a 12-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM). This PWM signal output also allows the generation of a direct proportional analogue voltage, by using an external Low-Pass-Filter.

The AS5045 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

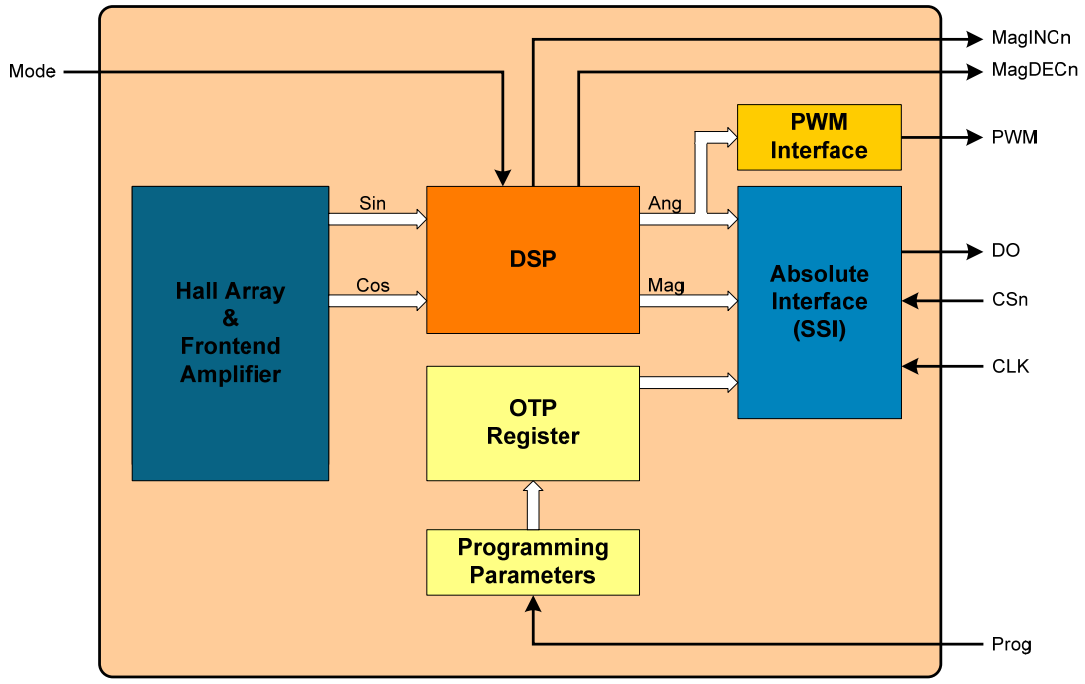


Figure 3: AS5045 block diagram

4 Mode Input Pin

The mode input pin activates or deactivates an internal filter, that is used to reduce the analog output noise.

Activating the filter (Mode pin = LOW or open) provides a reduced output noise of 0.03° rms. At the same time, the output delay is increased to 384µs. This mode is recommended for high precision, low speed applications.

Deactivating the filter (Mode pin = HIGH) reduces the output delay to 96µs and provides an output noise of 0.06° rms. This mode is recommended for higher speed applications.

Switching the Mode pin affects the following parameters:

Parameter	slow mode (Mode = low or open)	fast mode (Mode = high, VDD5V)
sampling rate	2.61 kHz (384 µs)	10.42 kHz (96µs)
transition noise (1 sigma)	≤ 0.03° rms	≤ 0.06° rms
output delay	384µs	96µs
max. speed @ 4096 samples/rev.	38 rpm	153 rpm
max. speed @ 1024 samples/rev.	153 rpm	610 rpm
max. speed @ 256 samples/rev.	610 rpm	2441 rpm
max. speed @ 64 samples/rev.	2441 rpm	9766 rpm

Table 2: Slow and fast mode parameters

4.1 Synchronous Serial Interface (SSI)

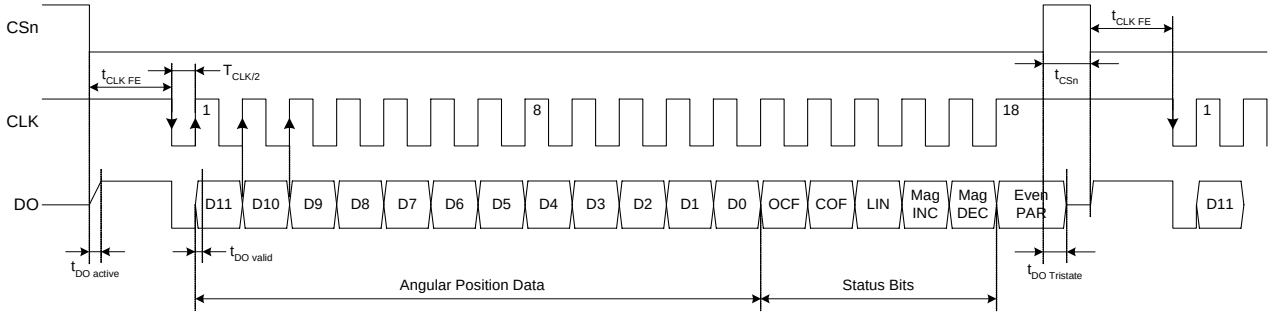


Figure 4: Synchronous serial interface with absolute angular position data

If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK\ FE,}$ data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 18 bits, the first 12 bits are the angular information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease) .
- A subsequent measurement is initiated by a "high" pulse at CSn with a minimum duration of $t_{CSn.}$

4.1.1 Data Content

D11:D0 absolute angular position data (MSB is clocked out first)

OCF (Offset Compensation Finished), logic high indicates the finished Offset Compensation Algorithm

COF (Cordic Overflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value.

This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (Linearity Alarm), logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Even Parity bit for transmission error detection of bits 1...17 (D11...D0, OCF, COF, LIN, MagINC, MagDEC)

Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D11:D0 is valid, when the status bits have the following configurations:

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	even checksum of bits 1:15
			0	1	
			1	0	
			1*)	1*)	

Table 3: Status bit outputs

*) MagInc=MagDec=1 is only recommended in YELLOW mode (see Table 5)

4.1.2 Z-axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5045 provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins #1 and 2) and as status bits in the serial data stream (see Figure 4). Additionally, an OTP programming option is available with bit MagCompEn (see Figure 9) that enables additional features:

In the default state, the status bits MagINC, MagDec and pins MagINCn, MagDECn have the following function:

Status bits		Hardware pins		OTP: Mag CompEn = 0 (default)
Mag INC	Mag DEC	Mag INCn	Mag DECn	Description
0	0	Off	Off	No distance change Magnetic input field OK (in range, ~45…75mT)
0	1	Off	On	Distance increase; pull-function. This state is dynamic and only active while the magnet is moving away from the chip.
1	0	On	Off	Distance decrease; push- function. This state is dynamic and only active while the magnet is moving towards the chip.
1	1	On	On	Magnetic input field invalid – out of recommended range: too large, too small (missing magnet)

Table 4: Magnetic field strength variation indicator

When bit MagCompEn is programmed in the OTP, the function of status bits MagINC, MagDec and pins MagINCn, MagDECn is changed to the following function:

Status bits			Hardware pins		OTP: Mag CompEn = 1 (red-yellow-green programming option)
Mag INC	Mag DEC	LIN	Mag INCn	Mag DECn	Description
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, ~45…75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25…45mT or ~75…135mT. The AS5045 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5045 in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Table 5: Magnetic field strength red-yellow-green indicator (OTP option)

Note: Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Table 4 and Table 5).

4.2 Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5045's in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 5 below). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PROG; pin 8) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is

n * (18+1) bits:

e.g. 38 bit for two devices, 57 bit for three devices, etc...

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D11), etc... (see Figure 6)

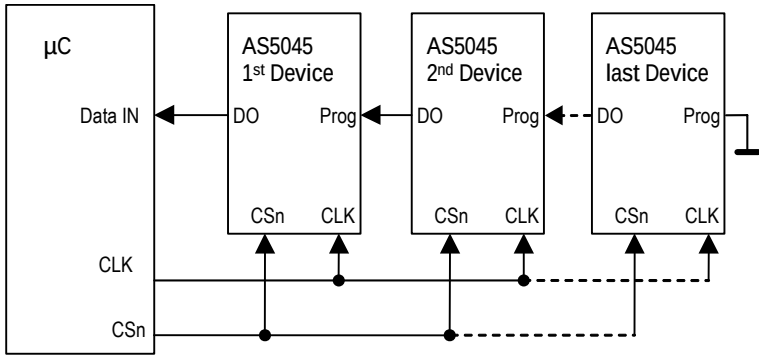


Figure 5: Daisy Chain hardware configuration

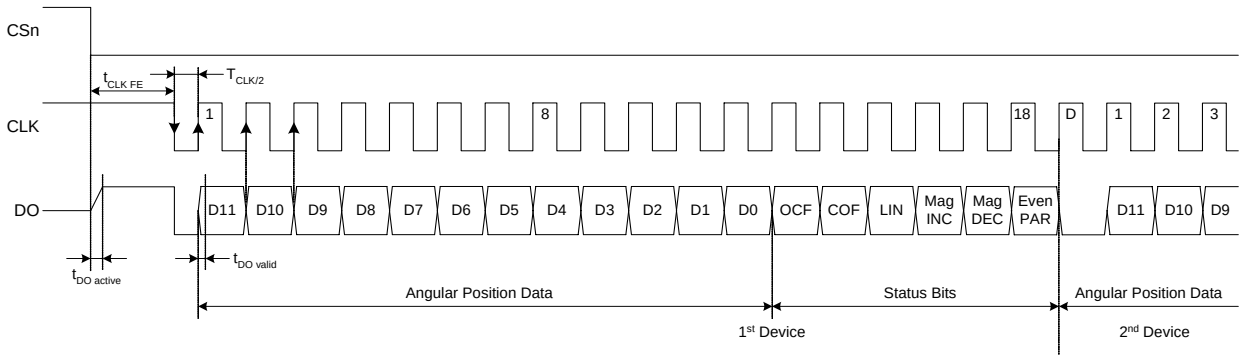


Figure 6: Daisy Chain mode data transfer

5 Pulse Width Modulation (PWM) Output

The AS5045 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle:

$$Position = \frac{t_{on} \cdot 4097}{(t_{on} + t_{off})} - 1$$

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

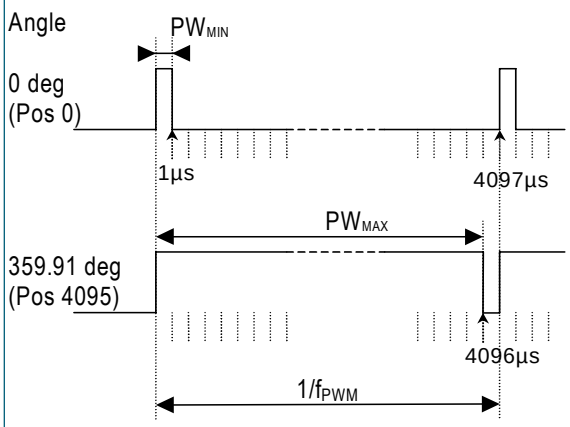


Figure 7: PWM output signal

5.1 Changing the PWM Frequency

The PWM frequency of the AS5045 can be divided by two by setting a bit (PWMhalfEN) in the OTP register (see chapter 7). With PWMhalfEN = 0 the PWM timing is as shown in Table 6:

Parameter	Symbol	Typ	Unit	Note
PWM frequency	f_{PWM}	244	Hz	Signal period: 4097µs
MIN pulse width	PW_{MIN}	1	µs	- Position 0d - Angle 0 deg
MAX pulse width	PW_{MAX}	4096	µs	- Position 4095d - Angle 359,91 deg

Table 6: PWM signal parameters (default mode)

When PWMhalfEN = 1, the PWM timing is as shown in Table 7:

Parameter	Symbol	Typ	Unit	Note
PWM frequency	f_{PWM}	122	Hz	Signal period: 4097µs
MIN pulse width	PW_{MIN}	2	µs	- Position 0d - Angle 0 deg
MAX pulse width	PW_{MAX}	8192	µs	- Position 4095d - Angle 359,91 deg

Table 7: PWM signal parameters with half frequency (OTP option)

6 Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive lowpass filter. The analog output voltage is proportional to the angle: 0°= 0V; 360° = VDD5V.

Using this method, the AS5045 can be used as direct replacement of potentiometers.

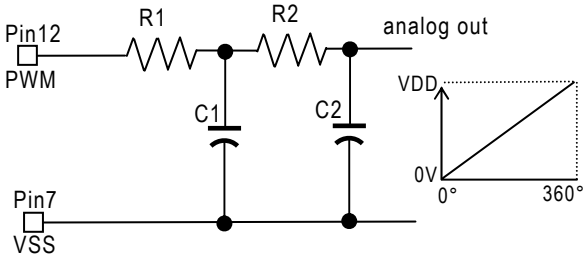


Figure 8: Simple 2nd order passive RC lowpass filter

Figure 8 shows an example of a simple passive lowpass filter to generate the analog output.

R1,R2 ≥ 4k7 C1,C2 ≥ 1µF / 6V

R1 should be ≥4k7 to avoid loading of the PWM output. Larger values of Rx and Cx will provide better filtering and less ripple, but will also slow down the response time.

7 Programming the AS5045

After power-on, programming the AS5045 is enabled with the rising edge of CSn and Prog = logic high. 16 bit configuration data must be serially shifted into the OTP register via the Prog pin. The first “CCW” bit is followed by the zero position data (MSB first) and the Mode setting bits. Data must be valid at the rising edge of CLK (see Figure 9).

After writing the data into the OTP register it can be permanently programmed by rising the Prog pin to the programming voltage V_{PROG}. 16 CLK pulses (t_{PROG}) must be applied to program the fuses (Figure 10). To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

Note: During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the V_{PROG} switching transistor and pin Prog should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins VPROG and VSS. This capacitor is only required for programming, it is not required for normal operation. The clock timing t_{clk} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK (see Figure 9). Additionally, the programming supply voltage should be buffered with a 10µF capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming. The specified programming voltage at pin Prog is 7.3 – 7.5V (see section 15.2).

To compensate for the voltage drop across the V_{PROG} switching transistor, the applied programming voltage may be set slightly higher (7.5 - 8.0V, see Figure 11).

OTP Register Contents:

CCW Counter Clockwise Bit
ccw=0 – angular value increases in clockwise direction
ccw=1 – angular value increases in counterclockwise direction

Z [11:0]:	Programmable Zero Position
PWM dis:	Disable PWM output
MagCompEn:	when set, activates LIN alarm both when magnetic field is too high and too low (see Table 5).
PWMhalfEn:	when set, PWM frequency is 122Hz or 2µs / step (when PWMhalfEN = 0, PWM frequency is 244Hz, 1µs / step)

7.1 Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the “off”-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits Z11:Z0 (see Figure 9) and programmed as described in section 7.

Note: The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180° (half turn) from the mechanical zero position, just add 2048 to the value read at the mechanical zero position and program the new value into the OTP register.

7.2 Repeated OTP Programming

Although a single AS5045 OTP register bit can be programmed only once (from 0 to 1), it is possible to program other, unprogrammed bits in subsequent programming cycles. However, a bit that has already been programmed should not be programmed twice. Therefore it is recommended that bits that are already programmed are set to “0” during a programming cycle.

7.3 Non-permanent Programming

It is also possible to re-configure the AS5045 in a non-permanent way by overwriting the OTP register.

This procedure is essentially a “Write Data” sequence (see Figure 9) without a subsequent OTP programming cycle.

The “Write Data” sequence may be applied at any time during normal operation. This configuration remains set while the power supply voltage is above the power-on reset level (see 14.6).

See Application Note AN5000-20 for further information.

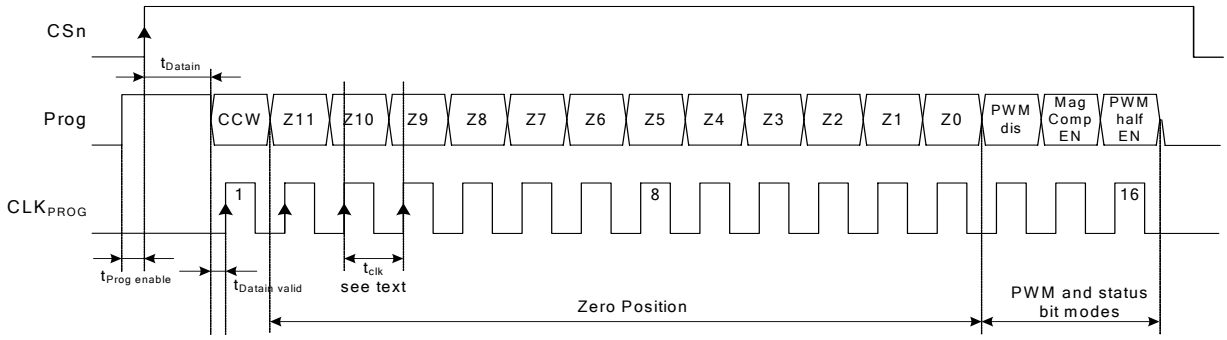


Figure 9: Programming access – write data (section of Figure 10)

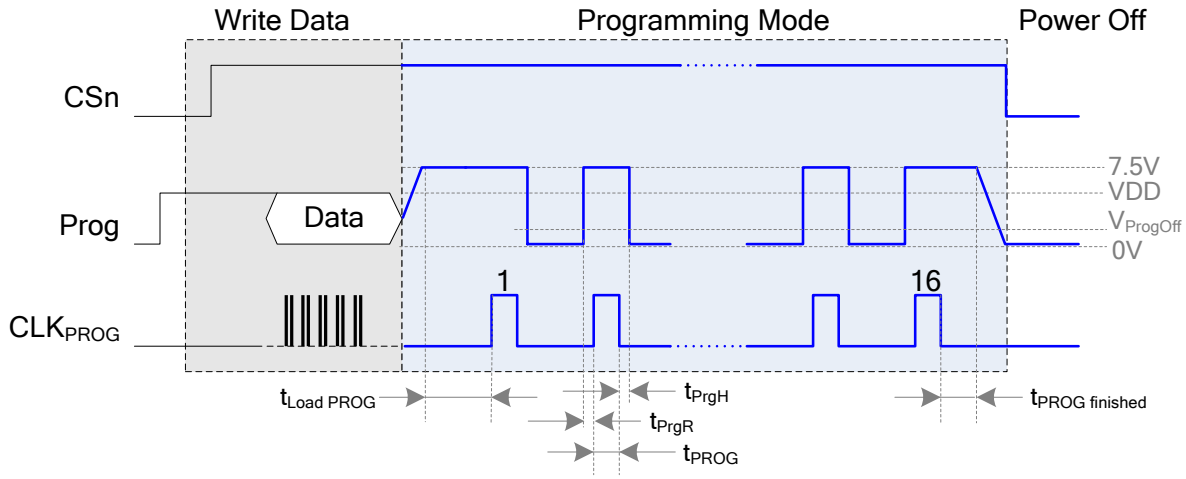


Figure 10: Complete programming sequence

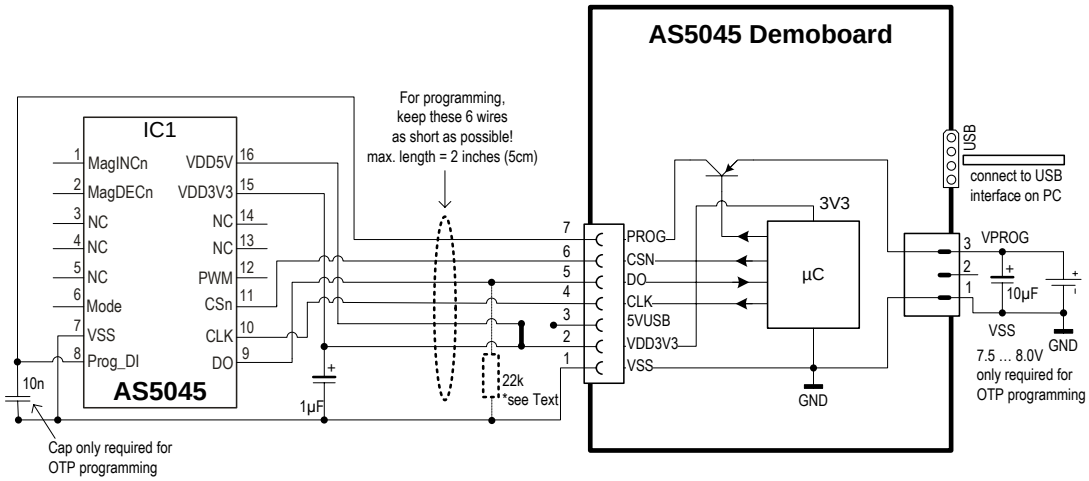


Figure 11: OTP programming connection of AS5045 (shown with AS5045 demoboard)

7.4 Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bit, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5045 in Analog Readback Mode, a digital sequence must be applied to pins CSn, PROG and CLK as shown in Figure 12. The digital level for this pin depends on the supply configuration (3.3V or 5V; see section 0).

The second rising edge on CSn (OutpEN) changes pin PROG to a digital output and the log. high signal at pin PROG must be removed to avoid collision of outputs (grey area in Figure 12).

The following falling slope of CSn changes pin PROG to an analog output, providing a reference voltage V_{ref}, that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits. Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming (see Figure 9: Md0-MD1-Div0,Div1-Indx-Z0...Z11, ccw).

If a capacitor is connected to pin PROG, it should be removed during analog readback mode to allow a fast readout rate. If the capacitor is not removed the analog voltage will take longer to stabilize due to the additional capacitance.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref}, and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up.

Following the 18th clock (after reading bit “ccw”), the chip must be reset by disconnecting the power supply.

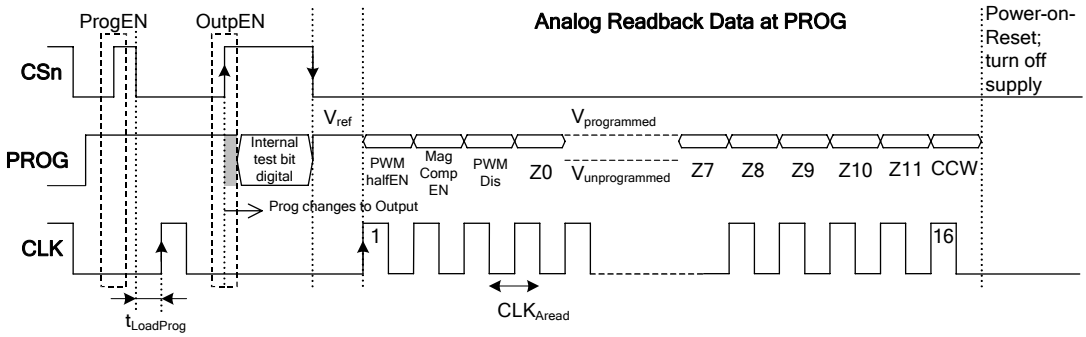


Figure 12: OTP register analog read

8 Alignment Mode

The alignment mode simplifies centering the magnet over the center of the chip to gain maximum accuracy.

Alignment mode can be enabled with the falling edge of CSn while Prog = logic high (Figure 13). The Data bits D9-D0 of the SSI change to a 12-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 128 over a full turn. The MagINCn and MagDECn indicators will be = 1 when the alignment mode reading is < 128. At the same time, both hardware pins MagINCn (#1) and MagDECn (#2) will be pulled to VSS. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360° turn of the magnet.

Stronger magnets or short gaps between magnet and IC may show values larger than 128. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The Alignment mode can be reset to normal operation by a power-on-reset (disconnect / re-connect power supply) or by a falling edge on CSn with Prog = low.

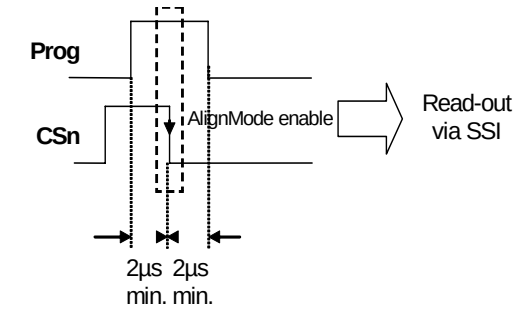


Figure 13: Enabling the alignment mode

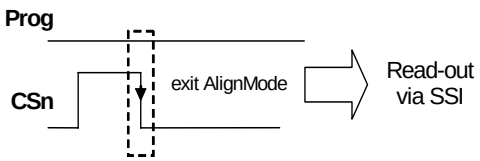


Figure 14: Exiting alignment mode

9 3.3V / 5V Operation

The AS5045 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.

For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 15).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10µF capacitor, which is supposed to be placed close to the supply pin (see Figure 15).

The VDD3V3 output is intended for internal use only It must not be loaded with an external load.

The output voltage of the digital interface I/O's corresponds to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin (see Figure 15).

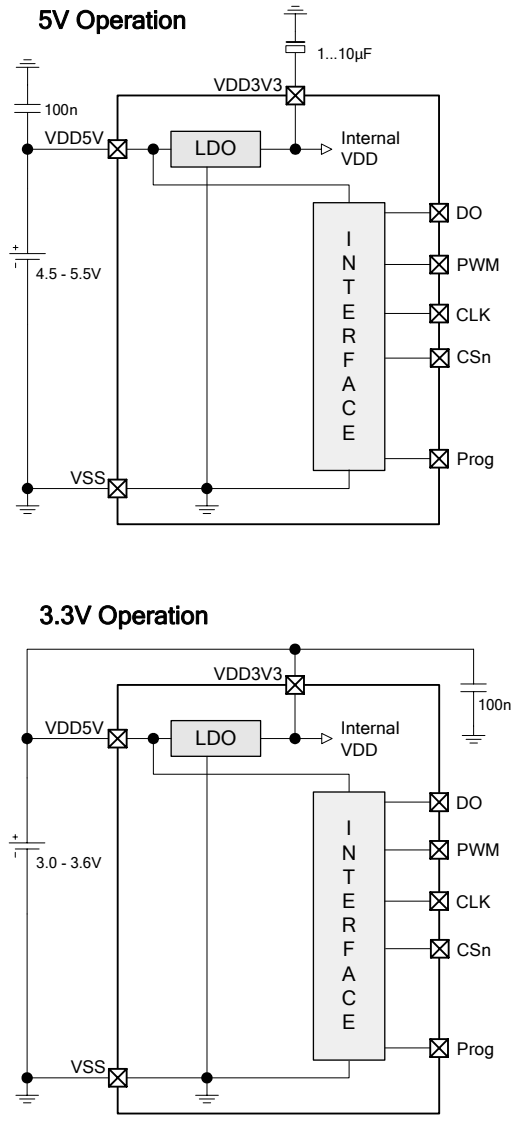


Figure 15: Connections for 5V / 3.3V supply voltages

A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

10 Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo/SmCo5 or NdFeB are recommended.

The magnetic field strength perpendicular to the die surface has to be in the range of ±45mT...±75mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT...±75mT. (see Figure 16).

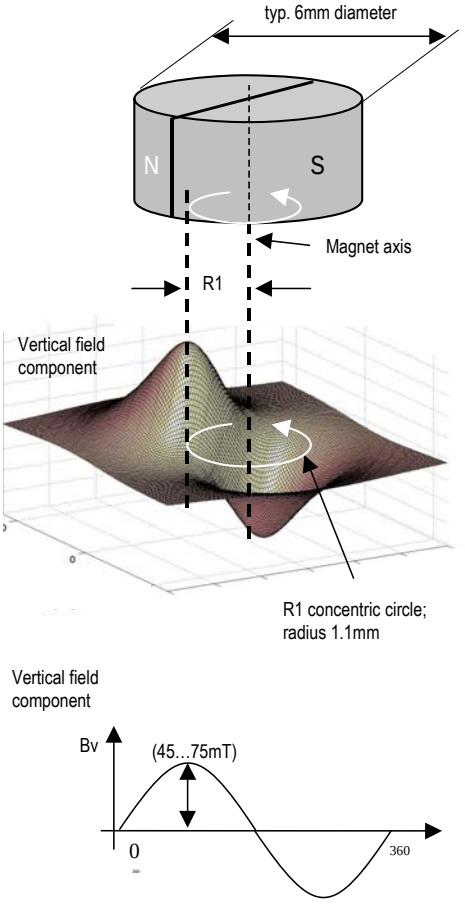


Figure 16: Typical magnet (6x3mm) and magnetic field distribution

10.1 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:

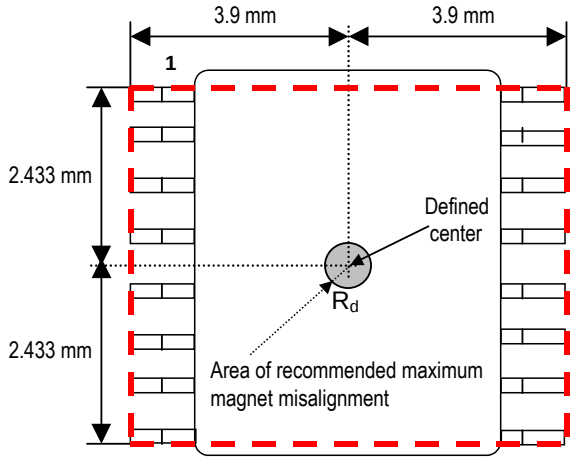


Figure 17: Defined chip center and magnet displacement radius

Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 16). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagINCn (pin 1) and MagDECn (pin 2), see Table 1.

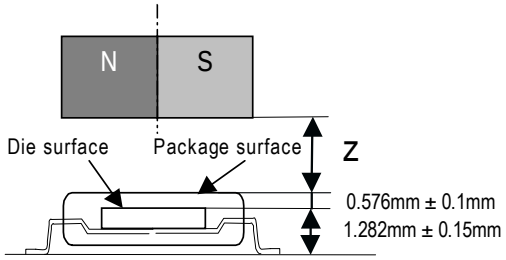


Figure 18: Vertical placement of the magnet

11 Simulation Modeling

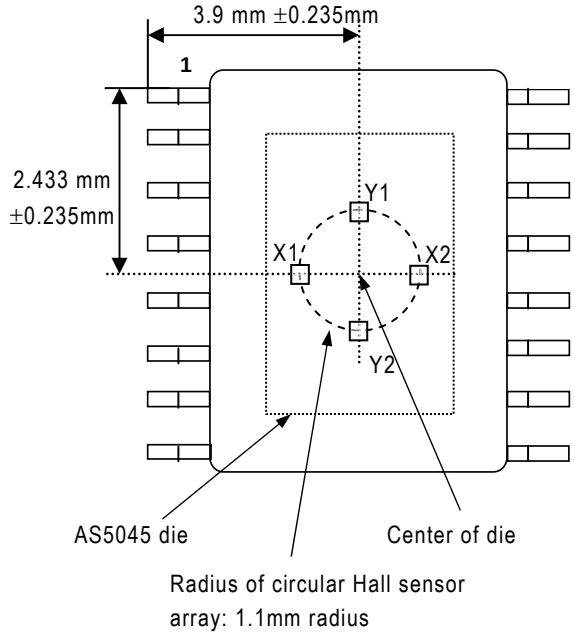


Figure 19: Arrangement of Hall sensor array on chip (principle)

With reference to Figure 19, a diametrically magnetized permanent magnet is placed above or below the surface of the AS5045. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially.

The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field.

The angular displacement (Θ) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$\Theta = \arctan\frac{(Y1-Y2)}{(X1-X2)} \pm 0.5°$$

The ±0.5° angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5045. Placement tolerances of the die within the package are ±0.235mm in X and Y direction, using a reference point of the edge of pin #1 (see Figure 19)

In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented.

The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

The recommended differential input range of the magnetic field strength ($B_{(X1-X2)}$, $B_{(Y1-Y2)}$) is ±75mT at the surface of the die. In addition to this range, an additional offset of ±5mT, caused by unwanted external stray fields is allowed.

The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

12 Failure Diagnostics

The AS5045 also offers several diagnostic and failure detection features:

12.1 Magnetic Field Strength Diagnosis

By software: the MagINC and MagDEC status bits will both be high when the magnetic field is out of range.

By hardware: Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned on (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs are low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

12.2 Power Supply Failure Detection

By software: If the power supply to the AS5045 is interrupted, the digital data read by the SSI will be all “0”s. Data is only valid, when bit OCF is high, hence a data stream with all “0”s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DO and VSS at the receiving side

By hardware: The MagINCn and MagDECn pins are open drain outputs and require external pull-up resistors. In normal operation, these pins are high ohmic and the outputs are high (see Table 5). In a failure case, either when the magnetic field is out of range of the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5045, the pull-up resistors (~10kΩ) from

each pin must be connected to the positive supply at pin 16 (VDD5V).

By hardware: PWM output: The PWM output is a constant stream of pulses with 1kHz repetition frequency. In case of power loss, these pulses are missing

13 Angular Output Tolerances

13.1 Accuracy

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- the non-linearity of the analog-digital converters,
- internal gain and mismatch errors,
- non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = (Err_{max} – Err_{min})/2 is specified as better than ±0.5 degrees @ 25°C (see Figure 21).

Misalignment of the magnet further reduces the accuracy. Figure 20 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

For each misalignment step, the measurement as shown in Figure 21 is repeated and the accuracy (Err_{max} – Err_{min})/2 (e.g. 0.25° in Figure 21) is entered as the Z-axis in the 3D-graph.

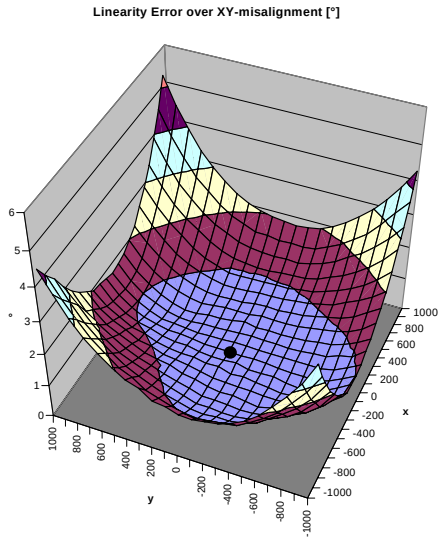


Figure 20: Example of linearity error over XY misalignment

The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees.

The magnet used for this measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

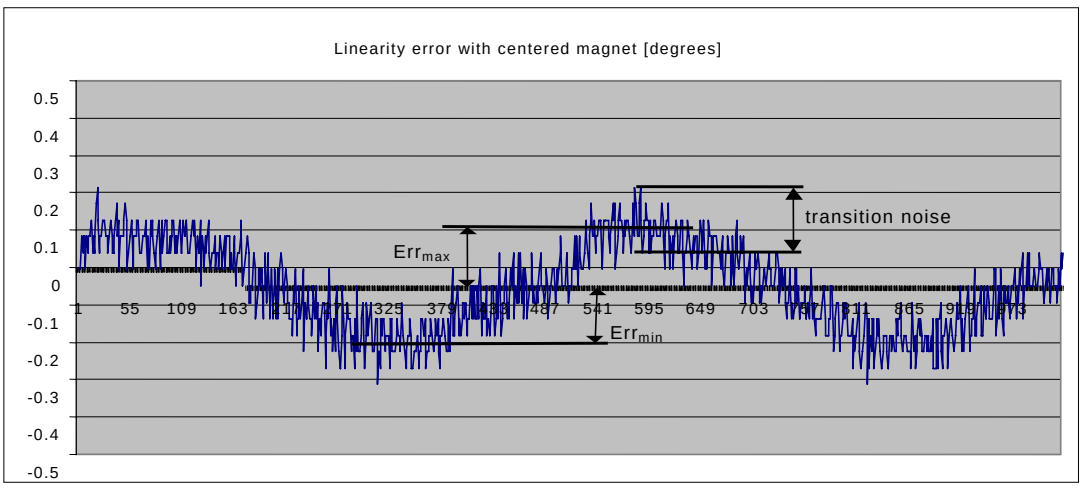


Figure 21: Example of linearity error over 360°

13.2 Transition Noise

Transition noise is defined as the jitter in the transition between two steps.

Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved.

This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)*1 in fast mode (pin MODE = high) and 0.03 degrees rms (1 sigma)*1 in slow mode (pin MODE = low or open).

This is the repeatability of an indicated angle at a given mechanical position.

The transition noise has different implications on the type of output that is used:

- Absolute output; SSI interface:
  The transition noise of the absolute output can be reduced by the user by implementing averaging of readings. An averaging of 4 readings will reduce the transition noise by 6dB or 50%, e.g. from 0.03°rms to 0.015°rms (1 sigma) in slow mode.
- PWM interface:
  If the PWM interface is used as an analog output by adding a low pass filter, the transition noise can be reduced by lowering the cutoff frequency of the filter.
  If the PWM interface is used as a digital interface with a counter at the receiving side, the transition noise may again be reduced by averaging of readings.

**1: statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.*

13.3 High Speed Operation

13.3.1 Sampling Rate

The AS5045 samples the angular value at a rate of 2.61k (slow mode) or 10.42k (fast mode, selectable by pin MODE) samples per second. Consequently, the absolute outputs are updated each 384µs (96µs in fast mode). At a stationary position of the magnet, the sampling rate creates no additional error.

Absolute Mode

At a sampling rate of 2.6kHz/10.4kHz, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by

$$n_{slow\,mode} = \frac{60}{rpm \cdot 384\mu s}$$

$$n_{fast\,mode} = \frac{60}{rpm \cdot 96\mu s}$$

The upper speed limit in slow mode is ~6.000rpm and ~30.000rpm in fast mode. The only restriction at high speed is that there will be fewer samples per revolution as the speed increases (see Table 2).

Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution of 12 bit.

13.4 Propagation Delays

The propagation delay is the delay between the time that the sample is taken until it is converted and available as angular data. This delay is 96µs in fast mode and 384µs in slow mode.

Using the SSI interface for absolute data transmission, an additional delay must be considered, caused by the asynchronous sampling (0 ... $1/f_{sample}$) and the time it takes the external control unit to read and process the angular data from the chip (maximum clock rate = 1MHz, number of bits per reading = 18).

13.4.1 Angular Error Caused by Propagation Delay

A rotating magnet will cause an angular error caused by the output propagation delay.
This error increases linearly with speed:

$$e_{sampling,} = rpm * 6 * prop.delay$$

where
$e_{sampling}$ = angular error [°]
rpm = rotating speed [rpm]
prop.delay = propagation delay [seconds]

Note: since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5045.

13.5 Internal Timing Tolerance

The AS5045 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5045 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to ±5% accuracy at room temperature (±10% over full temperature range). This tolerance influences the ADC sampling rate and the pulse width of the PWM output:

- Absolute output; SSI interface:
  A new angular value is updated every 400µs (typ.)
- PWM output:
  A new angular value is updated every 400µs (typ.).
  The PWM pulse timings T_{on} and T_{off} also have the same tolerance as the internal oscillator (see above).
  If only the PWM pulse width T_{on} is used to measure the angle, the resulting value also has this timing tolerance.
  However, this tolerance can be cancelled by measuring both T_{on} and T_{off} and calculating the angle from the duty cycle (see section 5):

$$Position = \frac{t_{on} \cdot 4097}{(t_{on} + t_{off})} - 1$$

13.6 Temperature

13.6.1 Magnetic Temperature Coefficient

One of the major benefits of the AS5045 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5045 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5045 operates with magnetic field strengths from ±45...±75mT.

Example:
A NdFeB magnet has a field strength of 75mT @ –40°C and a temperature coefficient of -0.12% per Kelvin. The temperature change is from –40° to +125° = 165K.
The magnetic field change is: 165 x -0.12% = -19.8%, which corresponds to
75mT at –40°C and 60mT at 125°C.

The AS5045 can compensate for this temperature related field strength change automatically, no user adjustment is required.

13.7 Accuracy over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is ≤ ±0.5° at room temperature, it may increase to ≤±0.9° due to increasing noise at high temperatures.

13.7.1 Timing Tolerance over Temperature

The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.
The only concern to the user is the width of the PWM output pulse, which relates directly to the timing tolerance of the internal oscillator. This influence however can be cancelled by measuring the complete PWM duty cycle instead of just the PWM pulse (see 13.5).

14 Electrical Characteristics

14.1 AS5045 Differences to AS5040

All parameters are according to AS5040 datasheet except for the parameters shown below:

Building Block	AS5045	AS5040
Resolution	12bits, 0.088°/step.	10bits, 0.35°/step
Data length	read: 18bits (12bits data + 6 bits status) OTP write: 18 bits (12bits zero position + 6 bits mode selection)	read: 16bits (10bits data + 6 bits status) OTP write: 16 bits (10bits zero position + 6 bits mode selection)
incremental encoder	Not used Pin 3: not used Pin 4:not used	quadrature, step/direction and BLDC motor commutation modes Pin 3:incremental output A_LSB_U Pin 4:incremental output B_DIR_V
Pins 1 and 2	MagINCn, MagDECn: same feature as AS5040, additional OTP option for red-yellow-green magnetic range	MagINCn, MagDECn indicate in-range or out-of-range magnetic field plus movement of magnet in z-axis
Pin 6	MODE pin, switch between fast and slow mode	Pin 6:Index output
Pin 12	PWM output: frequency selectable by OTP: 1µs / step, 4096 steps per revolution, f=244Hz 2µs/ step, 4096 steps per revolution, f=122Hz	PWM output: 1µs / step, 1024 steps per revolution, 976Hz PWM frequency
sampling frequency	selectable by MODE input pin: 2.5kHz, 10kHz	fixed at 10kHz @10bit resolution
Propagation delay	384µs (slow mode) 96µs (fast mode)	48µs
Transition noise (rms; 1sigma)	0.03 degrees max. (slow mode) 0.06 degrees max. (fast mode)	0.12 degrees
OTP programming options	zero position, rotational direction, PWM disable, 2 Magnetic Field indicator modes, 2 PWM frequencies	zero position, rotational direction, incremental modes, index bit width

14.2 Absolute Maximum Ratings (non operating)

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage at pin VDD5V	VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3	VDD3V3		5	V	
Input pin voltage	V_{in}	-0.3	VDD5V +0.3	V	Except VDD3V3
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD		± 2	kV	Norm: MIL 883 E method 3015
Storage temperature	T_{strg}	-55	125	°C	Min – 67°F ; Max +257°F
Body temperature (Lead-free package)	T_{Body}		260	°C	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin”
Humidity non-condensing	H	5	85	%	

14.3 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	T_{amb}	-40		125	°C	-40°F…+257°F
Supply current	I_{supp}		16	21	mA	
Supply voltage at pin VDD5V Voltage regulator output voltage at pin VDD3V3	VDD5V VDD3V3	4.5 3.0	5.0 3.3	5.5 3.6	V V	5V Operation
Supply voltage at pin VDD5V Supply voltage at pin VDD3V3	VDD5V VDD3V3	3.0 3.0	3.3 3.3	3.6 3.6	V V	3.3V Operation (pin VDD5V and VDD3V3 connected)

14.4 DC Characteristics for Digital Inputs and Outputs

14.4.1 CMOS Schmitt-Trigger Inputs: CLK, CSn. (CSn = internal Pull-up)

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDD5V		V	Normal operation
Low level input voltage	V_{IL}		0.3 * VDD5V	V	
Schmitt Trigger hysteresis	V_{Ion}- V_{Ioff}	1		V	
Input leakage current	I_{LEAK}	-1	1	µA	CLK only
Pull-up low level input current	I_{iL}	-30	-100	µA	CSn only, VDD5V: 5.0V

14.4.2 CMOS / Program Input: Prog

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDD5V	VDD5V	V	
High level input voltage	V_{PROG}	See "programming conditions"		V	During programming
Low level input voltage	V_{IL}		0.3 * VDD5V	V	
High level input current	I_{iL}	30	100	µA	VDD5V: 5.5V

14.4.3 CMOS Output Open Drain: MagINCn, MagDECn

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA	VDD5V: 4.5V VDD5V: 3V
Open drain leakage current	I_{OZ}		1	µA	

14.4.4 CMOS Output: PWM

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	V_{OH}	VDD5V-0.5		V	
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA mA	VDD5V: 4.5V VDD5V: 3V

14.4.5 Tristate CMOS Output: DO

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	V_{OH}	VDD5V –0.5		V	
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA mA	VDD5V: 4.5V VDD5V: 3V
Tri-state leakage current	I_{OZ}		1	µA	

14.5 Magnetic Input Specification

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Two-pole cylindrical diametrically magnetised source:

Parameter	Symbol	Min	Typ	Max	Unit	Note
Diameter	d_{mag}	4	6		mm	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets
Thickness	t_{mag}	2.5			mm	
Magnetic input field amplitude	B_{pk}	45		75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
Magnetic offset	B_{off}			± 10	mT	Constant magnetic stray field
Field non-linearity				5	%	Including offset gradient
Input frequency (rotational speed of magnet)	f_{mag_abs}			2,44	Hz	146 rpm @ 4096 positions/rev.; fast mode
				0,61		36.6rpm @ 4096 positions/rev.; slow mode
Displacement radius	Disp			0.25	mm	Max. offset between defined device center and magnet axis (see Figure 17)
Eccentricity	Ecc			100	µm	Eccentricity of magnet center to rotational axis
Recommended magnet material and temperature drift			-0.12		%/K	NdFeB (Neodymium Iron Boron)
			-0.035			SmCo (Samarium Cobalt)

14.6 Electrical System Specifications

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution	RES			12	bit	0.088 deg
Integral non-linearity (optimum)	INL_{opt}			± 0.5	deg	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{amb} =25 °C.
Integral non-linearity (optimum)	INL_{temp}			± 0.9	deg	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{amb} = -40 to +125°C
Integral non-linearity	INL			± 1.4	deg	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, T_{amb} = -40 to +125°C
Differential non-linearity	DNL			±0.044	deg	12bit, no missing codes
Transition noise	TN			0.06	Deg RMS	1 sigma, fast mode (MODE = 1)
				0.03		1 sigma, slow mode (MODE=0 or open)
Power-on reset thresholds On voltage; 300mV typ. hysteresis Off voltage; 300mV typ. hysteresis	V_{on} V_{off}	1,37 1.08	2.2 1.9	2.9 2.6	V V	DC supply voltage 3.3V (VDD3V3) DC supply voltage 3.3V (VDD3V3)
Power-up time	t_{PwrUp}			20	ms	Fast mode (Mode = 1); Until status bit OCF = 1
				80		Slow mode (Mode = 0 or open); Until OCF = 1
System propagation delay absolute output : delay of ADC, DSP and absolute interface	t_{delay}			96	µs	Fast mode (MODE=1)
				384		Slow mode (MODE=0 or open)
Internal sampling rate for absolute output:	f_S	2.48	2.61	2.74	kHz	T_{amb} = 25°C, slow mode (MODE=0 or open)
		2.35	2.61	2.87		T_{amb} = -40 to +125°C, slow mode (MODE=0 or open)
Internal sampling rate for absolute output	f_S	9.90	10.42	10.94	kHz	T_{amb} = 25°C, fast mode (MODE = 1)
		9.38	10.42	11.46		T_{amb} = -40 to +125°C, : fast mode (MODE = 1)
Read-out frequency	CLK			1	MHz	Max. clock frequency to read out serial data

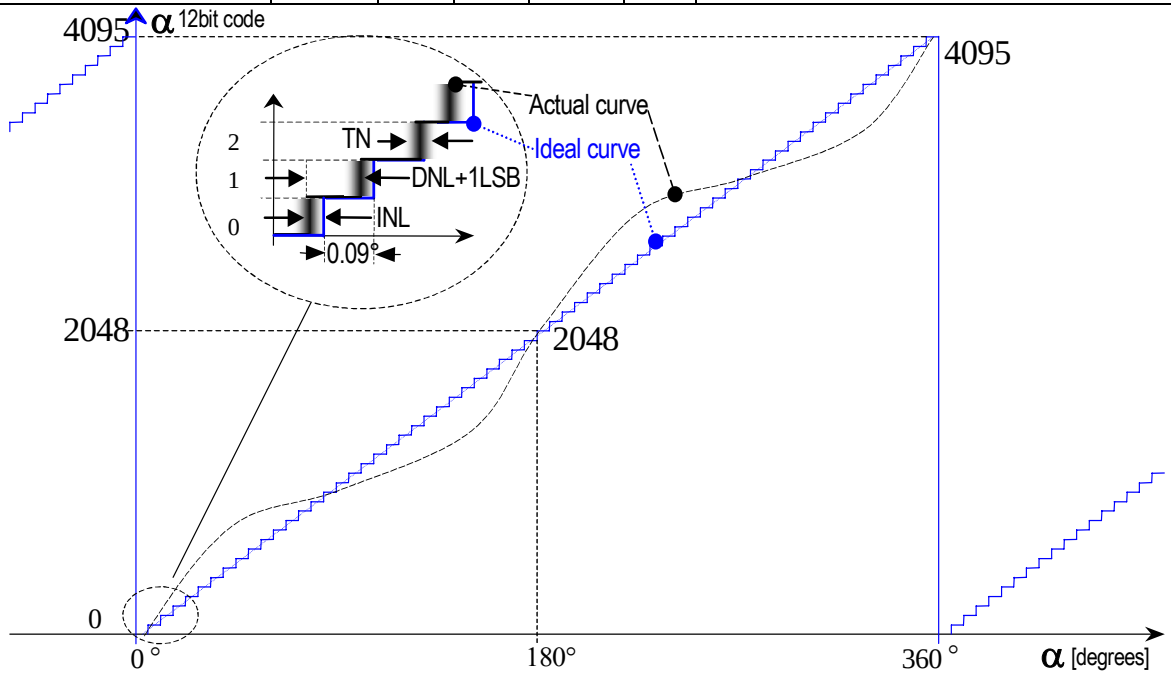


Figure 22: Integral and differential non-linearity (example)

Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position

15 Timing Characteristics

Synchronous Serial Interface (SSI)

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data output activated (logic high)	$t_{DO\ active}$			100	ns	Time between falling edge of CSn and data output activated
First data shifted to output register	$t_{CLK\ FE}$	500			ns	Time between falling edge of CSn and first falling edge of CLK
Start of data output	$T_{CLK\ /\ 2}$	500			ns	Rising edge of CLK shifts out one bit at a time
Data output valid	$t_{DO\ valid}$	357	375	394	ns	Time between rising edge of CLK and data output valid
Data output tristate	$t_{DO\ tristate}$			100	ns	After the last bit DO changes back to “tristate”
Pulse width of CSn	t_{CSn}	500			ns	CSn = high; To initiate read-out of next angular position
Read-out frequency	f_{CLK}	>0		1	MHz	Clock frequency to read out serial data

15.1.1 Pulse Width Modulation Output

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
PWM frequency	f_{PWM}	232	244	256	Hz	Signal period = 4097µs ±5% at T_{amb} = 25°C
		220	244	268		=4097µs ±10% at T_{amb} = -40 to +125°C
Minimum pulse width	PW_{MIN}	0.95	1	1.05	µs	Position 0d; Angle 0 degree
Maximum pulse width	PW_{MAX}	3891	4096	4301	µs	Position 4095d; Angle 359.91 degrees

Note: when OTP bit “PWMhalfEn” is set, the PWM pulse width PW is doubled (PWM frequency f_{PWM} is divided by 2)

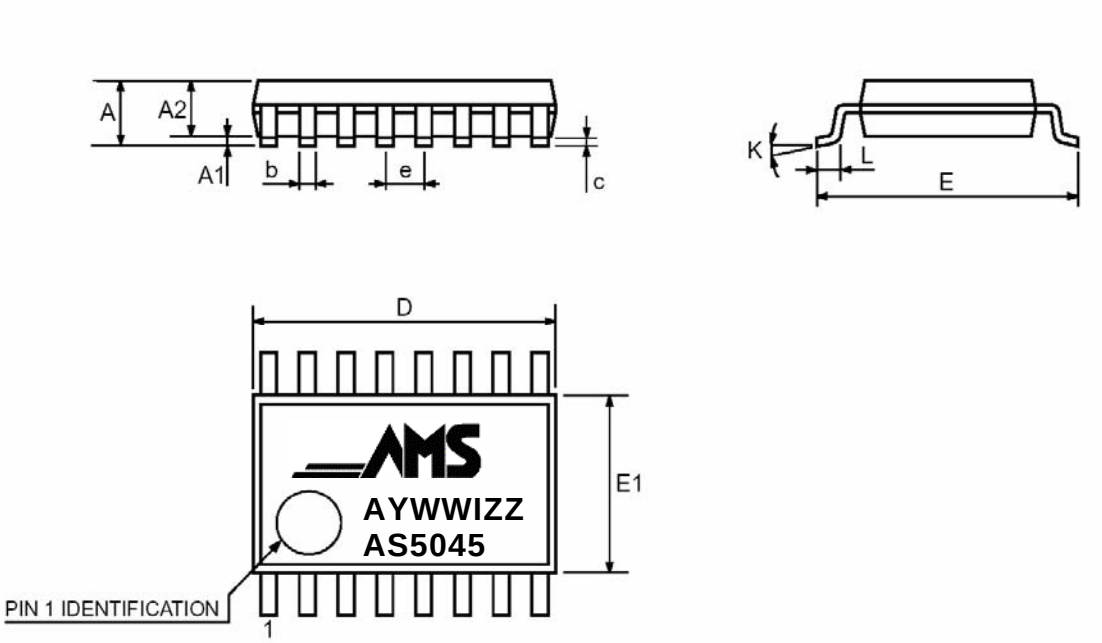
15.2 Programming Conditions

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Programming enable time	$t_{Prog\ enable}$	2			µs	Time between rising edge at Prog pin and rising edge of CSn
Write data start	$t_{Data\ in}$	2			µs	
Write data valid	$t_{Data\ in\ valid}$	250			ns	Write data at the rising edge of CLK_{PROG}
Load Programming data	$t_{Load\ PROG}$	3			µs	
Rise time of V_{PROG} before CLK_{PROG}	t_{PrgR}	0			µs	
Hold time of V_{PROG} after CLK_{PROG}	t_{PrgH}	0		5	µs	
Write data – programming CLK_{PROG}	CLK_{PROG}			250	kHz	ensure that V_{PROG} is stable with rising edge of CLK
CLK pulse width	t_{PROG}	1.8	2	2.2	µs	during programming; 16 clock cycles
Hold time of Vprog after programming	$t_{PROG\ finished}$	2			µs	Programmed data is available after next power-on
Programming voltage, pin PROG	V_{PROG}	7.3	7.4	7.5	V	Must be switched off after zapping
Programming voltage off level	$V_{ProgOff}$	0		1	V	Line must be discharged to this level
Programming current	I_{PROG}			130	mA	during programming
Analog Read CLK	CLK_{Aread}			100	kHz	Analog Readback mode
Programmed Zener Voltage (log.1)	$V_{programmed}$			100	mV	V_{Ref}-V_{PROG} during Analog Readback mode (see 7.4)
Unprogrammed Zener Voltage (log. 0)	$V_{unprogrammed}$	1			V	

16 Package Drawings and Markings

16-Lead Shrink Small Outline Package SSOP-16



Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.73	1.86	1.99	.068	.073	.078
A1	0.05	0.13	0.21	.002	.005	.008
A2	1.68	1.73	1.78	.066	.068	.070
b	0.25	0.315	0.38	.010	.012	.015
c	0.09	-	0.20	.004	-	.008
D	6.07	6.20	6.33	.239	.244	.249
E	7.65	7.8	7.9	.301	.307	.311
E1	5.2	5.3	5.38	.205	.209	.212
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.63	0.75	0.95	.025	.030	.037

Marking: AYWWIZZ

A: Pb-Free Identifier

Y: Last Digit of Manufacturing Year

WW: Manufacturing Week

I: Plant Identifier

ZZ: Traceability Code

JEDEC Package Outline Standard:
MO - 150 AC

Thermal Resistance $R_{th(j-a)}$:
typ. 151 K/W in still air, soldered on PCB

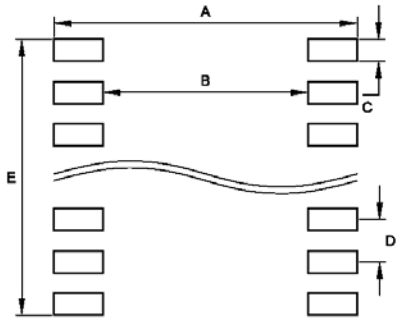
IC's marked with a white dot or the letters "ES" denote Engineering Samples

17 Ordering Information

Delivery: Tape and Reel (1 reel = 2000 devices)
Tubes (1 box = 100 tubes á 77 devices)

Order # AS5045ASSU for delivery in tubes
Order # AS5045ASST for delivery in tape and reel

18 Recommended PCB Footprint:



Recommended Footprint Data		
	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

19 Revision History

Revision	Date	Description
1.2	Oct. 03, 2006	Update description of Alignment Mode (8) and OTP programming (7.2, 7.3), Table 2, I_{supp} (14.3), B_{off} (14.5), $t_{DO\ valid}$ (15), definition of magnet thickness
1.1	Mar. 24, 2006	Added OTP prog. timing table 15.2, New Figure 10, Figure 11
1.0	Dec. 7, 2004 Sep. 26, 2005 Jan. 11, 2006	Initial revision Official release Modify Figure 1, thermal resistance (Package Drawings and Markings)

20 Contact

20.1 Headquarters

austriamicrosystems AG

A 8141 Schloss Premstätten, Austria

Phone: +43 3136 500 0

Fax: +43 3136 525 01

info@austriamicrosystems.com?subject=AS5045

www.austriamicrosystems.com