NEC Electronics Inc.

μPD8257 PROGRAMMABLE DMA CONTROLLER

Description

The μPD8257 is a programmable four-channel direct memory access (DMA) controller. It is designed to simplify high-speed transfers between peripheral devices and memories. Upon a peripheral request, the μPD8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the μPD8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080A. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other μPD8257 devices for systems requiring more than four DMA channels.

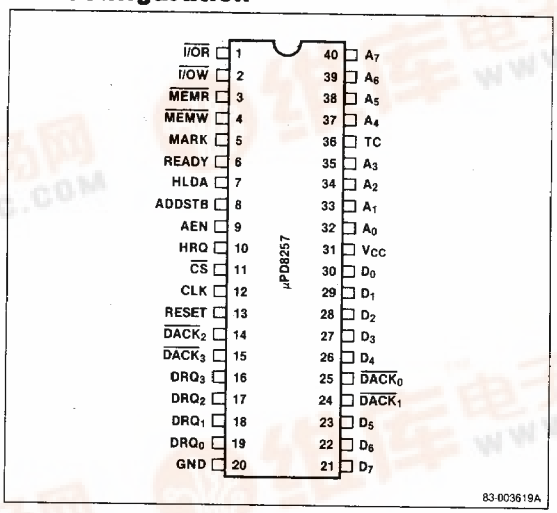
Features

- ☐ Four-channel DMA controller
- ☐ Priority DMA request logic
- ☐ Channel inhibit logic
- ☐ Terminal count and modulo 128 outputs
- ☐ Automatic load mode
- ☐ Single TTL clock
- ☐ Single +5 V ± 10% power supply
- ☐ Expandable
- ☐ Available in extended temperature range

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8257C-2	40-pin plastic DIP	5 MHz
μPD8257C-5	40-pin plastic DIP	3 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{I/OR}$	I/O read, control signal
2	$\overline{I/OW}$	I/O write, control signal
3	$\overline{MEMR}$	Memory read output
4	$\overline{MEMW}$	Memory write output
5	MARK	Modulo 128 mark
6	READY	Ready input
7	HLDA	Hold acknowledge input (from 8080A)
8	ADDSTB	Address strobe output
9	AEN	Address enable output
10	HRQ	Hold request (to 8080A)
11	$\overline{CS}$	Chip select input
12	CLK	Clock input
13	RESET	Reset input
14, 15, 24, 25	$\overline{DACK_2}$, $\overline{DACK_3}$, $\overline{DACK_1}$, $\overline{DACK_0}$	DMA acknowledge output
16-19	DRQ_3-DRQ_0	DMA request input
20	GND	Ground
21-23, 26-30	D_7-D_5, D_4-D_0	I/O data bus
31	V_{CC}	+5 V power supply
32-35	A_0-A_3	I/O address bus
36	TC	Terminal count output
37-40	A_4-A_7	Output address bus

8

Pin Functions

D_0-D_7 (I/O Data Bus)

During an I/O read, the CPU enables these lines as inputs, allowing it to read an address register, a word count register, or the status or temporary register. During an I/O write, these lines are enabled as outputs, allowing the CPU to program the μPD8257-2/-5 control registers. During DMA cycles, the eight MSBs of the address are output to the data bus to be strobed to an external latch via ADDSTB.

A_4-A_7 (Output Address Bus)

These lines, active only during DMA service, are outputs that provide the four MSBs of the address.

A_0-A_3 (I/O Address Bus)

During DMA active states, these lines are outputs that provide the 4 LSBs of the output address bus. During DMA idle states, these lines are inputs, allowing the CPU to load or examine control registers.

DRQ_0-DRQ_3 (DMA Request Input)

These are asynchronous channel request inputs used by peripherals to request DMA service. In a fixed priority scheme, DRQ_0 has the highest priority and DRQ_3 has the lowest. The polarity of these lines is programmable; however, reset initializes them to active high.

HLDA (Hold Acknowledge)

Indicates that the CPU has relinquished control of the system busses.

HRQ (Hold Request)

Requests control of the system bus. The μPD8257-2/-5 issues this signal in response to software requests or DRQ inputs from peripherals.

$\overline{DACK_0}$-$\overline{DACK_3}$ (DMA Acknowledge Output)

These lines indicate an active channel. They are sometimes used to select a peripheral. Only one DACK may be active at any time. All DACK lines are inactive unless DMA has control of the bus. The polarity of these lines is programmable; however, reset initializes them to active low.

TC (Terminal Count)

occurs, TC goes high, infor- ata transfer is complete.

RESET

Clears the command, status, request, and temporary registers, the first/last flip flop, and sets the mask register. The μPD8257-2/-5 is in idle state after a reset.

$\overline{CS}$ (Chip Select)

The CPU uses $\overline{CS}$ to select the μPD8257-2/-5 as an I/O device during an I/O read or write by the CPU. This provides CPU communication on the data bus. $\overline{CS}$ may be held low during multiple transfers to or from the μPD8257-2/-5 as long as $\overline{I/OR}$ or $\overline{I/OW}$ is toggled following each transfer.

READY

This signal can extend memory read and write pulses for slow memories or I/O peripherals.

CLK (Clock)

Controls internal operations and data transfer rate.

AEN (Address Enable)

This signal allows the external latch to output the upper address byte by disabling the system bus during DMA cycles. Use HLDA and AEN to deselect I/O peripherals that may be erroneously accessed during DMA transfers. The μPD8257-2/-5 deselects itself during DMA transfers.

ADDSTB (Address Strobe)

This signal strobes the upper address byte form D_0-D_7 into an external latch.

$\overline{MEMR}$ (Memory Read)

This signal accesses data from a specified memory location during memory-to-peripheral or memory-to-memory transfers.

$\overline{MEMW}$ (Memory Write)

This signal writes data to a specified memory location during peripheral-to-memory or memory-to-memory transfers.

$\overline{I/OR}$ (I/O Read)

In the idle state, this signal is an input control line used by the CPU to read control registers. In the active state, the μPD8257-2/-5 uses I/OR as an output control signal to access data from a peripheral during a DMA write.

$\overline{I/OW}$ (I/O Write)

In the idle state, the CPU uses I/OW as an input control signal to load information to the μPD8257-2/-5. In the active state, the μPD8257-2/-5 uses I/OW as an output control signal to load data to a peripheral during a DMA read.

The rising edge of $\overline{WR}$ must follow each data byte transfer in order for the CPU to write to the μPD8257-2/-5. Holding I/OW low while toggling CS does not produce the same effect.

MARK (Modulo 128 Mark)

This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block.

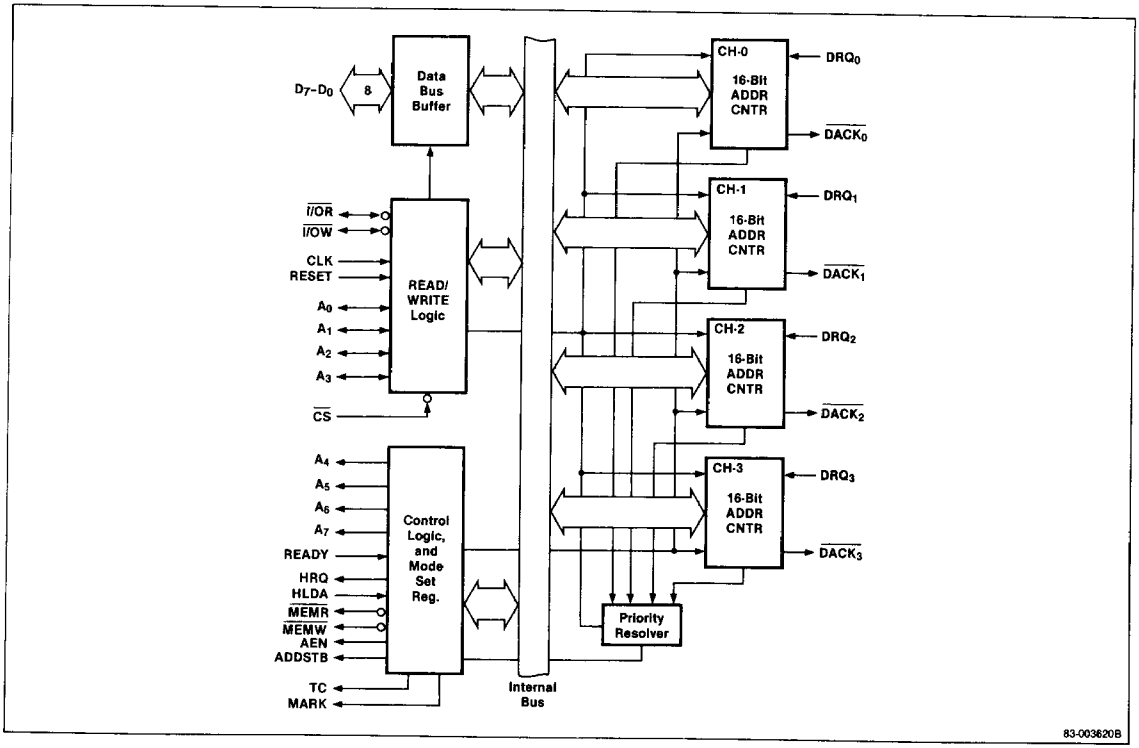
V_{CC}

Power supply.

GND

Ground.

Block Diagram



8

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	0°C to 70°C
Storage temperature, T_{STG}	−65°C to +150°C
Power supply voltage, V_{CC}	−0.5 V to +7 V (1)
Power dissipation	1 Watt

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

(1) With respect to Ground

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ±10% GND = 0 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5	0.8	V	
Input high voltage	V_{IH}	2.0	V_{CC} +0.5	V	
Output low voltage	V_{OL}		0.45	V	I_{OL} = 1.6 mA
Output high voltage	V_{OH}	2.4	V_{CC}	V	I_{OH} = −150 μA for AB, DB and AEN I_{OH} = −80 μA for others
HRQ output high voltage	V_{HH}	3.3	V_{CC}	V	I_{OH} = −80 μA
Power supply current	I_{CC}		100	mA	8257-2
			120	mA	8257-5
Input leakage	I_{IL}	−10	10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output leakage during float	I_{OFL}	−10	10	μA	$0.45 \leq V_{OUT} \leq V_{CC}$

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	f_c = 1 MHz
I/O capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ±10%; GND = 0 V

Parameter	Symbol	Limits μPD8257-2 Min	Limits μPD8257-2 Max	Limits μPD8257-5 Min	Limits μPD8257-5 Max	Unit	Test Conditions
Read							
ADR or $\overline{CS}$↓ Setup to $\overline{RD}$↓	t_{AR}	0				ns	
ADR or $\overline{CS}$ → hold from $\overline{RD}$↑	t_{RA}	0				ns	
Data Access from $\overline{RD}$↓	t_{RDE}	0	140	0	170	ns	C_L = 100 pF
DB → float delay from $\overline{RD}$↑	t_{RDF}	10	85	20	100	ns	C_L = 100 pF
$\overline{RD}$ width	t_{RW}	200		250		ns	
Write							
ADR setup to $\overline{WR}$↓	t_{AW}	20				ns	
ADR hold from $\overline{WR}$↑	t_{WA}	0				ns	
Data setup to $\overline{WR}$↓	t_{DW}	100		200		ns	
Data hold from $\overline{WR}$↑	t_{WD}	0				ns	
$\overline{WR}$ width	t_{WWS}	100		200		ns	
Other timing							
Reset pulse width	t_{RSTW}	300		300		ns	
Power supply ↑(V_{CC}) setup to reset↓	t_{RSTD}	500		500		μs	
Signal rise & fall times	t_r, t_f		20		20		
Reset to first $\overline{IOWR}$	t_{RSTS}	2		2		t_{CY}	

Note:

(1) All timing measurements are made at the following reference voltages unless specified otherwise: input "1" at 2.0 V, "0" at 0.8 V, output "1" at 2.0 V, "0" at 0.8 V.

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ±10%; GND = 0 V

Parameter	Symbol	Limits μPD8257-2 Min	Limits μPD8257-2 Max	Limits μPD8257-5 Min	Limits μPD8257-5 Max	Unit	Test Conditions
Cycle time (period)	t_{CY}	0.200	4	0.320	4	μs	
Clock active (high)	t_θ	80		80	$.8t_{CY}$	ns	
DRQ↑ setup to θ↓ (SI, S4)	t_{QS}	50		120			
DRQ↓ hold from HLDA↑	t_{QH}	0		0			(4)
HRQ↑ or ↓ delay from θ↑ (SI, S4) (measured at 2.0 V)	t_{DQ}		160		160	ns	
HRQ↑ or ↓delay from θ↑ (SI, S4)	t_{HS}		200	100	250	ns	(3)
HLDA↑ or ↓setup to θ↓ (SI, S4)	t_{HS}	50		100		ns	
AEN↑ delay from θ↓ (S1)	t_{AEL}		150		300	ns	
AEN↓ delay from θ↑ (SI)	t_{AET}		150		200	ns	
ADR (AB) (active) delay from AEN↑ (S1)	t_{AEA}	20		20		ns	(4)
ADR (AB) (active) delay from θ↑ (S1)	t_{FAAB}		200		250	ns	(2)
ADR (AB) (float) delay from θ↑ (SI)	t_{AFAB}		150		150	ns	(2)
ADR (AB) (stable) delay from θ↑ (S1)	t_{ASM}		200		250	ns	(2)
ADR (AB) (stable) hold from θ↑ (S1)	t_{AH}	$t_{ASM}-50$		$t_{ASM}-50$			(2)
ADR	t_{AHR}	60		60		ns	(4)

8

AC Characteristics (cont)

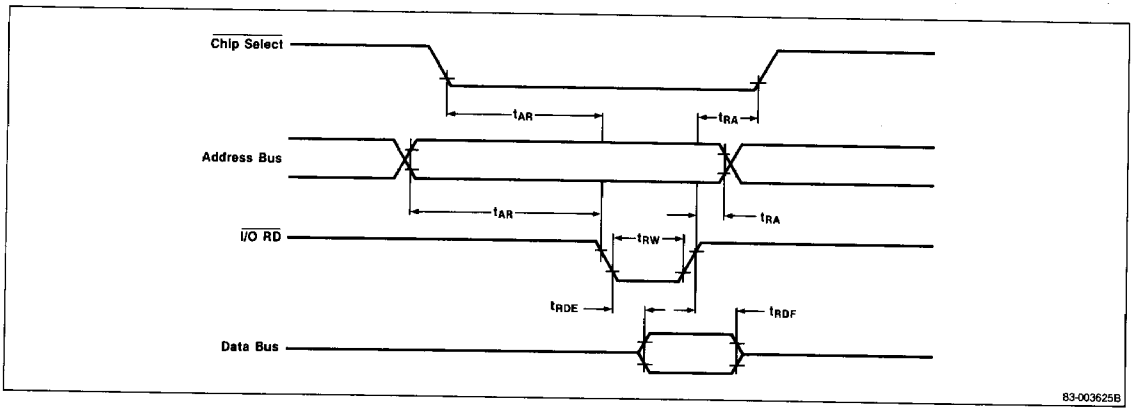
Parameter	Symbol	Limits μPD8257-2 Min	Limits μPD8257-2 Max	Limits μPD8257-5 Min	Limits μPD8257-5 Max	Unit	Test Conditions
ADR (AB) (valid) hold from WR↑ (S1, SI)	t_{AHW}	100		300		ns	(4)
ADR (DB) (active) delay from θ↑ (S1)	t_{FADB}		150		300	ns	(2)
ADR (DB) (float) delay from θ↑ (S2)	t_{AFDB}	t_{STT}	140	$t_{STT}+20$	170	ns	(2)
ADR (DB) setup to ADR STB↓ (S1-S2)	t_{ASS}	100		100		ns	(4)
ADR (DB) (valid) hold from ADR STB↓ (S2)	t_{AHS}	20		50		ns	(4)
ADR STB↑ delay from θ↑ (S1)	t_{STL}		150		200	ns	
ADR STB↓ delay from θ↑ (S2)	t_{STT}		140		140	ns	
ADR STB width (S1-S2)	T_{SW}	$t_{CY}-100$		$t_{CY}-100$		ns	(4)
$\overline{RD}$↓ or $\overline{WR}$ (ext)↓ delay from ADR STB↓ (S2)	t_{ASC}	20		70		ns	(4)
RD↓ or WR (ext)↓ delay from ADR (DB) (float) (S2)	t_{DBC}	0		20		ns	(4)
DACK↑ or ↓delay from θ↓ (S2, S1) and TC/Mark↑ delay from θ↑ (S3) and TC/Mark↓ delay from θ↑ (S4)	t_{AK}		200		250	ns	(5)
$\overline{RD}$↓ or $\overline{WR}$ (ext) ↓ delay from θ↑ (S2) and $\overline{WR}$↓ delay from θ↑ (S3)	t_{DCL}		150		200	ns	(2) (6)
$\overline{RD}$↑ delay from θ↓ (S1, SI) and $\overline{WR}$↑ delay from θ↑ (S4)	t_{DCT}		150		200	ns	(2) (7)
$\overline{RD}$ or $\overline{WR}$ (active) from θ↑ (S1)	t_{FAC}		200		300	ns	(2)
$\overline{RD}$ or $\overline{WR}$ (float) from θ↑ (SI)	t_{AFC}		150		150	ns	(2)
$\overline{RD}$ width (S2-S1 or SI)	T_{RWM}	$2t_{CY}+t_{\theta}-50$		$2t_{CY}+t_{\theta}-50$		ns	(4)
$\overline{WR}$ width (S3-S4)	t_{WWM}	$t_{CY}-50$		$t_{CY}-50$		ns	(4)
$\overline{WR}$ (ext) width (S2-S4)	t_{WWME}	$2t_{CY}-50$		$2t_{CY}-50$		ns	(4)
READY set up time to θ↑ (S3, Sw)	t_{RS}	30		30		ns	
READY hold time from θ↑ (S3, Sw)	t_{RH}	30		30		ns	

Note:

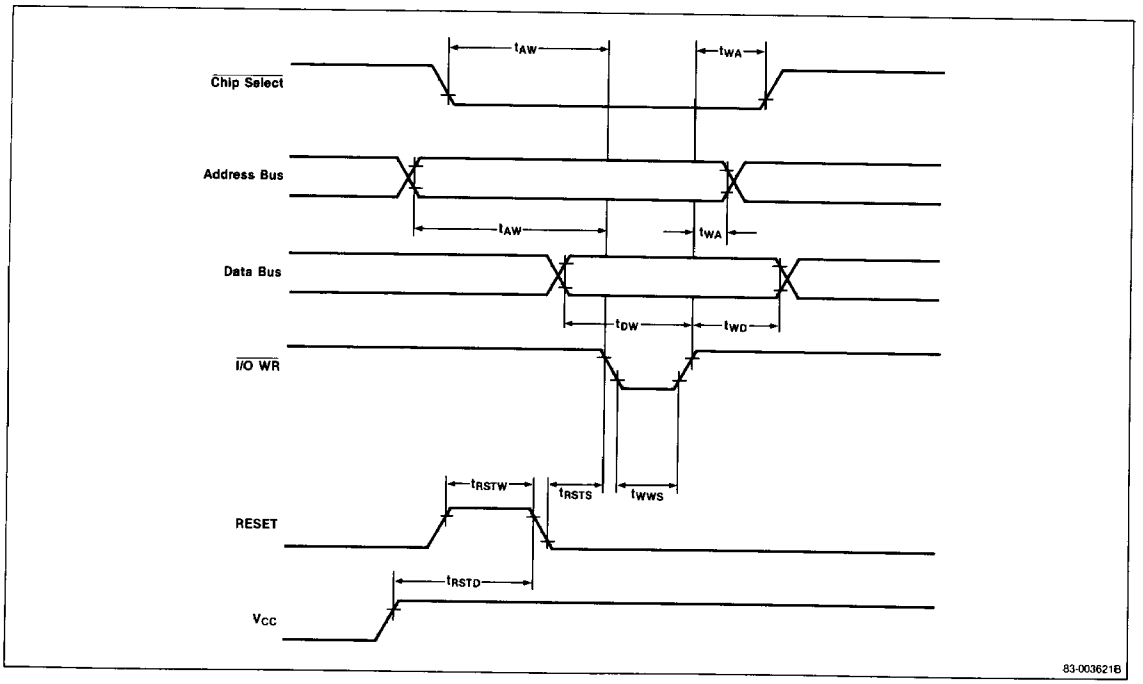
(1) Load = 1 TTL
(2) Load = 50 pF
(3) Load = V_{OH} = 3.3 V
(4) Tracking specification
(5) $\triangle t_{TAK} \leq 50$ ns
(6) $\triangle t_{DCL} \leq 50$ ns
(7) $\triangle t_{DCT} \leq 50$ ns

Timing Waveforms

Read Timing

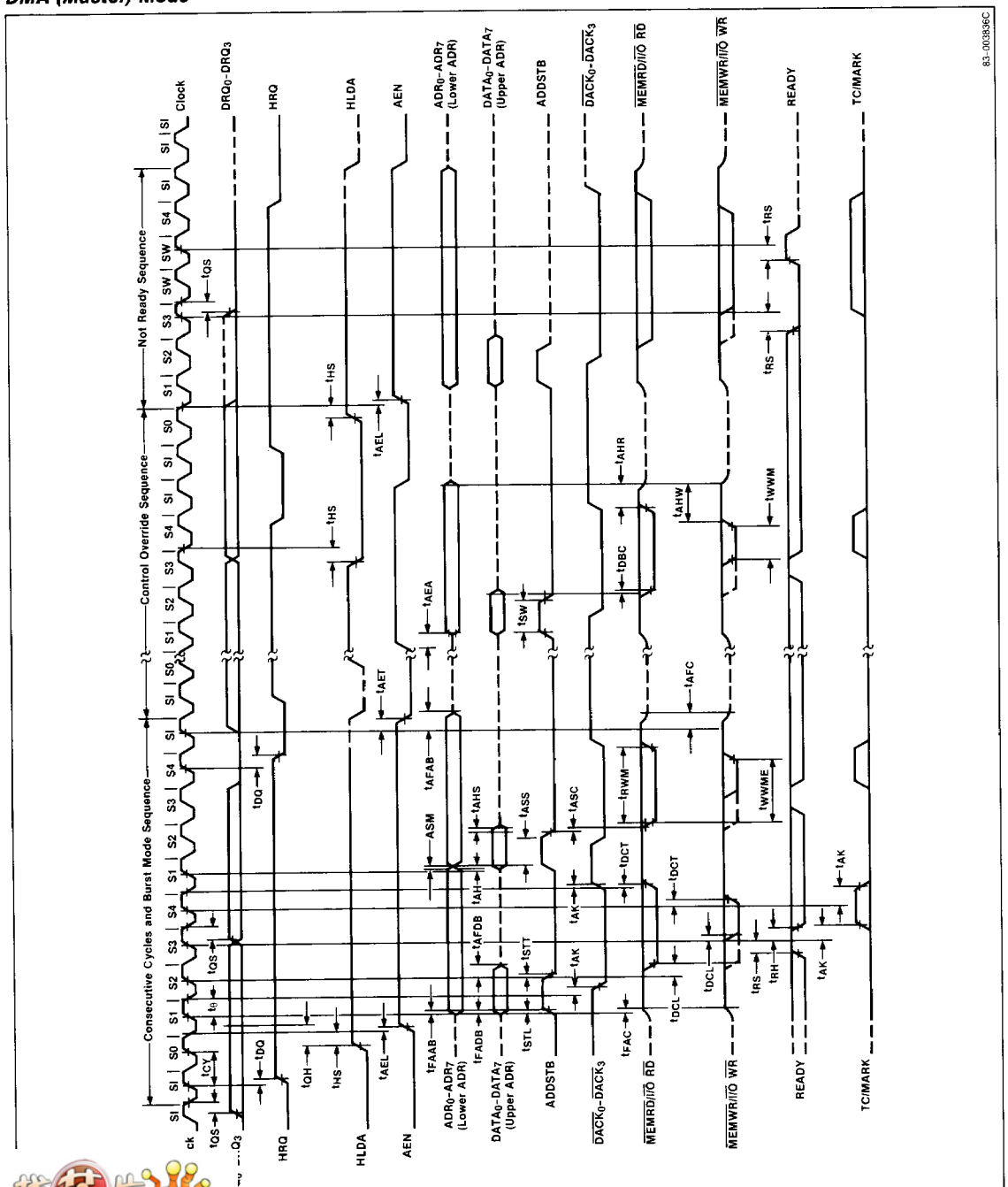


Write/Reset Timing



Timing Waveforms (cont)

DMA (Master) Mode



Functional Description

The μPD8257 is a programmable, direct memory Access (DMA) device. When used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080A/8085A based systems. Once initialized by an 8080A/8085A CPU, the μPD8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU. It will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occurs within the μPD8257.

(1) It acquires control of the system bus (placing 8080A/8085A in hold mode).

(2) Resolves priority conflicts if multiple DMA requests are made.

(3) A 16-bit memory address word is generated with the aid of an 8212 in the following manner:

  (a) The μPD8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  (b) The μPD8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.

(4) The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA request (DRQ_n). The μPD8257 retains control of the system bus as long as DRQ_n remains high or until the terminal count (TC) is reached. When the terminal count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

(1) DMA read, which causes data to be transferred from memory to a peripheral;

(2) DMA write, which causes data to be transferred from a peripheral to memory; and

(3) DMA verify, which does not actually involve the transfer of data.

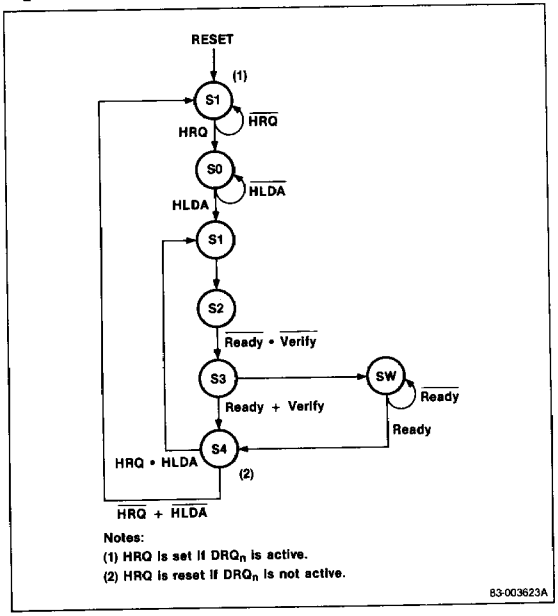
The DMA read and write modes are the normal operating conditions for the μPD8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (cycle redundancy code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

DMA Operation

As shown in figure 1, internally the μPD8257 contains six different states (S0, S1, S2, S3, S4 and SW). The duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA requests (DRQ_n). Then the μPD8257 enters the S0 state, during which a hold request (HRQ) is sent to the 8080A/8085A and the μPD8257 waits in S0 until the 8080A/8085A issues a hold acknowledge (HLDA) back. During S0, DMA requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme).

After receipt of HLDA, the DMA acknowledge line ($DACK_n$) with the highest priority is driven low, selecting that particular peripheral for the DMA cycle. The DMA request line (DRQ_n) must remain high until either a DMA acknowledge ($DACK_n$) or both $DACK_n$ and TC (terminal count) occur, indicating the end of a block or sector transfer (burst model).

Figure 1. DMA Operation State Diagram



The DMA cycle consists of four internal states; S1, S2, S3, and S4. If the access time of the memory or I/O device is not fast enough to return a ready command to the μPD8257 after it reaches state S3, then a wait state is initiated (SW). One or more than one wait state occurs until a ready signal is received, and the μPD8257 is allowed to go into state S4. Either the extended write option or the DMA verify mode may eliminate any wait state.

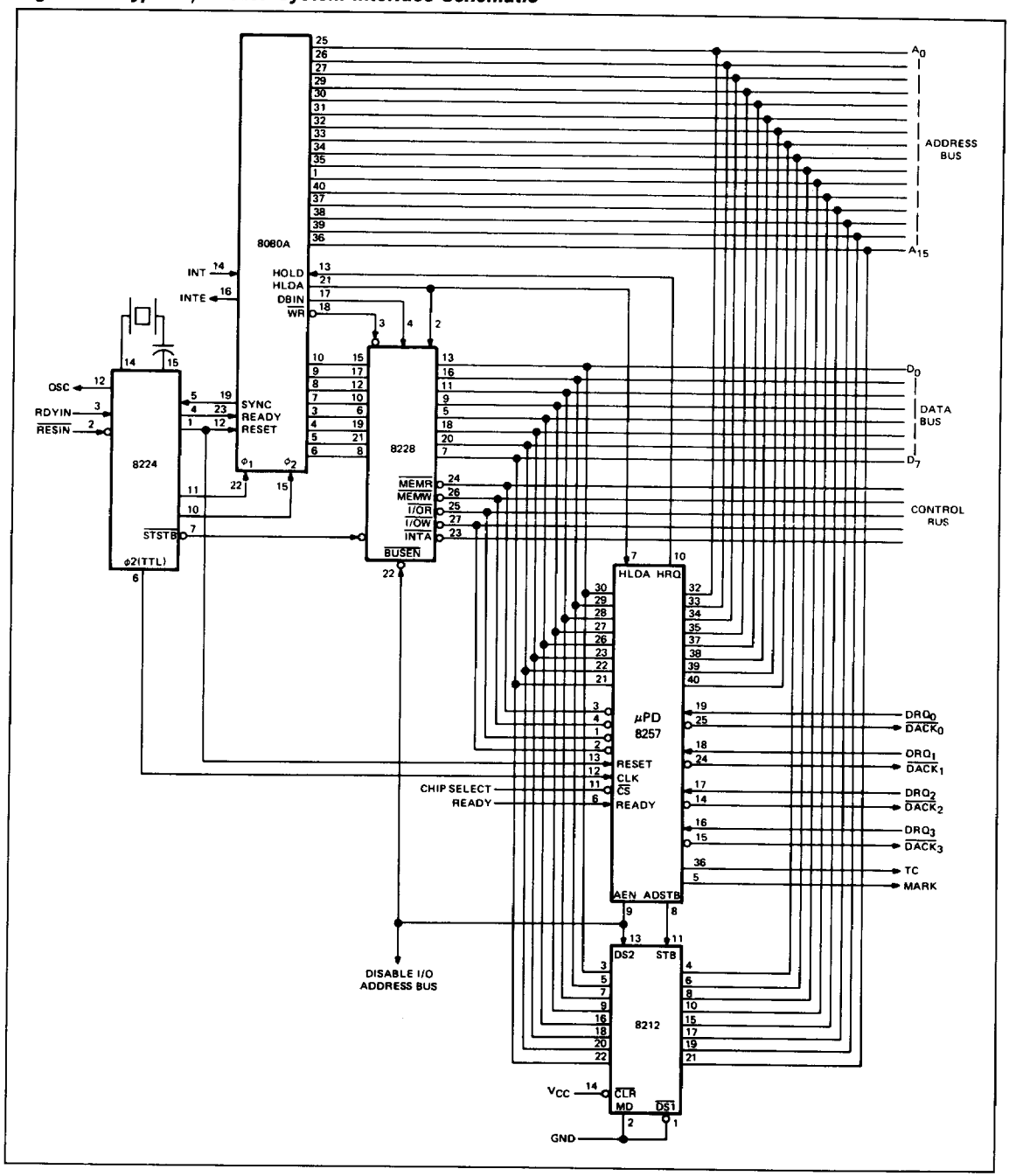
If the μPD8257 should lose control of the system bus, (i.e., HLDA goes low) then the current DMA cycle is completed; the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}), and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the μPD8257 and the 8080A/8085A.

During DMA write cycles, the I/O Read (I/O R) output is generated at the beginning of state S2 and the memory write (MEMW) output is generated at the beginning of S3. During DMA read cycles, the memory read (MEMR) output is generated at the beginning of state S2 and the I/O write (I/O W) goes low at the beginning of state S3. No read or write control signals are generated during DMA verify cycles.

System Interface

Figure 2 is the schematic diagram of a μPD8257 system interface with the 8080A CPU, 8212 I/O Port, 8224 Clock Generator, and 8228 System Controller and Bus Driver.

Figure 2. Typical μPD8257 System Interface Schematic



8