



### Description

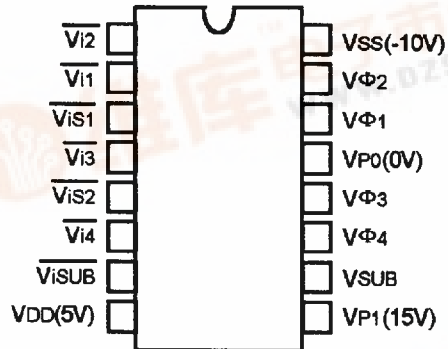
The GCD1001S is a clock driver for the vertical resistor drive of CCD.

GCD1001S is well suited for the B/W or color CCD camera/camcorder in NTSC or PAL system.

### Feature

- 4 channel vertical clock driver and 1 channel substrate driver.
- Implemented with high voltage(50V) and high performance CMOS process.

### Pin Configuration



16SSOP

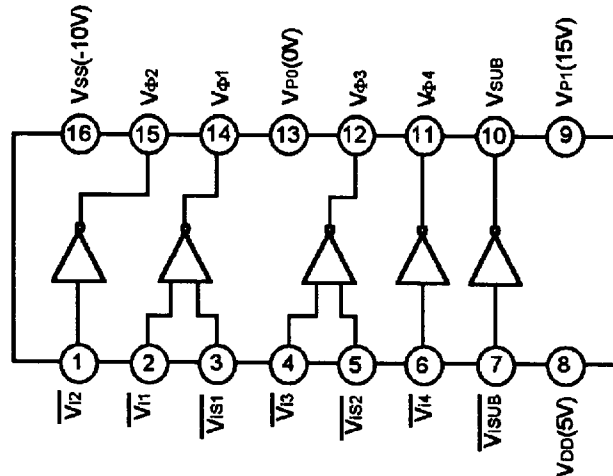
### Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>SS</sub>	Reference voltage	V
	V <sub>DD</sub> , V <sub>PO</sub> , V <sub>P1</sub>	V <sub>SS</sub> -0.3 to V <sub>SS</sub> +35	V
Input voltage	V <sub>I</sub>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O2</sub> , V <sub>O4</sub>	V <sub>SS</sub> -0.3 to V <sub>PO</sub> +0.3	V
	V <sub>O1</sub> , T <sub>O3</sub> , T <sub>Sub</sub>	V <sub>SS</sub> -0.3 to V <sub>P1</sub> +0.3	V
Operating temperature	T <sub>OPR</sub>	-25 to +85	°C
Storage temperature	T <sub>STG</sub>	-40 to +125	°C

### Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> +15	V
	V <sub>PO</sub>	V <sub>SS</sub> +10	V
	V <sub>P1</sub>	V <sub>SS</sub> +25	V
Operating temperature	T <sub>OPR</sub>	-20 to +75	°C



**Block Diagram and Pin Configuration (Top View)**

**Truth Table**

Input				Output		
$\overline{Vi1,3}$	$\overline{ViS1,2}$	$\overline{Vi2,4}$	$\overline{ViSub}$	V01,3	V02,4	Vsub
L L H H	L H L H			VP1 VP0 *Z VSS		
		L H			VP0 VSS	
			L H			VP1 VSS

\*Z is high impedance.

**DC Characteristics** ( $T_A=25^\circ\text{C}$ ,  $V_{DD}=5\text{V}$ ,  $V_{SS}=-10\text{V}$ ,  $V_{P0}=0\text{V}$ ,  $V_{P1}=15\text{V}$ )

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Input high voltage	$V_{IP1}$		3.5			V
Input low voltage	$V_{ISS}$				1.5	V
Output high voltage	$V_{\phi P1}$	$I_{\phi P1} = -20 \mu\text{A}$	14.9	15		V
Output middle voltage	$V_{\phi P0}$	$I_{\phi P0} = -20 \mu\text{A}$		0	0.1	V
Output middle voltage	$V_{\phi P0}$	$I_{\phi P0} = 20 \mu\text{A}$	-0.1	0		V
Output low voltage	$V_{\phi SS}$	$I_{\phi SS} = 20 \mu\text{A}$		-10	-9.9	V
Input current	$I_{IN}$			1.0		$\mu\text{A}$
Power supply current	$I_{P0}$			0.3	0.5	mA
Power supply current	$I_{P1}$			0.15	0.3	mA
Power supply current	$I_{P0}$			4.5	5.0	mA



**Pin Description**

No.	Symbol	I/O	Description
1	$\overline{Vi2}$	I	Output control (V02)
2	$\overline{Vi1}$	I	Output control (V01)
3	$\overline{Vis1}$	I	Output control (V01)
4	$\overline{Vi3}$	I	Output control (V03)
5	$\overline{Vis2}$	I	Output control (V03)
6	$\overline{Vi4}$	I	Output control (V04)
7	$\overline{VisUB}$	I	Output control (VSub)
8	VDD	-	Power supply (5V)
9	VP1	-	Power supply (15V)
10	VSUB	O	Output (2 level : VP1, VSS)
11	V $\phi$ 4	O	Output (2 level : VP0, VSS)
12	V $\phi$ 3	O	Output (3 level : VP1, VP0, VSS)
13	VP0	-	Power supply (0V)
14	V $\phi$ 1	O	Output (3 level : VP1, VP0, VSS)
15	V $\phi$ 2	O	Output (2 level : VP0, VSS)
16	VSS	-	Power supply (-10V)

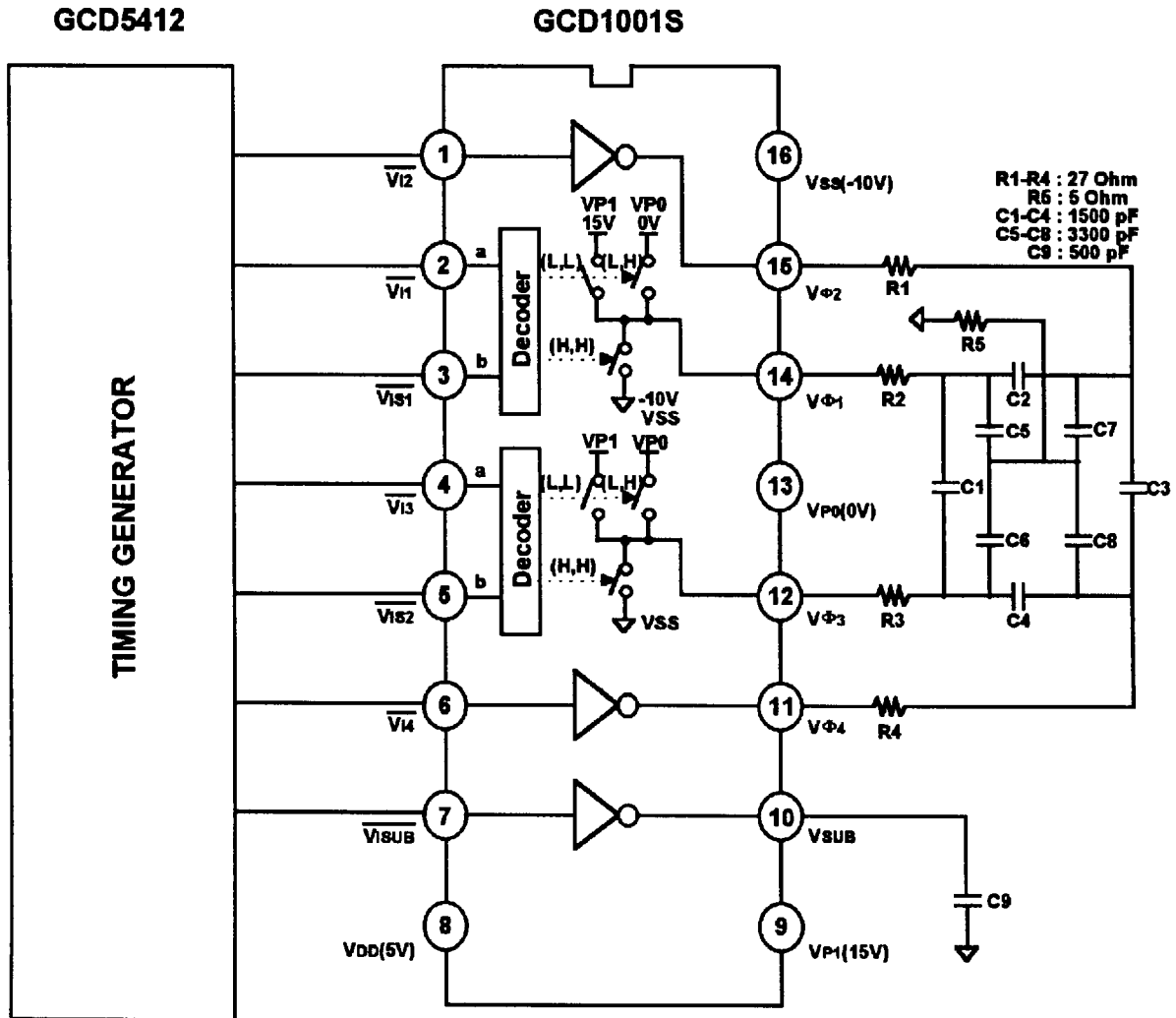
**Switching Characteristics**

(See the Test Circuit  $T_A = 25^\circ\text{C}$ ,  $VP1=15\text{V}$ ,  $VP0=0\text{V}$ ,  $V_{DD}=5\text{V}$ ,  $V_{SS}=-10\text{V}$ )

Item	Symbol	Conditions	Max.	Min.	Unit
Output Current	$I_L$	V01 to 4 = -9.5V	-25		mA
Output Current	$I_{M1}$	V01 to 4 = -0.5V		10	mA
Output Current	$I_{M2}$	V01, 3 = 0.5V	-9		mA
Output Current	$I_H$	V01, 3 = 14.5V		12	mA
Output Current	$I_{SL}$	VSub = -9.5V	-12		mA
Output Current	I	VSub = 14.5V		12	mA
Rise time VSS $\rightarrow$ VP0	$T_{TLM}$	V01 to 4 = -0.5V After input transient	1000		ns
Fall time VP0 $\rightarrow$ VSS	$T_{TML}$	V01, 3 = -9.5V After input transient	1000		ns
Rise time VP0 $\rightarrow$ VP1	$T_{TMH}$	V01, 3 = 14V After input transient	1000		ns
Fall time VP1 $\rightarrow$ VP0	$T_{THM}$	V01, 3 = 1V After input transient	1000		ns
Rise time VP0 $\rightarrow$ VP1	$T_{TLHH}$	VSub = 14V	200		ns
Fall time VP1 $\rightarrow$ VSS	$T_{THHL}$	VSub = -9.5V	200		ns
Coupling amplitude (middle level)	$V_{COM}$	V01 to 4	0.5		V
Coupling amplitude (low level)	$V_{COL}$	V01 to 4	0.5		V



Test Circuit

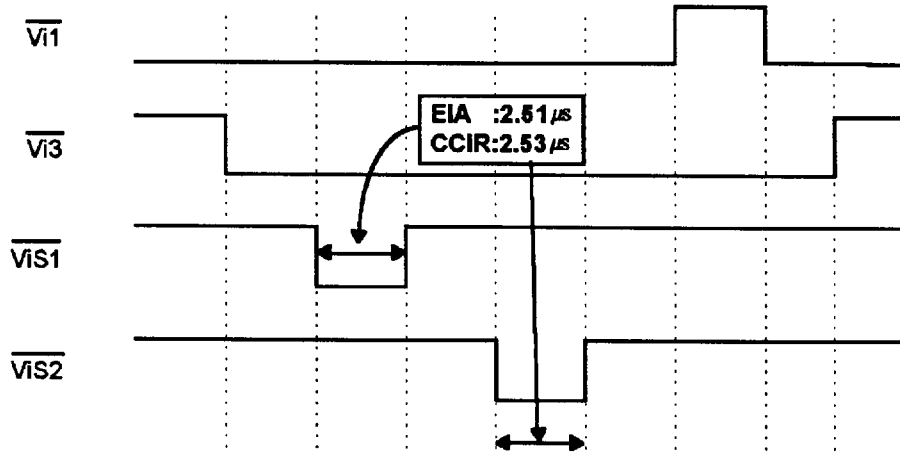


\*(L, H) means the on-status of the switch when a = "L", b = "H".

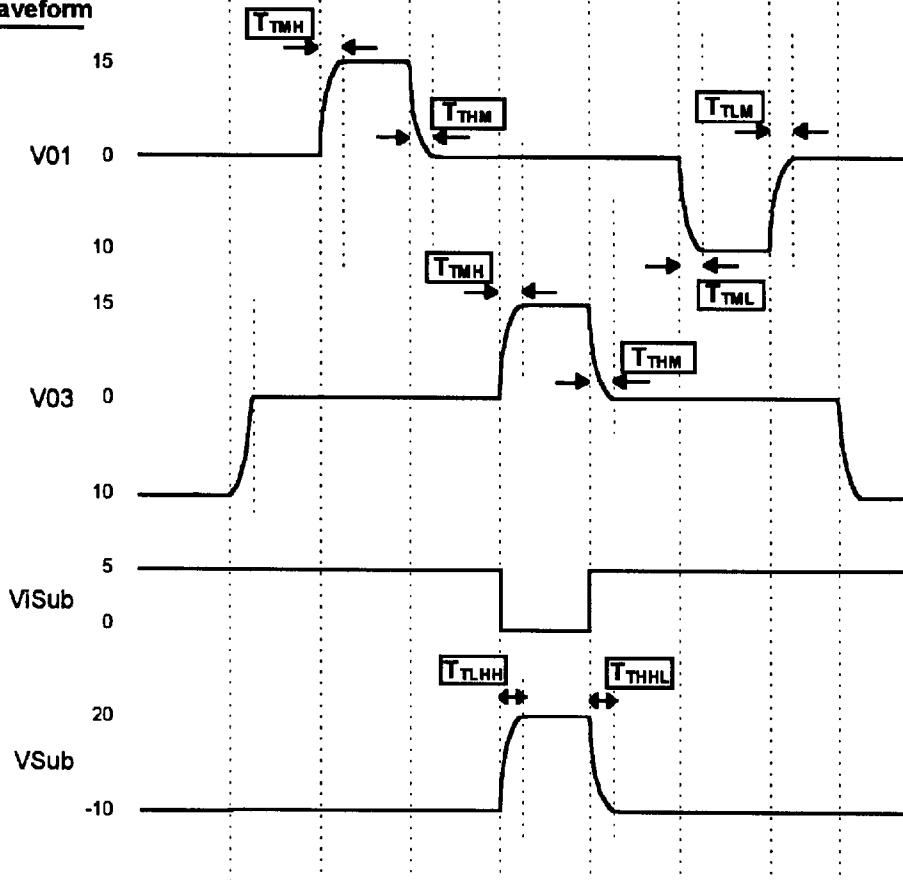


Test Circuit I/O Waveform Diagram

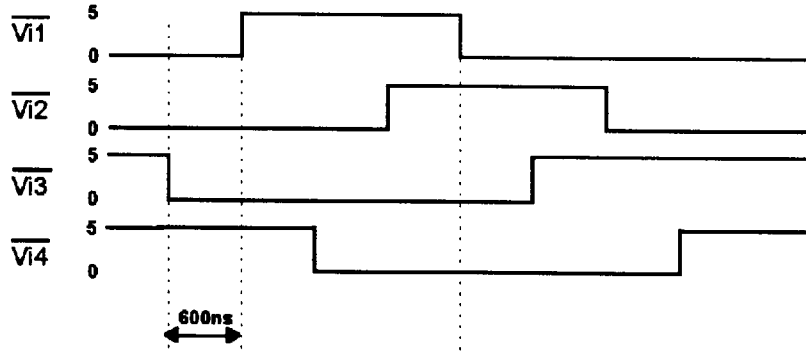
Input waveform



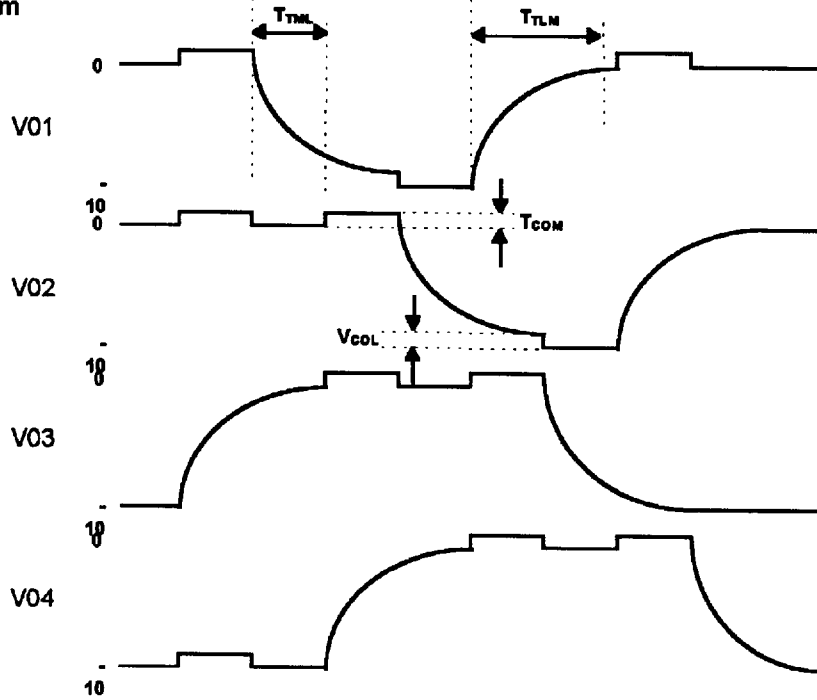
Output waveform



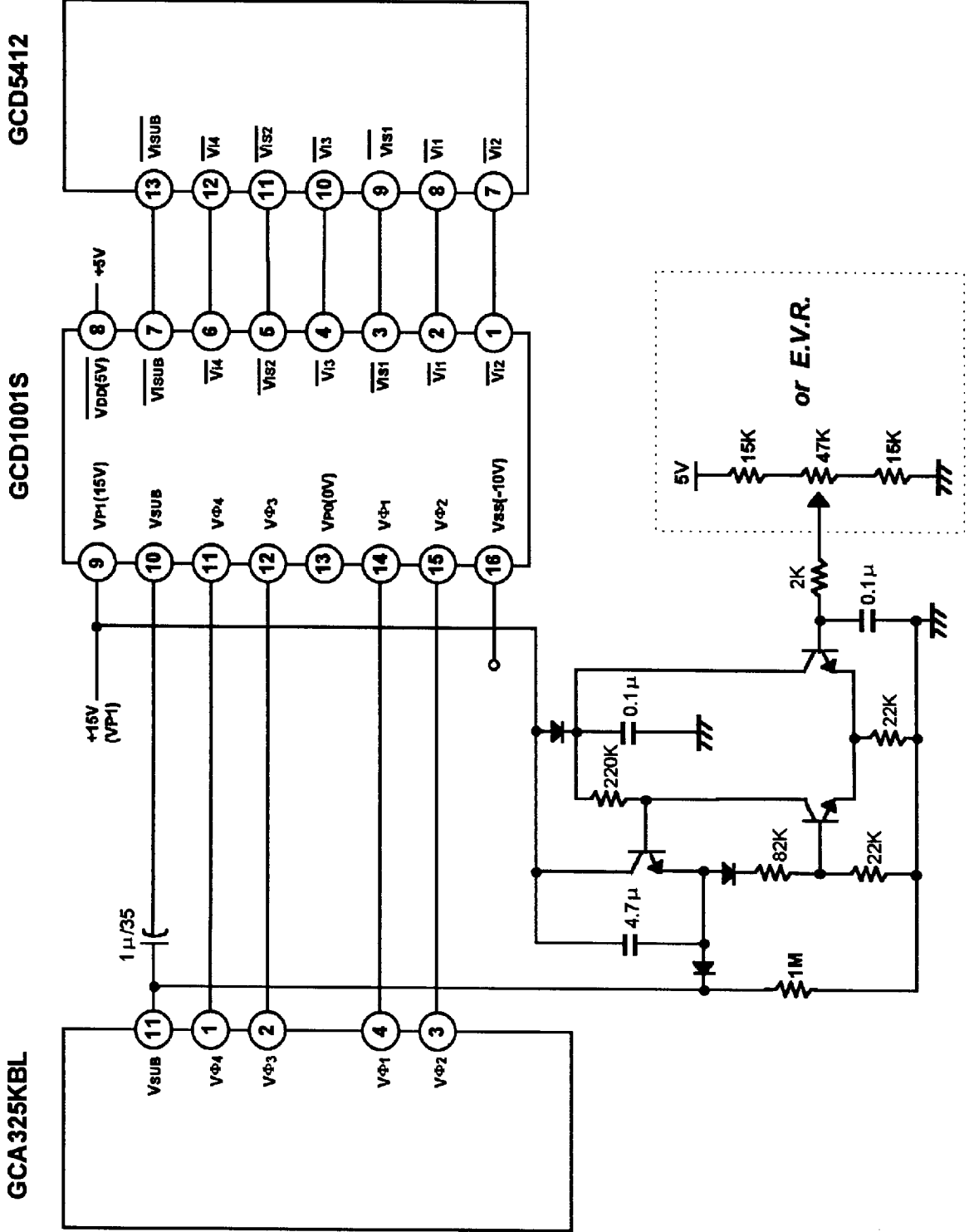
Input waveform  
(Repeat Cycle 16.7kHz)



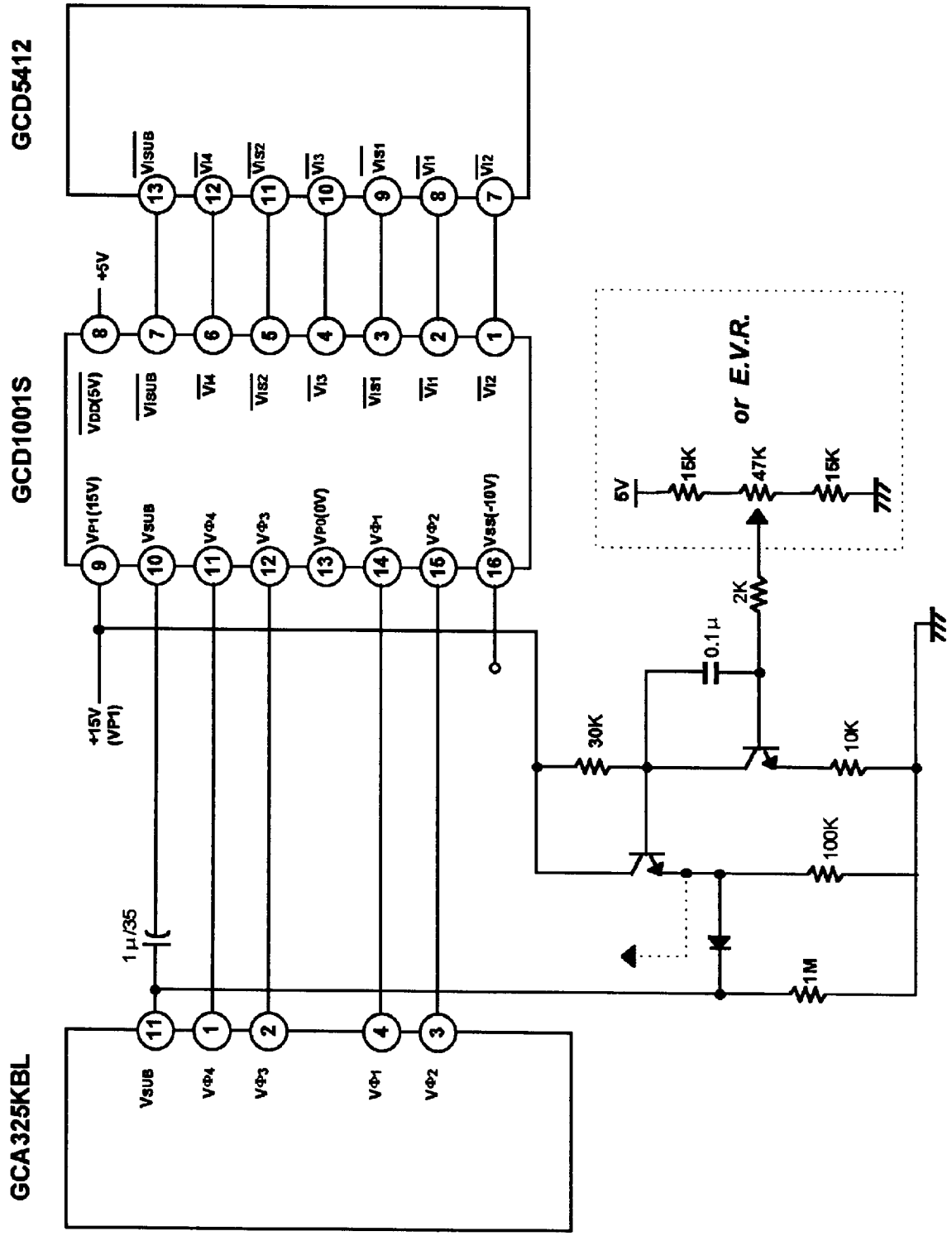
Output waveform



Application Circuit I



Application Circuit II





16 SSOP

