

KA2130A

LINEAR INTEGRATED CIRCUIT

TV VERTICAL DEFLECTION SYSTEM

The KA2130A is a monolithic integrated circuit for use in the vertical deflection circuit of monochrome and small-sized color television receivers. It oscillates vertical signal synchronizing with the vertical synchronization signal and outputs the vertical deflection current with a single chip.

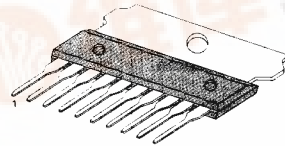
FUNCTIONS

- Vertical synchronization circuit.
- Vertical oscillation circuit.
- Vertical saw-tooth shaper.
- Vertical-output circuit.
- Clamping circuit for blanking pulse.
- Temperature compensating circuit.

FEATURES

- Less number of external components.
- Wide range of operational voltage (9V ~ 18 volts).
- Freely adjustable pull-in range.
- Adjustable blanking pulse-width.
- Large output current-capacity (2 A_{p-p}).
- Built-in adjusting circuit for flyback time.
- Easy mounting on printed circuit board.

10 SIP H/S



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ORDERING INFORMATION

Device	Package	Operating Temperature
KA2130A	10 SIP H/S	- 20 ~ + 75°C

TYPICAL APPLICATION CIRCUIT

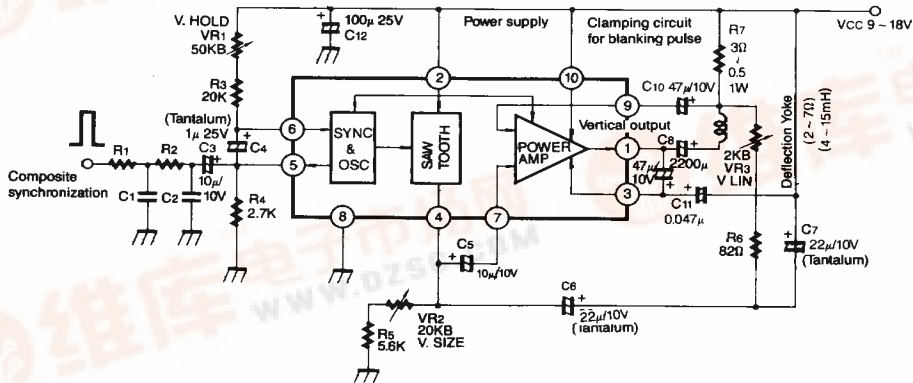


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Output Current	I_{p-p}	2	Ap-p
Power Dissipation	P_{d1}	1.5 ($T_a = +75^\circ\text{C}$) With aluminum heatsink	W
Power Dissipation	P_{d2}	2.15 ($T_a = +75^\circ\text{C}$) With aluminium heatsink (31.6×31.6×1mm t)	W
Operating Temperature	T_{opr}	-20 ~ +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{V}$, $T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Circuit Current	I_{CC}	No input signal and no load condition	15	30	46	mA	2
Output Terminal Voltage	V_N	No input signal and no load condition	5.6	6.0	6.4	V	2
Vertical Oscillation Frequency	f_v	Synchronization signal voltage applied at Terminal 5 is 1.3 V_{p-p}	—	50/60	—	Hz	2
Free-running Frequency	f_{vo}	Oscillation capacitor, 1 μF (Tantalum) resistor, 38.1K Ω	53	60	67	Hz	2
Pull-in Range	f_p	With specified integration circuit, applied voltage of synchronization signal is 1.3 V_{p-p} at Terminal 5	-10	-12	—	Hz	2
Drift of Free-running Frequency vs. Power Supply Voltage	Δf_{vo}	Frequency drift from standard frequency (f_{vo} 60 Hz at $V_{CC} = 12\text{V}$) vs. power supply voltage ($V_{CC} = 12 \pm 2\text{V}$)	—	—	± 1.0	Hz	2
Deviation of Pull-in Range vs. Power Supply Voltage	Δf_p	Deviation from the range for pull in (at $V_{CC} = 12\text{V}$) vs. power supply voltage ($V_{CC} = 12 \pm 2\text{V}$)	—	—	± 3.0	Hz	2
Output Saturation Voltage	V_{sat}	Output current: 0.7A	—	1.3	1.6	V	2
Output Pulse Width of Terminal 4	T_o	Oscillation capacitor, 1 μF (Tantalum) resistor, 38.1K Ω	300	420	600	μsec	2

TEST CIRCUIT

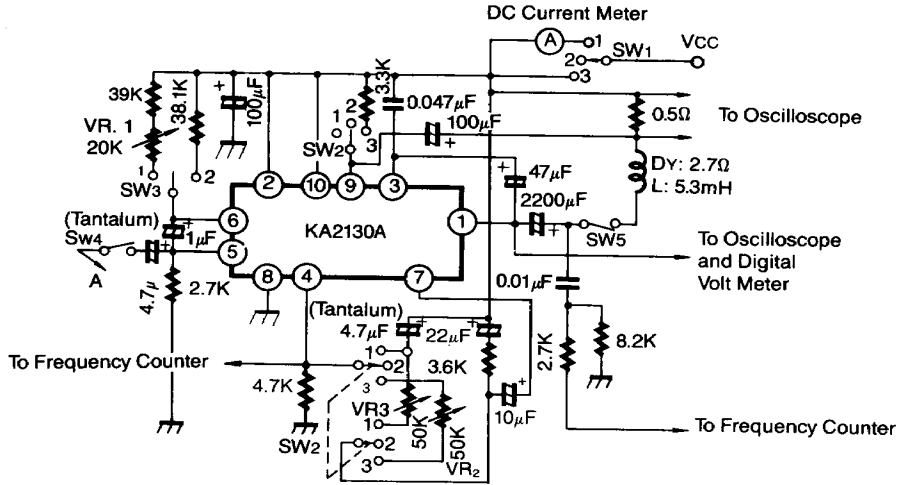


Fig. 2

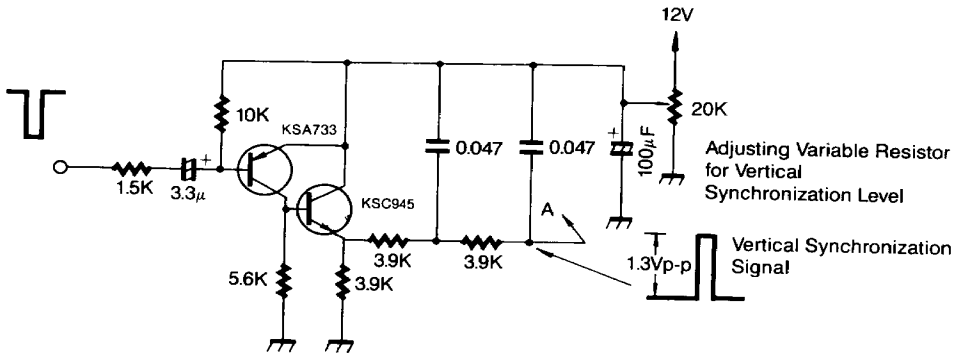


Fig. 3