

NEC®

ULTRA-WIDEBAND
DIFFERENTIAL VIDEO AMPLIFIERSUPC1663C
UPC1663G

T-74-07-01

FEATURES

- **BANDWIDTH AND TYPICAL GAIN**
120 MHz at $A_{vol} = 300$
170 MHz at $A_{vol} = 100$
700 MHz at $A_{vol} = 10$
- **VERY SMALL PHASE DELAY**
- **GAIN ADJUSTABLE FROM 10 TO 300**
- **NO FREQUENCY COMPENSATION REQUIRED**

DESCRIPTION

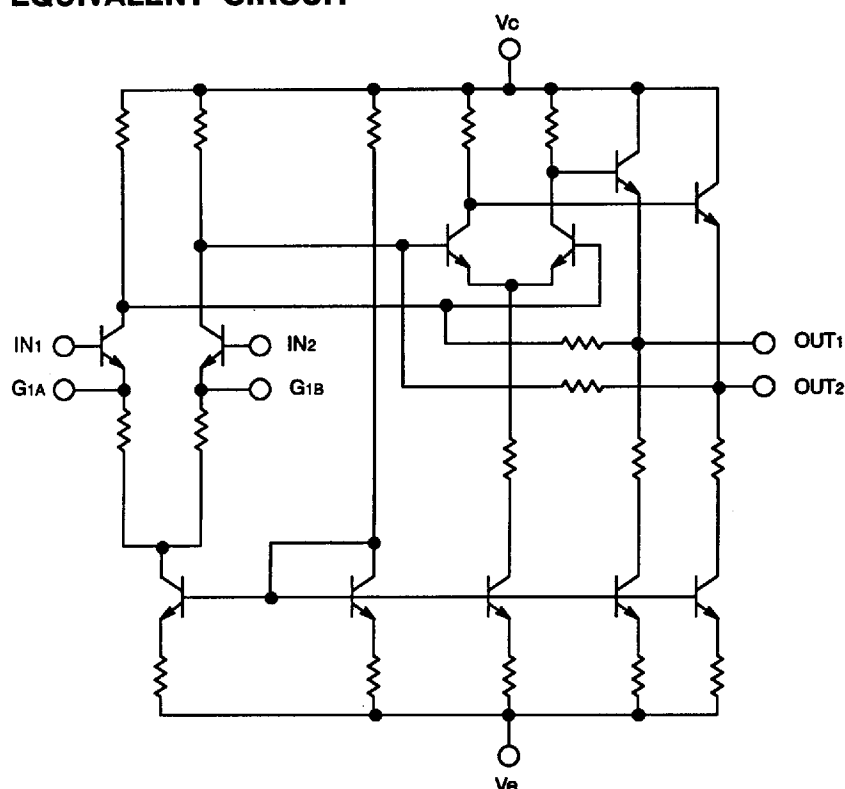
The UPC1663C and UPC1663G are video amplifiers with differential input and output stages. An ultrahigh frequency process ($f_T = 6$ GHz) improves AC performance compared with industry-standard video amplifiers. The UPC1663C and UPC1663G are excellent as sense amplifiers for high-density CCDs, as video or pulse amplifiers in high-resolution displays and in communications equipment.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_C = 6\text{ V}$, $V_E = -6\text{ V}$)

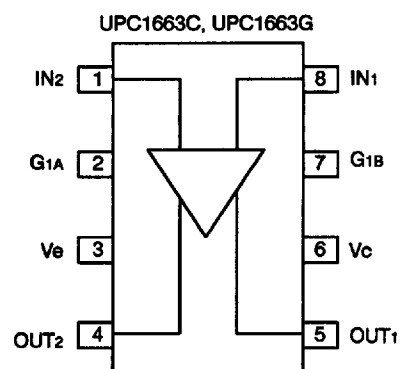
SYMBOLS	CHARACTERISTIC		CONDITIONS	UNITS	MIN	TYP	MAX
A_{vd}	Differential Voltage Gain	Gain 1	(Note 1)		200	320	500
		Gain 2	(Note 2)		80	100	120
		Gain 3	(Note 3)		8	10	12
BW	Bandwidth	Gain 1	$R_s = 50\ \Omega$ (3 dB down point)	MHz		120	
		Gain 2				170	
		Gain 3				700	
t_r	Rise Time	Gain 1	$R_s = 50\ \Omega$, $V_{out} = 1\text{ V}_{p-p}$	ns		2.9	
		Gain 2				2.7	
		Gain 3				2.7	
t_{pd}	Propagation Delay	Gain 1	$R_s = 50\ \Omega$, $V_{out} = 1\text{ V}_{p-p}$	ns		2	
		Gain 2				1.6	
		Gain 3				1.2	
R_{in}	Input Impedance	Gain 1		k Ω		4.0	
		Gain 2			6.7	13	
		Gain 3			50	180	
C_{in}	Input Capacitance			pF		2	
I_{io}	Input Offset Current			μA		0.4	5.0
I_b	Input Bias Current			μA		20	40
V_n	Input Noise Voltage		$R_s = 50\ \Omega$, 10 k to 10 MHz	$\mu\text{V}_{r.m.s.}$		3	
V_i	Input Voltage Range			V	± 1.0		
CMRR	Common Mode Rejection Ratio		$V_{cm} = \pm 1\text{ V}$, $f \leq 100\text{ kHz}$	dB	55	70	
			$V_{cm} = \pm 1\text{ V}$, $f = 5\text{ MHz}$		53	60	
SVRR	Supply Voltage Rejection Ratio		$\Delta V = \pm 0.5\text{ V}$	dB	50	70	
$V_{o(off)}$	Output Offset Voltage	Gain 1	$V_{o(off)} = OUT_1 - OUT_2 $	V		0.3	1.5
		Gain 2, 3				0.1	1.0
$V_{o(CM)}$	Output Common Mode Voltage			V	2.4	2.9	3.4
V_{op-p}	Max. Output Voltage Swing			V_{p-p}	3.0	4.0	
I_{sink}	Output Sink Current			mA	2.5	3.6	
I_{cc}	Power Supply Current			mA		13	20

Notes:

1. Gain select pins G1A and G1B are connected.
2. Gain select pins G2A and G2B are connected.
3. All gain select pins are open.
4. Insert adjustment resistor (0 to 10 k Ω) between G1A and G1B when variable gain is necessary.

UPC1663C, UPC1663G**EQUIVALENT CIRCUIT****CONNECTION DIAGRAM**

TOP VIEW

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$)

SYMBOLS	PARAMETERS	UNITS	UPC1663C	UPC1663G
Vc	Positive Supply Voltage	V	+8	+7
Ve	Negative Supply Voltage	V	-8	-7
Pr	Power Dissipation	mW	500	*280 ($T_A = 75^\circ\text{C}$)
V _{ID}	Differential Input Voltage	V	±5	±5
V _{ICM}	Input Voltage	V	±6	±6
I _O	Output Current	mA	35	35
T _{opt}	Operating Temperature Range	°C	-45 to +85	-45 to +75
T _{stg}	Storage Temperature Range	°C	-55 to +150	-55 to +150

* Mounted on 5 cm x 5 cm x 0.16 mm glass epoxy PCB

RECOMMENDED OPERATING CONDITIONS

SYMBOLS	CHARACTERISTIC	UNITS	MIN	TYP	MAX
Vc (1663C)	Positive Supply Voltage	V	+2	+6	+7
Ve (1663C)	Negative Supply Voltage	V-	-2	-6	-7
Vc (1663G)	Positive Supply Voltage	V	+2	+6	+6.5
Ve (1663G)	Negative Supply Voltage	V-	-2	-6	-6.5
I _{O source}	Source Current	mA			20
I _{O sink}	Sink Current	mA			2.5
	Frequency Range	MHz	DC		200

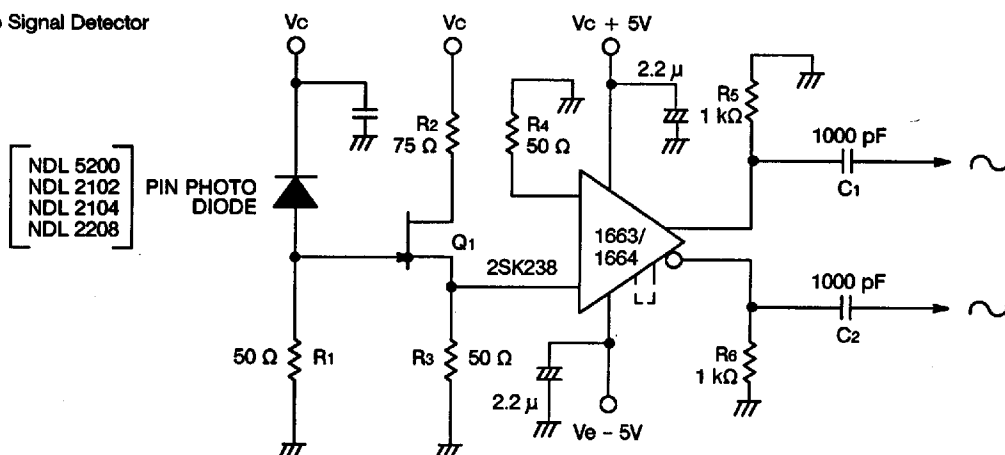
Attention:

Due to ultrahigh frequency characteristics, the physical circuit layout is very critical. Supply voltage line bypass, double-sided printed-circuit board, and wide-area ground line layout are necessary for stable operation. Two signal resistors connected to both inputs and two load resistors connected to both outputs should be balanced for stable operation.



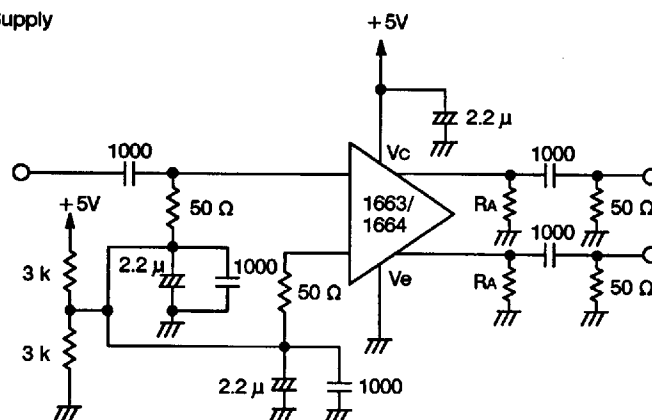
TYPICAL APPLICATIONS

• Photo Signal Detector



Since the input impedance of the IC falls when the gain rises, stable operation can be achieved by inserting a FET buffer when necessary as illustrated above.

• Application for +5 V Single Supply



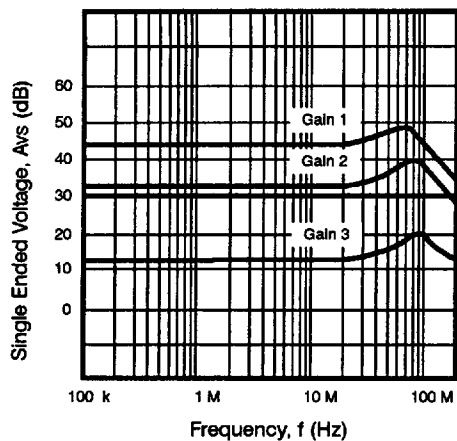
TYPICAL PERFORMANCE UNDER SINGLE SUPPLY +5 V OPERATION

PARAMETER		CONDITIONS	TYPICAL	UNITS
Differential Gain	Gain 1	15 MHz	35	dB
	Gain 3		11	
Bandwidth	Gain 1	3 dB down point	106	MHz
	Gain 3		115	
Rise Time	Gain 1	$R_s = 50 \Omega$, $V_{OUT} = 80 \text{ mV}_{p-p}$	2.2	ns
Propagation Delay	Gain 1	$R_s = 50 \Omega$, $V_{OUT} = 80 \text{ mV}_{p-p}$	2.8	ns
	Gain 3	$R_s = 50 \Omega$, $V_{OUT} = 60 \text{ mV}_{p-p}$	1.8	
Phase Shift	Gain 1	100 MHz	-123	degree
	Gain 3		-93	
Output Power	$R_A = 240 \Omega$	$Z_L = 50 \Omega$ 15 MHz	5.0	dBm
	$R_A = 910 \Omega$		0	
	$R_A = 80 \Omega$		-11.5	

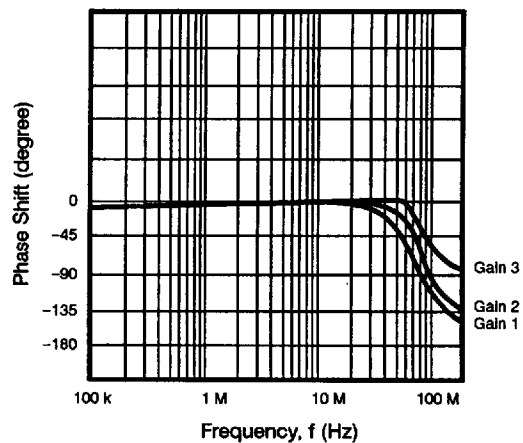
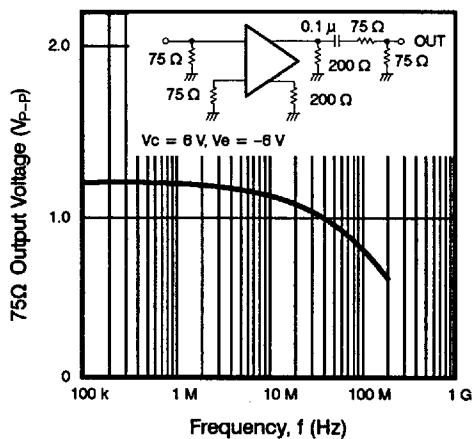
UPC1663C, UPC1663G

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

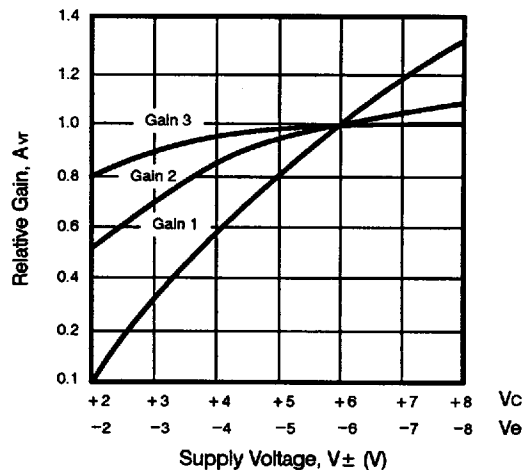
SINGLE ENDED VOLTAGE GAIN



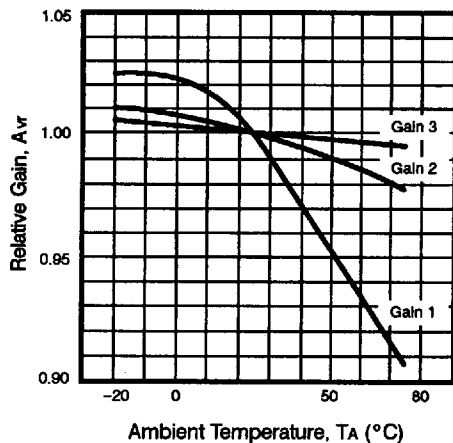
PHASE SHIFT

VIDEO LINE SINGLE ENDED
OUTPUT VOLTAGE SWING

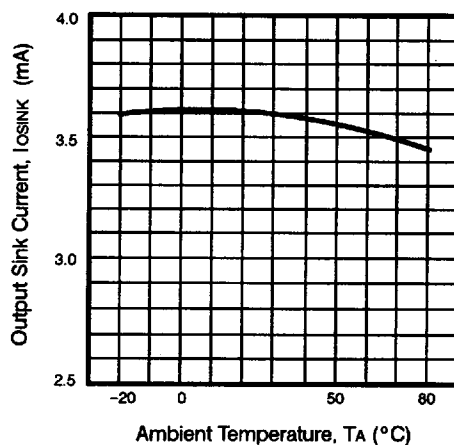
VOLTAGE GAIN

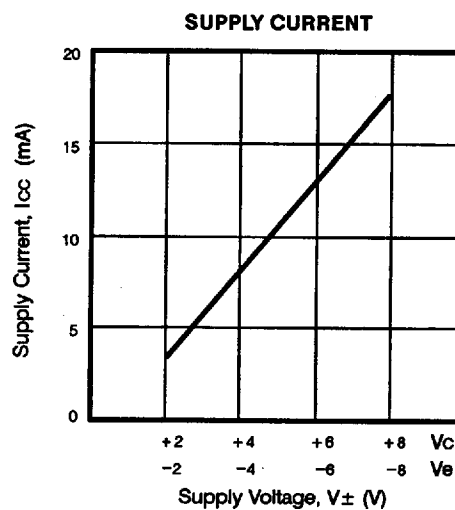
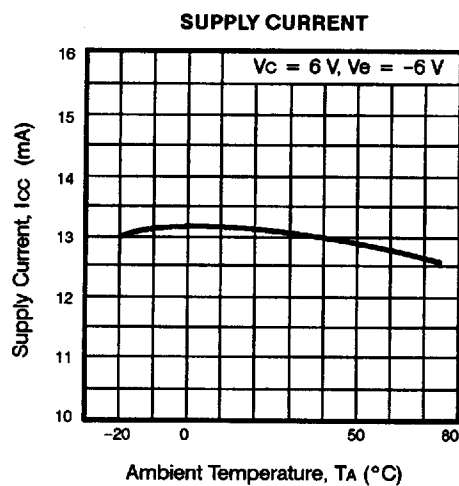
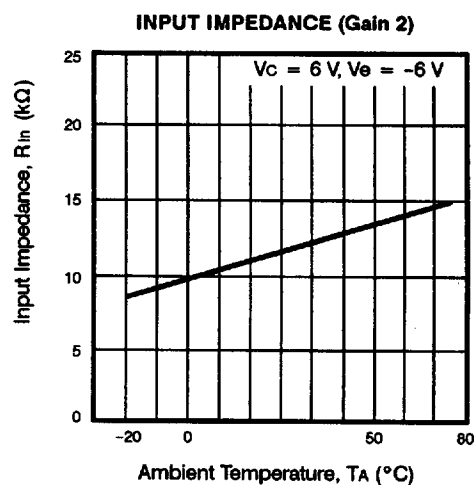
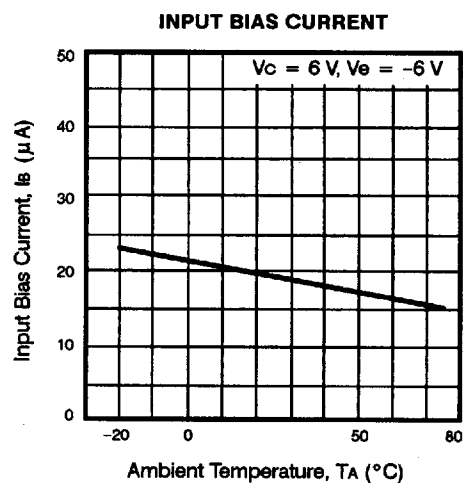
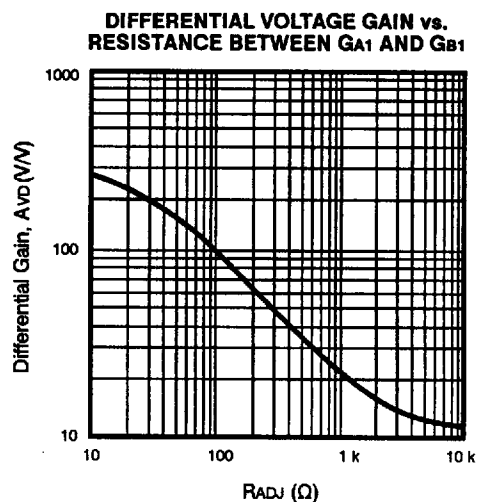
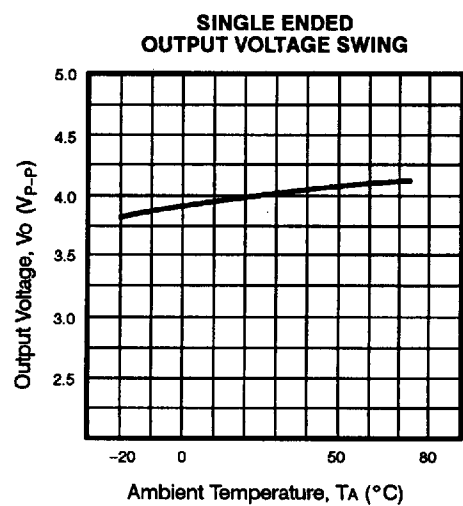


VOLTAGE GAIN



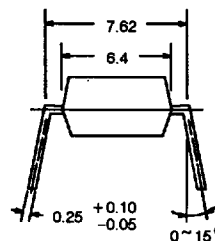
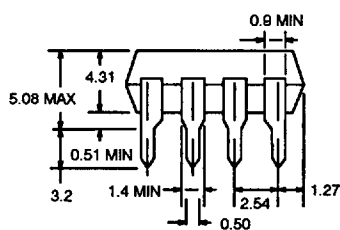
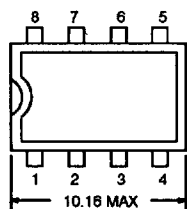
SINK CURRENT



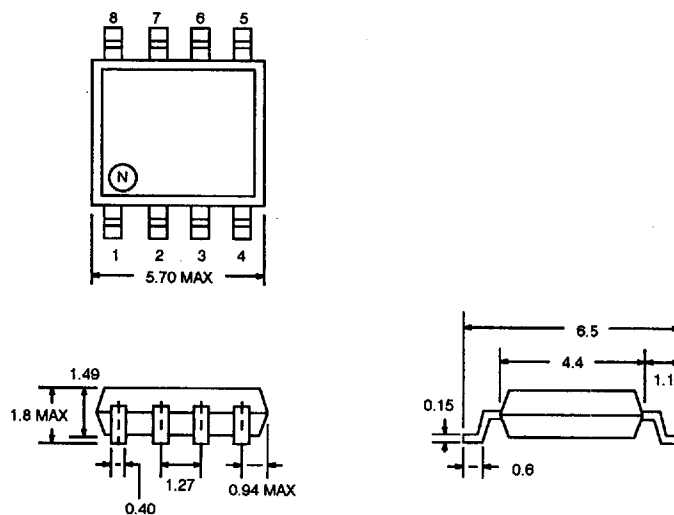
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

UPC1663C, UPC1663G**ORDERING INFORMATION**

PART NUMBER	PACKAGE DESCRIPTION	PACKAGE CODE
UPC1663C	8 Pin Plastic DIP (300 mil)	C08
UPC1663G	8 Pin Plastic SOP (225 mil)	G08

OUTLINE DIMENSIONS (Units in mm)**OUTLINE C08****UPC1663C****Notes:**

1. Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

OUTLINE DIMENSIONS (Units in mm)**OUTLINE G08**
UPC1663G**Note:**

1. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.