DATA SHEET



NEC

MOS INTEGRATED CIRCUIT

# μPD78P058F

## 8-BIT SINGLE-CHIP MICROCONTROLLER

## DESCRIPTION

The μPD78P058F is an Electro Magnetic Interface (EMI) noise reduction version in comparison with the usual μPD78P058.

The μPD78P058F is a member of the μPD78058F subseries of 78K/0 series products, in which the on-chip mask ROM is replaced with one-time programmable (OTP) ROM.

Because this device can be programmed by users, it is ideally suited for applications involving the small-scale production of many different products, and rapid development and time-to-market of a new product.

**Details are given in the following User's Manuals. Be sure to read them before starting design.**
**μPD78058F, 78058FY Subseries User's Manual (to be prepared)**
**78K Series User's Manual—Instruction (IEU-1372)**

## FEATURES

- EMI noise reduction version (The overall peak level is reduced by 5 to 10 dB)
- Pin compatible with mask ROM versions (except the $V_{PP}$ pin)
- Internal PROM : 60 Kbytes[Note1]
  Programmable once only (ideal for small-scale production)
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes[Note2]
- Buffer RAM : 32 bytes
- Operable in the same supply voltage range as mask ROM versions ($V_{DD}$ = 2.7 to 6.0 V)
- One of the QTOP™ microcontrollers

**Notes** 1. Internal PROM capacity can be changed by memory size switching register (IMS).
2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

**Remarks** 1. For the difference between PROM and Mask ROM versions, see the chapter **1. DIFFERNCES BETWEEN μPD78P058F AND MASK ROM VERSIONS.**
2. QTOP Microcontroller is the general name of the microcontrollers with on-chip one-time PROM that are totally supported by NEC write service (from write to marking, screening and testing.)

**The information in this document is subject to change without notice.**

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The mark * shows major revised points.

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## ORDERING INFORMATION

| Part Number | Package | On-Chip ROM |
|---|---|---|
| μPD78P058FGC-3B9 | 80-pin plastic QFP (14 × 14 mm, Resin thickness: 2.7mm) | One-time PROM |
| μPD78P058FGC-8BT[Note] | 80-pin plastic QFP (14 × 14 mm, Resin thickness: 1.4mm) | One-time PROM |

**Note** Under development

**Remark** The μPD78P058FGC contains two types of packages (see the chapter **8. PACKAGE DRAWINGS**). For packages which can be supplied, consult your local NEC personnel.

## 78K/0 SERIES LINE-UP

These products are a further development in the 78K/0 series. The designations appearing inside the boxes are subseries names.

Products in mass production

Products under development

Y subseries are compatible with $I^2C$ bus.

78K/0 Series

| Application | Pins | Subseries | Y subseries | Description |
|---|---|---|---|---|
| Control | 100-pin | μPD78078 | μPD78078Y | A timer was added to the μPD78054 and external interface function was enhanced |
| | 100-pin | μPD78070A | μPD78070AY | ROM-less versions of the μPD78078 |
| | 100-pin | μPD780018 Note | μPD780018Y Note | Serial I/O of the μPD78078 was enhanced and only selected funcitons are provided |
| | 80-pin | μPD78058F | μPD78058FY | EMI noise reduction versions of the μPD78078 |
| | 80-pin | μPD78054 | μPD78054Y | UART and D/A converter were added to the μPD78014 and I/O was enhanced |
| | 64-pin | μPD78018F | μPD78018FY | Low-voltage (1.8 V) operation versions of the μPD78014 with several ROM and RAM capacities are available |
| | 64-pin | μPD78014 | μPD78014Y | An A/D converter and 16-bit timer were added to the μPD78002 |
| | 64-pin | μPD780001 | | An A/D converter was added to the μPD78002 |
| | 64-pin | μPD78002 | μPD78002Y | Basic subseries for control |
| | 42/44-pin | μPD78083 | | On-chip UART, capable of operating at a low-voltage (1.8 V) |
| FIP™ drive | 100-pin | μPD780208 | | The I/O and FIP C/D of the μPD78044F were enhanced, Display output total: 53 |
| | 80-pin | μPD78044F | | A 6-bit U/D counter was added to the μPD78024, Display output total: 34 |
| | 64-pin | μPD78024 | | Basic subseries for driving FIP, Display output total: 26 |
| LCD drive | 100-pin | μPD780308 | μPD780308Y | SIO of the μPD78064 was enhanced and ROM and RAM were expanded |
| | 100-pin | μPD78064B | | EMI noise reduction version of the μPD78064 |
| | 100-pin | μPD78064 | μPD78064Y | Subseries for driving LCDs, on-chip UART |
| IEBus™ supported | 80-pin | μPD78098 | | The IEBus controller was added to the μPD78054 |
| LV | 64-pin | μPD78P0914 | | On-chip PWM output, LV digital code decoder, Hsync counter |

**Note** Under planning

The major functional differences among the subseries are shown below.

| Subseries name \ Function | | ROM Capacity | Timer 8-bit | Timer 16-bit | Timer Watch | Timer WDT | 8-bit A/D | 8-bit D/A | Serial Interface | I/O | $V_{DD}$ MIN. Value | External Expansion |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Control | μPD78078 | 32 K-60 K | 4ch | 1ch | 1ch | 1ch | 8ch | 2ch | 3ch (UART: 1ch) | 88 | 1.8 V | √ |
| | μPD78070A | – | | | | | | | | 61 | 2.7 V | |
| | μPD780018 | 48 K-60 K | | | | | | – | 2ch | 88 | | |
| | μPD78058F | | 2ch | | | | | 2ch | 3ch (UART: 1ch) | 69 | | |
| | μPD78054 | 16 K-60 K | | | | | | | | | 2.0 V | |
| | μPD78018F | 8 K-60 K | | | | | | – | 2ch | 53 | 1.8 V | |
| | μPD78014 | 8 K-32 K | | | | | | | | | 2.7 V | |
| | μPD780001 | 8 K | | – | – | | | | 1ch | 39 | | – |
| | μPD78002 | 8 K-16 K | | | 1ch | | – | | | 53 | | √ |
| | μPD78083 | | | | – | | 8ch | | 1ch (UART: 1ch) | 33 | 1.8 V | – |
| FIP driving | μPD780208 | 32 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | – | 2ch | 74 | 2.7 V | – |
| | μPD78044F | 16 K-40 K | | | | | | | | 68 | | |
| | μPD78024 | 24 K-32 K | | | | | | | | 54 | | |
| LCD driving | μPD780308 | 48 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | – | 3ch (UART: 1ch) | 57 | 1.8 V | – |
| | μPD78064B | 32 K | | | | | | | 2ch (UART: 1ch) | | 2.0 V | |
| | μPD78064 | 16 K-32 K | | | | | | | | | | |
| IEBus supported | μPD78098 | 32 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | 2ch | 3ch (UART: 1ch) | 69 | 2.7 V | √ |
| LV | μPD78P0914 | 32 K | 6ch | – | – | 1ch | 8ch | – | 2ch | 54 | 4.5 V | √ |

## FUNCTION DESCRIPTION

| Item | | Function |
|---|---|---|
| Internal memory | | • PROM : 60 Kbytes[Note1]<br>• RAM<br>Internal high-speed RAM : 1024 bytes<br>Internal expansion RAM : 1024 bytes[Note2]<br>Buffer RAM : 32 bytes |
| Memory space | | 64 Kbytes |
| General register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) |
| Instruction cycles | | Instruction execution time is variable. |
| | When main system clock is selected | 0.4μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz) |
| | When subsystem clock is selected | 122 μs (@ 32.768 kHz) |
| Instruction set | | • 16-bit operation<br>• Multiply/divide (8-bit × 8-bit, 16-bit / 8-bit)<br>• Bit manipulation (set, reset, test, Boolean operation)<br>• BCD adjust, etc. |
| I/O ports | | Total : 69<br>• CMOS input : 2<br>• CMOS input/output : 63<br>• N-ch open-drain input/output : 4 |
| A/D converter | | • 8-bit resolution × 8 ch |
| D/A converter | | • 8-bit resolution × 2 ch |
| Serial interface | | • 3-wire serial I/O, SBI, or 2-wire serial I/O mode selectable : 1 ch<br>• 3-wire serial I/O mode (with on-chip max. 32-byte automatic transmit/receive function) : 1 ch<br>• 3-wire serial I/O or UART mode selectable : 1 ch |
| Timer | | • 16-bit timer/event counter : 1 ch<br>• 8-bit timer/event counter : 2 ch<br>• Watch timer : 1 ch<br>• Watchdog timer : 1 ch |
| Timer output | | 3 pins (14-bit PWM output: 1 pin) |
| Clock output | | 19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0 MHz with main system clock)<br>32.768 kHz (@ 32.768 kHz with subsystem clock) |
| Buzzer output | | 1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz<br>(@ 5.0 MHz with main system clock) |
| Vectored interrupts | Maskable interrupts | Internal: 13, external: 7 |
| | Non-maskable interrupts | Internal: 1 |
| | Software interrupts | 1 |
| Test inputs | | Internal: 1, external: 1 |
| Supply voltage | | $V_{DD}$ = 2.7 to 6.0 V |
| Operating ambient temperature | | $T_A$ = –40 to +85 °C |
| Packages | | • 80-pin plastic QFP (14 × 14 mm, Resin thickness: 2.7 mm)<br>• 80-pin plastic QFP (14 × 14 mm, Resin thickness: 1.4 mm) |

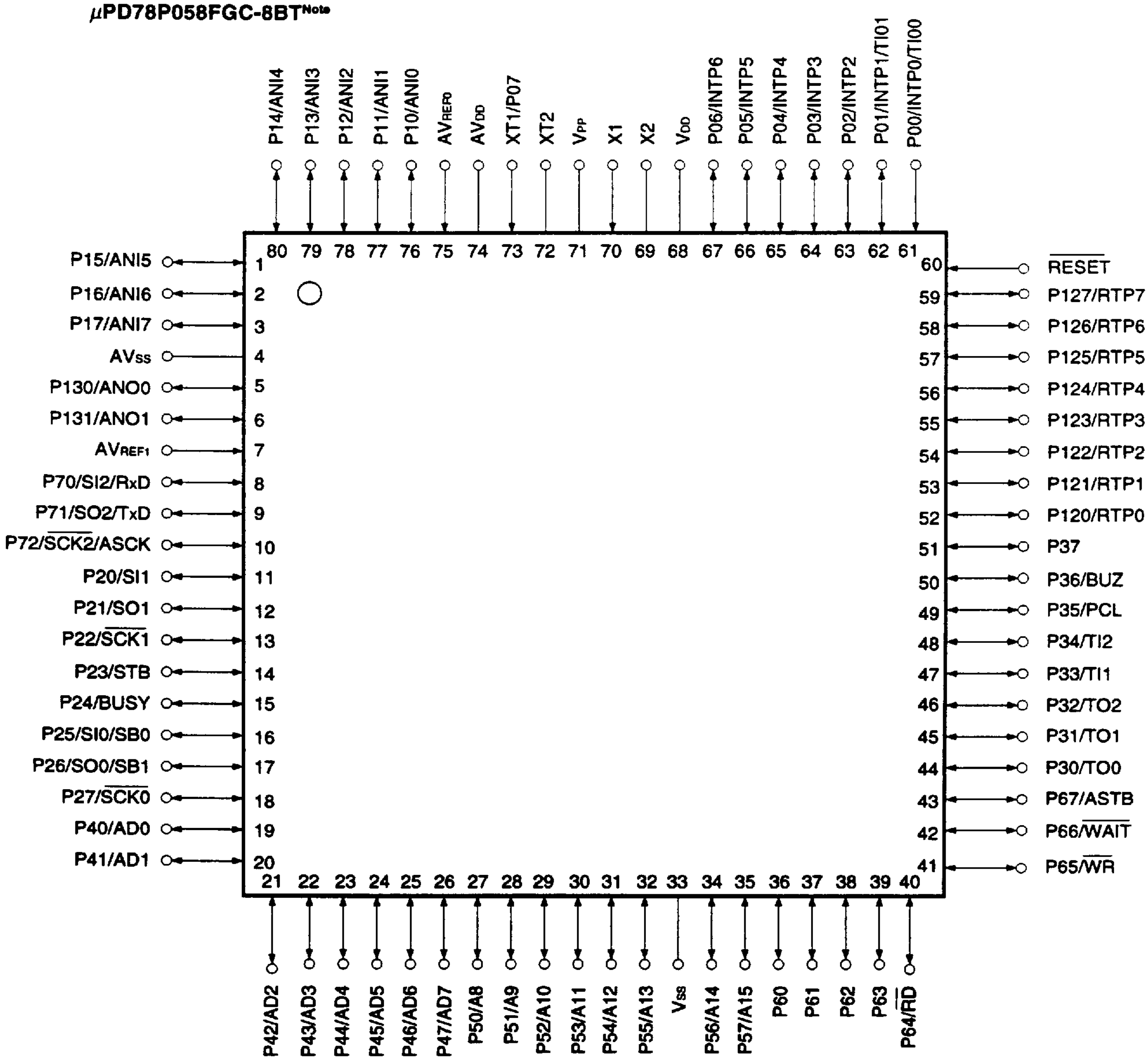
**Notes** 1. Internal PROM capacity can be changed by memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

## PIN CONFIGURATIONS (TOP VIEW)

### (1) Normal Operating Mode

- 80-pin plastic QFP (14 × 14 mm, Resin thickness: 2.7 mm)
  μPD78P058FGC-3B9
- 80-pin plastic QFP (14 × 14 mm, Resin thickness: 1.4 mm)
  μPD78P058FGC-8BT[Note]



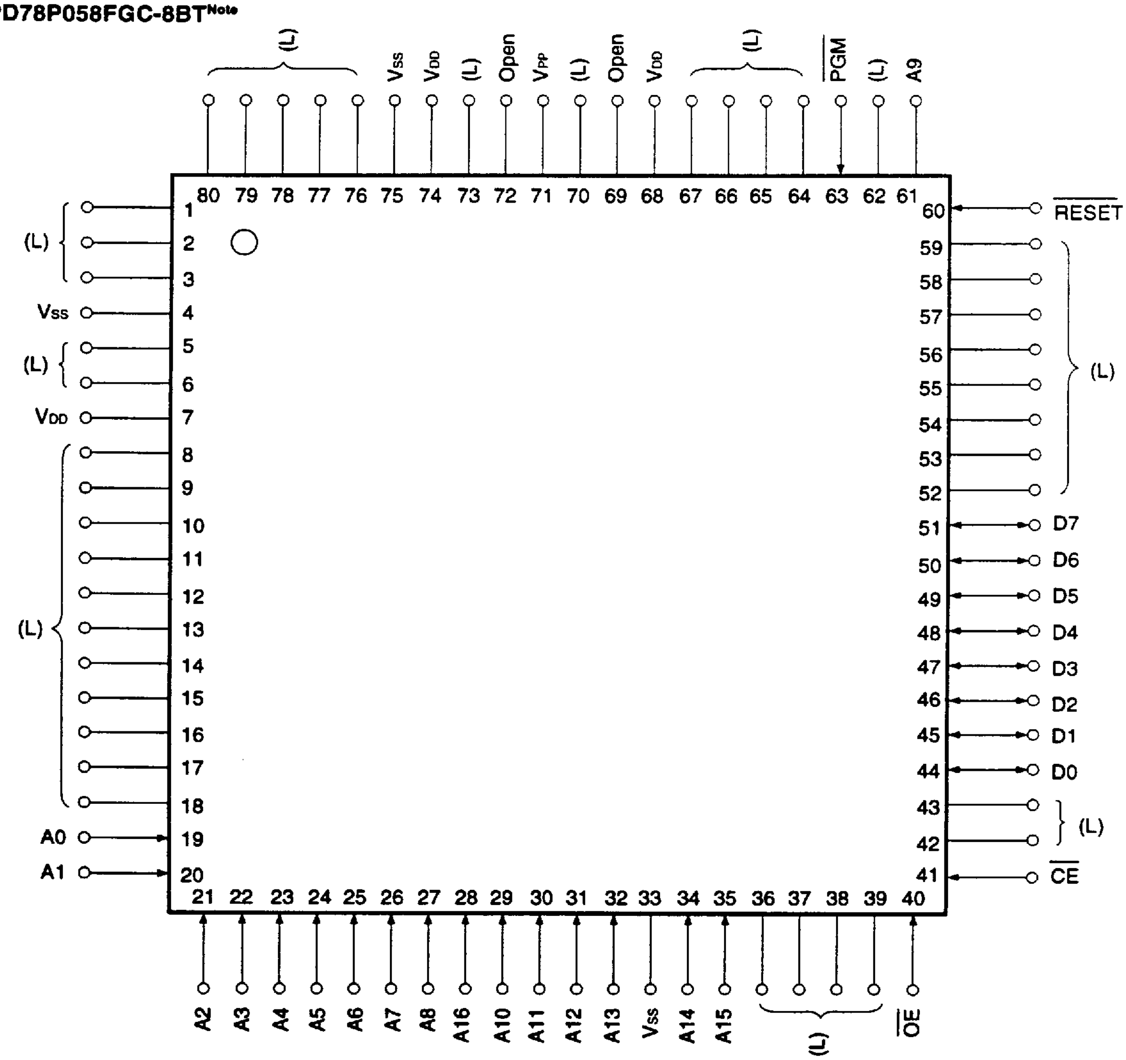

**Note** Under development

**Cautions**
1. Connect the $V_{PP}$ pin to $V_{SS}$.
2. The $AV_{DD}$ pin functions as both an A/D converter power supply and a port power supply. When the μPD78P058F is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the $AV_{DD}$ pin to another power supply which has the same potencial as $V_{DD}$.
3. The $AV_{SS}$ pin functions as both grounds of an A/D converter and D/A converter and of a port. When the μPD78P058F is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the $AV_{SS}$ pin to another ground line than $V_{SS}$.

A8 to A15 : Address Bus
AD0 to AD7 : Address/ Data Bus
ANI0 to ANI7 : Analog Input
ANO0 to ANO1 : Analog Output
ASCK : Asynchronous Serial Clock
ASTB : Address Strobe
$AV_{DD}$ : Analog Power Supply
$AV_{REF0}$, $AV_{REF1}$ : Analog Reference Voltage
$AV_{SS}$ : Analog Ground
BUSY : Busy
BUZ : Buzzer Clock
INTP0 to INTP6 : Interrupt from Peripherals
P00 to P07 : Port 0
P10 to P17 : Port 1
P20 to P27 : Port 2
P30 to P37 : Port 3
P40 to P47 : Port 4
P50 to P57 : Port 5
P60 to P67 : Port 6
P70 to P72 : Port 7
P120 to P127 : Port 12
P130, P131 : Port 13
PCL : Programmable Clock
$\overline{RD}$ : Read Strobe
$\overline{RESET}$ : Reset
RTP0 to RTP7 : Real-Time Output Port
RxD : Receive Data
SB0, SB1 : Serial Bus
$\overline{SCK0}$ to $\overline{SCK2}$ : Serial Clock
SI0 to SI2 : Serial Input
SO0 to SO2 : Serial Output
STB : Strobe
TI00, TI01 : Timer Input
TI1,TI2 : Timer Input
TO0 to TO2 : Timer Output
TxD : Transmit Data
$V_{DD}$ : Power Supply
$V_{PP}$ : Programming Power Supply
$V_{SS}$ : Ground
$\overline{WAIT}$ : Wait
$\overline{WR}$ : Write Strobe
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)

(2) **PROM Programming Mode**

- **80-pin plastic QFP (14 × 14 mm, Resin thickness: 2.7 mm)**
  **μPD78P058FGC-3B9**
- **80-pin plastic QFP (14 × 14 mm, Resin thickness: 1.4 mm)**
  **μPD78P058FGC-8BT[Note]**

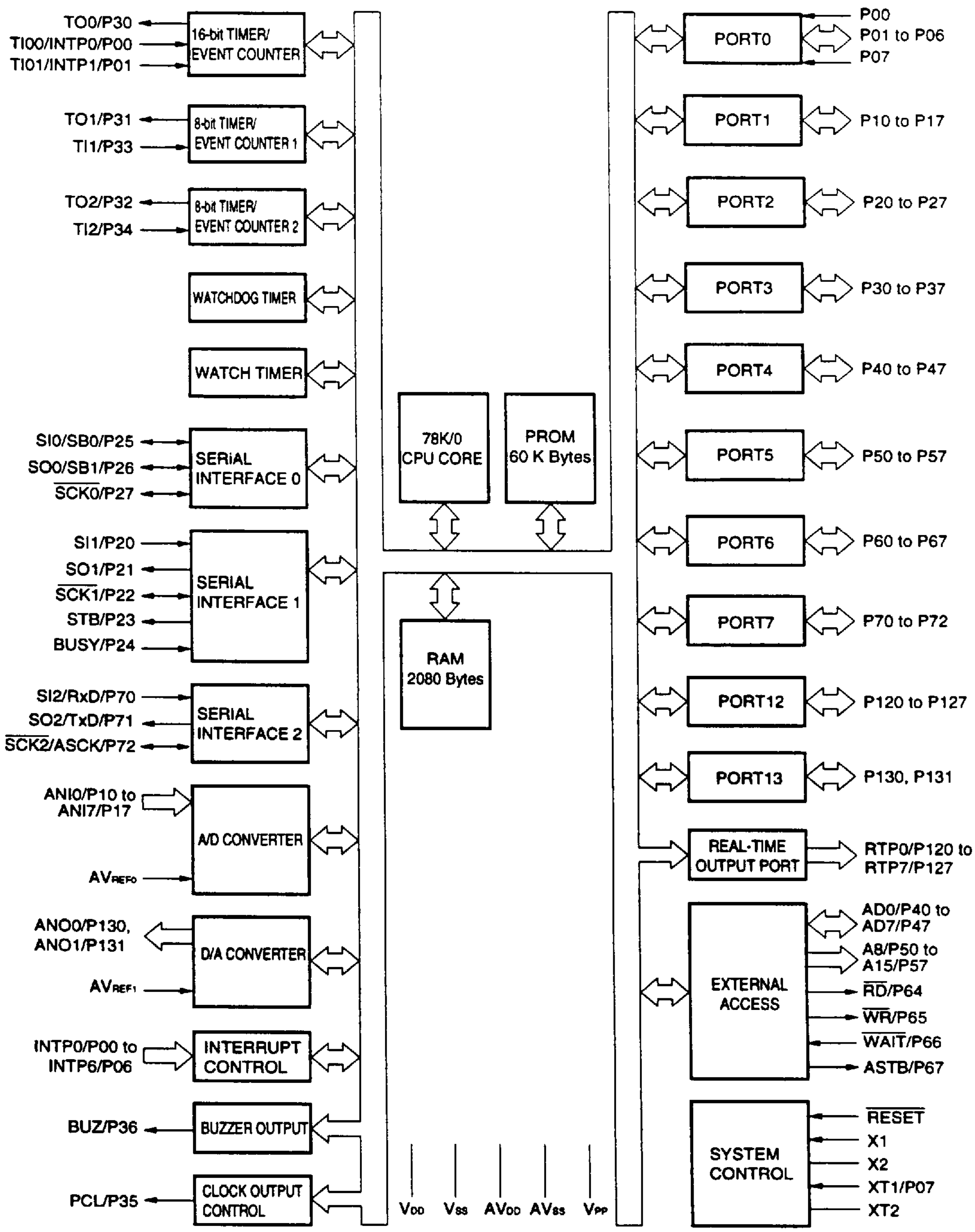



**Note** Under development

**Cautions 1. (L) : Individually connect to Vss via a pull-down resistor.**
**2. Vss : Connect to GND.**
**3. RESET : Set to low level.**
**4. Open : No connection**

| | | | |
|---|---|---|---|
| A0 to A16 | : Address Bus | RESET | : Reset |
| D0 to D7 | : Data Bus | VDD | : Power Supply |
| CE | : Chip Enable | VPP | : Programming Power Supply |
| OE | : Output Enable | Vss | : Ground |
| PGM | : Program | | |

## BLOCK DIAGRAM



CONTENTS

# 1. DIFFERENCES BETWEEN μPD78P058F AND MASK ROM VERSIONS

The μPD78P058F is a single-chip microcontroller with an on-chip one-time writable PROM.

Setting the memory size switching register (IMS) and internal expansion RAM size switching register (IXS) enables the identical functions to mask ROM versions (μPD78P056F, 58F) except the functions of PROM specifications and of mask options for P60 to P63.

Differences between the μPD78P058F and mask ROM versions are shown in Table 1-1.

**Table 1-1. Differences between μPD78P058F and Mask ROM Versions**

| Item | μPD78P058F | Mask ROM versions |
|---|---|---|
| ROM structure | One-time PROM | Mask ROM |
| ROM capacity | 60 Kbytes | μPD78056F : 48 Kbytes<br>μPD78058F : 60 Kbytes |
| Internal expansion RAM capacity | 1024 bytes | μPD78056F : None<br>μPD78058F : 1024 bytes |
| Change of internal ROM capacity by memory size switching register | Can be changed[Note] | Cannot be changed |
| Change of internal expansion RAM capacity by internal expansion RAM size switching register | Can be changed[Note] | Cannot be changed |
| IC pin | None | Provided |
| $V_{PP}$ pin | Provided | None |
| Electrical chatacteristics | See each Data Sheet | |

**Note** The $\overline{RESET}$ input sets the internal PROM and internal expansion RAM to 60 Kbytes and 1024 bytes, respectively.

## 2. PIN FUNCTIONS

### 2.1 Pins in Normal Operating Mode

**(1) Port Pins (1/2)**

| Pin Name | Input/Output | Function | | After Reset | Alternate Function |
|---|---|---|---|---|---|
| P00 | Input | Port 0<br>8-bit input/output port | Input only | Input | INTP0/TI00 |
| P01 | Input/output | | Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software. | Input | INTP1/TI01 |
| P02 | | | | | INTP2 |
| P03 | | | | | INTP3 |
| P04 | | | | | INTP4 |
| P05 | | | | | INTP5 |
| P06 | | | | | INTP6 |
| P07[Note1] | Input | | Input only | Input | XT1 |
| P10 to P17 | Input/output | Port 1<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software.[Note2] | | Input | ANI0 to ANI7 |
| P20 | Input/output | Port 2<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | SI1 |
| P21 | | | | | SO1 |
| P22 | | | | | $\overline{SCK1}$ |
| P23 | | | | | STB |
| P24 | | | | | BUSY |
| P25 | | | | | SI0/SB0 |
| P26 | | | | | SO0/SB1 |
| P27 | | | | | $\overline{SCK0}$ |
| P30 | Input/output | Port 3<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | TO0 |
| P31 | | | | | TO1 |
| P32 | | | | | TO2 |
| P33 | | | | | TI1 |
| P34 | | | | | TI2 |
| P35 | | | | | PCL |
| P36 | | | | | BUZ |
| P37 | | | | | — |

**Notes** 1. When P07/XT1 pins are used as the input ports, set the processor clock control register (PCC) bit 6 (FRC) to 1, be sure not to use the feedback resistor of the subsystem clock oscillation circuit.

2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, their pull-up resistor are automatically disabled.

**Caution** **For pins which also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept (except for LCD segment output alternate-function pin).**

**<1> Rewrite the output latch while the pin is used as a port pin.**

**<2> Change the output level of the pin used as an output pin, even if it is not used as a port pin.**

(1) Port Pins (2/2)

| Pin Name | Input/Output | Function | | After Reset | Alternate Function |
|---|---|---|---|---|---|
| P40 to P47 | Input/output | Port 4<br>8-bit input/output port<br>Input/output is specifiable as 8-bit unit.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software.<br>Set test input flag(KRIF) to 1 by falling edge detection. | | Input | AD0 to AD7 |
| P50 to P57 | Input/output | Port 5<br>8-bit input/output port<br>It is possible to directly drive LEDs.<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | A8 to A15 |
| P60 | Input/output | Port 6<br>8-bit input/output port<br>Input/output is specifiable bit-wise. | N-ch open-drain input/output port.<br>It is possible to directly drive LEDs. | Input | — |
| P61 | | | | | |
| P62 | | | | | |
| P63 | | | | | |
| P64 | | | When used as the input port, it is possible to connect an on-chip pull-up resistor by software. | Input | $\overline{\text{RD}}$ |
| P65 | | | | | $\overline{\text{WR}}$ |
| P66 | | | | | $\overline{\text{WAIT}}$ |
| P67 | | | | | ASTB |
| P70 | Input/output | Port 7<br>3-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | SI2/RxD |
| P71 | | | | | SO2/TxD |
| P72 | | | | | $\overline{\text{SCK2}}$/ASCK |
| P120 to P127 | Input/output | Port 12<br>8-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | RTP0 to RTP7 |
| P130, P131 | Input/output | Port 13<br>2-bit input/output port<br>Input/output is specifiable bit-wise.<br>When used as the input port, it is possible to use an on-chip pull-up resistor by software. | | Input | ANO0, ANO1 |

**Caution For pins which also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept (except for LCD segment output alternate-function pin).**

**<1> Rewrite the output latch while the pin is used as a port pin.**

**<2> Change the output level of the pin used as an output pin, even if it is not used as a port pin.**

(2) **Non-Port Pins (1/2)**

| Pin Name | Input/Output | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| INTP0 | Input | External interrupt inputs, with specifiable valid edges (rising edge, falling edge, and both rising and falling edges). | Input | P00/TI00 |
| INTP1 | | | | P01/TI01 |
| INTP2 | | | | P02 |
| INTP3 | | | | P03 |
| INTP4 | | | | P04 |
| INTP5 | | | | P05 |
| INTP6 | | | | P06 |
| SI0 | Input | Serial data input of the serial interface | Input | P25/SB0 |
| SI1 | | | | P20 |
| SI2 | | | | P70/RxD |
| SO0 | Output | Serial data output of the serial interface | Input | P26/SB1 |
| SO1 | | | | P21 |
| SO2 | | | | P71/TxD |
| SB0 | Input/output | Serial data input/output of the serial interface | Input | P25/SI0 |
| SB1 | | | | P26/SO0 |
| $\overline{SCK0}$ | Input/output | Serial clock input/output of the serial interface | Input | P27 |
| $\overline{SCK1}$ | | | | P22 |
| $\overline{SCK2}$ | | | | P72/ASCK |
| STB | Output | Automatic transmitting/receiving strobe output of the serial interface | Input | P23 |
| BUSY | Input | Automatic transmitting/receiving busy input of the serial interface | Input | P24 |
| RxD | Input | Serial data input for asynchronous serial interface | Input | P70/SI2 |
| TxD | Output | Serial data output for asynchronous serial interface | Input | P71/SO2 |
| ASCK | Input | Serial clock input for asynchronous serial interface | Input | P72/$\overline{SCK2}$ |
| TI00 | Input | External count clock input to 16-bit timer (TM0) | Input | P00/INTP0 |
| TI01 | | Capture trigger signal input to capture register (CR00) | | P01/INTP1 |
| TI1 | | External count clock input to 8-bit timer (TM1) | | P33 |
| TI2 | | External count clock input to 8-bit timer (TM2) | | P34 |
| TO0 | Output | 16-bit timer (TM0) output (Can be used together with 14-bit PWM output.) | Input | P30 |
| TO1 | | 8-bit timer (TM1) output | | P31 |
| TO2 | | 8-bit timer (TM2) output | | P32 |



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(2) Non-Port Pins (2/2)

| Pin Name | Input/Output | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| PCL | Output | Clock output (for trimming main system clock and subsystem clock) | Input | P35 |
| BUZ | Output | Buzzer output | Input | P36 |
| RTP0 to RTP7 | Output | Real-time output port which outputs data in synchronization with trigger. | Input | P120 to P127 |
| AD0 to AD7 | Input/output | Low-order address/data bus when expanding memory to the outside. | Input | P40 to P47 |
| A8 to A15 | Output | High-order address bus when expanding memory to the outside. | Input | P50 to P57 |
| $\overline{RD}$ | Output | Strobe signal output for the external memory read operation | Input | P64 |
| $\overline{WR}$ | | Strobe signal output for the external memory write operation | Input | P65 |
| $\overline{WAIT}$ | Input | Wait insertion when accessing external memory | Input | P66 |
| ASTB | Output | Strobe output to externally latches address information which is output to ports 4 and 5 for accessing external memory. | Input | P67 |
| ANI0 to ANI7 | Input | Analog input of A/D converter | Input | P10 to P17 |
| ANO0, ANO1 | Output | Analog output of D/A converter | Input | P130, P131 |
| $AV_{REF0}$ | Input | Reference voltage input of A/D converter | — | — |
| $AV_{REF1}$ | Input | Reference voltage input of D/A converter | — | — |
| $AV_{DD}$ | — | Analog power supply of A/D converter (shared with the port power supply). | — | — |
| $AV_{SS}$ | — | Ground potential of A/D converter and D/A converter (shared with the port ground potential). | — | — |
| $\overline{RESET}$ | Input | System reset input | — | — |
| X1 | Input | Main system clock oscillation crystal connection | — | — |
| X2 | — | | — | — |
| XT1 | Input | Subsystem clock oscillation crystal connection | Input | P07 |
| XT2 | — | | — | — |
| $V_{DD}$ | — | Positive power supply (except for port) | — | — |
| $V_{PP}$ | — | High-voltage applied during program write/verify. Connected to $V_{SS}$ in normal operating mode. | — | — |
| $V_{SS}$ | — | Ground potential (except for port) | — | — |

**Cautions**

**1. The $AV_{DD}$ pin functions as both an A/D converter power supply and a port power supply. When the μPD78P058F is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the $AV_{DD}$ pin to another power supply which has the same potential as $V_{DD}$.**

**2. The $AV_{SS}$ pin functions as both grounds of an A/D converter and D/A converter and of a port. When the μPD78P058F is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the $AV_{SS}$ pin to another ground line than $V_{SS}$.**

### 2.2 Pins in PROM Programming Mode

| Pin Name | Input/Output | Function |
|---|---|---|
| $\overline{\text{RESET}}$ | Input | PROM programming mode setting<br>When +5 V or +12.5 V is applied to the $V_{PP}$ pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode. |
| $V_{PP}$ | Input | PROM programming mode setting and high-voltage applied during program write/verification |
| A0 to A16 | Input | Address bus |
| D0 to D7 | Input/output | Data bus |
| $\overline{\text{CE}}$ | Input | PROM enable input/program pulse input |
| $\overline{\text{OE}}$ | Input | Read strobe input to PROM |
| $\overline{\text{PGM}}$ | Input | Program/program inhibit input in PROM programing mode. |
| $V_{DD}$ | — | Positive power supply |
| $V_{SS}$ | — | Ground potential |



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### 2.3 Pin Input/Output Circuits and Recomended Connection of Unused Pins

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in Table 2-1.
For the configuration of each type of input/output circuit, see Figure 2-1.

**Table 2-1. Pin Input/Output Circuits (1/2)**

| Pin Name | Input/Output Circuit Type | Input/Output | Recommended Connecting Method when Unused |
|---|---|---|---|
| P00/INTP0/TI00 | 2 | Input | Connect to $V_{SS}$. |
| P01/INTP1/TI01 | 8-D | Input/output | Independently connect to $V_{SS}$ through resistor. |
| P02/INTP2 | | | |
| P03/INTP3 | | | |
| P04/INTP4 | | | |
| P05/INTP5 | | | |
| P06/INTP6 | | | |
| P07/XT1 | 16 | Input | Connect to $V_{DD}$. |
| P10/ANI0 to P17/ANI7 | 11-C | Input/output | Independently connect to $V_{DD}$ or $V_{SS}$ through resistor. |
| P20/SI1 | 8-D | | |
| P21/SO1 | 5-J | | |
| P22/$\overline{\text{SCK1}}$ | 8-D | | |
| P23/STB | 5-J | | |
| P24/BUSY | 8-D | | |
| P25/SI0/SB0 | 10-C | | |
| P26/SO0/SB1 | | | |
| P27/$\overline{\text{SCK0}}$ | | | |
| P30/TO0 | 5-J | | |
| P31/TO1 | | | |
| P32/TO2 | | | |
| P33/TI1 | 8-D | | |
| P34/TI2 | | | |
| P35/PCL | 5-J | | |
| P36/BUZ | | | |
| P37 | | | |
| P40/AD0 to P47/AD7 | 5-O | | Independently connect to $V_{DD}$ through resistor. |


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**Table 2-1. Pin Input/Output Circuits (2/2)**

| Pin Name | Input/Output Circuit Type | Input/Output | Recommended Connecting Method when Unused |
|---|---|---|---|
| P50/A8 to P57/A15 | 5-J | Input/output | Independently connect to $V_{DD}$ or $V_{SS}$ through resistor. |
| P60 to P63 | 13-H | | Independently connect to $V_{DD}$ through resistor. |
| P64/$\overline{RD}$ | 5-J | Input/output | Independently connect to $V_{DD}$ or $V_{SS}$. |
| P65/$\overline{WR}$ | | | |
| P66/$\overline{WAIT}$ | | | |
| P67/ASTB | | | |
| P70/SI2/RxD | 8-D | Input/output | |
| P71/SO2/TxD | 5-J | | |
| P72/$\overline{SCK2}$/ASCK | 8-D | | |
| P120/RTP0 to P127/RTP7 | 5-J | Input/output | |
| P130/ANO0, P131/ANO1 | 12-B | Input/output | Independently connect to $V_{SS}$ through resistor. |
| $\overline{RESET}$ | 2 | Input | — |
| XT2 | 16 | — | Leave open. |
| $AV_{REF0}$ | — | | Connect to $V_{SS}$. |
| $AV_{REF1}$ | | | Connect to $V_{DD}$. |
| $AV_{DD}$ | | | Connect to another ground line which has the same potential as $V_{DD}$. |
| $AV_{SS}$ | | | Connect to another power supply which has the same potential as $V_{SS}$. |
| $V_{PP}$ | | | Connect to $V_{SS}$. |

Figure 2-1. Pin Input/Output Circuits (1/2)

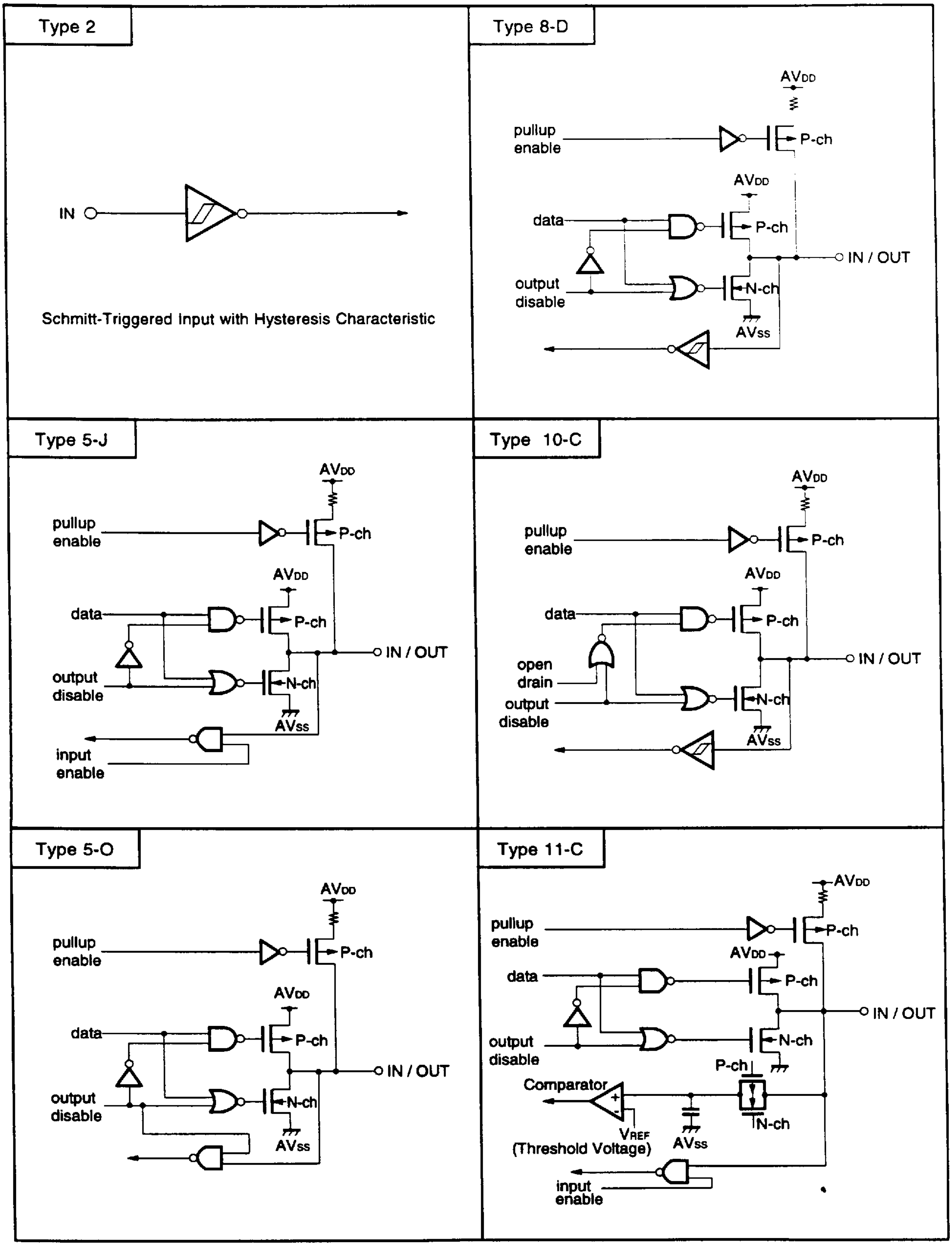
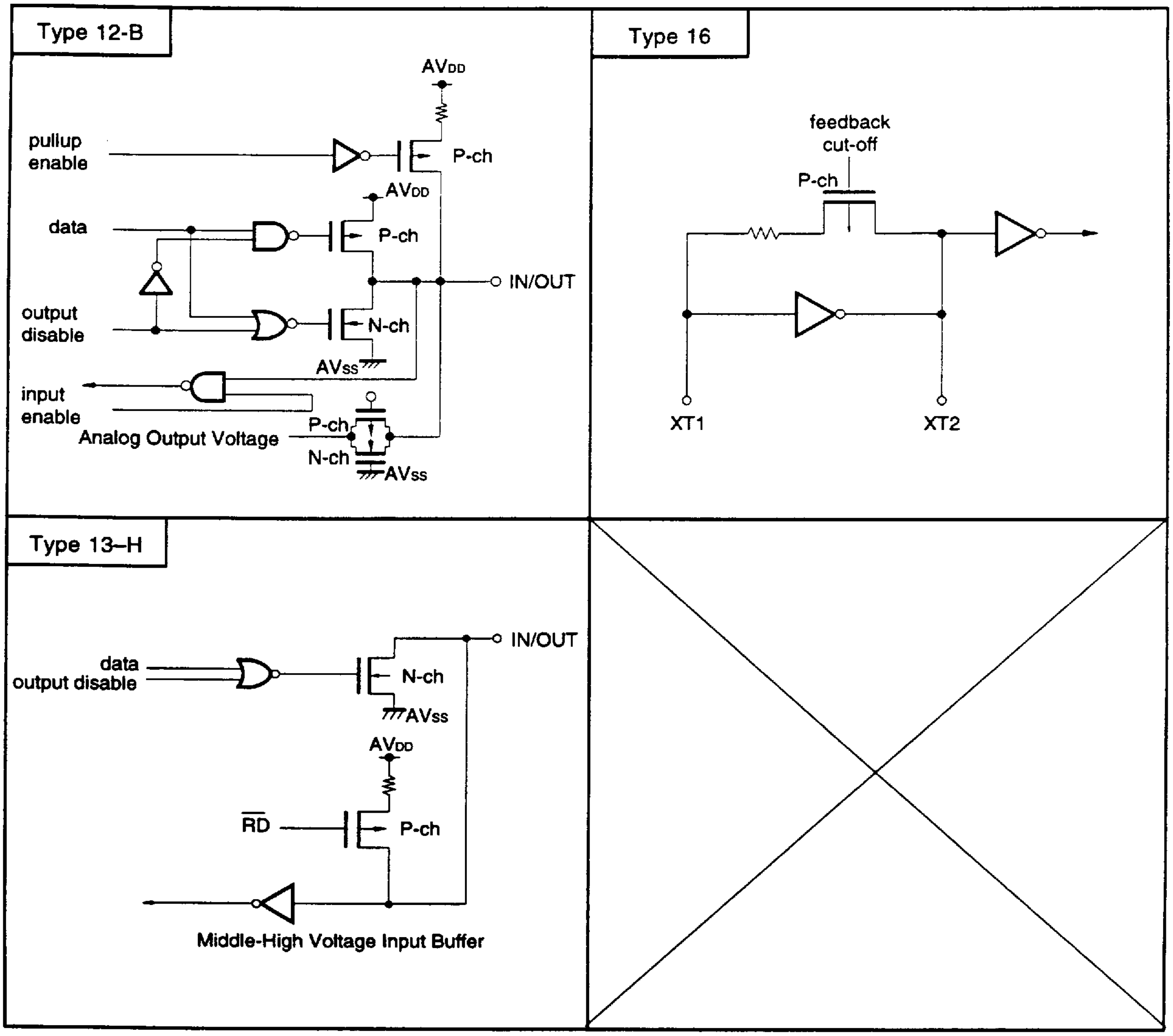


**Figure 2-1. Pin Input/Output Circuits (2/2)**



## 3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM version having different internal memories (ROM).

The IMS is set up by the 8-bit memory manipulation instruction.

CFH will result by the $\overline{\text{RESET}}$ input.

**Figure 3-1. Memory Size Switching Register Format**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After Reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IMS | RAM2 | RAM1 | RAM0 | 0 | ROM3 | ROM2 | ROM1 | ROM0 | FFF0H | CFH | R/W |

| ROM3 | ROM2 | ROM1 | ROM0 | Selection of Internal ROM Capacity |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 48K bytes |
| 1 | 1 | 1 | 0 | 56K bytes[Note] |
| 1 | 1 | 1 | 1 | 60K bytes |
| Other than above | | | | Setting prohibited |

| RAM2 | RAM1 | RAM0 | Selection of Internal High-Speed RAM Capacity |
|---|---|---|---|
| 1 | 1 | 0 | 1024 bytes |
| Other than above | | | Setting prohibited |

**Note** Set the internal ROM capacity to 56K bytes or less when external device expansion function is used.

Table 3-1 shows the setting values of IMS which makes the memory mapping the same as that of the various mask ROM versions.

**Table 3-1. Memory Size Switching Register Setting Values**

| Target Mask ROM Version | IMS Setting Value |
|---|---|
| μPD78056F | CCH |
| μPD78058F | CFH |

## 4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This is a register to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size switching register (IXS), it is possible to get the same memory mapping as that of mask ROM version having different internal expansion RAM.

The IXS is set up by 8-bit memory manipulation instruction.

0AH will result by the $\overline{\text{RESET}}$ input.

**Figure 4-1. Internal Expansion RAM Size Switching Register Format**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After Reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IXS | 0 | 0 | 0 | 0 | IXRAM3 | IXRAM2 | IXRAM1 | IXRAM0 | FFF4H | 0AH | W |

| IXRAM3 | IXRAM2 | IXRAM1 | IXRAM0 | Selection of Internal Expansion RAM Capacity |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 byte |
| 1 | 0 | 1 | 0 | 1024 bytes |
| Other than above | | | | Setting prohibited |

Table 4-1 shows the setting values of IXS which makes the memory mapping the same as that of the various mask ROM versions.

**Table 4-1. Internal Expansion RAM Size Switching Register Setting Values**

| Target Mask ROM Version | IXS Setting Value |
|---|---|
| μPD78056F | 0CH |
| μPD78058F | 0AH |

**Remark** Even if the μPD78P058F program that includes "MOV IXS, #0CH" is implemented on the μPD78056F, its operation will not be affected.

## 5. PROM PROGRAMMING

The $\mu$PD78P058F has an on-chip 60K-byte PROM as a program memory. For programming, set the PROM programming mode by the $V_{PP}$ and $\overline{\text{RESET}}$ pins. For connecting unused pins, refer to **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM Programming Mode."**

**Caution** **Program writing should be performed in the address range 0000H to EFFFH (the last address, EFFFH, should be specified). Writing cannot be performed with a PROM programmer that cannot specify the write addresses.**

### 5.1 Operating Modes

When +5 V or +12.5 V is applied to the $V_{PP}$ pin and a low level signal is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{\text{CE}}$, $\overline{\text{OE}}$ and $\overline{\text{PGM}}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

**Table 5-1. Operating Modes of PROM Programming**

| Pin / Operating Mode | $\overline{\text{RESET}}$ | $V_{PP}$ | $V_{DD}$ | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{PGM}}$ | D0 to D7 |
|---|---|---|---|---|---|---|---|
| Page data latch | L | +12.5 V | +6.5 V | H | L | H | Data input |
| Page write | | | | H | H | L | High-impedance |
| Byte write | | | | L | H | L | Data input |
| Program verify | | | | L | L | H | Data output |
| Program inhibit | | | | × | H | H | High-impedance |
| | | | | × | L | L | |
| Read | | +5 V | +5 V | L | L | H | Data output |
| Output disable | | | | L | H | × | High-impedance |
| Standby | | | | H | × | × | High-impedance |

**Remark** × : L or H



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**(1) Read mode**

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

**(2) Output disable mode**

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.
Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P058F are connected to the data bus.

**(3) Standby mode**

Standby mode is set if $\overline{CE}$ = H is set.
In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

**(4) Page data latch mode**

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.
In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

**(5) Page write mode**

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.
If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

**(6) Byte write mode**

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.
If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

**(7) Program verify mode**

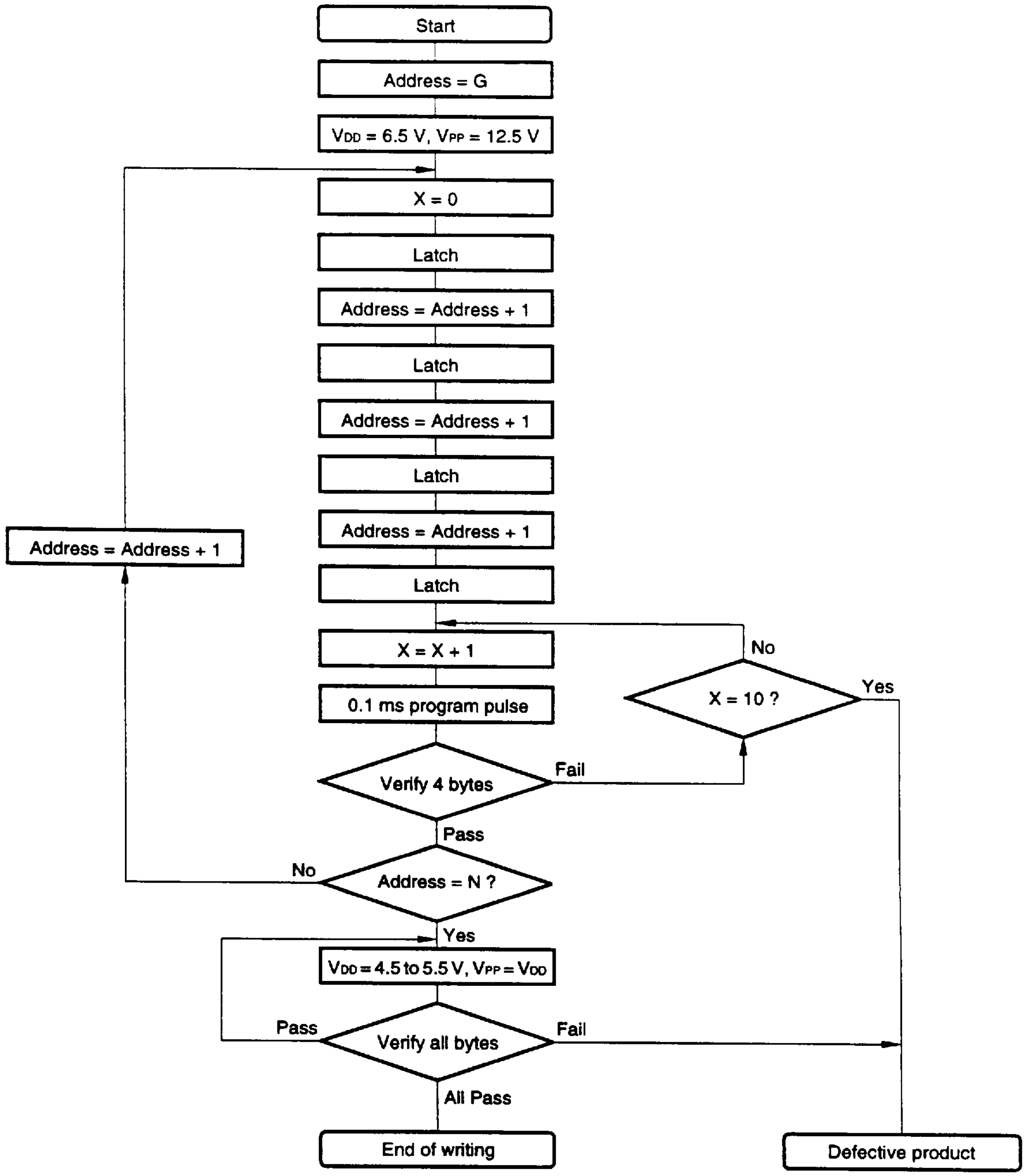
Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.
In this mode, check if a write operation is performed correctly, after the write.

**(8) Program inhibit mode**

Program inhibit mode is used when the $\overline{OE}$ pin, $V_{PP}$ pin, and D0 to D7 pins of multiple μPD78P058Fs are connected in parallel and a write is performed to one of those devices.
When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

### 5.2 PROM Write Pocedure

**Figure 5-1. Page Program Mode Flowchart**




**Remark** G = Start address
N = Program last address

**Figure 5-2. Page Program Mode Timing**

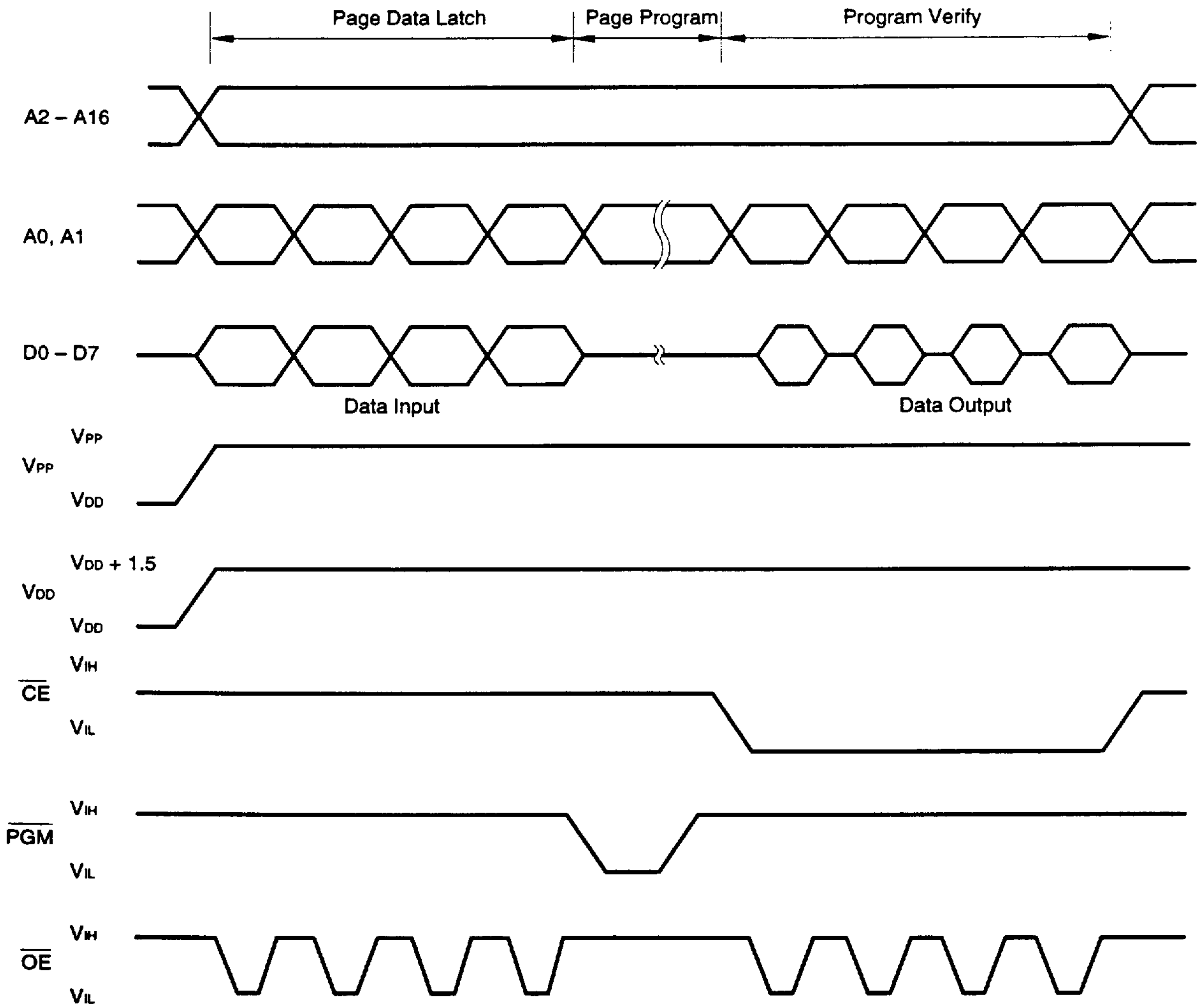
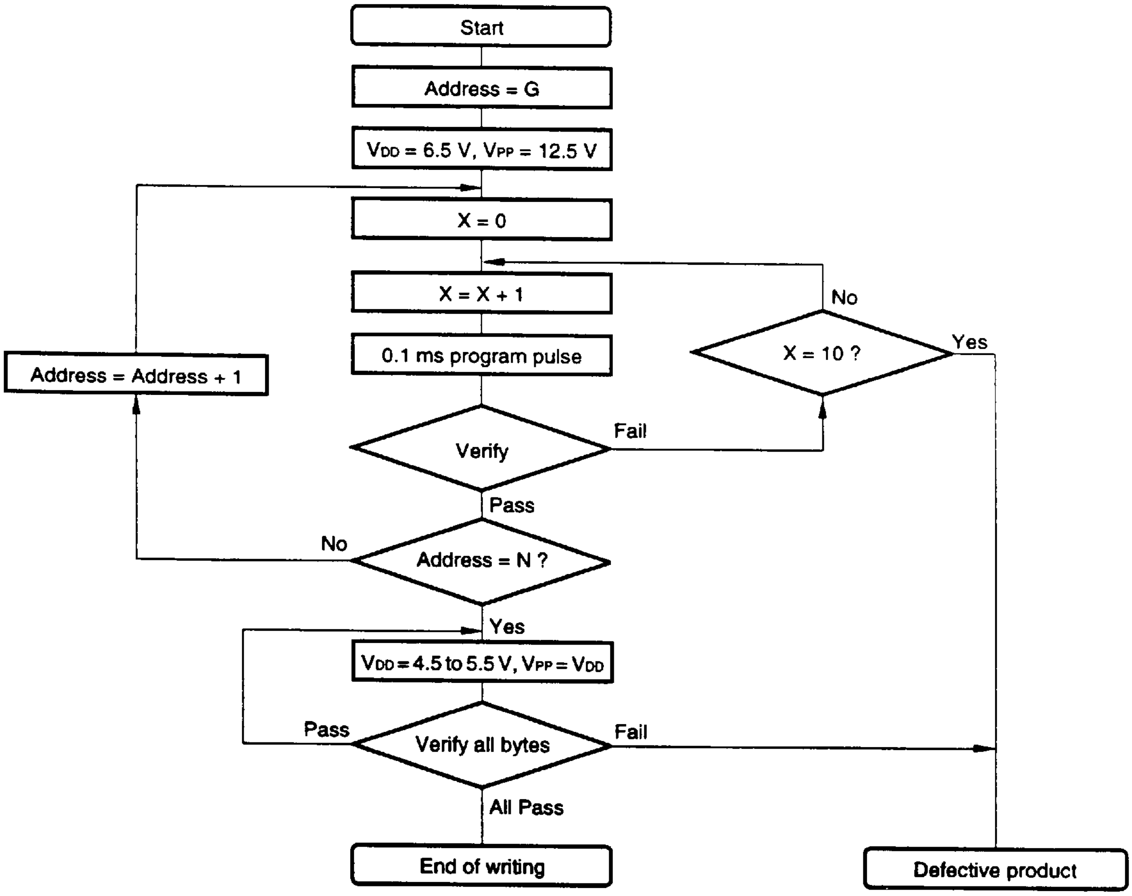
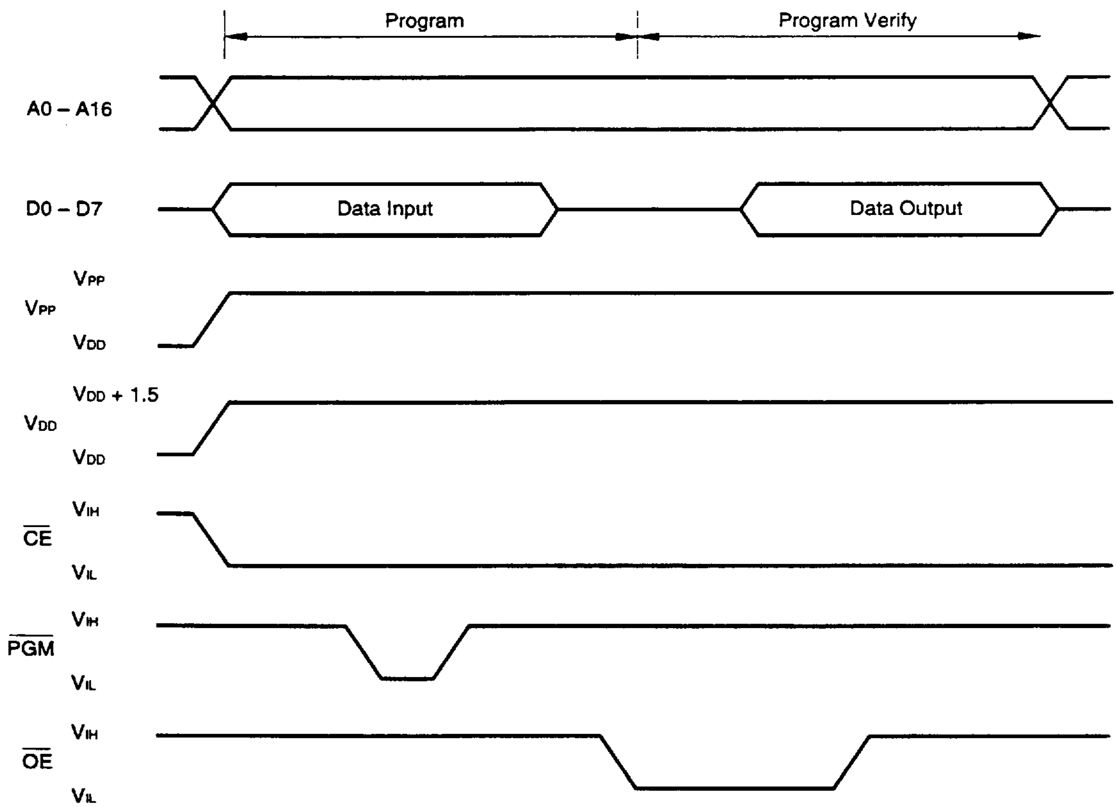


**Figure 5-3. Byte Program Mode Flowchart**




**Remark** G = Start address
N = Program last address

Figure 5-4. Byte Program Mode Timing




**Cautions 1. $V_{DD}$ should be applied before $V_{PP}$ and removed after $V_{PP}$.**

**2. $V_{PP}$ must not exceed +13.5 V including overshoot.**

**3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to $V_{PP}$.**



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### 5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the $V_{PP}$ pin, and connect all other unused pins as shown in **"PIN CONFIGURATION (TOP VIEW) (2) PROM Programming Mode"**.

(2) Supply +5 V to the $V_{DD}$ and $V_{PP}$ pins.

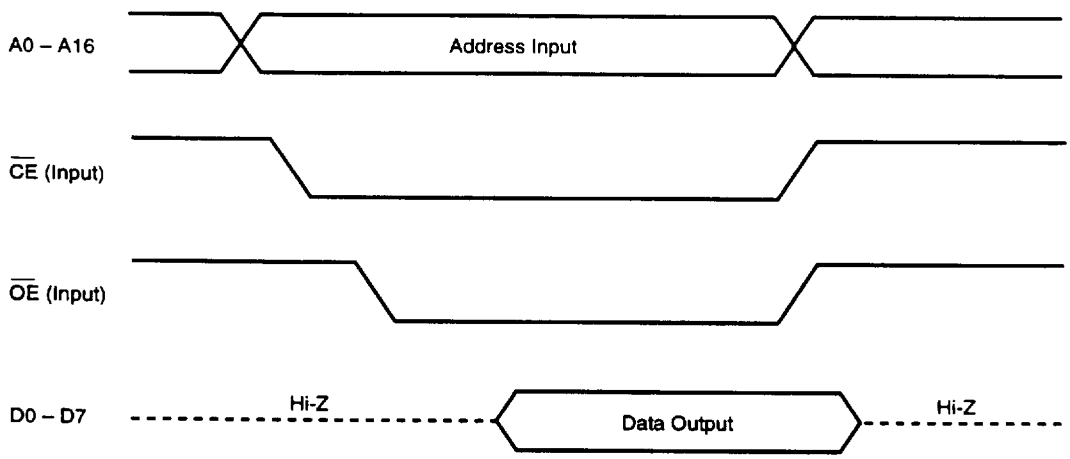
(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

**Figure 5-5. PROM Read Timings**



## 6. SCREENING OF ONE-TIME PROM VERSIONS

The one-time PROM version (μPD78P058FGC-3B9, 78P058FGC-8BT) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

| Storage Temperature | Storage Time |
|---|---|
| 125 °C | 24 hours |

At present, a fee is charged by NEC for one-time PROM after-programming imprinting, screening, and verify service for the QTOP Microcontroller. For details, contact your sales representative.

## 7. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings** ($T_A$ = 25 °C)

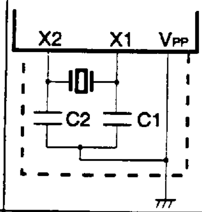
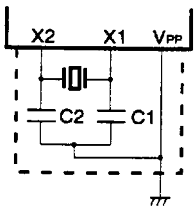
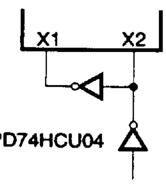
| PARAMETER | SYMBOL | TEST CONDITIONS | | RATING | UNIT |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| | $V_{PP}$ | | | –0.3 to +13.5 | V |
| | $AV_{DD}$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $AV_{REF0}$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $AV_{REF1}$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $AV_{SS}$ | | | –0.3 to + 0.3 | V |
| Input voltage | $V_{I1}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to 47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$ | | –0.3 to $V_{DD}$ + 0.3 | |
| | $V_{I2}$ | P60 to P63 | N-ch open drain | –0.3 to +16 | V |
| | $V_{I3}$ | A9 | PROM programming mode | –0.3 to +13.5 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| Analog input voltage | $V_{AN}$ | P10 to P17 | Analog input pins | $AV_{SS}$ – 0.3 to $AV_{REF0}$ + 0.3 | V |
| Output current, high | $I_{OH}$ | Per pin | | –10 | mA |
| | | Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127 | | –15 | mA |
| | | Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 | | –15 | mA |
| Output current, low | $I_{OL}$ Note | Per pin | peak value | 30 | mA |
| | | | r.m.s. value | 15 | mA |
| | | Total for P50 to P55 | peak value | 100 | mA |
| | | | r.m.s. value | 70 | mA |
| | | Total for P56, P57, P60 to P63 | peak value | 100 | mA |
| | | | r.m.s. value | 70 | mA |
| | | Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 | peak value | 50 | mA |
| | | | r.m.s. value | 20 | mA |
| | | Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127 | peak value | 50 | mA |
| | | | r.m.s value | 20 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Note** r.m.s. values should be calculated as follows: [r.m.s. value] = [peak value] x $\sqrt{\text{Duty}}$

**Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**Main System Clock Oscillator Characteristics** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| RESONATOR | RECOMMENDED CIRCUIT | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |   | Oscillatior frequency (fx)[Note1] | $V_{DD}$ = Oscillation voltage range | 1.0 | | 5.0 | MHz |
| | | Oscillatior stabilization time[Note2] | After $V_{DD}$ has reached MIN. of oscillation voltage range | | | 4 | ms |
| Crystal resonator |   | Oscillatior frequency (fx)[Note1] | | 1.0 | | 5.0 | MHz |
| | | Oscillatior stabilization time[Note2] | $V_{DD}$ = 4.5 to 6.0 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock |   μPD74HCU04 | X1 input frequency (fx)[Note1] | | 1.0 | | 5.0 | MHz |
| | | X1 input high-/low-level width ($t_{XH}$/$t_{XL}$) | | 85 | | 500 | ns |

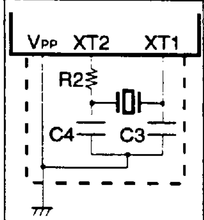
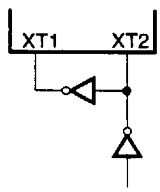
**Notes** 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.
2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

**Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by broken lines to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as $V_{SS}$.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

**2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.**

**Subsystem Clock Oscillator Characteristics** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| RESONATOR | RECOMMENDED CIRCUIT | PARAMETER | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |   | Oscillatior frequency ($f_X$)Note1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillatior stabilization timeNote2 | $V_{DD}$ = 4.5 to 6.0 V | | 1.2 | 2 | s |
| | | | | | | 10 | |
| External clock |   | X1 input frequency ($f_{XT}$)Note1 | | 32 | | 100 | kHz |
| | | X1 input high-/low-level width ($t_{XTH}/t_{XTL}$) | | 5 | | 15 | μs |

**Notes** 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.
2. This is the time required for oscillation to stabilize after power ($V_{DD}$) is turned on.

**Cautions** 1. **When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by broken lines to prevent the influence of wiring capacitance, etc.**

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as VSS.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. **The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.**

**Capacitance** ($T_A$ = 25 °C, $V_{DD}$ = $V_{SS}$ = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz, Measured pins returned to 0 V. | | | | 15 | pF |
| Input/output capacitance | $C_{IO}$ | f = 1 MHz Measured pins returned to 0 | P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131 | | | 15 | pF |
| | | | P60 to P63 | | | 20 | pF |

**Remark** Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** ($T_A$ = –40 to +85°C, $V_{DD}$ = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131 | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | P60 to P63 (N-ch open-drain) | | 0.7 $V_{DD}$ | | 15 | V |
| | $V_{IH4}$ | X1, X2 | | $V_{DD}$ – 0.5 | | $V_{DD}$ | V |
| | $V_{IH5}$ | XT1/P07, XT2 | $V_{DD}$ = 4.5 to 6.0 V | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL2}$ | P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL3}$ | P60 to P63 | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 0.3 $V_{DD}$ | V |
| | | | | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL4}$ | X1, X2 | | 0 | | 0.4 | V |
| | $V_{IL5}$ | XT1/P07, XT2 | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 0.2 $V_{DD}$ | V |
| | | | | 0 | | 0.1 $V_{DD}$ | V |
| Output voltage, high | $V_{OH}$ | $V_{DD}$ = 4.5 to 6.0 V, $I_{OH}$ = – 1mA | | $V_{DD}$ – 1.0 | | | V |
| | | $I_{OH}$ = –100 μA | | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P50 to P57, P60 to P63 | $V_{DD}$ = 4.5 to 6.0 V, $I_{OL}$ = 15 mA | | 0.4 | 2.0 | V |
| | | P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131 | $V_{DD}$ = 4.5 to 6.0 V, $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | SB0, SB1, $\overline{\text{SCK0}}$ | $V_{DD}$ = 4.5 to 6.0 V, N-ch open-drain at pull-up time (R = 1 kΩ) | | | 0.2 $V_{DD}$ | V |
| | $V_{OL3}$ | $I_{OL}$ = 400 μA | | | | 0.5 | V |
| Input leakage current, high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$ | | | 3 | μA |
| | $I_{LIH2}$ | | X1, X2, XT1/P07, XT2 | | | 20 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 15 V | P60 to P63 | | | 80 | μA |

**Remark** Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input leakage current, low | $I_{LIL1}$ | $V_{IN}$ = 0 V | P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$ | | | –3 | $\mu$A |
| | $I_{LIL2}$ | | X1, X2, XT1/P07, XT2 | | | –20 | $\mu$A |
| | $I_{LIL3}$ | | P60 to P63 | | | –3[Note] | $\mu$A |
| Output leakage current, high | $I_{LOH}$ | $V_{OUT}$ = $V_{DD}$ | | | | 3 | $\mu$A |
| Output leakage current, low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | –3 | $\mu$A |
| Software pull-up resistor | $R_2$ | $V_{IN}$ = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131 | $V_{DD}$ = 4.5 to 6.0 V | 15 | 40 | 90 | kΩ |
| | | | | 20 | | 500 | kΩ |

**Note** When the pull-up resistor is not included in P60 to P63 (specified by a mask option), the –200 $\mu$A (MAX.) low-level input leakage current is passed only at the 1.5 clock interval (no wait) when the read instruction to the port6 (P6) and port mode register (PM6) is executed. Other than the 1.5 clock interval, –3 $\mu$A (MAX.) is passed.

**Remark** Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | 5.0 MHz crystal oscillation operating mode ($f_{XX}$ = 2.5 MHz)[Note 2] | $V_{DD}$ = 5.0 V ± 10%[Note 5] | | 5 | 15 | mA |
| | | | $V_{DD}$ = 3.0 V ± 10%[Note 6] | | 0.7 | 2.1 | mA |
| | | 5.0 MHz crystal oscillation operating mode ($f_{XX}$ = 5.0 MHz)[Note 3] | $V_{DD}$ = 5.0 V ± 10%[Note 5] | | 9.0 | 27.0 | mA |
| | | | $V_{DD}$ = 3.0 V ± 10%[Note 6] | | 1.0 | 3.0 | mA |
| | $I_{DD2}$ | 5.0 MHz crystal oscillation HALT mode ($f_{XX}$ = 2.5 MHz)[Note 2] | $V_{DD}$ = 5.0 V ± 10% | | 1.4 | 4.2 | mA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 0.5 | 1.5 | mA |
| | | 5.0 MHz crystal oscillation HALT mode ($f_{XX}$ = 5.0 MHz)[Note 3] | $V_{DD}$ = 5.0 V ± 10% | | 1.6 | 4.8 | mA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 0.65 | 1.95 | mA |
| | $I_{DD3}$ | 32.768 kHz crystal oscillation operating mode[Note 4] | $V_{DD}$ = 5.0 V ± 10% | | 135 | 270 | μA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 95 | 190 | μA |
| | $I_{DD4}$ | 32.768 kHz crystal oscillation HALT mode[Note 4] | $V_{DD}$ = 5.0 V ± 10% | | 25 | 55 | μA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 5 | 15 | μA |
| | $I_{DD5}$ | XT1 = $V_{DD}$ STOP mode Feedback resistor used | $V_{DD}$ = 5.0 V ± 10% | | 1 | 30 | μA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 0.5 | 10 | μA |
| | $I_{DD6}$ | XT1 = $V_{DD}$ STOP mode Feedback resistor not used | $V_{DD}$ = 5.0 V ± 10% | | 0.1 | 30 | μA |
| | | | $V_{DD}$ = 3.0 V ± 10% | | 0.05 | 10 | μA |

**Notes**
1. Passed through the $V_{DD}$ and $AV_{DD}$ pins. Not include the current which is passed through the A/D converter, D/A converter, and on-chip pull-up resistor.
2. fxx = fx/2 operation (when an oscillation mode selection register (OSMS) is set to 00H)
3. fxx = fx operation (when the OSMS is set to 01H)
4. When the main system clock is stopped
5. High-speed mode operation (when a processor clock control register (PCC) is set to 00H)
6. Low-speed mode operation (when the PCC is set to 04H)

**Remarks**
1. fxx : Main system clock frequency (fx or fx/2)
2. fx : Main system clock oscillator frequency

## AC Characteristics

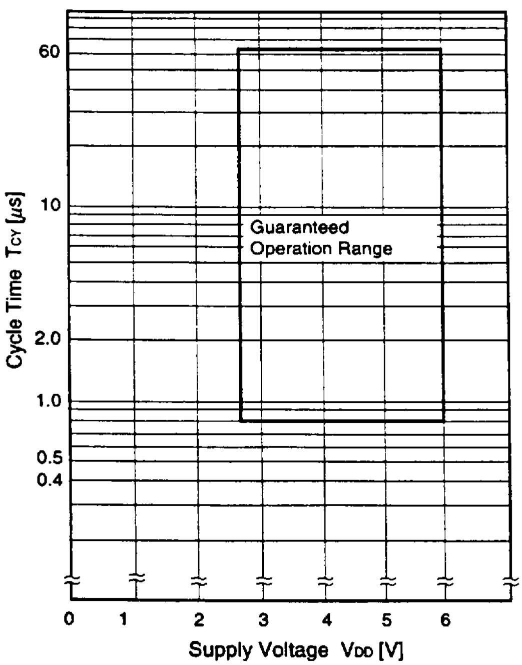
**(1) Basic Operation** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Cycle time (minimum instruction execution time) | $T_{CY}$ | Operating on main system clock | $f_{XX} = f_X/2$ [Note 1] | | 0.8 | | 64 | μs |
| | | | $f_{XX} = f_X$ [Note 2] | $V_{DD}$ = 4.5 to 6.0 V | 0.4 | | 32 | μs |
| | | | | | 0.8 | | 32 | μs |
| | | Operating on subsystem clock | | | 40 | 122 | 125 | μs |
| TI00 input high-/low level width | $t_{TIH00}$, $t_{TIL00}$ | $V_{DD}$ = 4.5 to 6.0 V | | | $2/f_{sam} + 0.1$ [Note 3] | | | μs |
| | | | | | $2/f_{sam} + 0.2$ [Note 3] | | | μs |
| TI01 input high-/low level width | $t_{TIH01}$, $t_{TIL01}$ | | | | 10 | | | μs |
| TI1, TI2 input frequency | $f_{TI1}$ | $V_{DD}$ = 4.5 to 6.0 V | | | 0 | | 4 | MHz |
| | | | | | 0 | | 275 | kHz |
| TI1, TI2 input high-/low-level width | $t_{TIH1}$, $t_{TIL1}$ | $V_{DD}$ = 4.5 to 6.0 V | | | 100 | | | ns |
| | | | | | 1.8 | | | μs |
| Interrupt input high-/low-level width | $t_{INTL}$, $t_{INTH}$ | INTP0 | | $V_{DD}$ = 4.5 to 6.0 V | $2/f_{sam} + 0.1$ [Note 3] | | | μs |
| | | | | | $2/f_{sam} + 0.2$ [Note 3] | | | μs |
| | | INTP1 to INTP6, KR0 to KR7 | | | 10 | | | μs |
| $\overline{RESET}$ low-level width | $t_{RSL}$ | | | | 10 | | | μs |

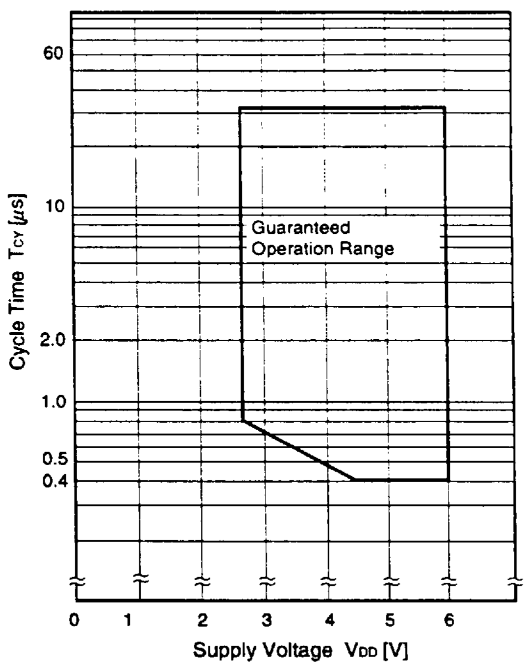
**Notes** 1. When oscillation mode selection register (OSMS) is set to 00H.
2. When OSMS is set to 01H.
3. $f_{sam}$ can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, or $f_{XX}/128$ (N = 0 to 4) by bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (SCS).

**Remarks** 1. $f_{XX}$ : Main system clock frequency ($f_X$ or $f_X/2$)
2. $f_X$ : Main system clock oscillatior frequency

$T_{CY}$ vs $V_{DD}$ (Main System Clock, $f_{XX} = f_X/2$)




$T_{CY}$ vs $V_{DD}$ (Main System Clock, $f_{XX} = f_X$)



(2) **Read/Write Operations**

(a) **When MCS = 1, PCC2 to PCC0 = 000B** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 4.5 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| ASTB high-level width | $t_{ASTH}$ | | 0.85 $t_{CY}$ – 50 | | ns |
| Address setup time | $t_{ADS}$ | | 0.85 $t_{CY}$ – 50 | | ns |
| Address hold time | $t_{ADH}$ | | 50 | | ns |
| Data input time from address | $t_{ADD1}$ | | | (2.85 + 2n)$t_{CY}$ – 80 | ns |
| | $t_{ADD2}$ | | | (4 + 2n)$t_{CY}$ – 100 | ns |
| Data input time from $\overline{\text{RD}}$↓ | $t_{RDD1}$ | | | (2 + 2n)$t_{CY}$ – 100 | ns |
| | $t_{RDD2}$ | | | (2.85 + 2n)$t_{CY}$ – 100 | ns |
| Read data hold time | $t_{RDH}$ | | 0 | | ns |
| $\overline{\text{RD}}$ low-level width | $t_{RDL1}$ | | (2 + 2n)$t_{CY}$ – 60 | | ns |
| | $t_{RDL2}$ | | (2.85 + 2n)$t_{CY}$ – 60 | | ns |
| $\overline{\text{WAIT}}$↓ input time from $\overline{\text{RD}}$↓ | $t_{RDWT1}$ | | | 0.85 $t_{CY}$ – 50 | ns |
| | $t_{RDWT2}$ | | | 2 $t_{CY}$ – 60 | ns |
| $\overline{\text{WAIT}}$↓ input time from $\overline{\text{WR}}$↓ | $t_{WRWT}$ | | | 2 $t_{CY}$ – 60 | ns |
| $\overline{\text{WAIT}}$ low-level width | $t_{WTL}$ | | (1.15 + 2n)$t_{CY}$ | (2 + 2n)$t_{CY}$ | ns |
| Write data setup time | $t_{WDS}$ | | (2.85 + 2n)$t_{CY}$ – 100 | | ns |
| Write data hold time | $t_{WDH}$ | | 20 | | ns |
| $\overline{\text{WR}}$ low-level width | $t_{WRL1}$ | | (2.85 + 2n)$t_{CY}$ – 60 | | ns |
| $\overline{\text{RD}}$↓ delay time from ASTB↓ | $t_{ASTRD}$ | | 25 | | ns |
| $\overline{\text{WR}}$↓ delay time from ASTB↓ | $t_{ASTWR}$ | | 0.85 $t_{CY}$ + 20 | | ns |
| ASTB↑delay time from $\overline{\text{RD}}$↑ in external fetch | $t_{RDAST}$ | | 0.85 $t_{CY}$ – 10 | 1.15 $t_{CY}$ + 20 | ns |
| Address hold time from $\overline{\text{RD}}$↑ in external fetch | $t_{RDADH}$ | | 0.85 $t_{CY}$ – 50 | 1.15 $t_{CY}$ + 50 | ns |
| Write data output time from $\overline{\text{RD}}$↑ | $t_{RDWD}$ | | 40 | | ns |
| Write data output time from $\overline{\text{WR}}$↓ | $t_{WRWD}$ | | 0 | 50 | ns |
| Address hold time from $\overline{\text{WR}}$↑ | $t_{WRADH}$ | | 0.85 $t_{CY}$ | 1.15 $t_{CY}$ + 40 | ns |
| $\overline{\text{RD}}$↑ delay time from $\overline{\text{WAIT}}$↑ | $t_{WTRD}$ | | 1.15 $t_{CY}$ + 40 | 3.15 $t_{CY}$ + 40 | ns |
| $\overline{\text{WR}}$↑ delay time from $\overline{\text{WAIT}}$↑ | $t_{WTWR}$ | | 1.15 $t_{CY}$ + 30 | 3.15 $t_{CY}$ + 30 | ns |

**Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
3. $t_{CY}$ = $T_{CY}$/4
4. n indicates the number of waits.

**(b) Except when MCS = 1, PCC2 to PCC0 = 000B** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| ASTB high-level width | $t_{ASTH}$ | | $t_{CY}$ – 80 | | ns |
| Address setup time | $t_{ADS}$ | | $t_{CY}$ – 80 | | ns |
| Address hold time | $t_{ADH}$ | | 0.4 $t_{CY}$ – 10 | | ns |
| Data input time from address | $t_{ADD1}$ | | | (3 + 2n)$t_{CY}$ – 160 | ns |
| | $t_{ADD2}$ | | | (4 + 2n)$t_{CY}$ – 200 | ns |
| Data input time from $\overline{\text{RD}}\downarrow$ | $t_{RDD1}$ | | | (1.4 + 2n)$t_{CY}$ – 70 | ns |
| | $t_{RDD2}$ | | | (2.4 + 2n)$t_{CY}$ – 70 | ns |
| Read data hold time | $t_{RDH}$ | | 0 | | ns |
| $\overline{\text{RD}}$ low-level width | $t_{RDL1}$ | | (1.4 + 2n)$t_{CY}$ – 20 | | ns |
| | $t_{RDL2}$ | | (2.4 + 2n)$t_{CY}$ – 20 | | ns |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{RD}}\downarrow$ | $t_{RDWT1}$ | | | $t_{CY}$ – 100 | ns |
| | $t_{RDWT2}$ | | | 2 $t_{CY}$ – 100 | ns |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{WR}}\downarrow$ | $t_{WRWT}$ | | | 2$t_{CY}$ – 100 | ns |
| $\overline{\text{WAIT}}$ low-level width | $t_{WTL}$ | | (1 + 2n)$t_{CY}$ | (2 + 2n)$t_{CY}$ | ns |
| Write data setup time | $t_{WDS}$ | | (2.4 + 2n)$t_{CY}$ – 60 | | ns |
| Write data hold time | $t_{WDH}$ | | 20 | | ns |
| $\overline{\text{WR}}$ low-level width | $t_{WRL1}$ | | (2.4 + 2n)$t_{CY}$ – 20 | | ns |
| $\overline{\text{RD}}\downarrow$ delay time from ASTB$\downarrow$ | $t_{ASTRD}$ | | 0.4 $t_{CY}$ – 30 | | ns |
| $\overline{\text{WR}}\downarrow$ delay time from ASTB$\downarrow$ | $t_{ASTWR}$ | | 1.4 $t_{CY}$ – 30 | | ns |
| ASTB$\uparrow$delay time from $\overline{\text{RD}}\uparrow$ in external fetch | $t_{RDAST}$ | | $t_{CY}$ – 10 | $t_{CY}$ + 20 | ns |
| Address hold time from $\overline{\text{RD}}\uparrow$ in external fetch | $t_{RDADH}$ | | $t_{CY}$ – 50 | $t_{CY}$ + 50 | ns |
| Write data output time from $\overline{\text{RD}}\uparrow$ | $t_{RDWD}$ | | 0.4$t_{CY}$ – 20 | | ns |
| Write data output time from $\overline{\text{WR}}\downarrow$ | $t_{WRWD}$ | | 0 | 60 | ns |
| Address hold time from $\overline{\text{WR}}\uparrow$ | $t_{WRADH}$ | | $t_{CY}$ | $t_{CY}$ + 60 | ns |
| $\overline{\text{RD}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$ | $t_{WTRD}$ | | 0.6 $t_{CY}$ + 180 | 2.6 $t_{CY}$ + 180 | ns |
| $\overline{\text{WR}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$ | $t_{WTWR}$ | | 0.6 $t_{CY}$ + 120 | 2.6 $t_{CY}$ + 120 | ns |

**Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
3. $t_{CY}$ = $T_{CY}$/4
4. n indicates the number of waits.

(3) **Serial Interface** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V)

(a) **Serial interface channel 0**

(i) **3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH1}$, $t_{KL1}$ | $V_{DD}$ = 4.5 to 6.0 V | $t_{KCY1}/2 - 50$ | | | ns |
| | | | $t_{KCY1}/2 - 100$ | | | ns |
| SI0 setup time (to $\overline{SCK0}$↑) | $t_{SIK1}$ | $V_{DD}$ = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI0 hold time (from $\overline{SCK0}$↑) | $t_{KSI1}$ | | 400 | | | ns |
| SO0 output delay time from $\overline{SCK0}$↓ | $t_{KSO1}$ | C = 100 pF[Note] | | | 300 | ns |

**Note** C is the $\overline{SCK0}$ and SO0 output line load capacitance.

(ii) **3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH2}$, $t_{KL2}$ | $V_{DD}$ = 4.5 to 6.0 V | 400 | | | ns |
| | | | 800 | | | ns |
| SI0 setup time (to $\overline{SCK0}$↑) | $t_{SIK2}$ | | 100 | | | ns |
| SI0 hold time (from $\overline{SCK0}$↑) | $t_{KSI2}$ | | 400 | | | ns |
| SO0 output delay time from $\overline{SCK0}$↓ | $t_{KSO2}$ | C = 100 pF[Note] | | | 300 | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R2}$, $t_{F2}$ | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

**Note** C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY3}$ | $V_{DD}$ = 4.5 to 6.0 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH3}$, | $V_{DD}$ = 4.5 to 6.0 V | | $t_{KCY3}/2 - 50$ | | | ns |
| | $t_{KL3}$ | | | $t_{KCY3}/2 - 100$ | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK3}$ | $V_{DD}$ = 4.5 to 6.0 V | | 100 | | | ns |
| | | | | 300 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI3}$ | | | $t_{KCY3}/2$ | | | ns |
| SB0, SB1 output delay time from | $t_{KSO3}$ | R = 1 kΩ, | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 250 | ns |
| $\overline{SCK0}$↓ | | C = 100 pF[Note] | | 0 | | 1000 | ns |
| SB0, SB1↓ from $\overline{SCK0}$↑ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| $\overline{SCK0}$↓ from SB0, SB1↓ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, SB1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |
| SB0, SB1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |

**Note** R and C are the $\overline{SCK0}$, SB0, and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY4}$ | $V_{DD}$ = 4.5 to 6.0 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH4}$, | $V_{DD}$ = 4.5 to 6.0 V | | 400 | | | ns |
| | $t_{KL4}$ | | | 1600 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK4}$ | $V_{DD}$ = 4.5 to 6.0 V | | 100 | | | ns |
| | | | | 300 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI4}$ | | | $t_{KCY4}/2$ | | | ns |
| SB0, SB1 output delay time from | $t_{KSO4}$ | R = 1 kΩ, | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 300 | ns |
| $\overline{SCK0}$↓ | | C = 100 pF[Note] | | 0 | | 1000 | ns |
| SB0, SB1↓ from $\overline{SCK0}$↑ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK0}$↓ from SB0, SB1↓ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, SB1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |
| SB0, SB1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R4}$, $t_{F4}$ | When using external device expansion function | | | | 160 | ns |
| | | When not using external device expansion function | | | | 1000 | ns |

**Note** R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY5}$ | R = 1 kΩ, C = 100 pF[Note] | | 1600 | | | ns |
| $\overline{SCK0}$ high-level width | $t_{KH5}$ | | | $t_{KCY5}/2 - 160$ | | | ns |
| $\overline{SCK0}$ low-level width | $t_{KL5}$ | | $V_{DD}$ = 4.5 to 6.0 V | $t_{KCY5}/2 - 50$ | | | ns |
| | | | | $t_{KCY5}/2 - 100$ | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK5}$ | | $V_{DD}$ = 4.5 to 6.0 V | 300 | | | ns |
| | | | | 350 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI5}$ | | | 600 | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO5}$ | | | 0 | | 300 | ns |

**Note** R and C are the $\overline{SCK0}$, SB0, and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY6}$ | | | 1600 | | | ns |
| $\overline{SCK0}$ high-level width | $t_{KH6}$ | | | 650 | | | ns |
| $\overline{SCK0}$ low-level width | $t_{KL6}$ | | | 800 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK6}$ | | | 100 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI6}$ | | | $t_{KCY6}/2$ | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO6}$ | R = 1 kΩ, C = 100 pF[Note] | $V_{DD}$ = 4.5 to 6.0 V | 0 | | 300 | ns |
| | | | | 0 | | 500 | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R6}$, $t_{F6}$ | When using external device expansion function | | | | 160 | ns |
| | | When not using external device expansion function | | | | 1000 | ns |

**Note** R and C are the SB0 and SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$...internal clock output)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{\text{SCK1}}$ cycle time | $t_{KCY7}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | $t_{KH7}$, | $V_{DD}$ = 4.5 to 6.0 V | $t_{KCY7}/2 - 50$ | | | ns |
| | $t_{KL7}$ | | $t_{KCY7}/2 - 100$ | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}$↑) | $t_{SIK7}$ | $V_{DD}$ = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI1 hold time (to $\overline{\text{SCK1}}$ ↑ ) | $t_{KSI7}$ | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}$↓ | $t_{KSO7}$ | C = 100 pF Note | | | 300 | ns |

**Note** C is the $\overline{\text{SCK1}}$ and SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$...external clock output)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{\text{SCK1}}$ cycle time | $t_{KCY8}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | $t_{KH8}$, | $V_{DD}$ = 4.5 to 6.0 V | 400 | | | ns |
| | $t_{KL8}$ | | 800 | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}$ ↑) | $t_{SIK8}$ | | 100 | | | ns |
| SI1 hold time (to $\overline{\text{SCK1}}$ ↑) | $t_{KSI8}$ | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}$ | $t_{KSO8}$ | C = 100 pF Note | | | 300 | ns |
| $\overline{\text{SCK1}}$ rise, fall time | $t_{R8}$, $t_{F8}$ | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

**Note** C is the SO1 output line load capacitance.

**(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY9}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH9}$, | $V_{DD}$ = 4.5 to 6.0 V | $t_{KCY9}/2 - 50$ | | | ns |
| | $t_{KL9}$ | | $t_{KCY9}/2 - 100$ | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK9}$ | $V_{DD}$ = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI9}$ | | 400 | | | ns |
| SO1 output delay time from $\overline{SCK1}$↓ | $t_{KSO9}$ | C = 100 pF[Note] | | | 300 | ns |
| STB↑ from $\overline{SCK1}$↑ | $t_{SBD}$ | | $t_{KCY9}/2 - 100$ | | $t_{KCY9}/2 + 100$ | ns |
| Strobe signal high-level width | $t_{SBW}$ | | $t_{KCY9} - 30$ | | $t_{KCY9} + 30$ | ns |
| Busy signal setup time (to busy signal detection timing) | $t_{BYS}$ | | 100 | | | ns |
| Busy signal hold time (from busy signal detection timing) | $t_{BYH}$ | $V_{DD}$ = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| $\overline{SCK1}$↓ from busy inactivation | $t_{SPS}$ | | | | $2t_{KCY9}$ | ns |

**Note** C is the $\overline{SCK1}$ and SO1 output line load capacitance.

**(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY10}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH10}$, | $V_{DD}$ = 4.5 to 6.0 V | 400 | | | ns |
| | $t_{KL10}$ | | 800 | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK10}$ | | 100 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI10}$ | | 400 | | | ns |
| SO output delay time from $\overline{SCK1}$↓ | $t_{KSO10}$ | C = 100 pF[Note] | | | 300 | ns |
| $\overline{SCK1}$ rise, fall time | $t_{R10}$, $t_{F10}$ | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

**Note** C is the SO1 output line load capacitance.



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**(c) Serial interface channel 2**

**(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$...internal clock output)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{\text{SCK2}}$ cycle time | $t_{KCY11}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK2}}$ high-/low-level width | $t_{KH11}$, | $V_{DD}$ = 4.5 to 6.0 V | $t_{KCY11}/2 - 50$ | | | ns |
| | $t_{KL11}$ | | $t_{KCY11}/2 - 100$ | | | ns |
| SI2 setup time (to $\overline{\text{SCK2}}$↑) | $t_{SIK11}$ | $V_{DD}$ = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI2 hold time (to $\overline{\text{SCK2}}$↑) | $t_{KSI11}$ | | 400 | | | ns |
| SO2 output delay time from $\overline{\text{SCK2}}$↓ | $t_{KSO11}$ | C = 100 pF[Note] | | | 300 | ns |

**Note** C is the load capacitance of $\overline{\text{SCK2}}$ and SO2 output lines.

**(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$...external clock output)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\overline{\text{SCK2}}$ cycle time | $t_{KCY12}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK2}}$ high-/low-level width | $t_{KH12}$, | $V_{DD}$ = 4.5 to 6.0 V | 400 | | | ns |
| | $t_{KL12}$ | | 800 | | | ns |
| SI2 setup time (to $\overline{\text{SCK2}}$ ↑) | $t_{SIK12}$ | | 100 | | | ns |
| SI2 hold time (to $\overline{\text{SCK2}}$ ↑) | $t_{KSI12}$ | | 400 | | | ns |
| SO2 output delay time from $\overline{\text{SCK2}}$↓ | $t_{KSO12}$ | C = 100 pF[Note] | | | 300 | ns |
| $\overline{\text{SCK2}}$ rise, fall time | $t_{R12}$, $t_{F12}$ | $V_{DD}$ = 4.5 to 6.0 V, when not using external device expansion function | | | 1000 | ns |
| | | | | | 160 | ns |

**Note** C is the SO2 output line load capacitance.

(iii) UART mode (Dedicated baud rate generator output)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Transfer rate | | $V_{DD}$ = 4.5 to 6.0 V | | | 78125 | bps |
| | | | | | 39063 | bps |

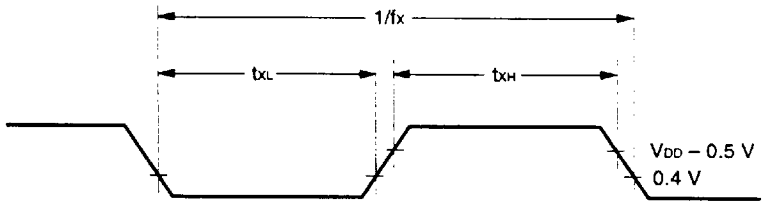
(iv) UART mode (External clock input)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| ASCK cycle time | $t_{KCY13}$ | $V_{DD}$ = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| ASCK high-/low-level width | $t_{KH13}$, $t_{KL13}$ | $V_{DD}$ = 4.5 to 6.0 V | 400 | | | ns |
| | | | 800 | | | ns |
| Transfer rate | | $V_{DD}$ = 4.5 to 6.0 V | | | 39063 | bps |
| | | | | | 19531 | bps |
| $\overline{SCK}$ rise, fall time | $t_{R13}$, $t_{F13}$ | $V_{DD}$ = 4.5 to 6.0 V, when not using external device expansion function | | | 1000 | ns |
| | | | | | 160 | ns |

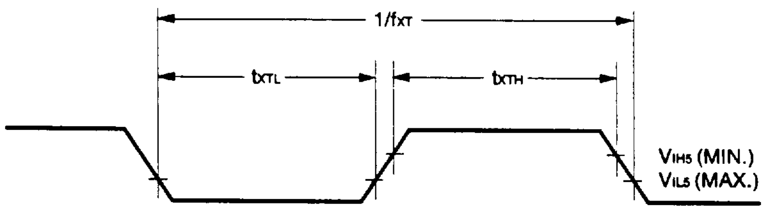
**AC Timing Test Point (Excluding X1, XT1 Input)**


**Clock Timing**

X1 Input

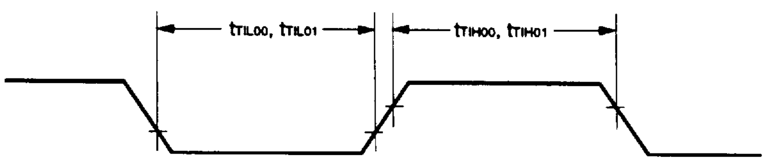



XT1 Input

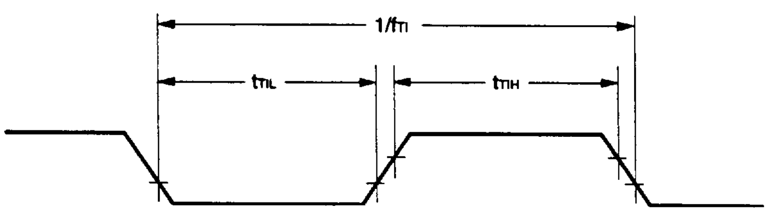



**TI Timing**

TI00, TI01

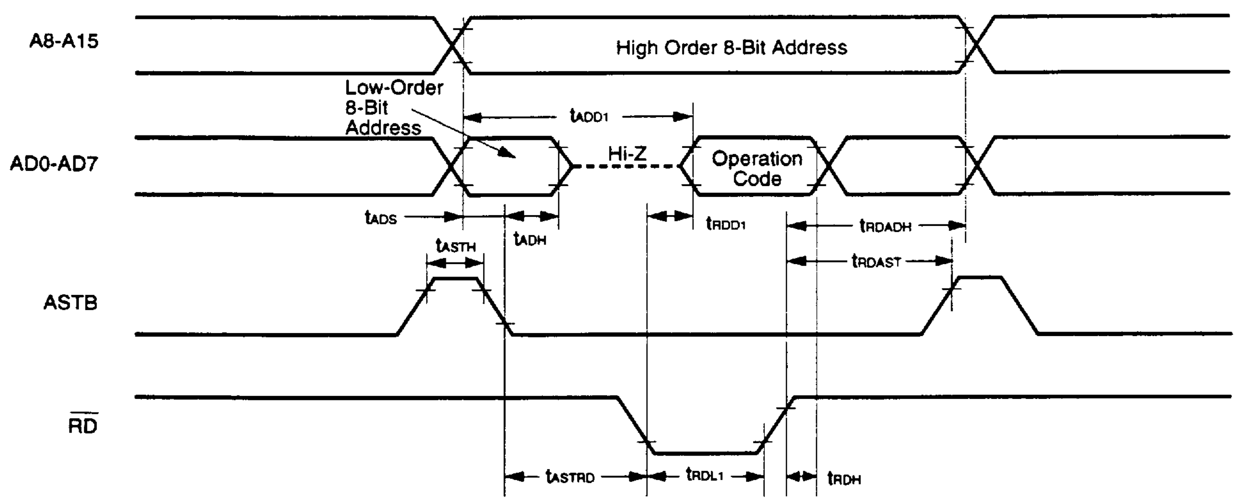



TI1, TI2

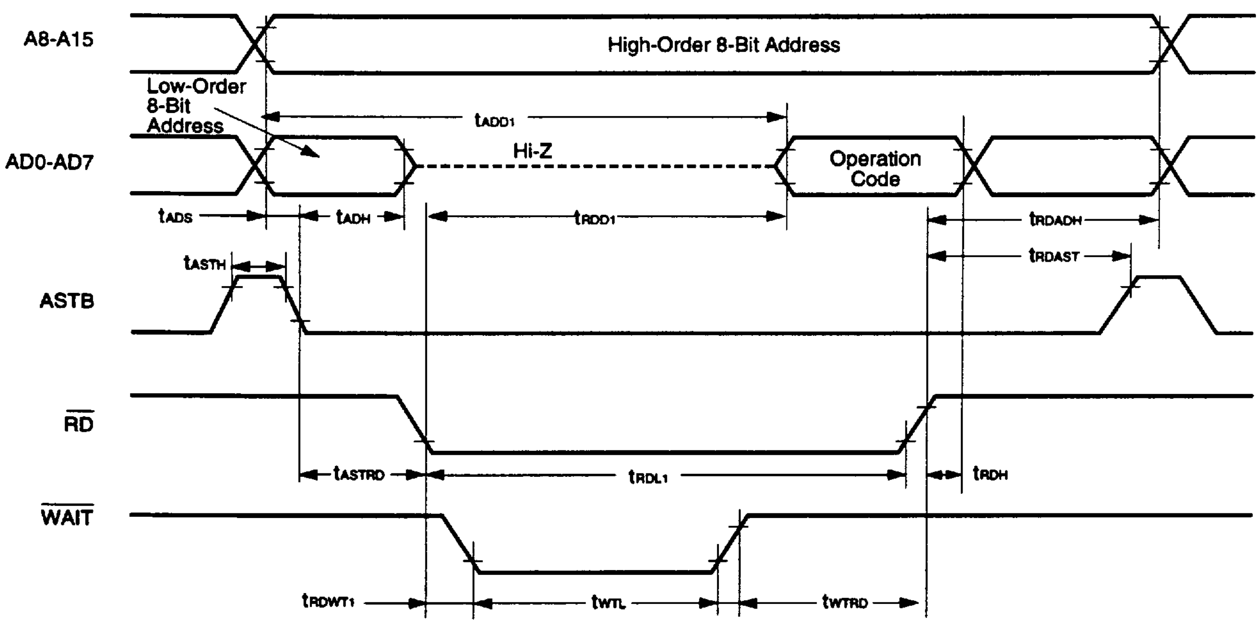


Read/Write Operations

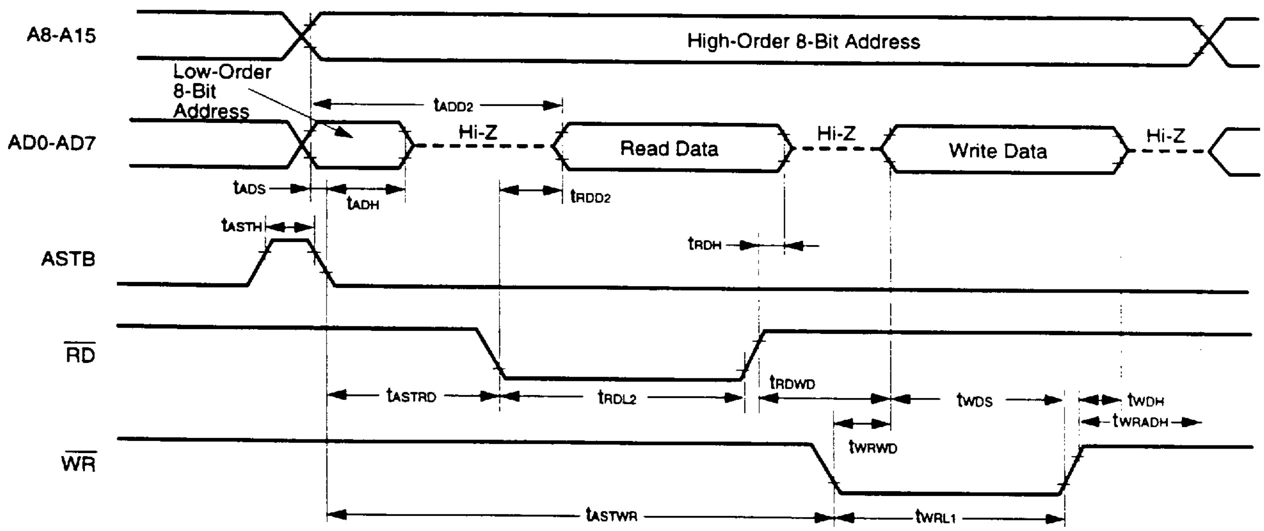
**External fetch (no wait):**



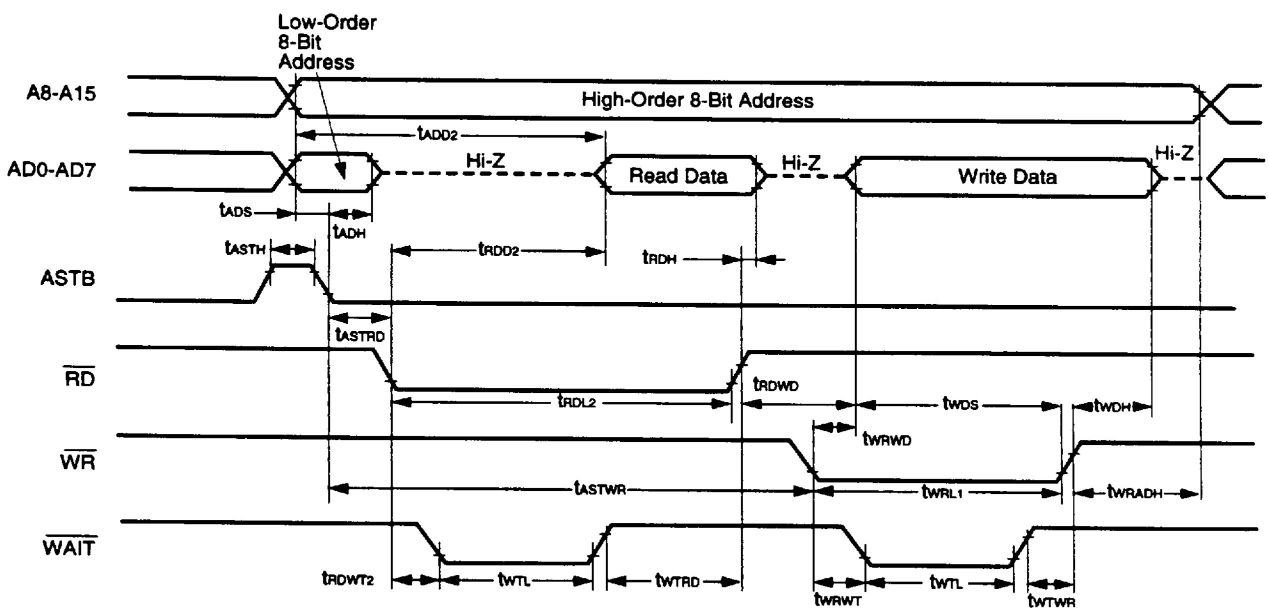

**External fetch (wait insertion):**



**External data access (no wait):**




**External data access (wait insertion):**



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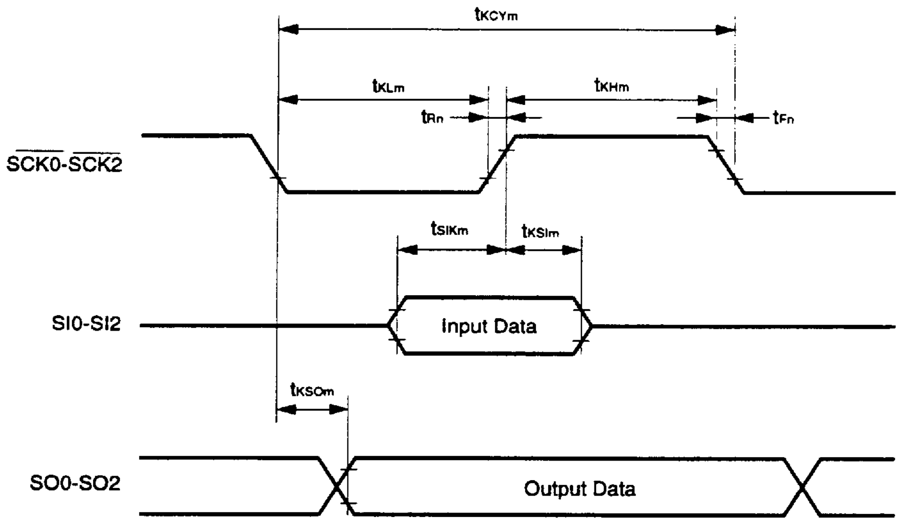
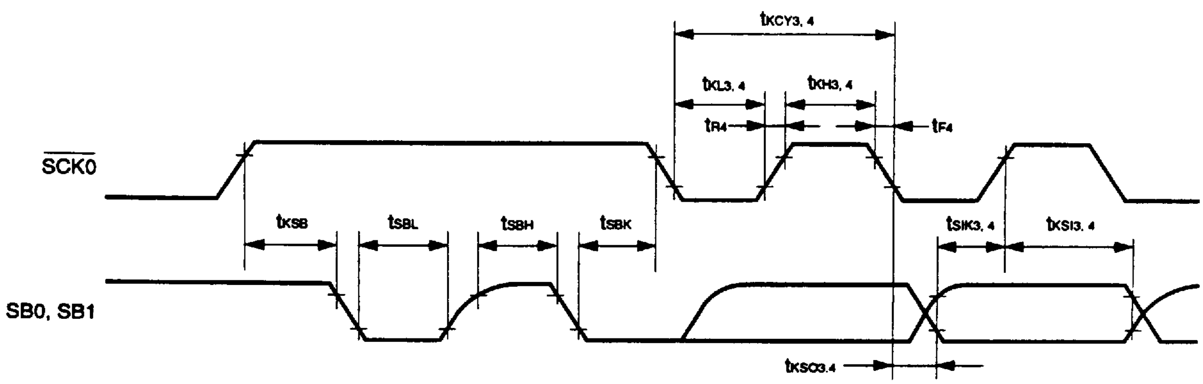
Serial Transfer Timing

**3-wire serial I/O mode:**

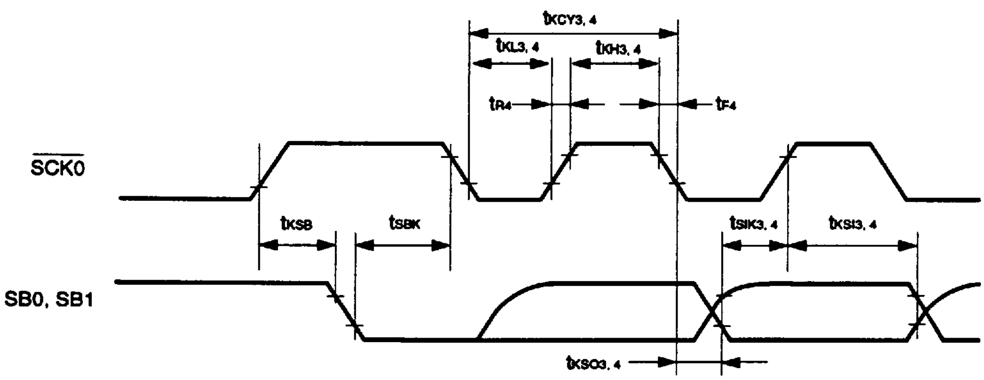



**Remark** m = 1, 2, 7, 8, 11 or 12
n = 2, 8, or 12

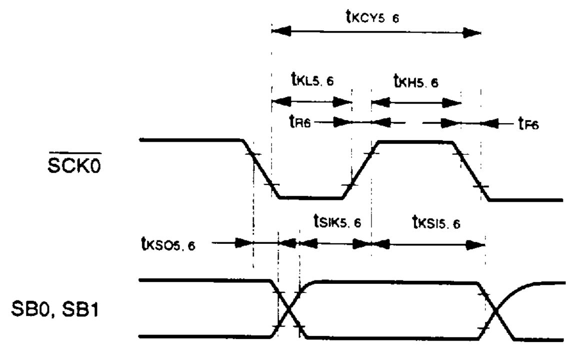
**SBI mode (bus release signal transfer):**



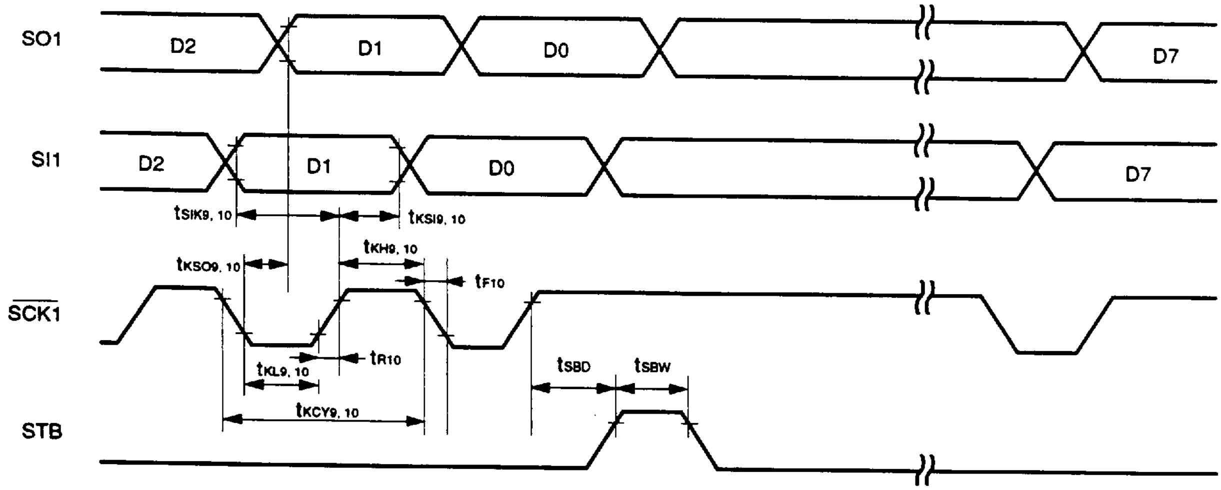

**SBI mode (command signal transfer):**



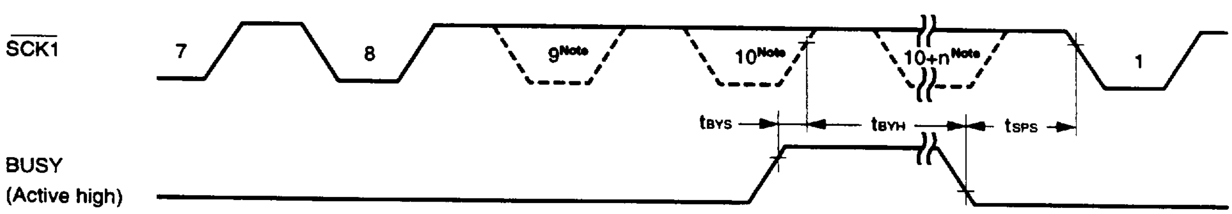
**2-wire serial I/O mode:**




**Automatic transmission/reception function 3-wire serial I/O mode:**

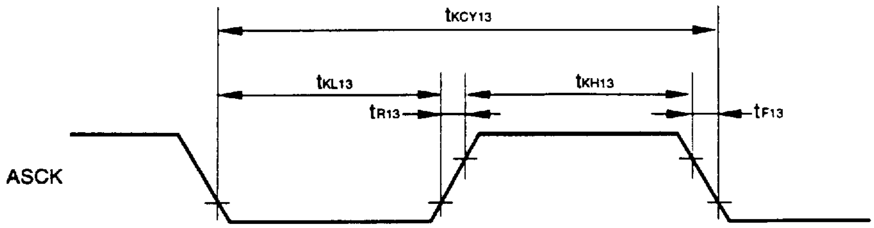



**Automatic transmission/reception function 3-wire serial I/O mode (busy processing):**




**Note** The signal is not actually low here, but is represented in this way to show the timing.

**UART mode (external Clock Input):**



**A/D Converter Characteristics** ($T_A$ = –40 to +85 °C, $AV_{DD}$ = $V_{DD}$ = 2.7 to 6.0 V, $AV_{SS}$ = $V_{SS}$ = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Resolution | | | 8 | 8 | 8 | bit |
| Total error[Note] | | 2.7 V ≤ $AV_{REF0}$ ≤ $AV_{DD}$ | | | 1.4 | % |
| Conversion time | $t_{CONV}$ | | 19.1 | | 200 | μs |
| Sampling time | $t_{SAMP}$ | | 12/fxx | | | μs |
| Analog input voltage | $V_{IAN}$ | | $AV_{SS}$ | | $AV_{REF0}$ | V |
| Reference voltage | $AV_{REF0}$ | | 2.7 | | $AV_{DD}$ | V |
| $AV_{REF0}$-$AV_{SS}$ resistance | $R_{AIREF0}$ | | 4 | 14 | | kΩ |

**Note** Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

**Caution For pins which also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept (except for LCD segment output alternate-function pin).**
**<1> Rewrite the output latch while the pin is used as a port pin.**
**<2> Change the output level of the pin used as an output pin, even if it is not used as a port pin.**

**Remarks 1.** fxx : Main system clock frequency (fx or fx/2)
**2.** fx : Main system clock oscillatior frequency

**D/A Converter Characteristics** ($T_A$ = –40 to +85 °C, $V_{DD}$ = 2.7 to 6.0 V, $AV_{SS}$ = $V_{SS}$ = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Resolution | | | | | 8 | bit |
| Total error | | R = 2 MΩ[Note 1] | | | 1.2 | % |
| | | R = 4 MΩ[Note 1] | | | 0.8 | % |
| | | R = 10 MΩ[Note 1] | | | 0.6 | % |
| Settling time | | C = 30 pF[Note 1], 4.5 V ≤ $AV_{REF1}$ ≤ 6.0 V | | | 10 | μs |
| | | C = 30 pF[Note 1], 2.7 V ≤ $AV_{REF1}$ < 4.5 V | | | 15 | μs |
| Output resistor | $R_O$ | **Note 2** | | 10 | | kΩ |
| Analog reference voltage | $AV_{REF1}$ | | 2.0 | | $V_{DD}$ | V |
| Resistance between $AV_{REF1}$ and $AV_{SS}$ | $R_{AIREF1}$ | DACS0, DACS1 = 55H[Note 2] | 4 | 8 | | mA |

**Notes 1.** R and C are the D/A converter output pin load resistance and load capacitance.
**2.** Value for one D/A converter channel.

**Remark** DACS0, DACS1 : D/A conversion value setting register 0, 1

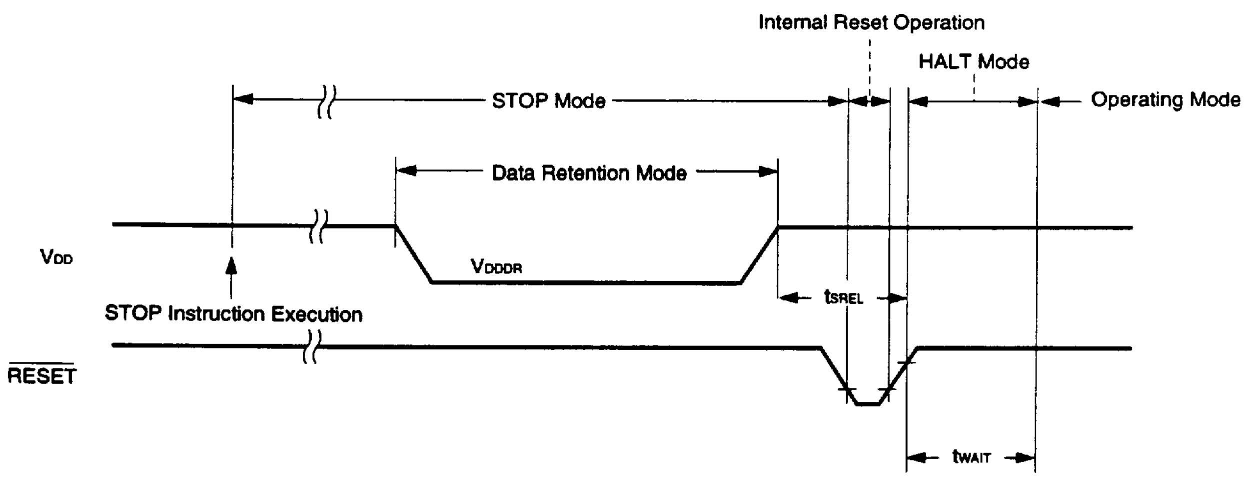
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A$ = –40 to +85 °C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.8 | | 6.0 | V |
| Data retention supply current | $I_{DDDR}$ | $V_{DDDR}$ = 1.8 V<br>Subsystem clock stopped,<br>feedback resister disconnected | | 0.1 | 10 | μA |
| Release signal setup time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time | $t_{WAIT}$ | Release by $\overline{RESET}$ | | $2^{17}/f_x$ | | ms |
| | | Release by interrupt | | **Note** | | ms |

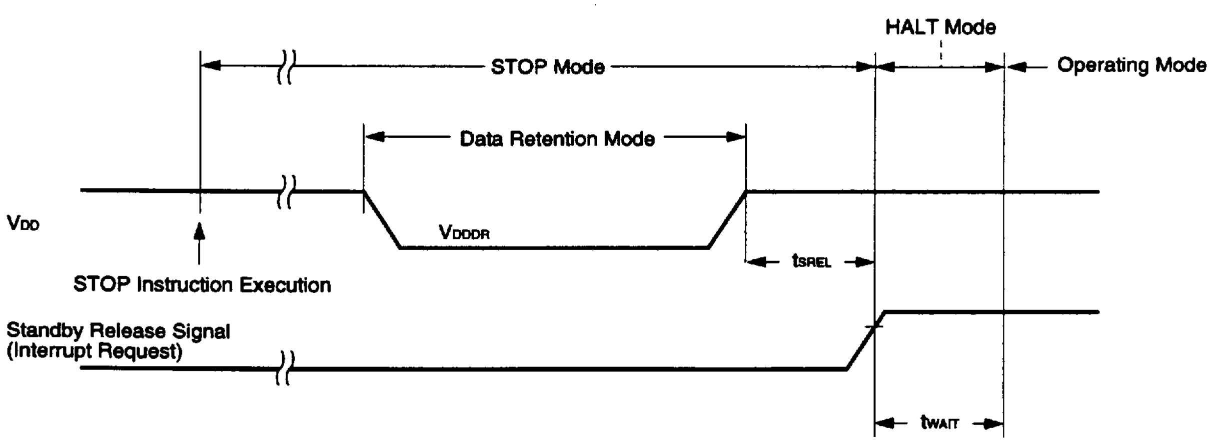
**Note** $2^{12}$/fxx, or $2^{14}$/fxx through $2^{17}$fxx can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

**Remark** fxx : Main system clock frequency (fx or fx/2)
fx : Main system clock oscillatior frequency

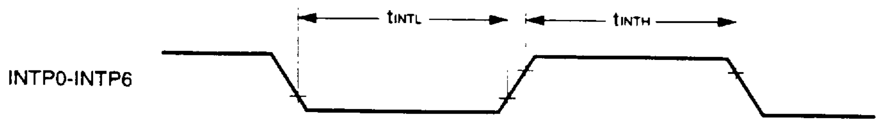
**Data Retention Timing (STOP mode release by $\overline{RESET}$)**



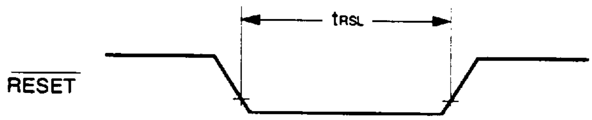

**Data Retention Timing (STOP mode release by standby release signal: interrupt signal)**



## Interrupt Input Timing




## $\overline{\text{RESET}}$ Input Timing



## PROM PROGRAMMING CHARACTERISTICS

### DC Characteristics

**(1) PROM Write Mode** ($T_A$ = 25 ± 5 °C, $V_{DD}$ = 6.5 ± 0.25 V, $V_{PP}$ = 12.5 ± 0.3 V)

| PARAMETER | SYMBOL | SYMBOL Note | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | $V_{IH}$ | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL}$ | $V_{IL}$ | | 0 | | 0.3 $V_{DD}$ | V |
| Output voltage, high | $V_{OH}$ | $V_{OH}$ | $I_{OH}$ = −1 mA | $V_{DD}$ − 1.0 | | | V |
| Output voltage, low | $V_{OL}$ | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $I_{LI}$ | $0 \le V_{IN} \le V_{DD}$ | −10 | | +10 | $\mu$A |
| $V_{PP}$ supply voltage | $V_{PP}$ | $V_{PP}$ | | 12.2 | 12.5 | 12.8 | V |
| $V_{DD}$ supply voltage | $V_{DD}$ | $V_{CC}$ | | 6.25 | 6.5 | 6.75 | V |
| $V_{PP}$ supply current | $I_{PP}$ | $I_{PP}$ | $\overline{PGM} = V_{IL}$ | | | 50 | mA |
| $V_{DD}$ supply current | $I_{DD}$ | $I_{CC}$ | | | | 50 | mA |

**(2) PROM Read Mode** ($T_A$ = 25 ± 5 °C, $V_{DD}$ = 5.0 ± 0.5 V, $V_{PP}$ = $V_{DD}$ ± 0.6 V)

| PARAMETER | SYMBOL | SYMBOL Note | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | $V_{IH}$ | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL}$ | $V_{IL}$ | | 0 | | 0.3 $V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | $V_{OH1}$ | $I_{OH}$ = −1 mA | $V_{DD}$ − 1.0 | | | V |
| | $V_{OH2}$ | $V_{OH2}$ | $I_{OH}$ = −100 $\mu$A | $V_{DD}$ − 0.5 | | | V |
| Output voltage, low | $V_{OL}$ | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $I_{LI}$ | $0 \le V_{IN} \le V_{DD}$ | −10 | | +10 | $\mu$A |
| Output leakage current | $I_{LO}$ | $I_{LO}$ | $0 \le V_{OUT} \le V_{DD}$, $\overline{OE} = V_{IH}$ | −10 | | +10 | $\mu$A |
| $V_{PP}$ supply voltage | $V_{PP}$ | $V_{PP}$ | | $V_{DD}$ − 0.6 | $V_{DD}$ | $V_{DD}$ + 0.6 | V |
| $V_{DD}$ supply voltage | $V_{DD}$ | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| $V_{PP}$ supply current | $I_{PP}$ | $I_{PP}$ | $V_{PP} = V_{DD}$ | | | 100 | $\mu$A |
| $V_{DD}$ supply current | $I_{DD}$ | $I_{CCA1}$ | $\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$ | | | 50 | mA |

**Note** Correspond symbols for the $\mu$PD27C1001A.



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AC Characteristics

## (1) PROM Write Mode

### (a) Page program mode ($T_A$ = 25 ± 5 °C, $V_{DD}$ = 6.5 ± 0.25 V, $V_{PP}$ = 12.5 ± 0.3 V)

| PARAMETER | SYMBOL | SYMBOL[Note] | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Address setup time (to $\overline{OE}$↓) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | $t_{OES}$ | | 2 | | | μs |
| $\overline{CE}$ setup time (to $\overline{OE}$↓) | $t_{CES}$ | $t_{CES}$ | | 2 | | | μs |
| Input data setup time (to $\overline{OE}$↓) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address hold time (from $\overline{OE}$↑) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| | $t_{AHL}$ | $t_{AHL}$ | | 2 | | | μs |
| | $t_{AHV}$ | $t_{AHV}$ | | 0 | | | μs |
| Input data hold time (from $\overline{OE}$↑) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| Data output float delay time from $\overline{OE}$↑ | $t_{DF}$ | $t_{DF}$ | | 0 | | 250 | ns |
| $V_{PP}$ setup time (to $\overline{OE}$↓) | $t_{VPS}$ | $t_{VPS}$ | | 1.0 | | | ms |
| $V_{DD}$ setup time (to $\overline{OE}$↓) | $t_{VDS}$ | $t_{VCS}$ | | 1.0 | | | ms |
| Program pulse width | $t_{PW}$ | $t_{PW}$ | | 0.095 | 0.1 | 0.105 | ms |
| Valid data delay time from $\overline{OE}$↓ | $t_{OE}$ | $t_{OE}$ | | | | 1 | μs |
| $\overline{OE}$ pulse width during data latching | $t_{LW}$ | $t_{LW}$ | | 1 | | | μs |
| $\overline{PGM}$ setup time | $t_{PGMS}$ | $t_{PGMS}$ | | 2 | | | μs |
| $\overline{CE}$ hold time | $t_{CEH}$ | $t_{CEH}$ | | 2 | | | μs |
| $\overline{OE}$ hold time | $t_{OEH}$ | $t_{OEH}$ | | 2 | | | μs |

### (b) Byte program mode ($T_A$ = 25 ± 5 °C, $V_{DD}$ = 6.5 ± 0.25 V, $V_{PP}$ = 12.5 ± 0.3 V)

| PARAMETER | SYMBOL | SYMBOL[Note] | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Address setup time (to $\overline{PGM}$↓) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | $t_{OES}$ | | 2 | | | μs |
| $\overline{CE}$ setup time (to $\overline{PGM}$↓) | $t_{CES}$ | $t_{CES}$ | | 2 | | | μs |
| Input data setup time (to $\overline{PGM}$↓) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address hold time (from $\overline{OE}$↑) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| Input data hold time (from $\overline{PGM}$↑) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| Data output float delay time from $\overline{OE}$↑ | $t_{DF}$ | $t_{DF}$ | | 0 | | 250 | ns |
| $V_{PP}$ setup time (to $\overline{PGM}$↓) | $t_{VPS}$ | $t_{VPS}$ | | 1.0 | | | ms |
| $V_{DD}$ setup time (to $\overline{PGM}$↓) | $t_{VDS}$ | $t_{VCS}$ | | 1.0 | | | ms |
| Program pulse width | $t_{PW}$ | $t_{PW}$ | | 0.095 | 0.1 | 0.105 | ms |
| Valid data delay time from $\overline{OE}$↓ | $t_{OE}$ | $t_{OE}$ | | | | 1 | μs |
| $\overline{OE}$ hold time | $t_{OEH}$ | — | | 2 | | | μs |

**Note** Correspond symbols for the μPD27C1001A.

**(2) PROM Read Mode** ($T_A$ = 25 ± 5 °C, $V_{DD}$ = 5.0 ± 0.5 V, $V_{PP}$ = $V_{DD}$ ± 0.6 V)

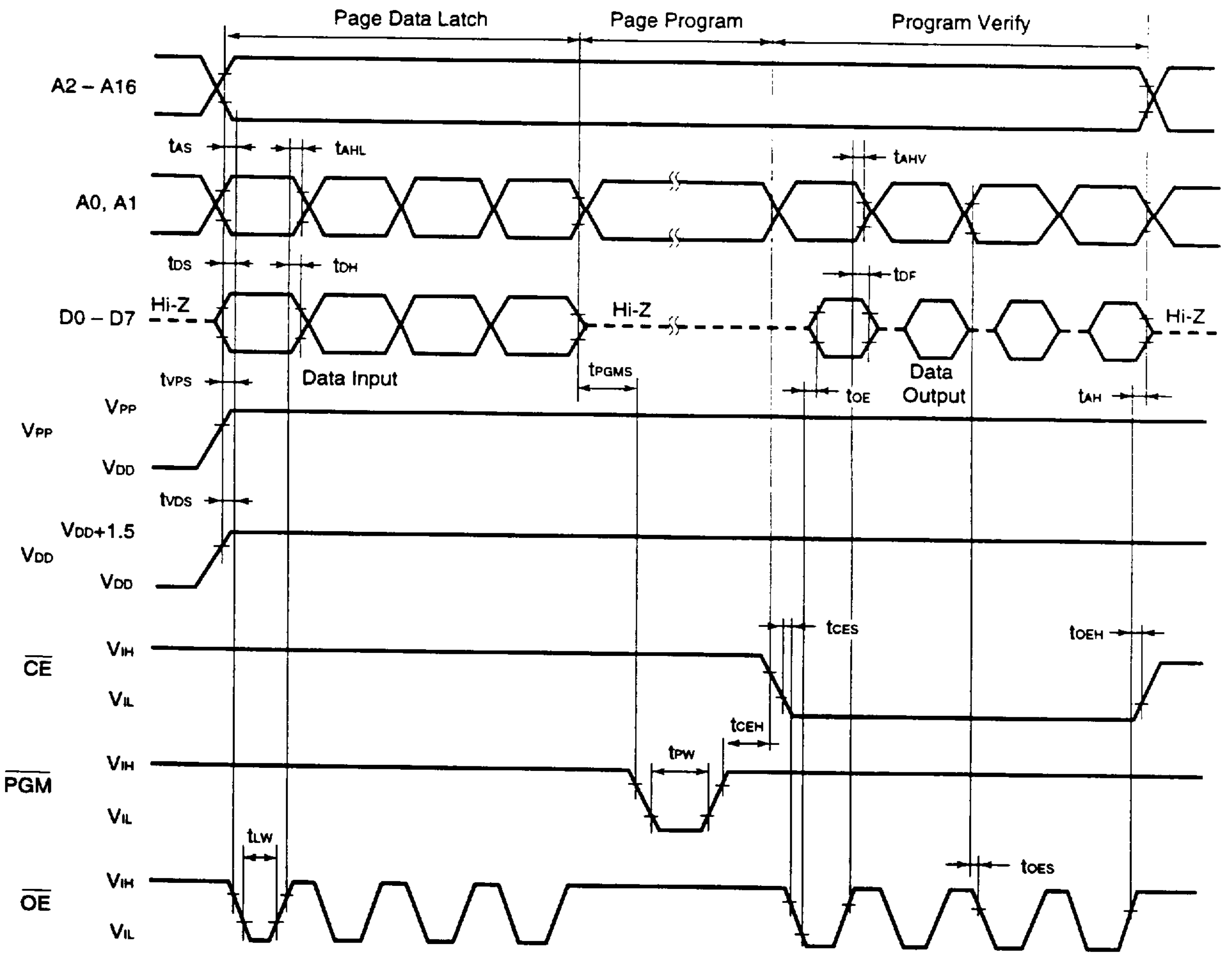
| PARAMETER | SYMBOL | SYMBOL[Note] | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Data output delay time from address | $t_{ACC}$ | $t_{ACC}$ | $\overline{CE} = \overline{OE} = V_{IL}$ | | | 800 | ns |
| Data output delay time from $\overline{CE}$↓ | $t_{CE}$ | $t_{CE}$ | $\overline{OE} = V_{IL}$ | | | 800 | ns |
| Data output delay time from $\overline{OE}$↓ | $t_{OE}$ | $t_{OE}$ | $\overline{CE} = V_{IL}$ | | | 200 | ns |
| Data output float delay time from $\overline{OE}$↑ | $t_{DF}$ | $t_{DF}$ | $\overline{CE} = V_{IL}$ | 0 | | 60 | ns |
| Data hold time from address | $t_{OH}$ | $t_{OH}$ | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | ns |

**Note** Correspond symbols for the μPD27C1001A.

**(3) PROM Programming Mode Setting** ($T_A$ = 25 °C, $V_{SS}$ = 0 V)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| PROM programming mode setup time | $t_{SMA}$ | | 10 | | | μs |

PROM Write Mode Timing (page program mode)



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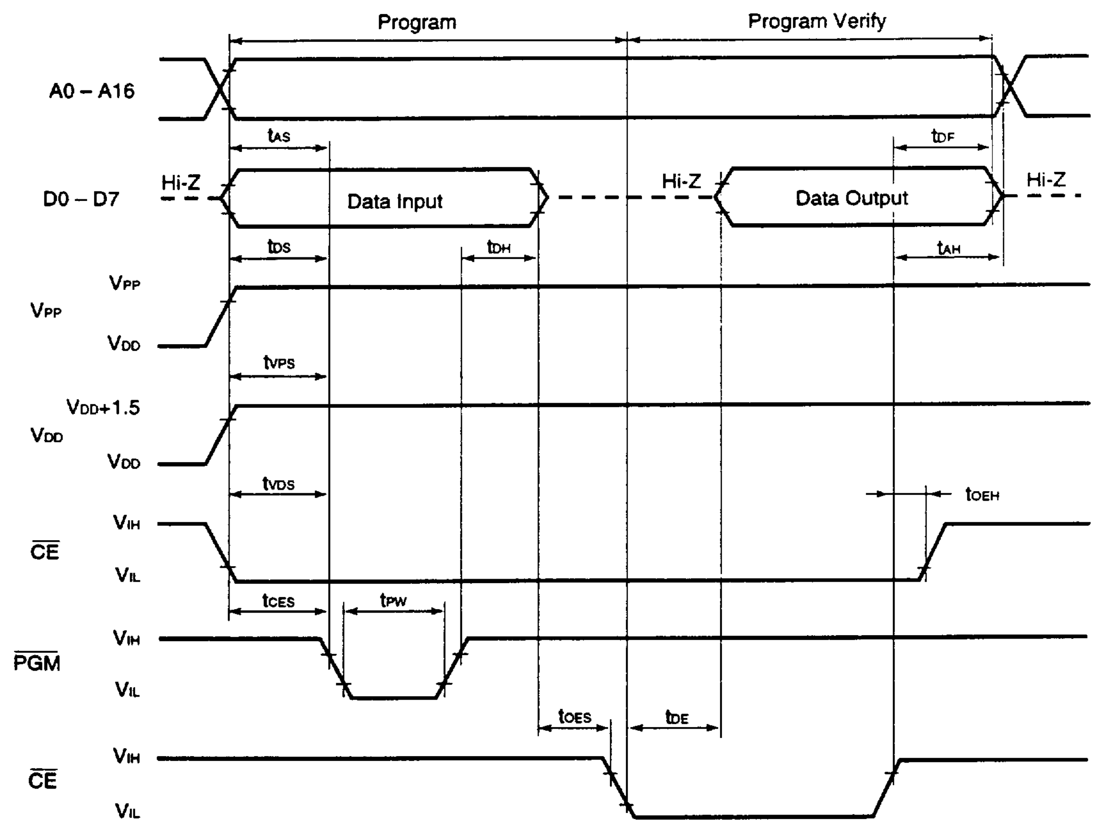
PROM Write Mode Timing (byte program mode)

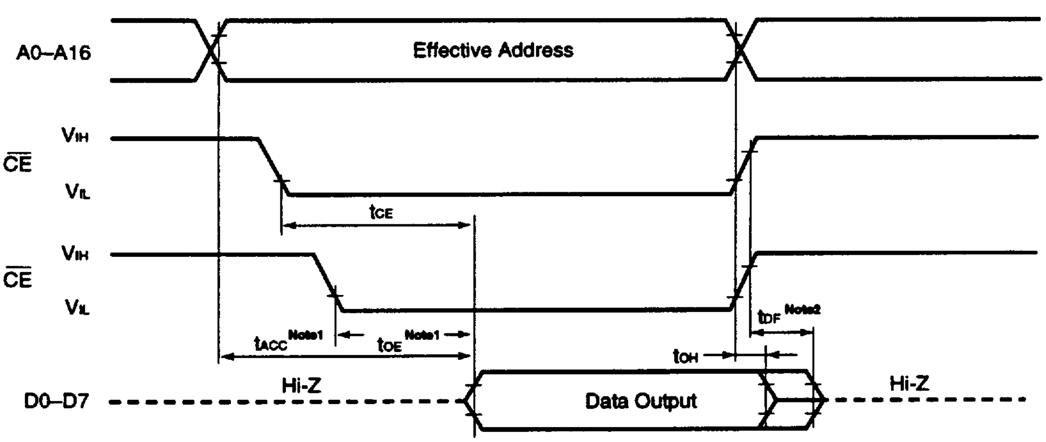



**Cautions 1. $V_{DD}$ shonld be applied before $V_{PP}$, and removed after $V_{PP}$.**

**2. $V_{PP}$ shonld not exceed +13.5 V including overshoot.**

**3. Disconnection during application of ±12.5V to VPP may have an adverse effect on reliability.**

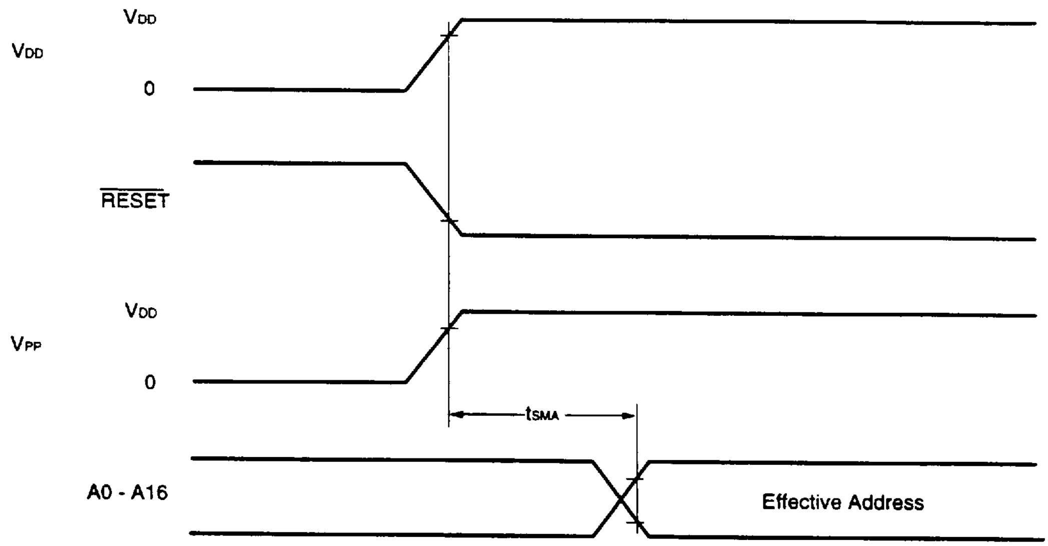
PROM Read Mode Timing




**Notes 1.** If you want to read within the $t_{ACC}$ range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maxmum of $t_{ACC} - t_{OE}$.

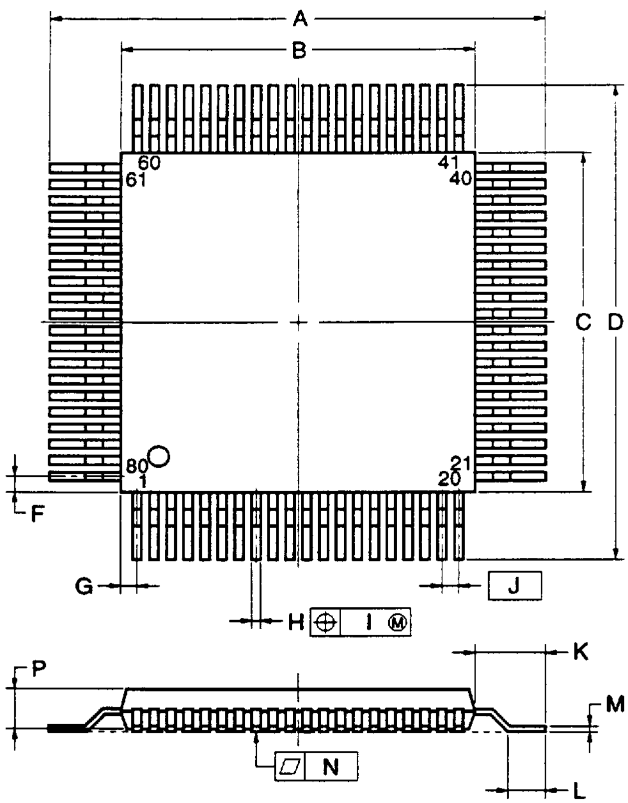
**2.** $t_{DF}$ is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches VIH.

PROM Programming Mode Setting Timing

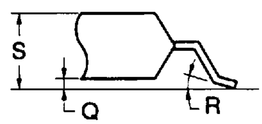


## 8. PACKAGE DRAWINGS

### 80 PIN PLASTIC QFP (14×14)




detail of lead end




**NOTE**

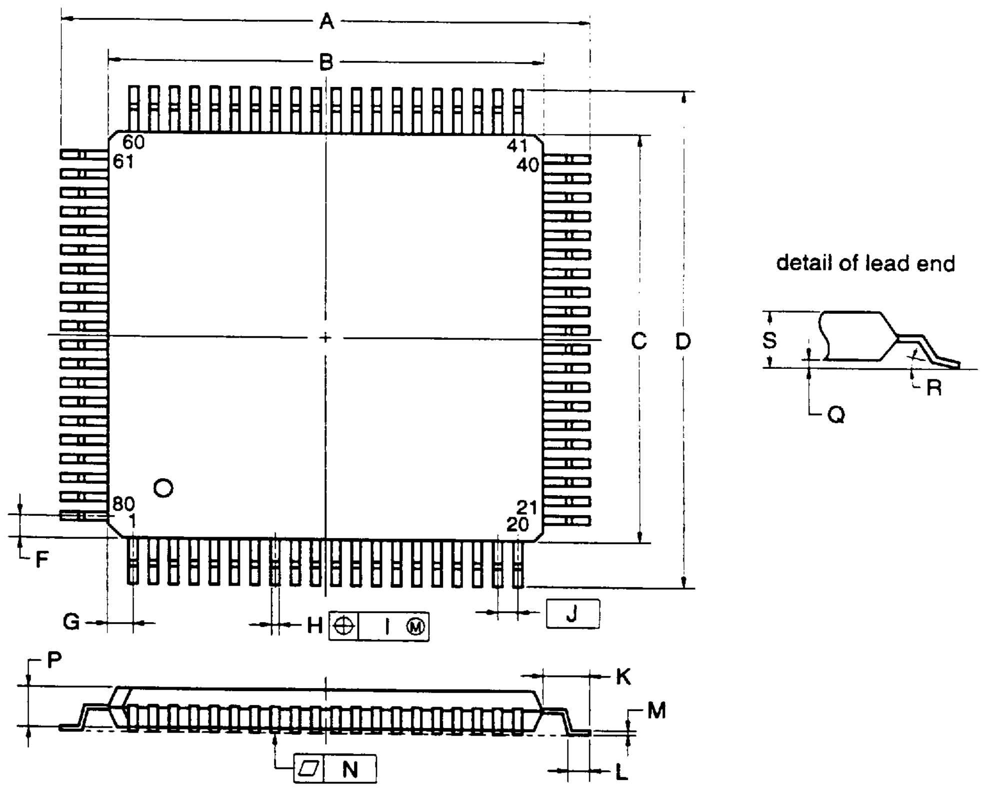
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 17.2±0.4 | 0.677±0.016 |
| B | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| C | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.2±0.4 | 0.677±0.016 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.30±0.10 | $0.012^{+0.004}_{-0.005}$ |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.6±0.2 | 0.063±0.008 |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.003}$ |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

S80GC-65-3B9-4

**Remark** Dimensions and materials of ES product are the same as those of mass-production products.

## 80 PIN PLASTIC QFP (14×14)




**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 17.20±0.20 | 0.677±0.008 |
| B | 14.00±0.20 | $0.551^{+0.009}_{-0.008}$ |
| C | 14.00±0.20 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.20±0.20 | 0.677±0.008 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.32±0.06 | $0.013^{+0.002}_{-0.003}$ |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.60±0.20 | 0.063±0.008 |
| L | 0.80±0.20 | $0.031^{+0.009}_{-0.008}$ |
| M | $0.17^{+0.03}_{-0.07}$ | $0.007^{+0.001}_{-0.003}$ |
| N | 0.10 | 0.004 |
| P | 1.40±0.10 | 0.055±0.004 |
| Q | 0.125±0.075 | 0.005±0.003 |
| R | $3°^{+7°}_{-3°}$ | $3°^{+7°}_{-3°}$ |
| S | 1.70 MAX. | 0.067 MAX. |

P80GC-65-8BT

## 9. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual (C10535E)"**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

**Table 9-1. Surface Mount Type Soldering Conditions**

**μPD78P058FGC-3B9 : 80-Pin Plastic QFP (14 × 14 mm, Resin thickness: 2.7 mm)**

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Duration: 30 sec. max. (210°C or above)<br>Number of times: Max. 2<br>Time limit: 7 days[Note] (thereafter 20 hours 125°C prebaking required) | IR35-207-3 |
| VPS | Package peak temperature: 215°C, Duration: 40 sec. max. (200°C or above)<br>Number of times: Max. 2<br>Time limit: 7 days[Note] (thereafter 20 hours 125°C prebaking required) | VP15-207-3 |
| Wave soldering | Solder bath temperature: 260°C max., Duration: 10 sec. max., Number of times: once,<br>Preheating temperature: 120°C max. (package serface temperature),<br>Time limit: 7 days[Note] (thereafter 20 hours 125°C prebaking required) | WS60-207-1 |
| Partial heating | Pin temperature: 300°C or less<br>Duration: 3 sec. max. (per side of device) | — |

**Note** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

**Caution Use of more than one soldering method should be avoided (except in the case of partial heating).**

## APPENDIX A. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD78P058.

### Language Processing Software

| | |
|---|---|
| RA78K/0[Notes 1, 2, 3, 4] | 78K/0 series common assembler package |
| CC78K/0[Notes 1, 2, 3, 4] | 78K/0 series common C compiler package |
| DF78054[Notes 1, 2, 3, 4] | μPD78054 subseries common device file |
| CC78K/0-L[Notes 1, 2, 3, 4] | 78K/0 series common C compiler library source file |

### PROM Writing Tools

| | |
|---|---|
| PG-1500 | PROM programmer |
| PA-78P054GC | Programmer adapter connected to a PG-1500 |
| PG-1500 controller[Notes 1, 2] | PG-1500 control program |

### Debugging Tools

| | |
|---|---|
| IE-78000-R | 78K/0 series common in-circuit emulator |
| IE-78000-R-A[Note 8] | 78K/0 series common in-circuit emulator (for integrated debugger) |
| IE-78000-R-BK | 78K/0 series common break board |
| IE-78064-R-EM | Emulation board common to μPD78064 subseries |
| EP-78230GC-R | Emulation probe common to μPD78234 subseries |
| EV-9200GC-80 | Socket for mounting on user system board created for 80-pin plastic QFP use |
| SM78K0[Notes 5, 6, 7] | 78K/0 series common system simulator |
| ID78K0[Notes 4, 5, 6, 7] | Integrarted debugger for IE-78000-R |
| SD78K/0[Notes 1, 2] | Screen debugger for IE-78000-R |
| DF78054[Notes 1, 2, 4, 5, 6, 7] | Device file for μPD78054 subseries |

**Notes**
1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT (PC DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

**Remarks**
1. For third party development tools, see the 78K/0 Series Selection Guide (U11126E).
2. RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 are used in combination with DF78054.

**Real-Time OS**

| | |
|---|---|
| RX78K/0[Notes 1, 2, 3, 4] | 78K/0 series real-time OS |
| MX78K0[Notes 1, 2, 3, 4] | 78K/0 series OS |

**Fuzzy Inference Development Support System**

| | |
|---|---|
| FE9000[Note 1]/FE9200[Note 5] | Fuzzy knowledge data creation tool |
| FT9080[Note 1]/FT9085[Note 2] | Translator |
| FI78K0[Notes 1, 2] | Fuzzy inference module |
| FD78K0[Notes 1, 2] | Fuzzy inference debugger |

**Notes**
1. PC-9800 series (MS-DOS) based
2. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS) based
3. HP9000 series 300 (HP-UX) based
4. HP9000 series 700 (HP-UX) based, SPARCstation (SunOS) based, EWS4800 series (EWS-UX/V) based
5. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

**Remarks**
1. For third party development tools, see the 78K/0 Series Selection Guide (U11126E).
2. RX78K/0 is used in combination with DF78054.

## APPENDIX B. RELATED DOCUMENTS

### Device Documents

| Document Name | Document No. (English) | Document No. (Japanese) |
|---|---|---|
| μPD78058F, 78058FY Subseries User's Manual | To be prepared | To be prepared |
| μPD78P058F Data Sheet | This document | U11796J |
| μPD78056F, 58F Data Sheet | To be prepared | U11795J |
| 78K/0 Series User's Manual Instruction | IEU-1372 | IEU-849 |
| 78K/0 Series Instruction Set | — | U10904J |
| 78K/0 Series Instruction Table | — | U10903J |

### Development Tool Documents (User's Manual)

| Document Name | | Document No. (English) | Document No. (Japanese) |
|---|---|---|---|
| RA78K Series Assembler Package | Operation | EEU-1399 | EEU-809 |
| | Language | EEU-1404 | EEU-815 |
| RA78K Series Structured Assembler Preprocessor | | EEU-1402 | EEU-817 |
| CC78K Series C Compiler | Operation | EEU-1280 | EEU-656 |
| | Language | EEU-1284 | EEU-655 |
| CC78K/0 C Compiler | Operation | — | U11517J |
| | Language | — | U11518J |
| CC78K Series Library Source File | | — | EEU-777 |
| PG-1500 PROM Programmer | | EEU-1335 | EEU-651 |
| PG-1500 Controller PC-9800 Series (MS-DOS) based | | EEU-1291 | EEU-704 |
| PG-1500 Controller IBM PC Series (PC DOS) based | | U10540E | EEU-5008 |
| IE-78000-R | | U11376E | EEU-810 |
| IE-78000-R-A | | U10057E | U10057J |
| IE-78000-R-BK | | EEU-1427 | EEU-867 |
| IE-78064-R-EM | | EEU-1443 | EEU-905 |
| EP-78230 | | EEU-1515 | EEU-985 |
| EP-78054GK-R | | EEU-1468 | EEU-932 |
| SM78K0 System Simulator Windows based | Reference | U10181E | U10181J |
| SM78K Series System Simulator | External parts user open interface specification | U10092E | U10092J |
| ID78K0 Integrated Debugger EWS based | Reference | U11151E | U11151J |
| ID78K0 Integrated Debugger PC based | Reference | U11539E | U11539J |
| ID78K0 Integrated Debugger Windows based | Guide | U11649E | U11649J |
| SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) based | Introduction | — | EEU-852 |
| | Reference | — | U10952J |
| SD78K/0 Screen Debugger IBM PC/AT (PC DOS) based | Introduction | EEU-1414 | EEU-5024 |
| | Reference | EEU-1413 | U11279J |

**Caution** **The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.**



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### Embedded Software Documents (User's Manual)

| Document Name | | Document No. (English) | Document No. (Japanese) |
|---|---|---|---|
| 78K/0 Series Realtime OS | Basics | — | U11537J |
| | Installation | — | U11536J |
| | Technical | — | U11538J |
| 78K/0 Series OS MX78K0 | Basics | — | EEU-5010 |
| Fuzzy Knowledge Data Creation Tool | | EEU-1438 | EEU-829 |
| 78K/0, 78K/II, 87AD Series<br>Fuzzy, Inference Development Support System—Translator | | EEU-1444 | EEU-862 |
| 78K/0 Series Fuzzy Inference Development Support System | Fuzzy Inference Module | EEU-1441 | EEU-858 |
| 78K/0 Series Fuzzy Inference Development Support System | Fuzzy Inference Debugger | EEU-1458 | EEU-921 |

### Other Documents

| Document Name | Document No. (English) | Document No. (Japanese) |
|---|---|---|
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535E | C10535J |
| Quality Guides on NEC Semiconductor Devices | IEI-1209 | IEI-620 |
| NEC Semiconductor Device Reliability and Quality Control | C10983E | C10983J |
| Electrostatic Discharge (ESD) Test | — | MEM-539 |
| Semiconductor Device Quality Assurance Guide | MEI-1202 | MEI-603 |
| Microcomputer-related Product Guide (Products by other Manufacturers) | — | MEI-604 |

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