SONY

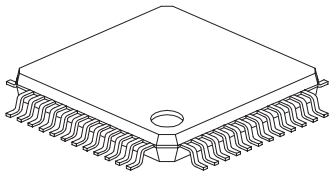
CXA7004R

LCD Driver

Description

The CXA7004R is a driver IC developed for use with Sony polycrystalline silicon TFT LCD panels. It supports 12-bit digital input, and the input data is demultiplexed into 6 phases and output. The CXA7004R can directly drive an LCD panel, and the VCOM setting circuit and precharge pulse waveform generator are also on-chip.

48 pin LQFP (Plastic)



Features

- Supports 12-bit input
- Low output deviation
- Various adjustment functions using a 3-wire serial interface
- Supports signals up to XGA
- Supports dot and line inversion
- VCOM voltage generation circuit
- Precharge pulse waveform generation circuit

Applications

LCD projectors and other video equipment

Absolute Maximum Ratings (V_{SS} = 0V)

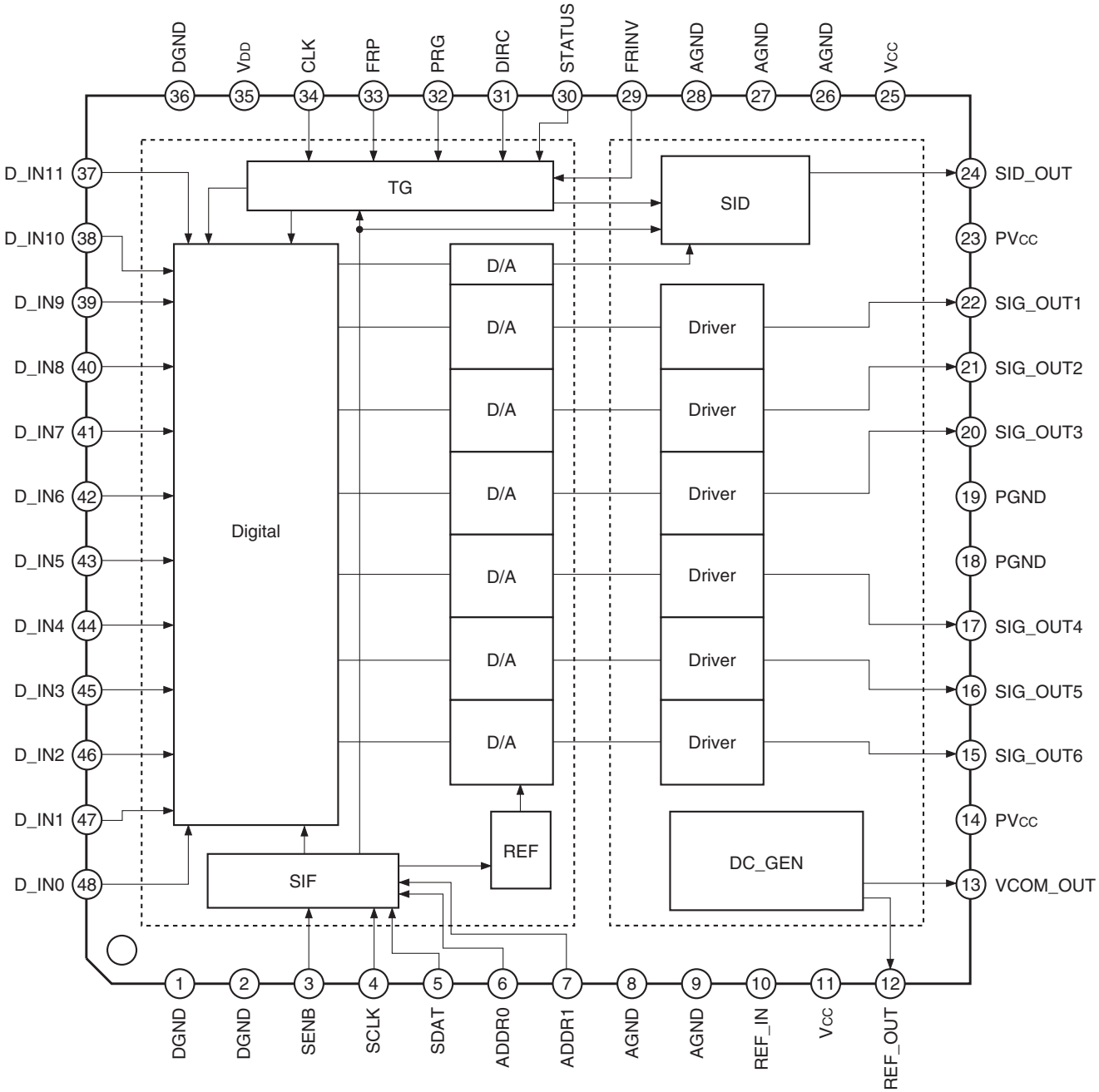
• Supply voltage	V_{CC}	16	V
	V_{DD}	5	V
• Operating temperature	Topr	–20 to +70	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1200	mW

Recommended Operating Conditions

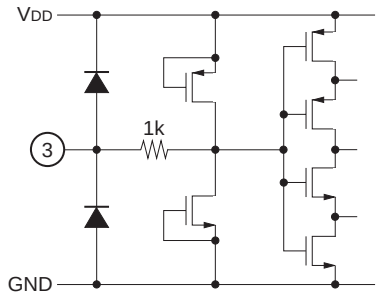
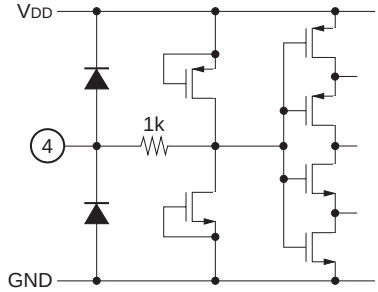
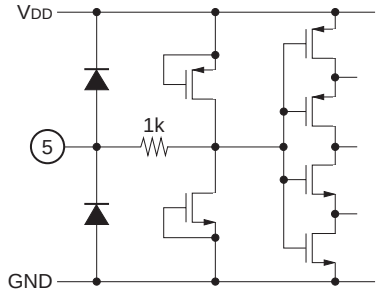
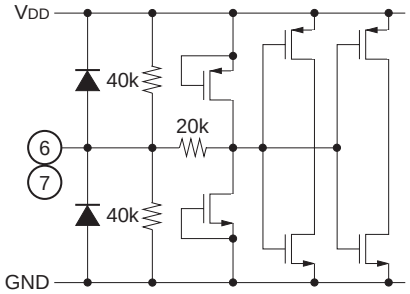
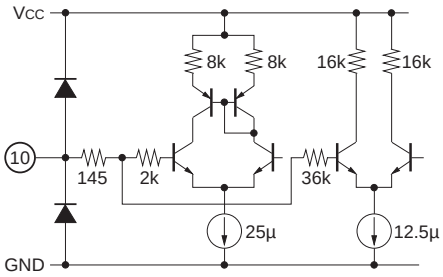
• Supply voltage	V_{CC}	15.0 to 15.5	V
	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +70	°C

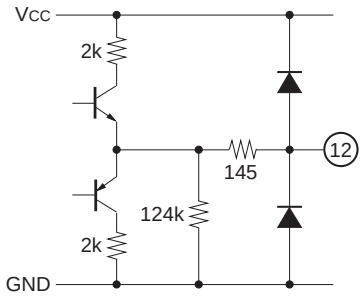
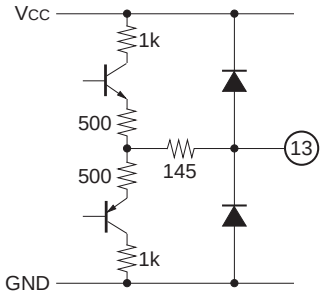
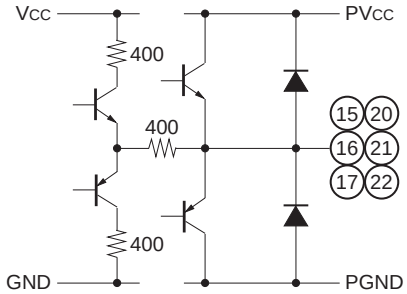
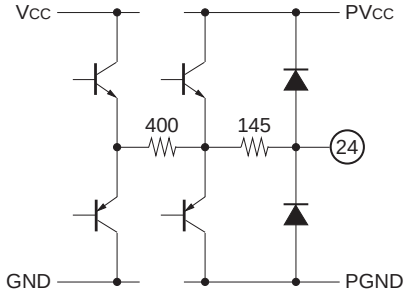
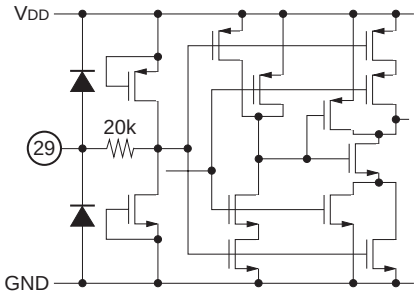
E02Y23A35

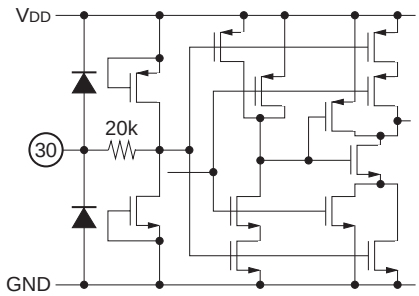
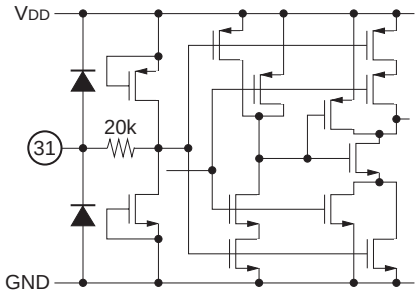
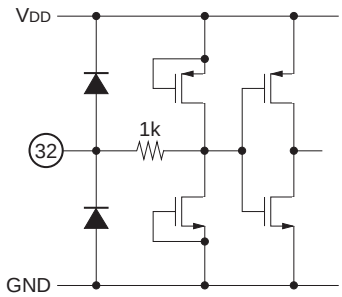
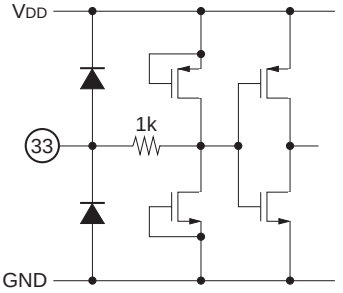
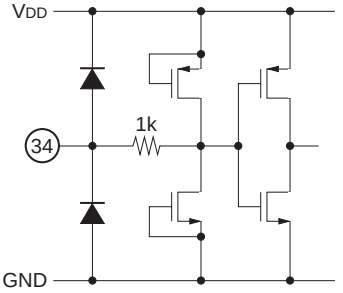
Block Diagram

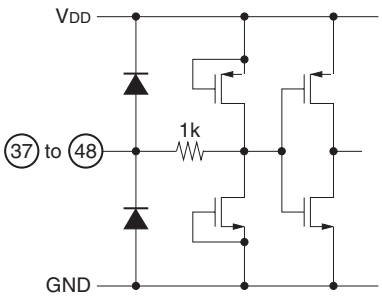


Pin Description

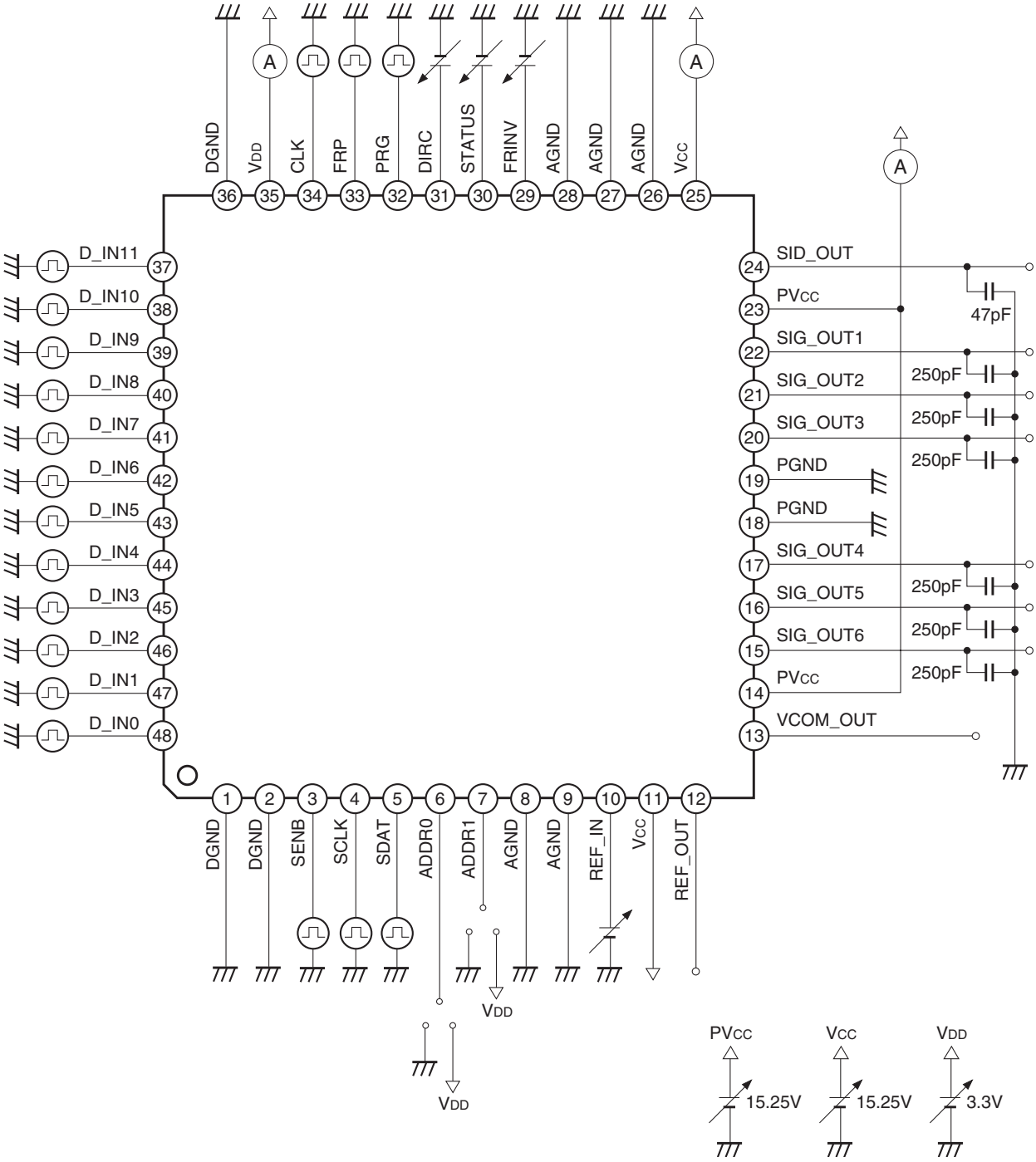
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
3	SENB	I	High: ≥ 2.0V Low: ≤ 0.8V		Enable input for 3-wire serial interface. Data is written only while this pin is low.
4	SCLK	I	High: ≥ 2.0V Low: ≤ 0.8V		Clock input for 3-wire serial interface. Supports a clock from 100kHz to 1MHz.
5	SDAT	I	High: ≥ 2.0V Low: ≤ 0.8V		Data input for 3-wire serial interface.
6 7	ADDR0 ADDR1	I	High = VDD Low = GND		IC address setting for 3-wire serial interface. Addresses from 0h to 7h can be set by changing this setting.
10	REF_IN	I	6.0V		Reference voltage (signal center) input. When using multiple CXA7004Rs, connect to REF_OUT that differs from the reference.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
12	REF_OUT	O	6.0V		Signal center voltage (inversion folded voltage) output. When using multiple CXA7004Rs, connect to REF_IN through a 1kΩ resistor.
13	VCOM_OUT	O	5.5 to 7.5V		Common voltage output of LCD panel. Adjustment is possible by the 3-wire serial interface setting.
15 16 17 20 21 22	SIG_OUT6 to SIG_OUT1	O	1.5 to 13.5V		Demultiplexed output of AC inverse driven video signals. Can be directly connected to the LCD panel.
24	SID_OUT	O	1.5 to 13.5V		Precharge waveform output. Adjustment is possible by the 3-wire serial interface setting. This pin cannot directly drive the LCD panel, so input to the LCD panel through a buffer.
29	FRINV	I	High: ≥ 2.0V Low: ≤ 0.8V		Input for switching the output polarity to inverted or non-inverted relative to the LCD panel AC drive inversion timing (FRP) pulse.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
30	STATUS	I	High: ≥ 2.0V Low: ≤ 0.8V		Master/slave setting when using two CXA7004Rs. When set high, this chip operates as the master IC; when set low, this chip operates as the slave IC. When using only one CXA7004R, leave this pin open.
31	DIRC	I	High: ≥ 2.0V Low: ≤ 0.8V		Scan direction setting. The scan direction is set in combination with the 3-wire serial interface setting DIRCR.
32	PRG	I	High: ≥ 2.0V Low: ≤ 0.8V		Timing pulse input for switching the Pin 24 (SID_OUT) output level. This pin is also used as the circuit reset pulse.
33	FRP	I	High: ≥ 2.0V Low: ≤ 0.8V		LCD panel AC drive inversion timing input. High: inverted Low: non-inverted
34	CLK	I	High: ≥ 2.0V Low: ≤ 0.8V		Dot clock input. The polarity is determined by the 3-wire serial interface setting CKPOL. High: reverse polarity Low: positive polarity

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
37 to 48	D_IN11 to D_IN0	I	High: ≥ 2.0V Low: ≤ 0.8V		Digital data input. D_IN0: LSB D_IN11: MSB
35	V_{DD}		3.3V		3.3V power supply.
11, 25	V_{CC}		15.5V		15V power supply.
14, 23	PV_{CC}		15.5V		Power V_{CC}.
1, 2, 36	DGND		DGND		GND.
8, 9, 26, 27, 28	AGND		AGND		GND.
18, 19	PGND		PGND		Power GND.

Electrical Characteristics Measurement Circuit



Electrical Characteristics (Ta = 50°C)

No.	Item	Symbol	Measurement description	Min.	Typ.	Max.	Unit
1	Digital input resolution	n		—	12	—	bit
2	Digital input setup time 1	Ts1	CKPOL: 3.3V, PRG and D_IN[11:0] setup time relative to CLK input.	0	—	—	ns
3	Digital input setup time 2	Ts2	CKPOL: 0V, PRG and D_IN[11:0] setup time relative to CLK input.	0.5	—	—	ns
4	Digital input hold time 1	Th1	CKPOL: 3.3V, PRG and D_IN[11:0] hold time relative to CLK input.	2.5	—	—	ns
5	Digital input hold time 2	Th2	CKPOL: 0V, PRG and D_IN[11:0] hold time relative to CLK input.	2	—	—	ns
6	CLK input frequency range 1	f_{CLK1}	SLDAT: 3.3V, maximum frequency at which the internal timing generator and D/A converter operate normally.	—	—	100	MHz
7	CLK input frequency range 2	f_{CLK2}	SLDAT: 0V, maximum frequency at which the internal timing generator and D/A converter operate normally.	—	—	80	MHz
8	SIG_OUT output voltage range	V_{SIGOUT}	Output voltage range of SIG_OUT1 to SIG_OUT6.	1.5	—	13.5	V
9	SIG_OUT output amplitude adjustable range	$V_{SIGOUTpp}$	Gain control: 00h, measure the SIG_OUT voltage difference at D_IN[11:0] = 000h and FFFh.	2	—	6	V
10	SIG_OUT slew rate	SR_{OUT}	Load capacitance C = 270pF; measure the slew rate at 10 to 90% of SIG_OUT1 to SIG_OUT6 rise and fall when D_IN[11:0] is varied from 000h to FFFh or from FFFh to 000h.	170	—	—	V/µs
11	SIG_OUT offset adjustable range	V_{OFST}	Offset adjustable range of SIG_OUT1 to SIG_OUT6 by Bright control.	0	—	1.175	V
12	Signal center adjustable range	V_{SIG}	Signal center voltage adjustable range when SIG center is varied.	6.375	—	8.625	V
13	SID amplitude adjustable range 1	A_{SID1}	SID_OUT amplitude adjustable range by SID control A.	0	—	6	V
14	SID amplitude adjustable range 2	A_{SID2}	SID_OUT amplitude adjustable range by SID control B.	0	—	6	V
15	VCOM adjustable range	VCOM	VCOM_OUT adjustable range relative to signal center voltage when VCOM control is varied.	–2	—	0	V
16	V_{DD} current consumption	I_{DD}	CLK = 80MHz, V_{DD} current consumption.	23	—	28	mA
17	V_{CC} current consumption 2	I_{CC}	CLK = 80MHz, inversion signal every D_IN = 000h, FRP = 60CLK, V_{CC} + PV_{CC} current consumption when SIG_OUT load capacitance = 250pF.	38	—	68	mA

No.	Item	Symbol	Measurement description	Min.	Typ.	Max.	Unit
18	Output deviation between SIG_OUT channels 1	D_{OUT1}	D_IN[11:0] = 7FFh, value obtained by subtracting minimum value from maximum value of SIG_OUT1 to SIG_OUT6 output at Gain control = BFh.	—	—	2	mV
19	Output deviation between SIG_OUT channels 2	D_{OUT2}	D_IN[11:0] = 000h or FFFh, value obtained by subtracting minimum value from maximum value of SIG_OUT1 to SIG_OUT6 at Gain control = BFh.	—	—	10	mV
20	Output deviation between SIG_OUT ICs 1	D_{IC1}	D_IN[11:0] = 7FFh, value obtained by subtracting minimum value from maximum value of SIG_OUT1 to SIG_OUT6 at Gain control = BFh.	—	—	2	mV
21	Output deviation between SIG_OUT ICs 2	D_{IC2}	D_IN[11:0] = 000h or FFFh, value obtained by subtracting minimum value from maximum value of SIG_OUT1 to SIG_OUT6 at Gain control = BFh.	—	—	10	mV
22	MAINDAC differential linearity error	DLE	MAINDAC differential linearity error	–1	—	1	LSB

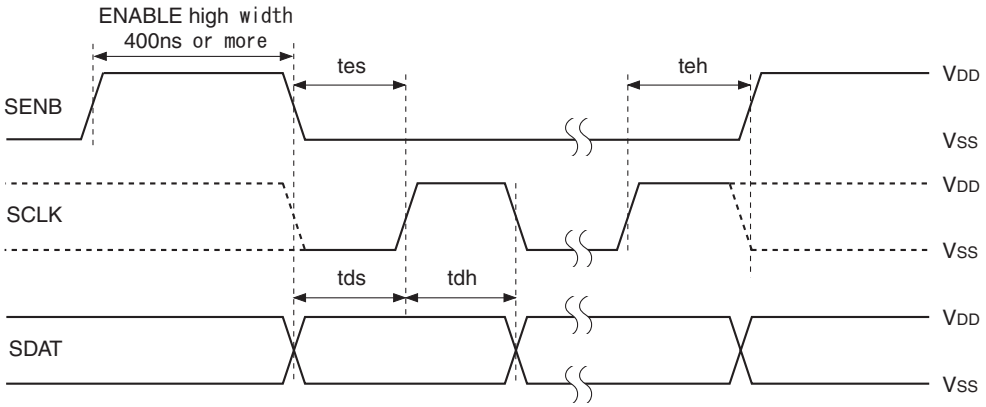
3-wire Serial Interface

The CXA7004R makes the various register settings using a 3-wire serial interface.
Up to 8 IC addresses can be designated by the ADDR0 and ADDR1 (Pins 6 and 7) settings, and these settings can be adjusted individually. The relationship between the IC address and ADDR0 and ADDR1 is shown below. In addition, the adjustable settings include the mode settings, gain, offset, signal center voltage, precharge, and common voltage (VCOM) settings. (See the Register Function Setting Table.)

AC Characteristics (Topr = –20 to +75°C, V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
SENB setup time relative to the rising edge of SCLK	tes	100	—	—	ns
SENB hold time relative to the rising edge of SCLK	teh	100	—	—	ns
SDAT setup time relative to the rising edge of SCLK	tds	100	—	—	ns
SDAT hold time relative to the rising edge of SCLK	tdh	100	—	—	ns

Timing Definition



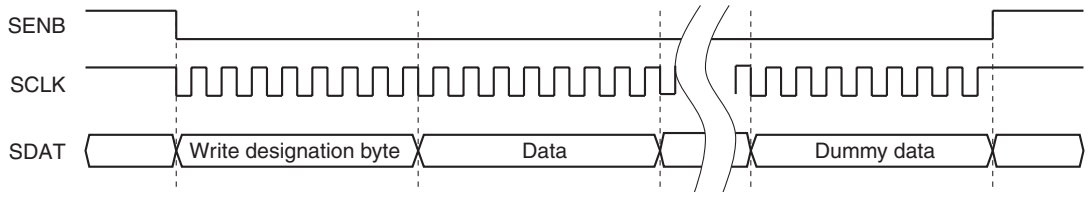
Input Format and Initialization

The 3-wire serial interface input format is shown below.
The minimum configuration is the 3 bytes of one write designation byte, one data byte, and one dummy data byte. In addition, the register address is automatically incremented by the number of input data.

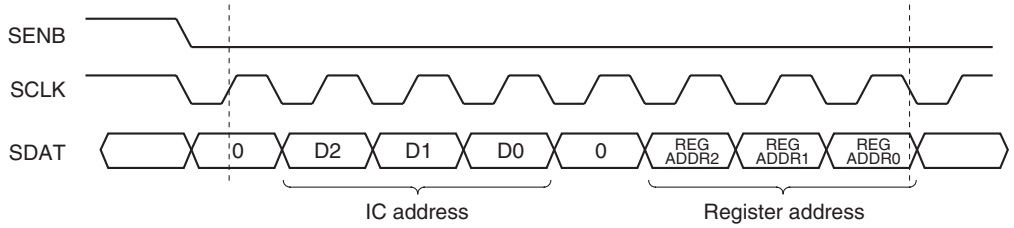
• Initialization

This IC must initialize the registers before setting the registers. Write "1" to register address (00h) RESET after power is turned on. This setting initializes this IC.
After initialization, register setting is performed by returning RESET to "0". When initialization is not performed, the setting value of a register may not be reflected correctly.

Input Format



Write Designation Byte



IC Address Definition

IC address	IC address for serial interface			External pin	
	D2	D1	D0	ADDR1	ADDR0
0	L	L	L	L	L
1	L	L	H	L	C
2	L	H	L	L	H
3	L	H	H	C	L
4	H	L	L	C	H
5	H	L	H	H	L
6	H	H	L	H	C
7	H	H	H	H	H

L: GND
C: 1/2V_{DD} or OPEN
H: V_{DD}

Register Function Setting Table

REG ADDR	Function	D7	D6	D5	D4	D3	D2	D1	D0
00	Mode	RESET	SIDAT	SLINV	FHCNT	DIRCR	SIDON	PRPOL	CKPOL
01	SIG center			SIGC5	SIGC4	SIGC3	SIGC2	SIGC1	SIGC0
02	Gain control	G7	G6	G5	G4	G3	G2	G1	G0
03	Bright control	B7	B6	B5	B4	B3	B2	B1	B0
04	VCOM control		VC6	VC5	VC4	VC3	VC2	VC1	VC0
05	SID control A		SIDA6	SIDA5	SIDA4	SIDA3	SIDA2	SIDA1	SIDA0
06	SID control B		SIDB6	SIDB5	SIDB5	SIDB3	SIDB2	SIDB1	SIDB0

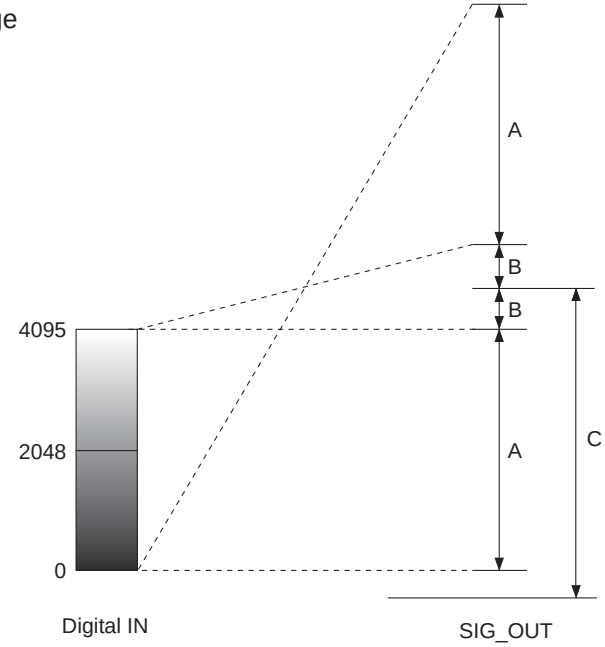
Mode: Various function settings
SIG center: Signal center voltage setting
Gain control: Voltage amplitude setting between SIG_OUT white and black levels
Bright control: Offset adjustment from SIG_OUT signal center voltage
VCOM control: VCOM voltage setting
SID control A: Precharge signal voltage setting A
SID control B: Precharge signal voltage setting B

Description of Operation

The flow of internal operations is described below.
The digital signals input to D_IN0 to D_IN11 are internally demultiplexed into 6 phases, and then data processed according to the various mode settings. After that, the signals are D/A converted into analog signals for each channel, amplified at the rear end, and output.

The output level relative to the output level setting changes according to the following settings.

A: Register Gain control setting
B: Register Bright control setting
C: Signal center voltage



- **Signal center voltage adjustment (C)**
  The signal center voltage is determined by the register setting SIG center.
  The signal center voltage can be adjusted in 35mV/LSB steps from 00h: 6.5V to 3Fh: 8.5V.

- **Offset adjustment relative to the signal center voltage (B)**
  The output voltage at digital input FFFh is determined by the SIG_C voltage and the register setting Bright control.
  The offset relative to the signal center voltage can be adjusted in 4mV/LSB steps from 00h: SIG_C ± 0.2V to FFh: SIG_C ± 1V.

- **White-black amplitude gain adjustment (A)**
  The white-black voltage amplitude when the digital input is varied from 000h to FFFh is determined by the register setting Gain control in the condition with the white level fixed.
  The gain relative to the signal center voltage can be adjusted in 16mV/LSB steps from 00h: SIG_C ± 2V to FFh: SIG_C ± 5.5V.

Other settings are as follows.

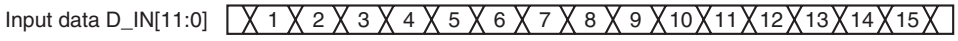
Mode setting

The CXA7004R can be set to master/slave mode, single mode, and right/left inversion, etc. This makes it possible to support various systems. (Various mode setting is designated with register and external pins.)

The various operating modes are described below.

• Operating mode setting <SLDAT>

The digital input of two ICs can be used together in master/slave mode by setting the Mode setting: SLDAT to high level, or single mode can be set by setting SLDAT to low level. In master/slave mode, the 12-bit input is shorted between the two ICs, and the ODD or EVEN data is selected by STATUS (Pin 30), DIRC (Pin 31) and the Mode setting: DIRCR. Input a clock having the same period as the input data rate to CLK (Pin 34) in both modes.



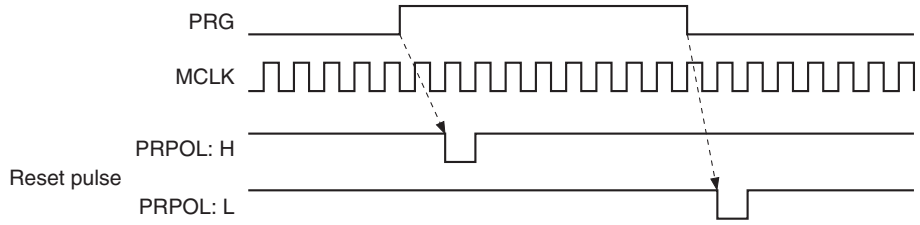
	SLDAT: L	SLDAT: H	
		STATUS: L	STATUS: H
DIRC ex-or DIRCR: H	SIG_OUT1: 1 SIG_OUT2: 2 SIG_OUT3: 3 SIG_OUT4: 4 SIG_OUT5: 5 SIG_OUT6: 6	SIG_OUT1: 2 SIG_OUT2: 4 SIG_OUT3: 6 SIG_OUT4: 8 SIG_OUT5: 10 SIG_OUT6: 12	SIG_OUT1: 1 SIG_OUT2: 3 SIG_OUT3: 5 SIG_OUT4: 7 SIG_OUT5: 9 SIG_OUT6: 11
DIRC ex-or DIRCR: L	SIG_OUT1: 6 SIG_OUT2: 5 SIG_OUT3: 4 SIG_OUT4: 3 SIG_OUT5: 2 SIG_OUT6: 1	SIG_OUT1: 11 SIG_OUT2: 9 SIG_OUT3: 7 SIG_OUT4: 5 SIG_OUT5: 3 SIG_OUT6: 1	SIG_OUT1: 12 SIG_OUT2: 10 SIG_OUT3: 8 SIG_OUT4: 6 SIG_OUT5: 4 SIG_OUT6: 2

• Clock polarity setting <CKPOL>

The polarity of the internal circuit operation clock (MCLK) is determined by the Mode setting: CKPOL.
The internal circuits operate at reverse polarity from CLK when CKPOL is high, and at the same polarity as CLK when CKPOL is low.

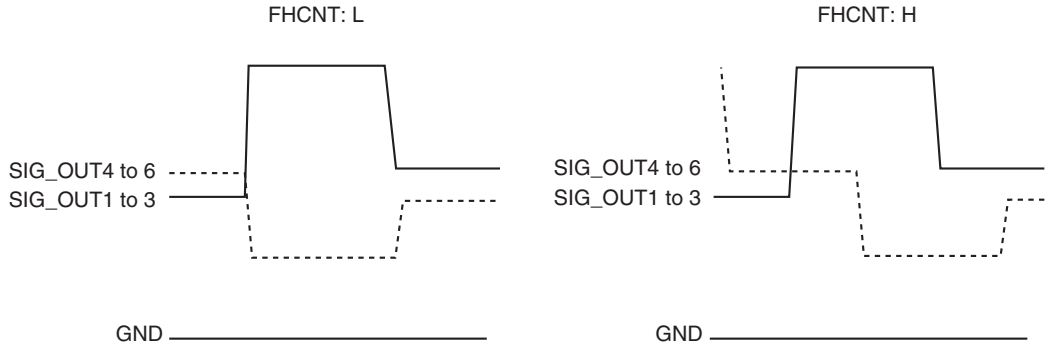
• Horizontal sync timing <PRPOL>

The horizontal sync signal PRG is also used as the internal circuit reset function.
The Mode setting: PRPOL sets whether to apply the reset at the rising edge or the falling edge of PRG.
The reset is applied at the rising edge of the PRG pulse when PRPOL is high, and at the falling edge of the PRG pulse when PRPOL is low.



• Output phase setting <FHCNT>

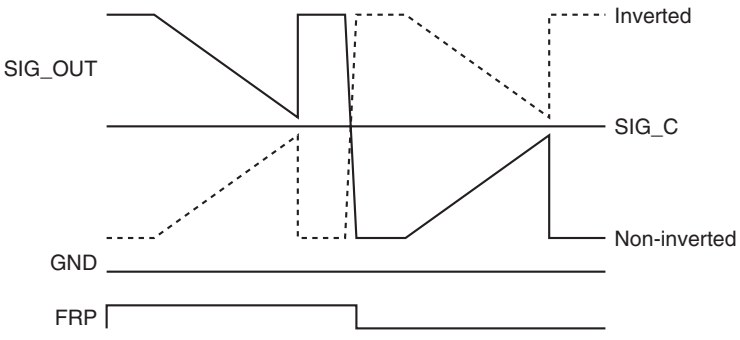
The SIG_OUT output timing phase can be set by the Mode setting: FHCNT.
When FHCNT is low, all SIG_OUT outputs are output at the same timing. When FHCNT is high, SIG_OUT1 to SIG_OUT3 and SIG_OUT4 to SIG_OUT6 are output at phases offset by 1/2 clock period from each other.



• Polarity setting <FRINV>

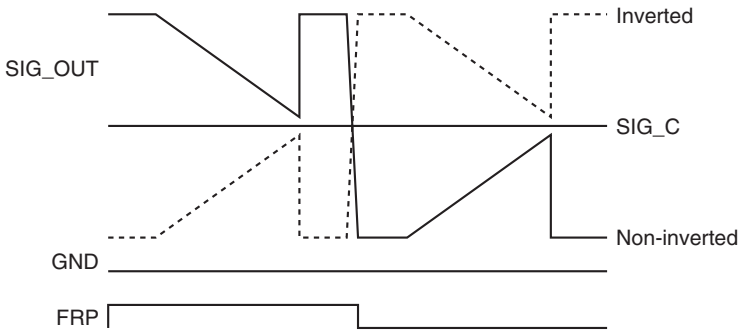
Output polarity inversion/non-inversion relative to the signal center voltage is set by the FRP input and the external pin FRINV (Pin 29). When set to the combinations shown in the table below, SIG_OUT is output non-inverted (solid line) or inverted (dotted line) relative to FRP.

	FRINV: H	FRINV: L
FRP: H	Non-inverted	Inverted
FRP: L	Inverted	Non-inverted

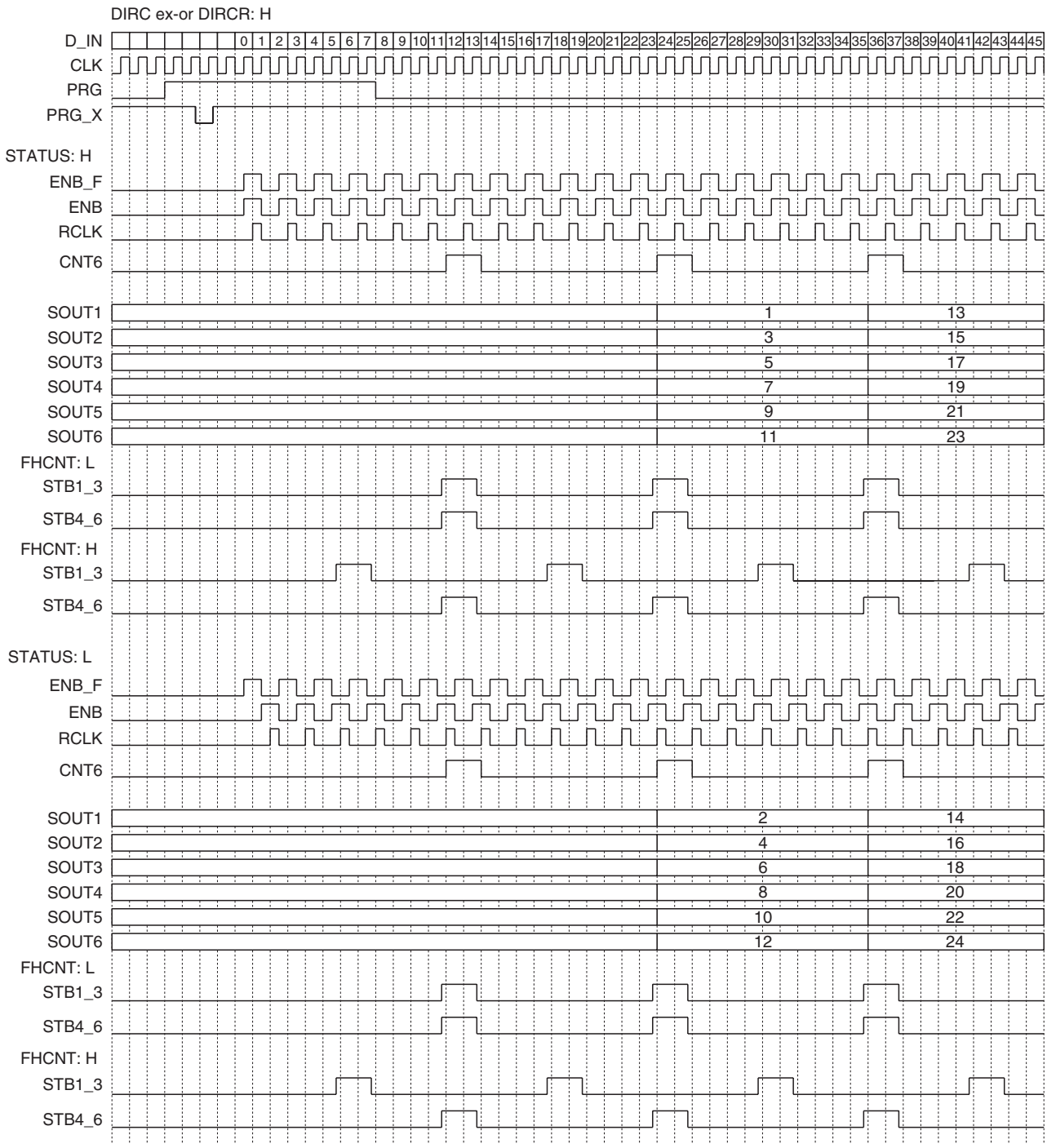


• Dot inversion and line inversion mode setting <SLINV>

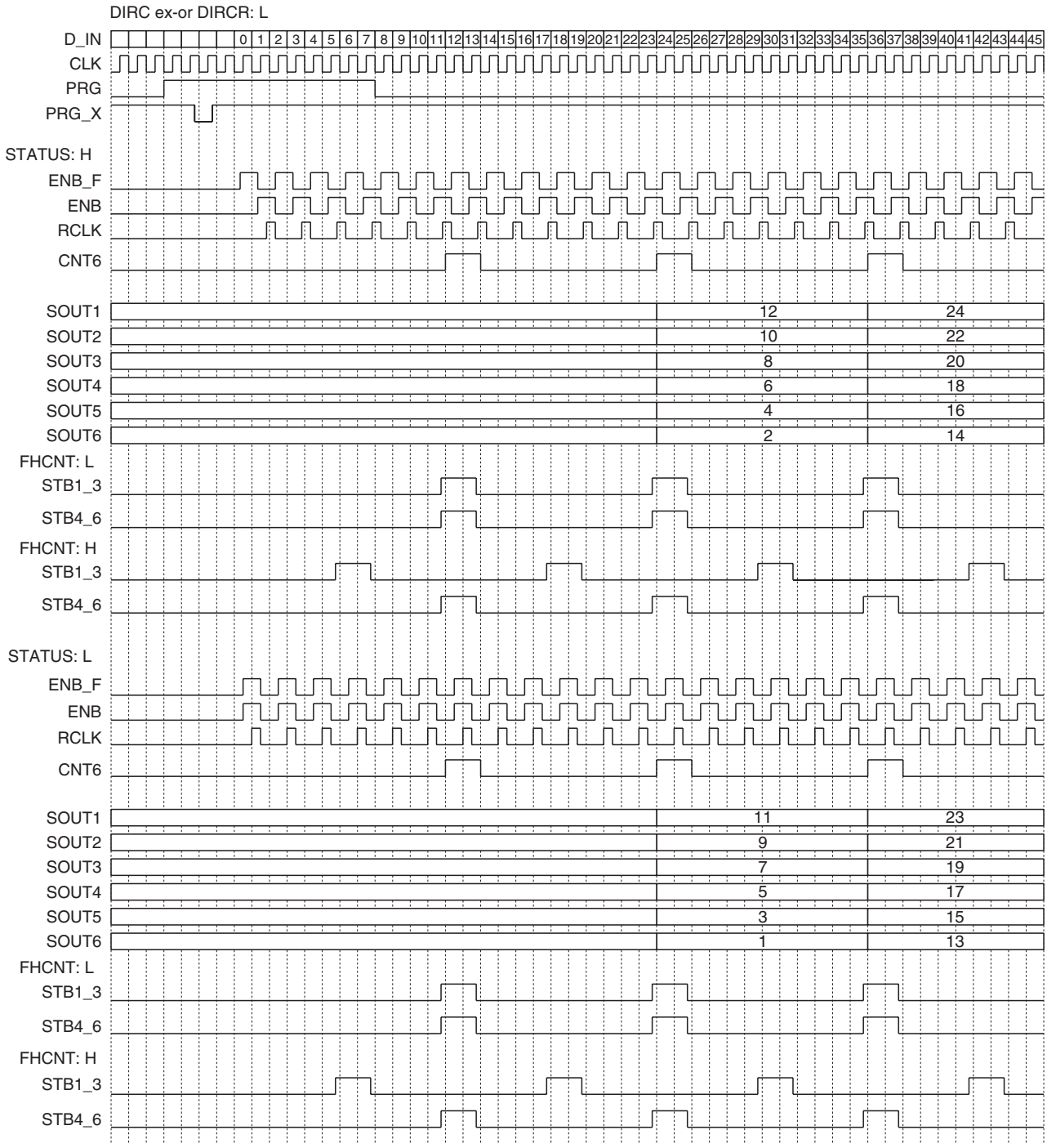
When Mode setting: SLINV is set to low level, all SIG_OUT channels are output at the same polarity as shown by the solid line in the figure below. When set to high level, the odd-numbered and even-numbered SIG_OUT outputs are output at inverse polarities. At this time the odd-numbered outputs are inverted when the FRP pulse is high, and non-inverted when the FRP pulse is low. Conversely, the even-numbered outputs are inverted when the FRP pulse is low, and non-inverted when the FRP pulse is high.



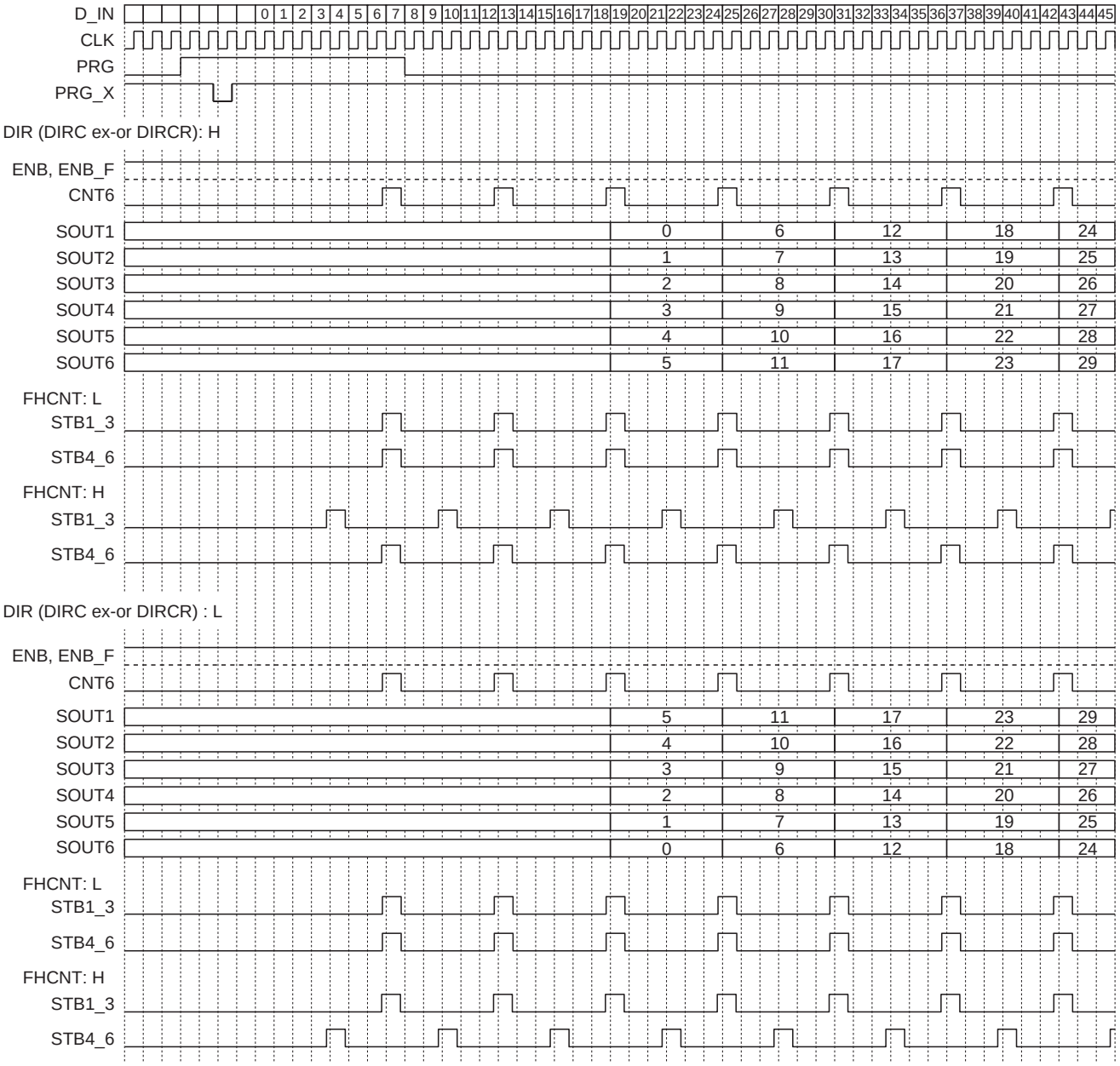
Master/Slave mode



Master/Slave mode

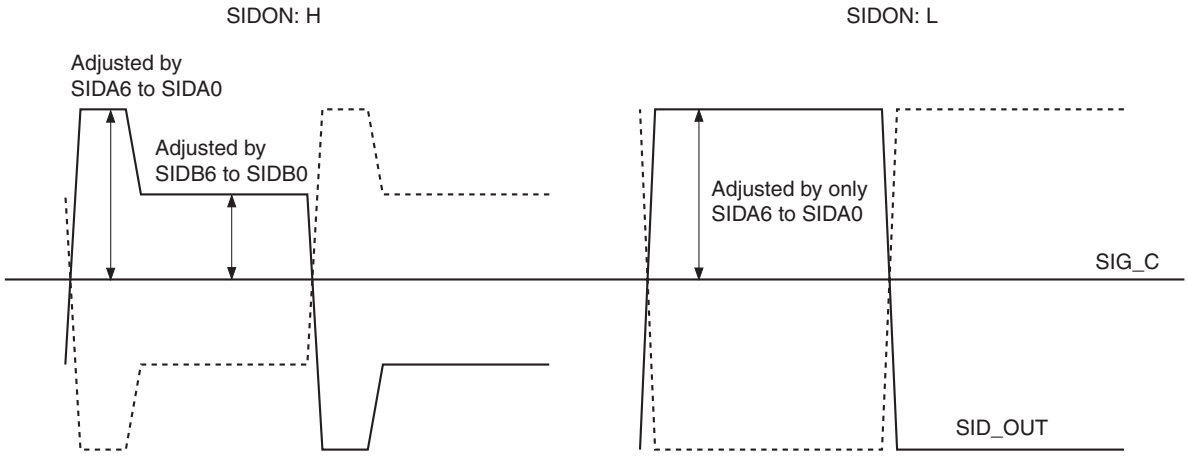


Single mode


D_IN
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45
CLK
PRG
PRG_X
DIR (DIRC ex-or DIRCR): H
ENB, ENB_F
CNT6
SOUT1 0 6 12 18 24
SOUT2 1 7 13 19 25
SOUT3 2 8 14 20 26
SOUT4 3 9 15 21 27
SOUT5 4 10 16 22 28
SOUT6 5 11 17 23 29
FHCNT: L
STB1_3
STB4_6
FHCNT: H
STB1_3
STB4_6
DIR (DIRC ex-or DIRCR) : L
ENB, ENB_F
CNT6
SOUT1 5 11 17 23 29
SOUT2 4 10 16 22 28
SOUT3 3 9 15 21 27
SOUT4 2 8 14 20 26
SOUT5 1 7 13 19 25
SOUT6 0 6 12 18 24
FHCNT: L
STB1_3
STB4_6
FHCNT: H
STB1_3
STB4_6

SID Signal Generator Block

This circuit generates the precharge signal waveform used by the LCD panel.
The SID_OUT output level switching function is set on and off by the Mode setting (D2): SIDON.
When SIDON is low level, adjustment uses only the register setting: SID control A. When SIDON is high level, adjustment is possible using both the register settings: SID control A and SID control B.
In addition, the SID_OUT output level relative to the signal center voltage can be set by the register settings: SID control A and SID control B. Adjustment is possible in 50mV/LSB steps from 00h: SIG_C ± 5.5V to 7Fh: SIG_C ± 0.1V for both settings.
SID_OUT cannot directly drive the precharge signal input of the LCD panel, so it should be connected through a buffer having sufficient current supply capability.

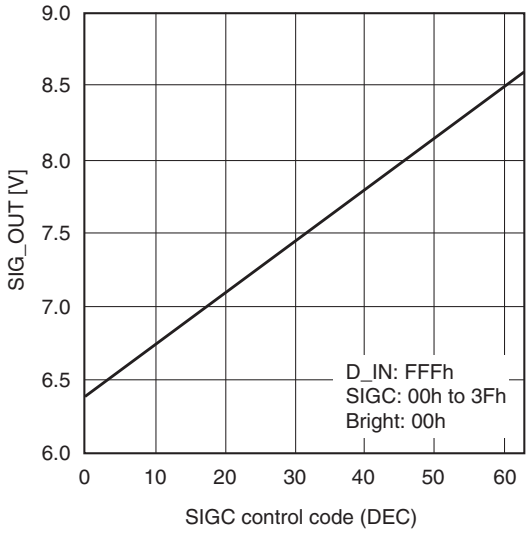


VCOM Voltage Generator Block

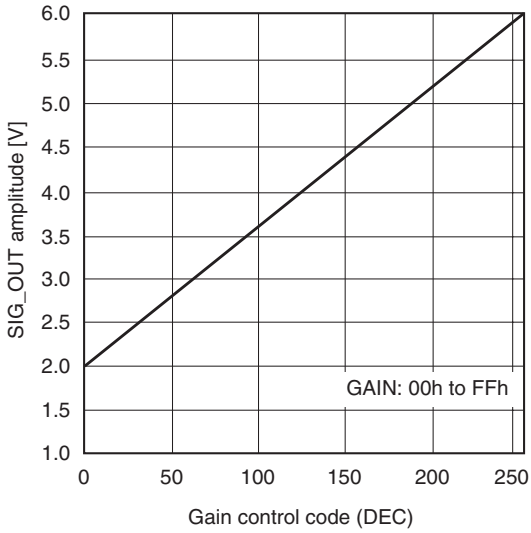
This block sets the DC common potential for the LCD panel.
The SIG_OUT center potential set by the SIG_C voltage can be adjusted by the register setting VCOM control. Adjustment is possible in 17.5mV/LSB steps from 00h: SIG_C – 2V to 7Fh: SIG_C – 0.1V.

Example of Representative Characteristics (V_{CC} = 15.25V, V_{DD} = 3.3V, Ta = 25°C)

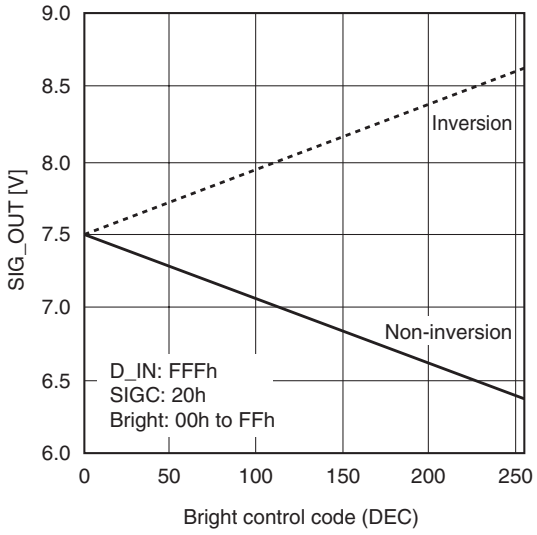
SIGC control characteristics



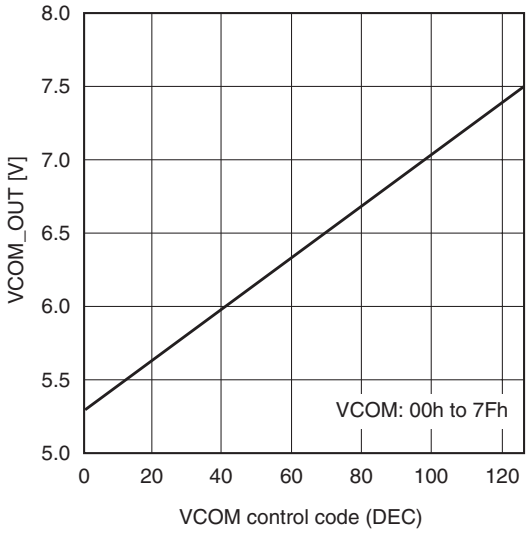
Gain control characteristics



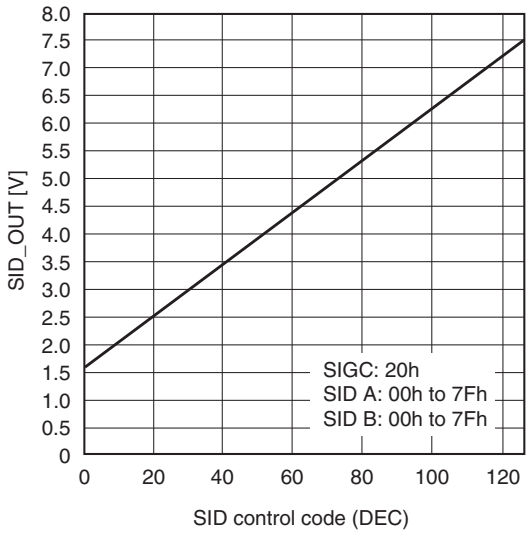
Bright control characteristics



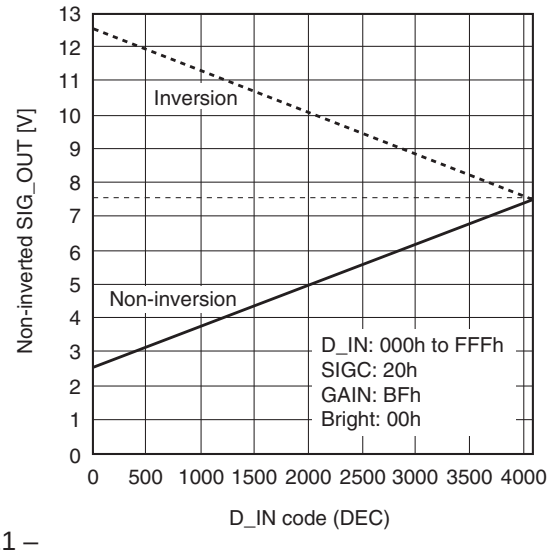
VCOM control characteristics



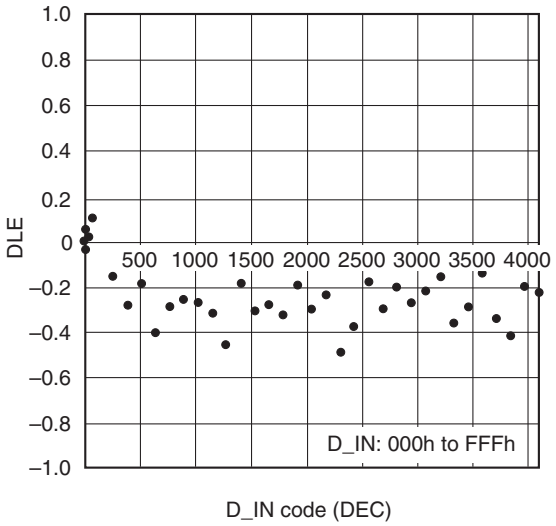
SID control characteristics



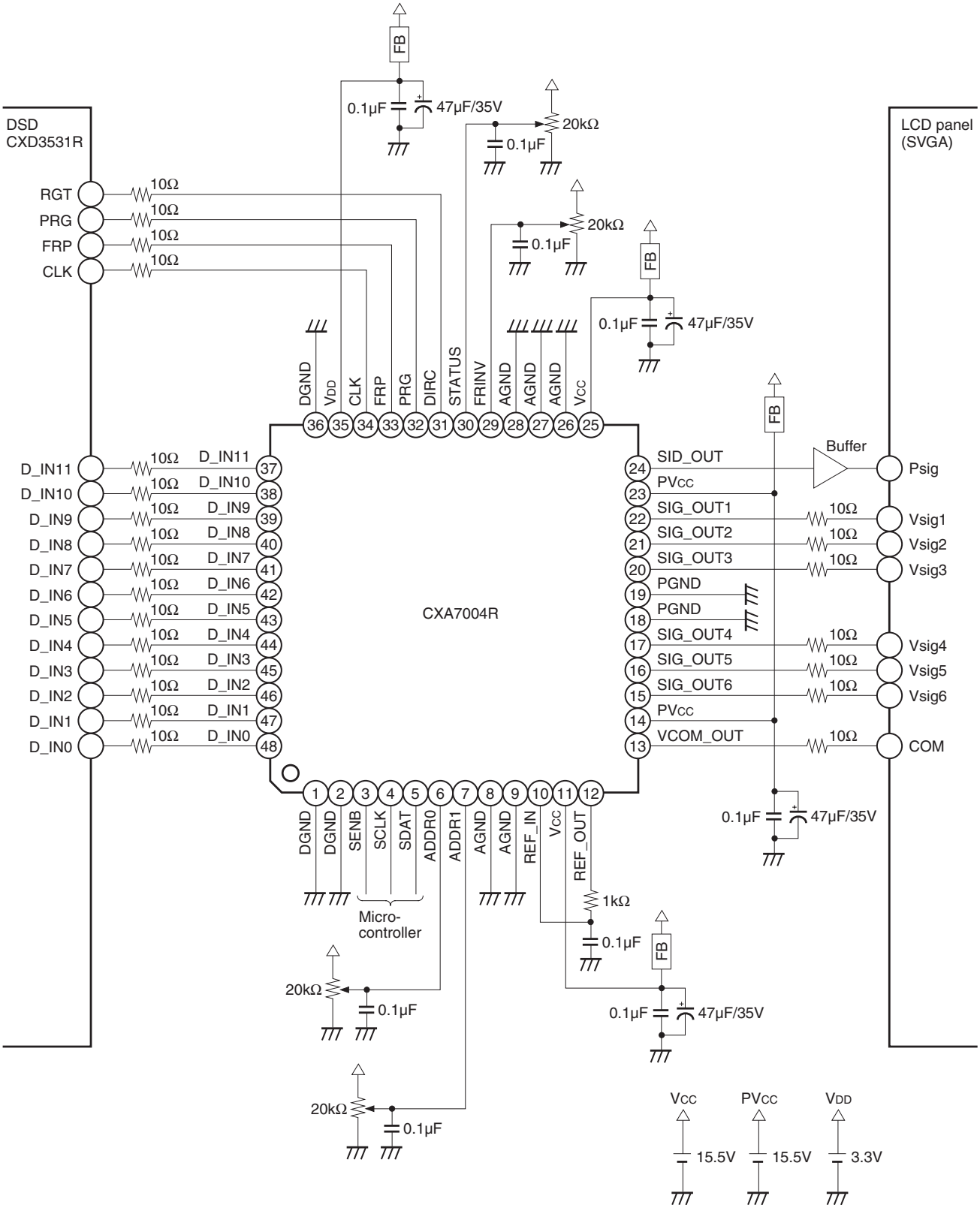
D_IN SIG_OUT characteristics



MAINDAC DLE characteristics

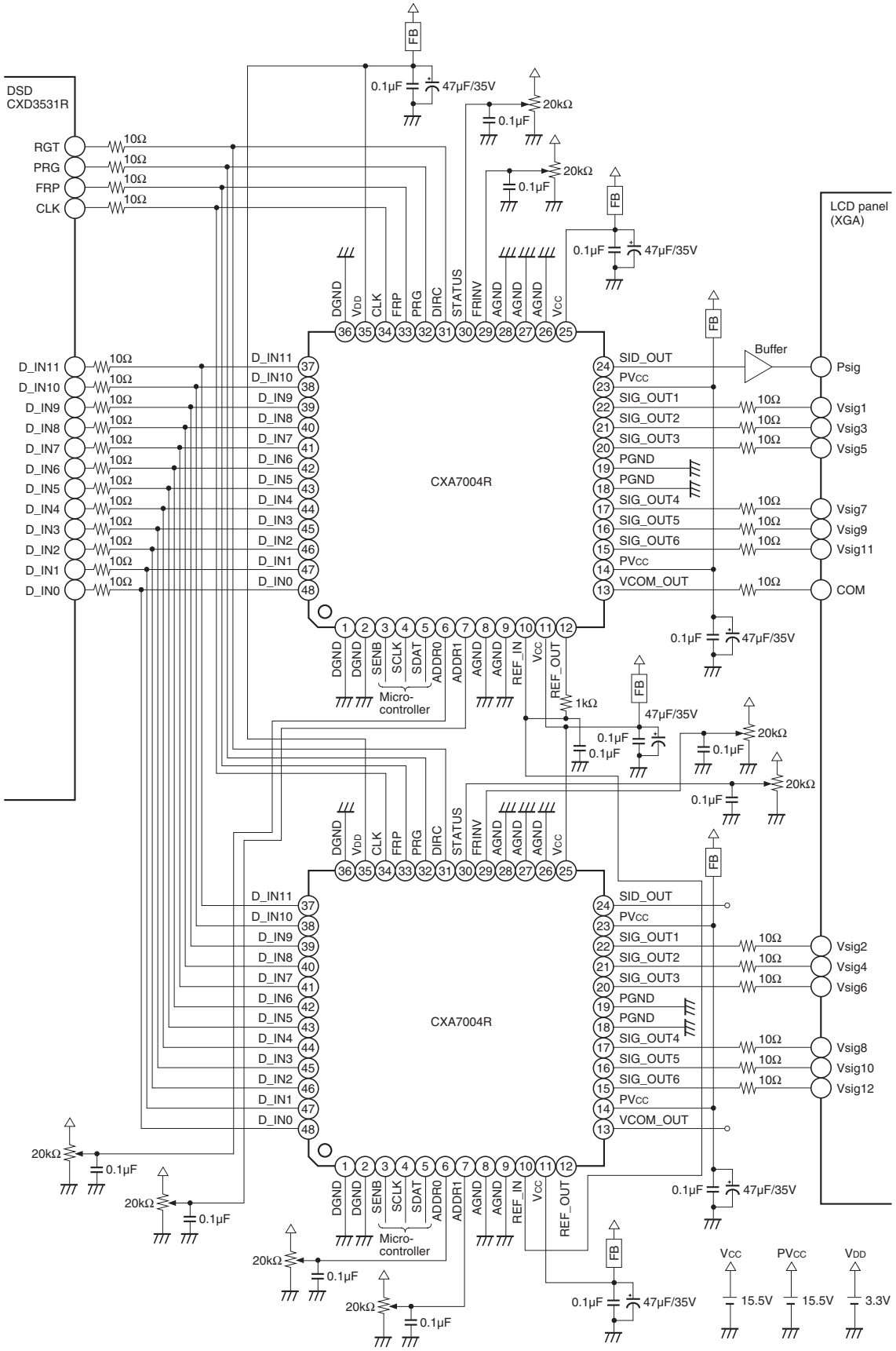


Application Circuit 1 — Application Circuit to SVGA Panel



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

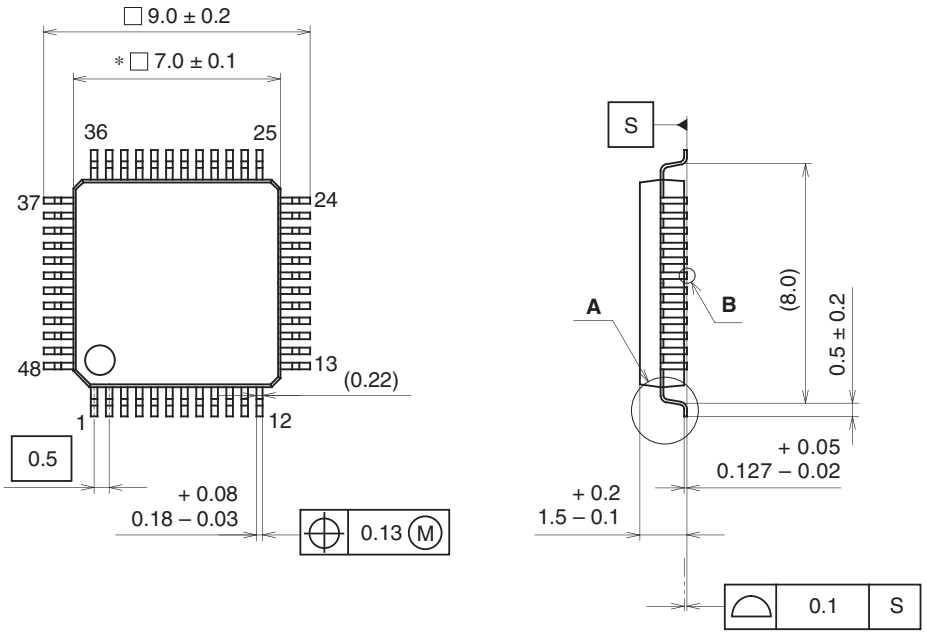
Application Circuit 2 — Application Circuit to XGA Panel

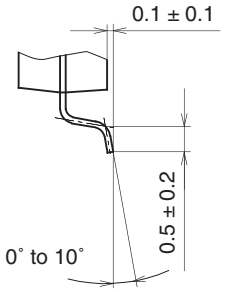


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

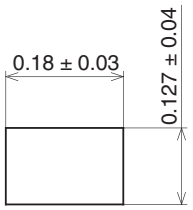
Package Outline Unit: mm

48PIN LQFP (PLASTIC)





DETAIL **A**



DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g