Am95C76

Orthogonal Rotation Processor (ORP)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Performs high-speed orthogonal rotation of font characters or blocks of bit-mapped data (0, 90, 180, and 270 degrees)
- Interfaces easily to the Am95C75 Raster Printer Controller (RPC) to allow high-speed printing with minimum font memory
- Can operate in standalone mode
- 64 x 64-bit internal memory is large enough to accommodate a standard-size font character at 400 dots-per-inch resolution
- Cascadable in all directions to handle large point-size fonts or bit-mapped data blocks
- Cascades automatically — interface signals make the ORP array function as one large ORP without additional user actions

GENERAL DESCRIPTION

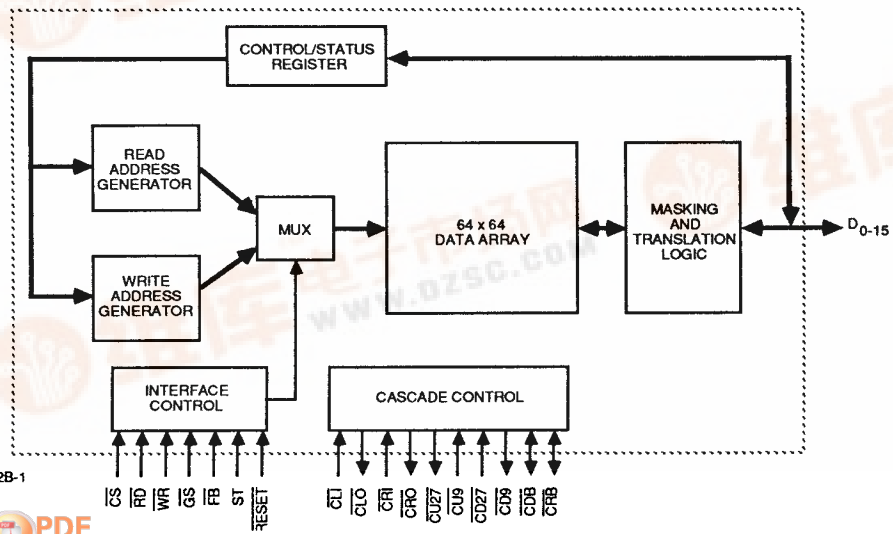
The Orthogonal Rotation Processor (ORP) is a high-performance CMOS device designed to provide orthogonal (0, 90, 180, and 270 degrees) rotation of font characters or blocks of bit-mapped data. In graphics systems, users may print data in portrait mode — where each line is printed across the narrow part of the page, or in landscape mode — where text is printed across the wide part of the page. To accomplish this, each font is usually stored in both portrait and landscape modes. Additionally, if two-sided (duplex) printing is desired, fonts must usually be stored with 180- and 270-degree rotations to print portrait and landscape modes on the back of a page. By using the ORP, 0-, 90-, 180-, and 270-degree rotations are possible, eliminating three-quarters of font memory conventionally used.

The ORP rotates an image block (a font character or other bit-mapped data) in two steps: first, the image block is loaded into the ORP where character size is user-programmed and data is transferred on 16-bit word boundaries; then the data is read from the ORP to the video buffer memory, where the page is assembled with the user-selected rotation.

The only user-accessible register in the ORP is the Control Status Register (CSR), which must be set up with valid parameters prior to each image block transfer. These parameters include image block dimensions, rotation angle, and an enable bit.

The 64 x 64-bit ORP memory may be increased by cascading additional ORPs; interface signals pass information between ORPs to allow the ORP array to function as one large ORP without additional control from the user.

BLOCK DIAGRAM



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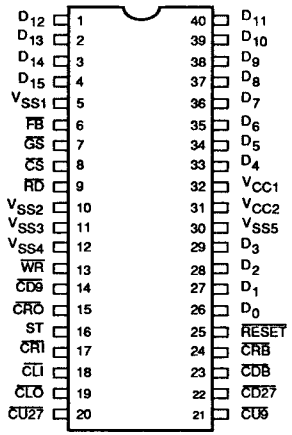
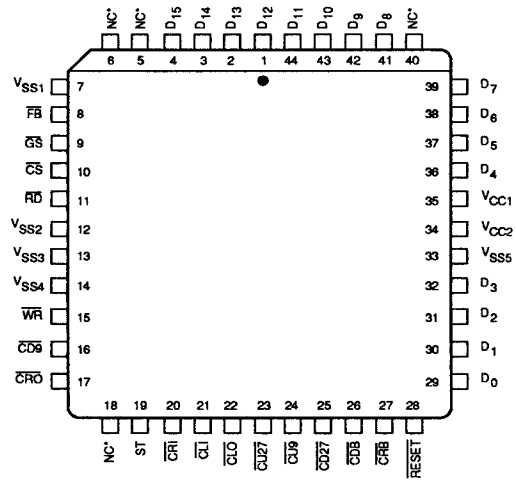
CONNECTION DIAGRAMS

Top View

DIP



PLCC



Note: Pin 1 marked for orientation.

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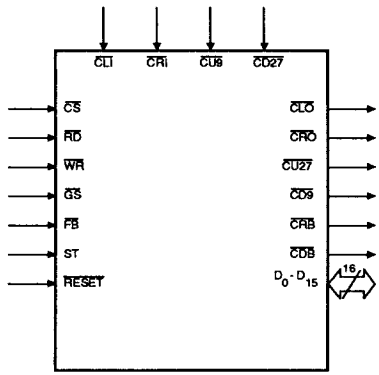
LOGIC SYMBOL



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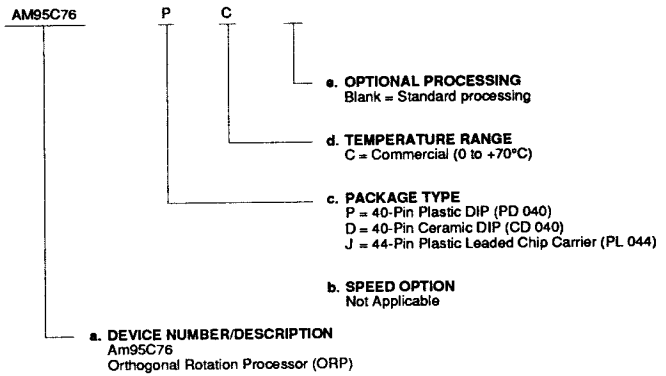
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations

Valid Combinations	
AM95C76	PC DC JC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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PIN DESCRIPTION

$\overline{CD9}$ Cascade Down 90 (Output; Active LOW)
The $\overline{CD9}$ output signal controls the vertical direction token passing in an ORP cascade. The $\overline{CD9}$ output pin of an ORP must be connected to the $\overline{CU9}$ input pin of the ORP below it in the cascade. The $\overline{CD9}$ pin is asserted LOW on **one** of the following conditions: 1) the ORP is in 90-degree Read mode and the current data array read access results in a complete vertical row access (as defined by the XAR field of CSR); and 2) the ORP is in Write mode or 0-degree Read mode, the $\overline{CLI}$ input is asserted LOW, and the entire font section assigned to the ORP has been written to/read from. $\overline{CD9}$ output assertion of an ORP causes the cascade token to be passed to the ORP below it in the cascade.

$\overline{CD27}$ Cascade Down 270 (Input; Active LOW)
The $\overline{CD27}$ input signal controls the vertical direction token passing in an ORP cascade. The $\overline{CD27}$ input pin of an ORP must be connected to the $\overline{CU27}$ output pin of the ORP below it in the cascade. The cascade token is passed through this input pin in 270-degree Read mode and 180-degree Read mode.

$\overline{CDB}$ Cascade Down Bypass (Input/Output; Open Drain, Active LOW)
The $\overline{CDB}$ signal controls the vertical direction token passing in an ORP cascade. This pin is an output when the ORP is in 90-degree Read mode. $\overline{CDB}$ is driven LOW if the ORP is disabled (bit 15 of the CSR is 0) and the $\overline{CU9}$ input pin is LOW. The $\overline{CDB}$ pins of all vertically cascaded ORPs should be connected together and tied to +5 V with an external pull-up resistor. $\overline{CDB}$ pin is an input if the ORP is in 270-degree Read mode; if the ORP is disabled (bit 15 of the CSR = 0) and the $\overline{CDB}$ input is asserted LOW, the $\overline{CU27}$ output pin will be driven LOW immediately.

$\overline{CLI}$ Cascade Left In (Input; Active LOW)
The $\overline{CLI}$ input signal controls the horizontal direction token passing in an ORP cascade. The $\overline{CLI}$ input pin of an ORP must be connected to the $\overline{CRO}$ output pin of the ORP to its right in the cascade. The cascade token is passed through this input pin in Write mode, 0-degree Read mode, and 270-degree Read mode.

$\overline{CLO}$ Cascade Left Out (Output; Active LOW)
The $\overline{CLO}$ output signal controls the horizontal direction token passing in an ORP cascade. The $\overline{CLO}$ output pin of an ORP must be connected to the $\overline{CRI}$ input pin of the ORP to its left in the cascade. The $\overline{CLO}$ pin is asserted LOW on **one** of the following conditions: 1) the ORP is in 90-degree Read mode, the $\overline{CU9}$ input is LOW, and the entire font section assigned to the ORP has been read; 2) the ORP is in 180-degree Read mode and the current data array read access results in a complete horizontal row access (as defined by the XAR field of the CSR); and 3) the ORP is in 180-degree Read mode, bit 15 of CSR is 0 (disabled), and $\overline{CRB}$ is LOW. $\overline{CLO}$ output assertion of an ORP causes the cascade token to be passed to the ORP to its left in the cascade.

$\overline{CRB}$ Cascade Right Bypass (Input/Output; Open Drain, Active LOW)
The $\overline{CRB}$ signal controls the horizontal direction token passing in an ORP cascade. This pin is an output when the ORP is in Write mode or 0-degree Read mode. In this case, $\overline{CRB}$ is driven LOW if the ORP is disabled (bit 15 of the CSR is 0) and the $\overline{CLI}$ input pin is asserted LOW. The $\overline{CRB}$ pins of all horizontally cascaded ORPs should be connected together and tied to +5 V with an external pull-up resistor. $\overline{CRB}$ pin is an input if the ORP is in 180-degree Read mode; if the ORP is disabled (bit 15 of the CSR = 0) and the $\overline{CRB}$ input is asserted LOW, the $\overline{CLO}$ output pin will be driven LOW immediately.

$\overline{CRI}$ Cascade Right In (Input; Active LOW)
The $\overline{CRI}$ input signal controls the horizontal direction token passing in an ORP cascade. The $\overline{CRI}$ input pin of an ORP must be connected to the $\overline{CLO}$ output pin of the ORP to its right in the cascade. The cascade token is passed through this input pin in 90-degree Read mode and 180-degree Read mode.

$\overline{CRO}$ Cascade Right Out (Output; Active LOW)
The $\overline{CRO}$ output signal controls the horizontal direction token passing in an ORP cascade. The $\overline{CRO}$ output pin of an ORP must be connected to the $\overline{CLI}$ input pin of the ORP to its right in the cascade. The $\overline{CRO}$ pin is asserted LOW on **one** of the following conditions: 1) the ORP is in 270-degree Read mode, the $\overline{CD27}$ input is LOW, and the entire font section assigned to the ORP has been read; and 2) the ORP is in Write mode or 0-degree Read mode and the current data array write/read access results in a complete horizontal row access (as defined by the XAR field of the CSR). $\overline{CRO}$ output assertion of an ORP causes the cascade token to be passed to the ORP to its right in the cascade.

$\overline{CS}$ Control/Status Select (Input; Active LOW)
The $\overline{CS}$ input is an active-LOW signal used by the host processor to access the Control Status Register (CSR) of the ORP. $\overline{CS}$ pins of cascaded ORPs must not be connected together.

$\overline{CU9}$ Cascade Up 90 (Input; Active LOW)
The $\overline{CU9}$ input signal controls the vertical direction token passing in an ORP cascade. The $\overline{CU9}$ input pin of an ORP must be connected to the $\overline{CD9}$ output pin of the ORP above it in the cascade. The cascade token is passed through this input pin in Write mode, 0-degree Read mode, and 90-degree Read mode.

$\overline{CU27}$ Cascade Up 270 (Output; Active LOW)
The $\overline{CU27}$ output signal controls the vertical direction token passing in an ORP cascade. The $\overline{CU27}$ output pin of an ORP must be connected to the $\overline{CD27}$ input pin of the ORP above it in the cascade. The $\overline{CU27}$ pin is asserted LOW on **one** of the following conditions: 1) the ORP is in 270-degree Read mode and the current data array read access results in a complete vertical row access (as defined by the XAR field of CSR); 2) the ORP is in 180-

degree Read mode, the $\overline{CRI}$ input is LOW, and the entire font section assigned to the ORP has been read; and 3) the ORP is in 270-degree Read mode, bit 15 of the CSR is 0 (disabled), and the $\overline{CDB}$ input is LOW. $\overline{CU27}$ output assertion of an ORP causes the cascade token to be passed to the ORP above it in the cascade.

D_0–D_{15} Data Bus (Input/Output; Three State)
The 16-bit Data Bus is used for data transfer between the ORP and the host processor or Font Memory.

$\overline{FB}$ $\overline{Fly\text{-}By}$ (Input; Active LOW)
The $\overline{FB}$ input is an active-LOW signal used by the host processor to access the data array of the ORP during a Fly-By operation. An $\overline{RD}$ strobe assertion in conjuction with an $\overline{FB}$ assertion causes a write access to the ORP data array if the R/$\overline{W}$ bit in the Control Status Register is 0. A $\overline{WR}$ assertion in conjunction with an $\overline{FB}$ assertion causes a read access to the ORP data array if the R/$\overline{W}$ bit in the CSR is 1. $\overline{FB}$ pins of cascaded ORPs should be connected together.

$\overline{GS}$ $\overline{Group\ Select}$ (Input; Active LOW)
The $\overline{GS}$ input is an active-LOW signal used by the host processor to access the data array of the ORP during a Normal Read/Write operation. $\overline{GS}$ pins of cascaded ORPs should be connected together.

$\overline{RD}$ $\overline{Read}$ (Input; Active LOW)
The $\overline{RD}$ input is an active-LOW signal used by the host processor to read the CSR when $\overline{CS}$ input is asserted, to read from the ORP data array when the $\overline{GS}$ input is asserted, and to write into the ORP data array when $\overline{FB}$ input is asserted. On either a CSR read access or a data array read access, the ORP will drive D_0–D_{15} with data while $\overline{RD}$ input is LOW. In Fly-By mode the $\overline{RD}$ input is used as a write strobe; the ORP uses the rising edge of $\overline{RD}$ to write the data on pins D_0–D_{15} into the internal data array. $\overline{RD}$ pins on cascaded ORPs should be connected together.

$\overline{RESET}$ $\overline{Reset}$ (Input; Active LOW)
$\overline{RESET}$ is an asynchronous active-LOW input which initializes the ORP. The effect of $\overline{RESET}$ is to clear all 16 bits of the Control Status Register, force D_0–D_{15} pins to high-impedance state, and force all cascade output pins inactive (HIGH).

ST Start (Input; Active HIGH)
The ST input is an active-HIGH signal used by the host processor to initiate a read/write access to the ORP. The ST inputs of all cascaded ORPs should be connected together. When connecting the ORP to the RPC (Am95C75), the ST input of the ORP should be connected to the FALE1 pin of the RPC.

V_{CC1}, V_{CC2} +5-V Power Supply

V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SS5} Ground

$\overline{WR}$ $\overline{Write}$ (Input; Active LOW)
The $\overline{WR}$ input is an active-LOW signal used by the host processor to write into the CSR when $\overline{CS}$ input is asserted, to write into the ORP data array when $\overline{GS}$ input is asserted, and to read from the ORP data array when $\overline{FB}$ input is asserted. On either a CSR write access or a Normal data array write access, D_0–D_{15} must be driven with valid data prior to the rising edge of $\overline{WR}$. In Fly-By mode, the $\overline{WR}$ input is used as a read strobe; the ORP will drive D_0–D_{15} with data from the internal data array while $\overline{WR}$ is LOW. $\overline{WR}$ pins of cascaded ORPs should be connected together.

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FUNCTIONAL DESCRIPTION

The block diagram for the Am95C76 is shown on the front cover. Communication with the external host processor takes place over the 16-bit Data Bus, D_0–D_{15}. Transfers over the Data Bus are controlled by the $\overline{CS}$, $\overline{GS}$, $\overline{FB}$, ST, $\overline{RD}$, and $\overline{WR}$ input lines. Communication between cascaded ORPs occur over the cascade control signals $\overline{CLO}$, $\overline{CRO}$, $\overline{CLI}$, $\overline{CRI}$, $\overline{CD9}$, $\overline{CU27}$, $\overline{CU9}$, $\overline{CD27}$, $\overline{CRB}$, and $\overline{CDB}$.

There are six major functional blocks in the ORP: 1) 64 x 64 data array, 2) cascade control logic, 3) host processor interface control logic, 4) control status register (CSR), 5) data array read/write address generation logic, and 6) data array read mask translation logic. The ORP is controlled by the 16-bit control status register (CSR). The CSR specifies the font horizontal size, font vertical size, Read/Write mode, angle of rotation, font clipping status, chip enable, and cascade token.

Control Status Register (CSR)

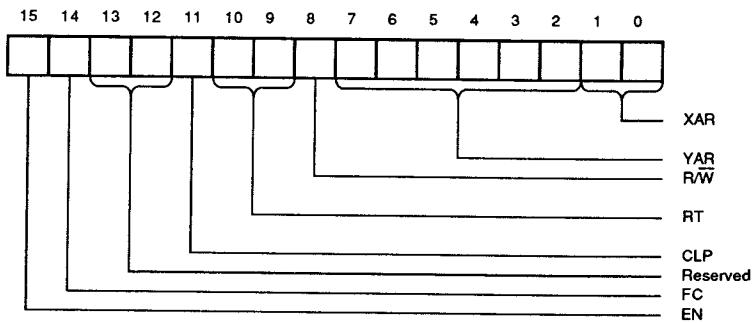
This 16-bit register is used for issuing commands and receiving status information. Figure 1 shows the bit assignment of the CSR. The $\overline{CS}$ input pin acts as the read/write enable for CSR. When the $\overline{RD}$ input is LOW, the ORP status information is driven onto the D_0–D_{15} lines; when the $\overline{WR}$ input is LOW, the data on D_0–D_{15} lines is loaded into the CSR. The CSR is cleared when the $\overline{RESET}$ input pin is LOW. There are two reserved bits in the CSR; these bits must be programmed to 0.

Chip Enable (EN)

The EN bit controls the state of the ORP. When this bit is set to 1, the ORP is enabled and data transfer between the internal data array and the D_0–D_{15} pins is allowed. When this bit is cleared to 0, the ORP is disabled and no data transfers between the internal data array and the D_0–D_{15} pins can occur. In a multiple ORP cascade, the unused ORPs should be disabled by programming their EN bits to 0.

First Chip (FC)

The FC bit is the cascade token. When this bit is set to 1, the ORP is enabled (provided EN is set to 1) and data transfer between the internal data array and the D_0–D_{15} pins is allowed. When this bit is programmed to 0, the ORP is disabled and data transfer between the internal data array and the D_0–D_{15} pins is inhibited. While initializing ORPs only one ORP should have its FC bit set to 1. The location of the ORP whose FC bit is to be initialized to 1 is a function of the rotation angle while performing a font or bit-map data array read; see Figure 2 for details. Before a font or bit-map data array write, the FC bit of the **top-left** ORP should be set to 1. **For a single ORP application, the FC bit should be set to 1 to enable data array read/write.** The FC bit is propagated between ORPs in the cascade configuration through the cascade interface control pins, without intervention by the host processor. Since the host processor interface signals (ST, $\overline{GS}$, $\overline{FB}$, $\overline{RD}$, $\overline{WR}$, D_0–D_{15}) of cascaded ORPs are inter-connected, the FC bit ensures that the internal data array of only **one** of the cascaded ORPs is connected to the D_0–D_{15} lines at any time.



Key: XAR = X image size in 16-bit words
YAR = Y pixel size
R/W = 1 (Read only)
0 (Write only)
RT = 00 (0° Rotation)
01 (90° Rotation)
10 (180° Rotation)
11 (270° Rotation)
CLP = 1 (No translation)
0 (Translates logical to physical address)
FC = 1 (Enable token)
0 (Disable token)
EN = 1 (Enable)
0 (Disable)

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Figure 1. Control Status Register Format

Clipping (CLP)

This bit is used to generate the starting address for the internal data array in conjunction with the YAR and XAR fields of the CSR. The CLP bit should be programmed to 0 when the XAR and YAR fields of the CSR specify the unprocessed font size (e.g., ORP initialization for a **complete** font write/read from the internal data array). The ORP translates the logical addresses to physical addresses for the internal data array if the CLP bit is programmed to 0.

The CLP bit is set to 1 by the ORP after an internal data array access has occurred. The CLP bit significantly reduces host processor overhead in resuming ORP data array writes/reads on a partially processed font. Partially processed fonts occur when the ORP is used in conjunction with image blocks larger than the video memory size. Typically the video memory is configured to hold an integral number of scan lines of the image block. Fonts get "clipped" at the video memory overflow boundary; therefore, the ORP is designed to rotate partially processed fonts. The ORP provides the host processor with the next physical Y address and the font X size on a CSR read after clipping. The host processor then stores the CSR value in memory and copies the stored value into CSR to resume processing on a clipped font. Since the CLP bit would be set by the ORP to 1 after a data array access, the XAR and YAR fields are interpreted as physical addresses for the internal data array. The CLP bit should not be cleared to 0 by the host processor on resuming clipped font processing.

Rotation Mode (RT)

These bits specify the angle of rotation while reading data out of the ORP internal data array. The ORP allows for 0-, 90-, 180-, and 270-degree rotations. The following table shows the definition of this field:

Bit 1	Bit 0	Rotation Angle (Counter Clockwise)
0	0	0 degree
0	1	90 degree
1	0	180 degree
1	1	270 degree

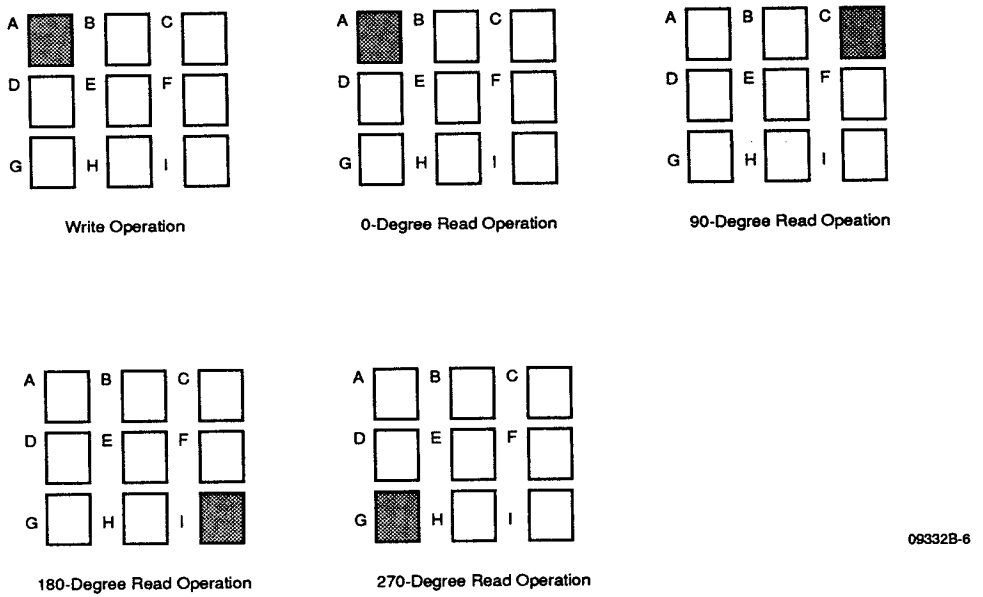

Figure 2. FC Bit Position in Cascade Configuration
(While processing 3 x 3 fonts/images > 128 pixels in both X & Y dimensions)

Reset Mode

The ORP enters into Reset mode when the $\overline{RESET}$ input pin is asserted. The Control Status Register is cleared; since the EN bit and FC bits are cleared, all data transfers through the Data Bus D_0–D_{15}, except for write to CSR, are ignored by the ORP.

Normal Read Mode

The ORP is in Normal Read mode when the R/$\overline{W}$ bit in CSR is 1 and the $\overline{GS}$ and $\overline{RD}$ input pins are asserted LOW. If the EN and FC bits in CSR are both set to 1, a data array read transaction occurs; if either bit is 0, the data array read transaction is inhibited and D_0–D_{15} output pins float.

Normal Write Mode

The ORP is in Normal Write mode when the R/$\overline{W}$ bit in CSR is 0 and the $\overline{GS}$ and $\overline{WR}$ input pins are asserted LOW. If the EN and FC bits in CSR are both set to 1, a data array write transaction occurs; if either bit is 0, the data array write transaction is inhibited and D_0–D_{15} input pins are ignored.

Fly-By Read Mode

The ORP is in Fly-By Read mode when the R/$\overline{W}$ bit in CSR is 1 and the $\overline{FB}$ and $\overline{WR}$ input pins are asserted LOW. The Fly-By Read mode allows the host processor to simultaneously read from the ORP data array and write into the Font Memory (e.g., while building a Font Memory of rotated fonts using the ORP to rotate font data). If the EN and FC bits in CSR are both set to 1, a data array read transaction occurs; if either bit is 0, the data array read transaction is inhibited and D_0–D_{15} pins float.

Fly-By Write Mode

The ORP is in Fly-By Write mode when the R/$\overline{W}$ bit in CSR is 0 and the $\overline{FB}$ and $\overline{RD}$ input pins are asserted LOW. The Fly-By Write mode allows the host processor to simultaneously read from the Font Memory and write into the ORP (e.g., while down-loading a font into the ORP for rotation). If the EN and FC bits in CSR are both set to 1, a data-array write transaction occurs; if either bit is 0, the data-array write transaction is inhibited and D_0–D_{15} input pins are ignored.

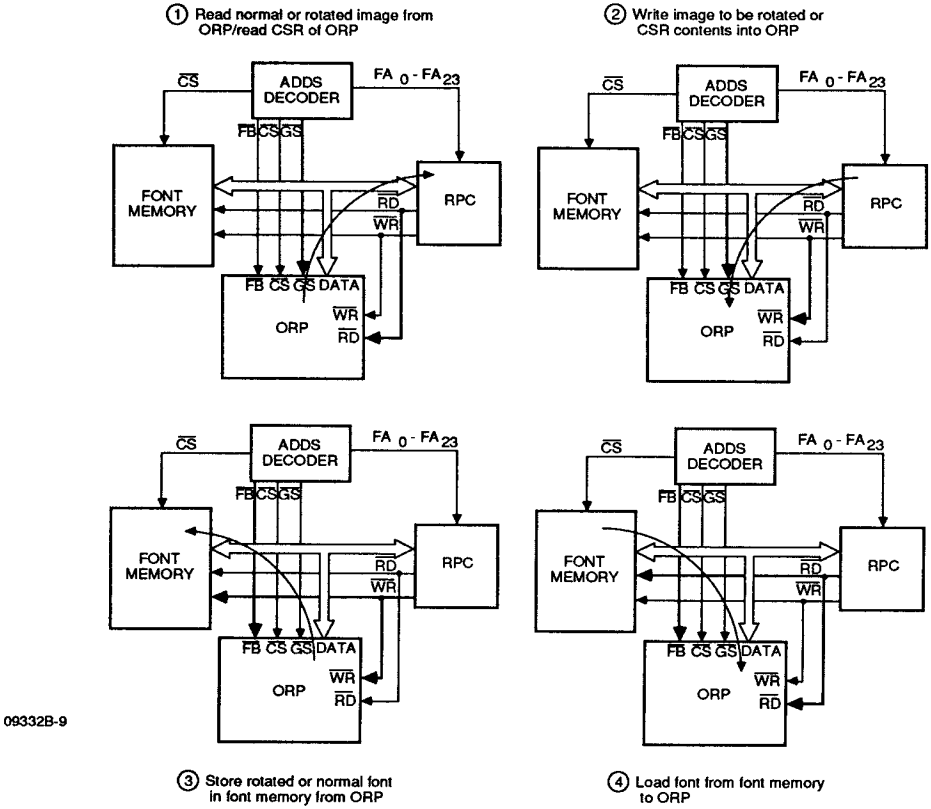

Figure 4. ORP Operation Modes

Figure 3-1 shows the output image of each rotation mode. Note that the RT field is ignored when data is written into the ORP data array (R/$\overline{W}$ = 0).

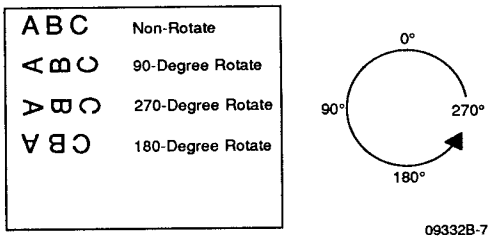

Figure 3-1. Output Format of Each Rotation Mode

Read/$\overline{\text{Write}}$ (R/$\overline{W}$)

The R/$\overline{W}$ bit controls the ORP operation mode. If this bit is programmed to 1, the ORP data array is configured as read only (i.e., Normal Read or Fly-By Read mode). If this bit is 0, the ORP data array is configured as write only (i.e., Normal Write or Fly-By Write mode).

Y Address Register (YAR)

The 6-bit YAR field specifies the Y size of the image block in pixels. The actual value loaded into YAR is the required number of pixels minus one.

In 90- and 180-degree rotation modes, the content of YAR represents the physical start address for the data array in the Y direction.

In 0- and 270-degree rotation modes, the initialized content of YAR represents the physical end address for the data array in the Y direction. If the CLP bit is programmed to 0, the physical start address is assumed to be 0 in the Y direction, whereas if the CLP bit is programmed to 1, the value in the YAR field is interpreted as the physical start address in the Y direction for processing a clipped font.

X Address Register (XAR)

The 2-bit XAR field specifies the X size of the image block in words. The value loaded into XAR is the required number of words minus one.

Under the 180- and 270-degree rotation modes, the content of XAR represents the physical start address for the data array in the X direction.

Under the 0- and 90-degree rotation modes, the content of XAR represents the physical end address of the data array in the X direction.

Operation Modes

The ORP has seven operation modes: 1) CSR Read, 2) CSR Write, 3) Reset, 4) Normal Read, 5) Normal Write, 6) Fly-By Read, and 7) Fly-By Write (see Figure 4). Any combination of inputs other than those defined below are invalid operating modes and are ignored by the ORP.

CSR Read Mode

When $\overline{CS}$ and $\overline{RD}$ are asserted LOW, the D_0–D_{15} lines are driven with CSR contents.

CSR Write Mode

When $\overline{CS}$ and $\overline{WR}$ are asserted LOW, the data on D_0–D_{15} is latched into the CSR on the trailing edge of $\overline{WR}$.

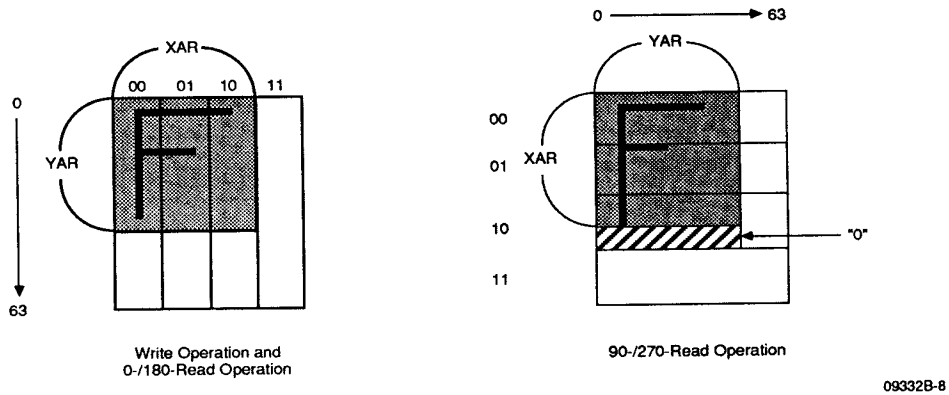

Figure 3-2. Relationship Between XAR Value and YAR Value

Data Handling and Formats

All data transferred on the host processor interface to the ORP are 16 bits wide; this is true for CSR transactions as well as data-array transactions. The internal data-array addressing and the bit assignment are different for the write access and the four read rotation modes. Figure 5 shows the MSB/LSB position in each operation.

In a data-array write operation, 0-degree read operation, and 90-degree read operation, the bit assignment of the data array corresponds to the actual image block; the top-left position is the MSB bit. In a 180- or 270-degree data-array read operation, the MSB/LSB is in reverse order; the bit reversal is handled within the ORP (see Figure 5).

Cascade Control

Multiple ORPs can be cascaded in any number, both horizontally and vertically, with respect to font scan direction. In a cascade configuration, any size font or bit-map image can be accommodated. The ten cascade signals (described in the pin description section) control the cascade token (FC) propagation through the multi-ORP cascade. $\overline{CLI}$, $\overline{CLO}$, $\overline{CRI}$, $\overline{CRO}$, and $\overline{CRB}$ control horizontal direction cascade token passing. $\overline{CU9}$, $\overline{CU27}$, $\overline{CD9}$, $\overline{CD27}$, and $\overline{CDB}$ control vertical direction cascade token passing. If the EN bit of CSR of a cascaded ORP is 0, then the cascade token will be passed through it to the next enabled ORP. $\overline{CRB}$ and $\overline{CDB}$ are bidirectional, open-drain signals and facilitate token pass-through on disabled ORPs.

Figure 6 shows the input/output definition of the cascade control signals in the data array write mode and the four read rotation modes.

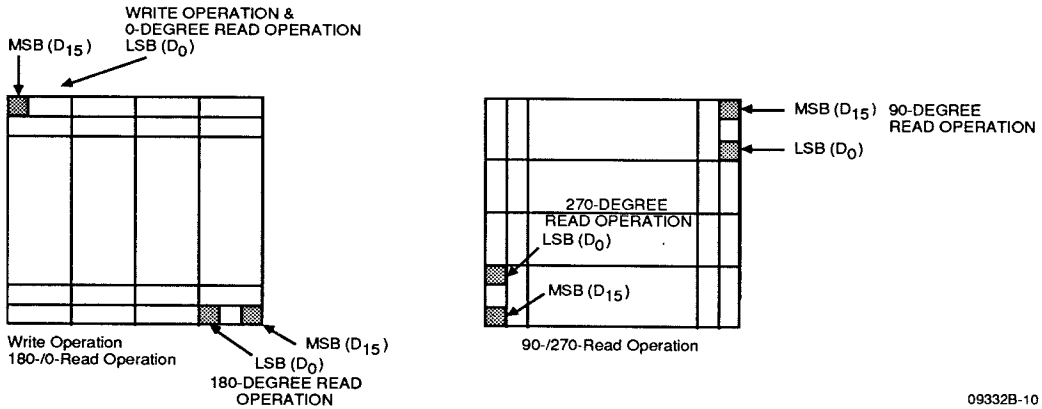

Figure 5. ORP Data Array Bit Position

	Write	0-Degree Read	90-Degree Read	180-Degree Read	270-Degree Read
$\overline{CLI}$	INPUT	INPUT			INPUT
$\overline{CLO}$			OUTPUT	OUTPUT	
$\overline{CRI}$			INPUT	INPUT	
$\overline{CRO}$	OUTPUT	OUTPUT			OUTPUT
$\overline{CU27}$				OUTPUT	OUTPUT
$\overline{CD9}$	OUTPUT	OUTPUT	OUTPUT		
$\overline{CD27}$				INPUT	INPUT
$\overline{CU9}$	INPUT	INPUT	INPUT		
$\overline{CRB}$	OUTPUT	OUTPUT		INPUT	
$\overline{CDB}$			OUTPUT		INPUT

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Figure 6. Cascade Signal Input/Output Definition

Multi-ORP Cascade Example

Figure 7 shows an example of a multi-ORP cascade using four ORPs supporting processing of an image block up to 128 pixels x 128 pixels.

Write Mode

$\overline{CRO}$ must be connected to $\overline{CLI}$ of the right-side ORP. Each right-most ORP must have its $\overline{CRO}$ fed back to the $\overline{CLI}$ of the corresponding left-most ORP. The $\overline{CRB}$ in each ORP must be connected to the $\overline{CLI}$ at the left-most ORP. Because the $\overline{CRB}$ pin is an open-drain output, a pull-up resistor must be connected to this pin. The FC bit in the first ORP will be set to 1 by the CPU. The other ORPs' FC bits must be 0. After (XAR + 1) words have been loaded, the $\overline{CRO}$ (ORP #1) will be driven LOW and the second ORP's FC bit will then be set to 1. This process is repeated until the entire memory area is loaded with data. When the entire font section assigned to an ORP is loaded, $\overline{CLI}$ is connected internally to $\overline{CD9}$. When the final data for the second ORP is loaded, $\overline{CLI}$ of the first ORP will be driven LOW; thus $\overline{CU9}$ of the third ORP will be driven LOW and its FC bit will be set to 1. This propagation of the FC bit will continue between the next two ORPs.

If the size of the image block is smaller than the cascade configuration — for instance 64 x 128 (in a 128 x 128 system) — the second and fourth ORPs will have to be programmed to the desired state. The EN bit of each should be set to 0. Under this condition $\overline{CLI}$ will be internally connected to $\overline{CRB}$ for the second and fourth ORP, preventing their FC bits from being set.

0-Degree Read Operation

In the 0-degree read operation, the FC bit propagation is the same as that of the write operation.

90-Degree Read Operation

During a 90-degree read operation, the $\overline{CLO}$ and $\overline{CRI}$ are used to propagate the FC bit in the vertical direction. These signals correspond to $\overline{CD9}$ and $\overline{CU9}$ in the write operation. $\overline{CDB}$ is now defined as an output. In the horizontal direction, $\overline{CD9}$ is driven LOW after all (XAR + 1) words are read out from the chip. $\overline{CD9}$ is connected to the lower ORP's $\overline{CU9}$. The lowest ORP's $\overline{CD9}$ must be fed back to the $\overline{CU9}$ at the top ORP through the open-drain buffer. $\overline{CDB}$ in each ORP must be connected together

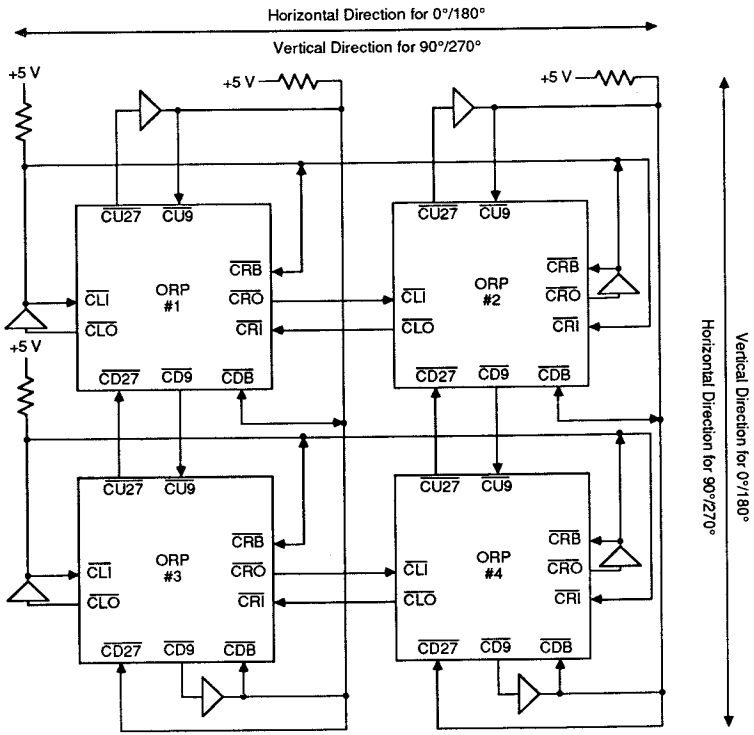

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Figure 7. Cascade Connection

to $\overline{CU9}$ at the top ORP. $\overline{CDB}$ is an open-drain output and needs a pull-up resistor. The FC bit in the second ORP will be set to 1 by the CPU. The other ORP's FC bit must be set to 0. The read operation will begin with ORP #2. The horizontal direction FC bit propagation will be done between the second and fourth ORP. When the entire font section assigned to the ORP is read out, $\overline{CU9}$ is internally connected to $\overline{CLO}$. When the final data in ORP #4 is read out, $\overline{CU9}$ of the second ORP will be driven LOW, causing ORP #2 to drive $\overline{CLO}$ LOW, resulting in the FC bit of the first ORP to be set to 1. Then the horizontal direction FC bit propagation will continue between the first and the third ORPs.

180-Degree Read Operation

In a 180-degree read operation, $\overline{CU27}$ and $\overline{CD27}$ are used to propagate the FC bit in the vertical direction. $\overline{CRB}$ is defined as an input. $\overline{CRI}$, $\overline{CLO}$, and $\overline{CRB}$ are used to propagate the FC bit in the horizontal direction. In this operation, the bottom-right ORP (ORP #4) needs to be programmed with the FC bit equal to 1. The other ORP's FC bit must be set to 0. The horizontal direction FC bit propagation will be done by $\overline{CLO}$ and $\overline{CRI}$ according to the XAR bits. The left-most ORP (ORP #3) must have $\overline{CLO}$ fed back to ORP #4's $\overline{CRI}$ and $\overline{CRB}$ through an open-drain buffer. The $\overline{CRB}$ input is effective only when that chip is in disable state (EN = 0). The ORP whose EN bit is set to 1 uses the $\overline{CRI}$ as a cascade input.

When the entire font section assigned to the ORP is read out, the $\overline{CRI}$ will be connected to $\overline{CU27}$ internally. When final data is read from ORP #3, ORP #4 will drive $\overline{CU27}$ LOW according to $\overline{CRI}$. The FC bit is then transferred to ORP #2. Then the horizontal direction FC bit propagation will be done between ORP #2 and ORP #1.

If the Y size of the image block is smaller than the cascade configuration, ORPs #3 and #4 will have to be programmed to a disabled state. The EN bit of these ORPs has to be set to 0. Under this condition, $\overline{CRB}$ will be connected directly to $\overline{CLO}$ internally.

270-Degree Read Operation

During a 270-degree read operation, the $\overline{CRO}$ and $\overline{CLI}$ pins are used to propagate the FC bit in the vertical direction. $\overline{CDB}$ is defined as an input. $\overline{CU27}$, $\overline{CD27}$, and $\overline{CDB}$ are used to propagate the FC bit in the horizontal direction. In this operation, the bottom-left ORP (ORP #3) needs to be programmed with the FC bit equal to 1. The other ORP's FC bit must be set to 0. The horizontal direction FC bit propagation will be done by $\overline{CU27}$ according to the XAR bits. The top ORP (ORP #1) must have $\overline{CU27}$ fed back to ORP #3's $\overline{CD27}$ and $\overline{CDB}$ through an open-drain buffer. The $\overline{CDB}$ input is effective only when that chip is in the disable state (EN = 0). The ORP whose EN bit is set to 1 uses the $\overline{CD27}$ pin as a cascade input.

When the entire font section assigned to the ORP is read out, the $\overline{CD27}$ input will be connected to the $\overline{CRO}$ output internally. When the final data is read from ORP #1, ORP #3 will drive $\overline{CRO}$ LOW according to $\overline{CD27}$. The FC bit is then transferred to ORP #4. The horizontal direction FC bit propagation will then be done between ORP #4 and ORP #2.

If the size of the image block is smaller than the cascade configuration, ORPs #3 and #4 will have to be programmed to a disabled state. The EN of these ORPs has to be set to 0. Under this condition, $\overline{CDB}$ will be connected directly to $\overline{CU27}$ internally.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150°C
Maximum V_{CC} Relative to V_{SS} ..... –0.3 to +7.0 V
DC Voltage Applied to Any
Pin Relative to V_{SS} ..... –0.5 to V_{CC} + 0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		+0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA	2.4		V
I_{OZ}	Output Leakage Current	.45 < V_{OUT} <		±10	µA
I_I	Input Current	0 < V_{IN} <		±10	µA
I_{CC}	Power Supply Current			50	mA

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	f = 1 MHz		15	pF
$C_{I/O}$	Bidirectional Pin Capacitance	f = 1 MHz		20	pF
C_{OUT}	Output Pin Capacitance	f = 1 MHz		20	pF
C_L	Output Load Capacitance			100	pF

* Parameters are not tested.

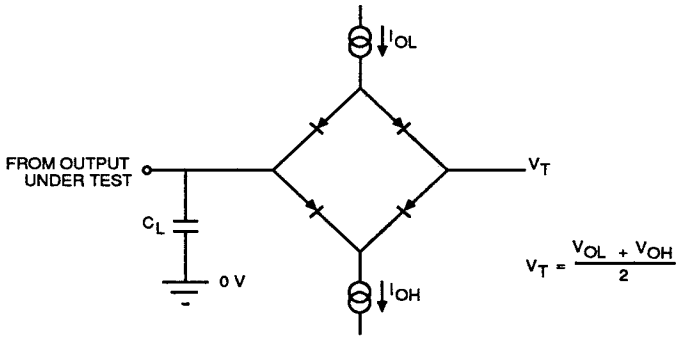
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
HOST INTERFACE TIMING					
1	t_{ARC}	$\overline{RD}/\overline{WR}$ ↑ to ST ↑, Access Recovery Time	30		ns
2	t_{STW}	ST ↑ to ST ↓, ST Pulse Width	30		ns
3	t_{GSFBS}	$\overline{GS}/\overline{FB}$ ↓ to $\overline{RD}/\overline{WR}$ ↓, $\overline{GS}/\overline{FB}$ Setup Time	10		ns
4	t_{GSFBH}	$\overline{RD}/\overline{WR}$ ↑ to $\overline{GS}/\overline{FB}$ ↑, $\overline{GS}/\overline{FB}$ Hold Time	0		ns
5	t_{CSS}	$\overline{CS}$ ↓ to $\overline{RD}/\overline{WR}$ ↓, $\overline{CS}$ Setup Time	10		ns
6	t_{CSH}	$\overline{RD}/\overline{WR}$ ↑ to $\overline{CS}$ ↑, $\overline{CS}$ Hold Time	20		ns
7	t_{WACCS}	ST ↓ to $\overline{WR}$ ↓, Write Access Time	40		ns
7A	t_{FWACCS}	ST ↓ to $\overline{RD}$ ↓, Fly-By Write Access Time	40		ns
8	t_{WDIS}	Data-In Setup Time to $\overline{WR}$ ↑	20		ns
8A	t_{FWDIS}	Fly-By Data-In Setup Time to $\overline{RD}$ ↑	20		ns
9	t_{WDIH}	Data-In Hold Time After $\overline{WR}$ ↑	10		ns
9A	t_{FWDIH}	Fly-By Data-In Hold Time After $\overline{RD}$ ↑	10		ns
10	t_{RACCS}	ST ↓ to $\overline{RD}$ ↓, Read Access Time	40		ns
10A	t_{FRACCS}	ST ↓ to $\overline{WR}$ ↓, Fly-By Read Access Time	40		ns
11	t_{RDOV}	$\overline{RD}$ ↓ to Data-Out Valid Delay		35	ns
11A	t_{FRDOV}	$\overline{WR}$ ↓ to Fly-By Data-Out Valid Delay		35	ns
12	t_{RDOZ}	$\overline{RD}$ ↑ to Data-Out Invalid Delay	0	30	ns
12A	t_{FRDOZ}	$\overline{WR}$ ↑ to Fly-By Data-Out Invalid Delay	0	30	ns
13	t_{RD}	$\overline{RD}$ Signal Pulse Width	50		ns
14	t_{WR}	$\overline{WR}$ Signal Pulse Width	50		ns
23	t_{RESET}	$\overline{RESET}$ Pulse Width	200		ns
ORP CASCADE INTERFACE TIMING					
15	t_{CAV}	$\overline{RD}/\overline{WR}$ ↓ to $\overline{CLO}/\overline{CRO}/\overline{CU27}/\overline{CD9}$ ↓ Cascade Output Valid Delay		55	ns
16	t_{CAIV}	ST ↓ to $\overline{CLO}/\overline{CRO}/\overline{CU27}/\overline{CD9}$ ↑ Cascade Output Invalid Delay		30	ns
17	t_{SCA}	$\overline{CLI}/\overline{CRI}/\overline{CU9}/\overline{CD27}/\overline{CDB}/\overline{CRB}$ ↓ to ST ↓ Cascade Input Setup Time	10		ns
18	t_{HCA}	ST ↓ to $\overline{CLI}/\overline{CRI}/\overline{CU9}/\overline{CD27}/\overline{CDB}/\overline{CRB}$ ↑ Cascade Input Hold Time	10		ns

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
ORP CASCADE INTERFACE TIMING (Cont'd.)					
19	t_{BCAL}	$\overline{CRB}\downarrow$ to $\overline{CLO}\downarrow$ (180° Read), $\overline{CDB}\downarrow$ to $\overline{CU27}\downarrow$ (270° Read)		25	ns
19A	t_{ODBCAL}	$\overline{CU9}\downarrow$ to $\overline{CDB}\downarrow$ (90° Read), $\overline{CLI}\downarrow$ to $\overline{CRB}\downarrow$ (Write, 0° Read) O.D. ORP Disabled Bypass Cascade Valid De		25	ns
20	t_{BCAH}	$\overline{CRB}\uparrow$ to $\overline{CLI}\uparrow$ (180° Read), $\overline{CDB}\uparrow$ to $\overline{CU27}\uparrow$ (270° R ORP Disabled Bypass		25	ns
20A	t_{ODBCAH}	$\overline{CU9}\uparrow$ to $\overline{C}$ $\overline{CL}$ to $\overline{CR}$ O.D.		25	ns
21	t_{FLBCAL}	$\overline{CLI}\downarrow$ to $\overline{CD9}\downarrow$, $\overline{CU9}\downarrow$ to $\overline{CLO}\downarrow$, $\overline{CRI}\downarrow$ to $\overline{CU27}\downarrow$, $\overline{CD27}\downarrow$ to $\overline{CRO}\downarrow$ ORP Font Section Complete Bypass Cascade Valid Delay		25	ns
22	t_{FLBCAH}	$\overline{CLI}\uparrow$ to $\overline{CD9}\uparrow$, $\overline{CU9}\uparrow$ to $\overline{CLO}\uparrow$, $\overline{CRI}\uparrow$ to $\overline{CU27}\uparrow$, $\overline{CD27}\uparrow$ to $\overline{CRO}\uparrow$ ORP Font Section Complete Bypass Cascade Invalid Delay		25	ns

5

SWITCHING TEST CIRCUIT
(Standard Load)



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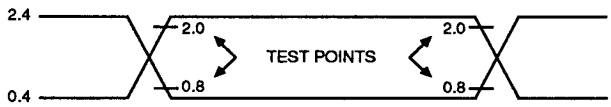
SWITCHING TEST WAVEFORM
(Input)



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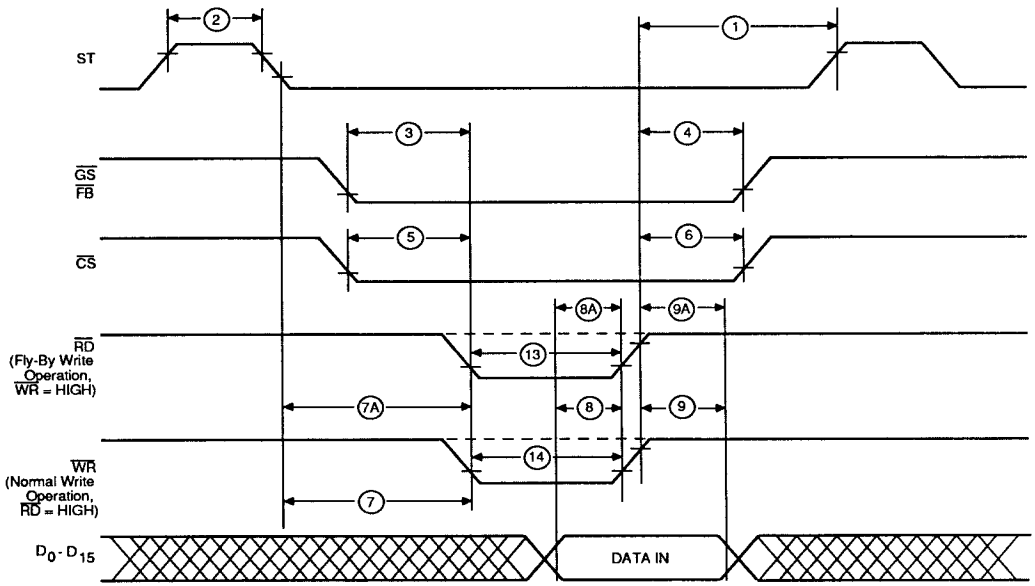
SWITCHING WAVEFORMS
KEY TO SWITCHING WAVEFORMS

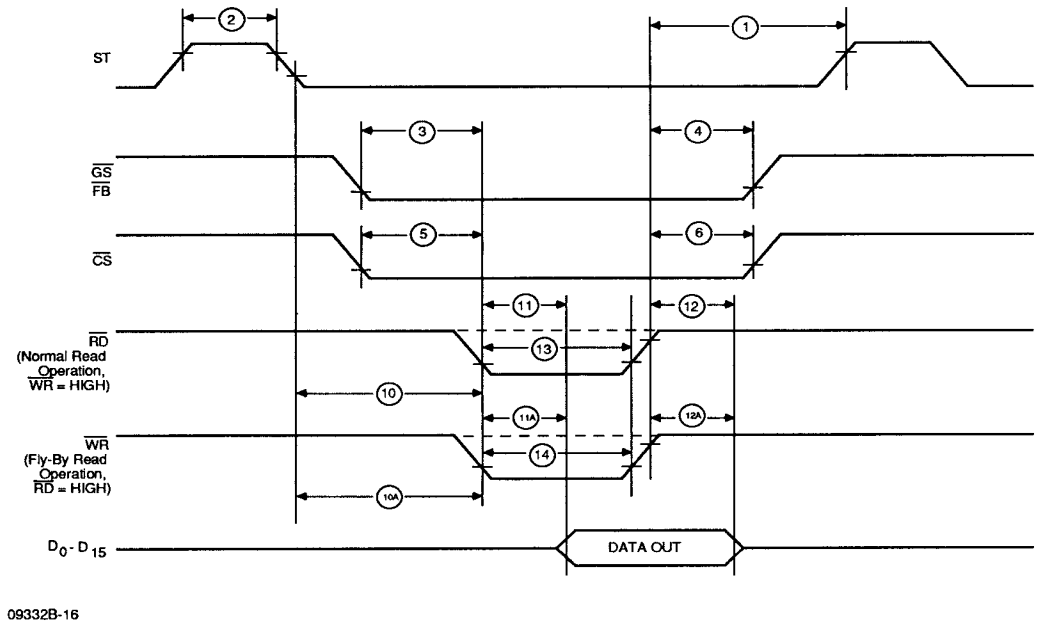
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟍⟋⟍	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010

SWITCHING WAVEFORMS (Cont'd.)



ORP Write Operation Timing



ORP Read Operation Timing

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