JUL 29 1993

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Q2220

DIRECT DIGITAL SYNTHESIZER

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March 1993
DL80-3749-1B

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QUALCOMM Incorporated, VLSI Products
10555 Sorrento Valley Road, San Diego, CA 92121-1617, USA, Telephone: (619) 597-5005, Fax: (619) 452-9096

FEATURES

- Low-Cost, High Resolution 50 MHz Direct Digital Synthesizer
- Simple-to-Use Parallel Frequency Control Interface
- Frequency Resolution: < 3.0 Hz with System Clock Frequency = 50 MHz
- Compact 44-pin PLCC Package (44-pin CLDCC for MIL version)
- Spurious Signal Levels: < -60 dBc
- Selectable Offset Binary or Two's Complement Output Format
- Low-power CMOS technology: 250 mW (max) at 50 MHz System Clock Frequency
- 50 MHz Hop and Sweep Rate
- Throughput Delay: 5 Clock Cycles

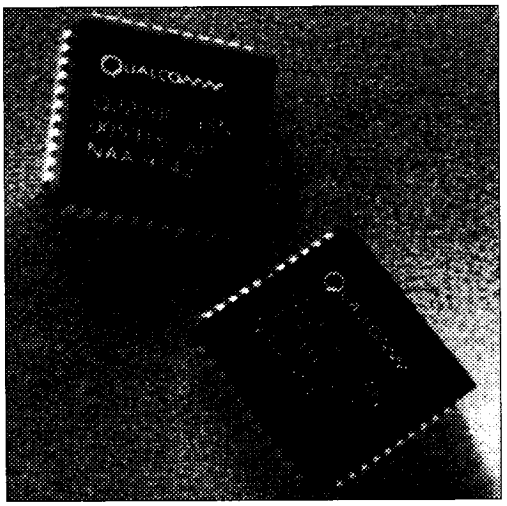
APPLICATIONS

- Portable Communications Terminals
- Radar and Sonar Systems
- Programmable Frequency Synthesizers
- Baseband Transmitters and Receivers
- Frequency Hopping Radios
- Digital Signal Processors

INTRODUCTION

The QUALCOMM Q2220 Direct Digital Synthesizer (DDS) is ideal for cost-sensitive systems that require the special advantages of DDS technology, including high resolution, good spectral purity, and fast switching times. The Q2220 is simple to program using parallel frequency control signals. High-volume applications, which previously found DDS technology to be too expensive or complex, now can take advantage of the small package size, simple interface, high-signal quality, fast switching capability, and low power requirements of the Q2220.

The Q2220 generates high-resolution, digitized sine waveform signals using phase accumulation combined with



on-chip sine lookup techniques. The Q2220 is a low-cost, low-power solution for DDS systems requiring frequency synthesis with fast switching times. Using a reference clock of 50 MHz, the Q2220 can synthesize frequencies from DC to 20 MHz with a resolution of approximately 3.0 Hz. The on-chip, precision sine computation function provides a digitized ten-bit value for the sine waveform output with spurious levels below -60 dBc.

GENERAL DESCRIPTION

The Q2220 is a complete DDS function (Figure 1) that includes the following:

- Parallel-Loaded Frequency Control Register
- 24-Bit High-Speed Phase Accumulator
- Sine Computation Function

THEORY OF OPERATION

A Direct Digital Synthesizer operates on the principle that a digitized waveform of a given frequency can be generated by accumulating phase changes at a higher frequency. Sampling theory requires that the generated frequency be no more than one-half of the clock frequency (Nyquist rate). In practical circuits, the output frequency is limited to about 40% of the

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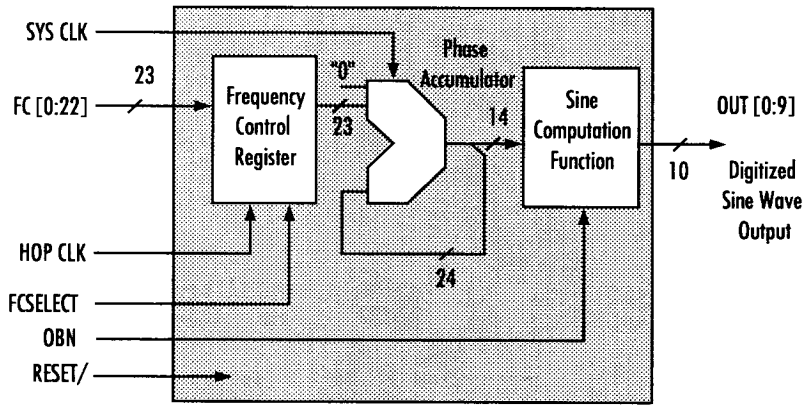
Figure 1. Q2220 Block Diagram



sampling frequency .

For example, the phase accumulation of a generated sine wave whose frequency is equal to 1/8th of the clock frequency can be illustrated using a circle (Figure 2). The circle shows the phase accumulation process of $\pi/4$ at each clock cycle. The letters on the circle represent the phase value at a given time, and the sine wave shows the corresponding amplitude representation. The phase-to-amplitude conversion occurs in the on-chip sine computation function. Note that the phase increment added during each clock period is $\pi/4$ radians, which equals 1/8th of a complete cycle (i.e., 2π).

General Q2220 Operation

The phase value stored in the Frequency Control (FC) Register (Figure 1) is added to the value in the Phase Accumulator once during each period of the system clock. The resulting phase value (from 0 to 2π) is then applied to the on-chip sine lookup once during each clock cycle. The lookup converts the phase information to its corresponding sine amplitude (Figure 2); then, the resulting 10-bit digital word is output from the Q2220 DDS device.

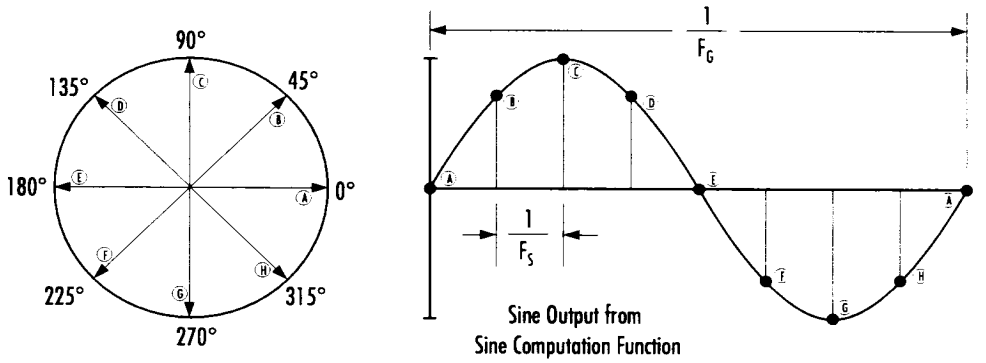
Computing the 23-Bit Frequency Control Value

To output a particular frequency, the associated phase increment value must be loaded into the FC Register. The generated frequency (F_G) and system clock frequency (F_S) are related to the phase increment value (Δf) by the following equation:

$$F_G = \frac{F_S \bullet \Delta\Phi}{2^{24}} \quad (1)$$

For example, given a system clock of 50 MHz (F_S = 50 MHz) and a desired

Figure 2. Sampled Sine Wave



F_G = Generated Output Frequency
F_S = SYS CLK Frequency

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generated frequency of 12.5 MHz (F_G = 12.5 MHz), the previous equation becomes the following:

12.5 MHz = (50 MHz • Δf)/2^{24}

Δf = (12.5 MHz)(2^{24})/50 MHz

= 4,194,304

= 100 0000 0000 0000 0000 0000_2

Using Equation 1, frequency resolution can be generated in exact Hz steps by properly setting the system clock frequency. For example, using 2^{25} Hz (33,554,432 Hz) as the system clock frequency, an exact decimal frequency (in Hz) can be generated.

Given: $F_S = 2^{25}$ Hz = 33,554,432 Hz

Frequency Resolution = 2^{25} Hz/2^{24}

= 2.0 Hz

Therefore, when $F_S = 2^{25}$ Hz,

then F_G = 2 Hz • Δf.

If we choose Δf = 2^0 (0...01 binary),

then F_G = 2.0 Hz.

If we choose Δf = 2^1 (0...010 binary),

then F_G = 4.0 Hz.

If we choose Δf = 2^2 (0...0100 binary),

then F_G = 8.0 Hz.

Frequency Resolution

Any frequency can be generated by programming the phase change within the bit resolution of the Phase Accumulator. The frequency resolution is determined by the following equation:

$$\text{Frequency Resolution} = F_S/2^{24} \quad (2)$$

where F_S = frequency of the system clock.

For example, when F_S = 50 MHz, the following applies:

Frequency Resolution

= 50 MHz/ 2^{24}

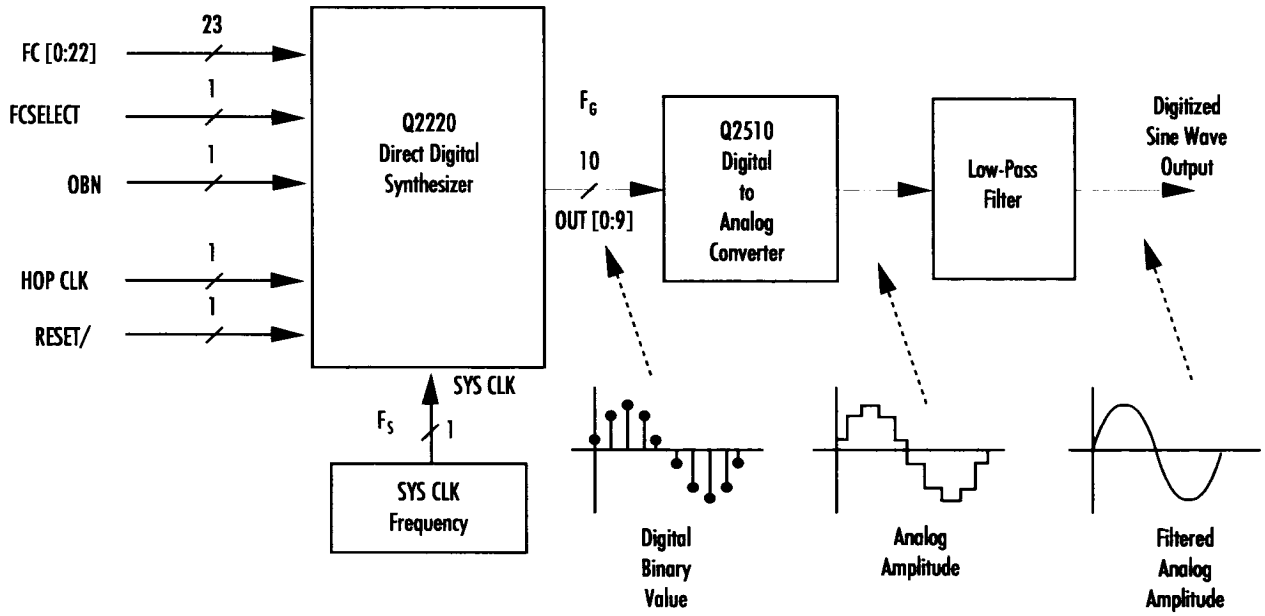
= 2.98 Hz

If F_S = 10 MHz, the frequency resolution = 0.59 Hz.

Typical DDS Application

Figure 3 illustrates a typical synthesizer application of the Q2220 DDS and the Q2510 DAC. This figure shows all of the external functions required for a simple, yet powerful synthesizer system. The digitized sine wave output from the DDS

Figure 3. Typical Q2220 DDS Application



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device is converted to an analog waveform by a Q2510 Digital-to-Analog Converter (DAC). The output of the DAC has the desired sine wave as a major component but also includes the higher frequency image components due to the conversion of a sampled waveform. A Low Pass Filter (LPF) is used to reduce these image signals to the desired level. The pass band of the LPF must be equal to or less than half the system clock frequency. Typically, the pass band of the LPF is restricted to about 40% of F_S.

INTERNAL ARCHITECTURE

The Q2220 device includes a parallel interface FC Register, a Phase Accumulator, and a Sine Computation Function. These components are detailed in the following paragraphs.

Parallel-Loaded Frequency Control Register

The parallel frequency control interface simplifies control of the Q2220 output frequency. The 23 bits of the input frequency control value are clocked into the device simultaneously. Using this interface, frequency changes can be made as fast as the system clock frequency.

FC Register Activation

The 23-bit FC Register is loaded asynchronously or synchronously with the system clock and synchronously activated. The mode of the load selection is determined by the setting of the FCSELECT signal (Figure 4).

If FCSELECT is set "high", then inputs FC0 through FC22 are clocked into the FC Register asynchronously by the positive transition of the HOP CLK signal. The HOP CLK signal is internally resynchronized to the SYS CLK signal. In this mode, the FC0-FC22 values must be valid for a minimum of two SYS CLK cycles. (See "Technical Specifications, Interface Timing", page 12.)

If FCSELECT is set "low", then FC0 through FC22 are clocked into the FC Register on the positive transition of the SYS CLK signal.

Phase Accumulator

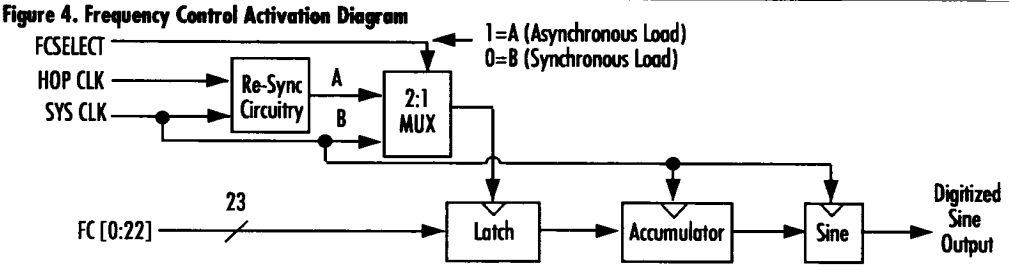
The Q2220 has a 24-bit Phase Accumulator. The most significant bit (MSB) of the 24-bit input to the Phase Accumulator is internally set to "0"; therefore, the phase increment input to the device is 23 bits wide, corresponding to the least significant 23 bits of a 24-bit input. This allows the Q2220 to output frequencies as high as $F_S/2$.

The Phase Accumulator takes in the value from the FC Register and adds that value to its previous output. The resulting sum is then output from the Phase Accumulator. At the output of the Phase Accumulator, the contents are input to the Sine Computation Function and fed back to the Phase Accumulator for the next cycle.

Sine Computation Function

From the Phase Accumulator, 14 bits of phase information are translated to a

Figure 4. Frequency Control Activation Diagram



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corresponding sine amplitude via the Sine Computation Function. The resulting digitized sine amplitude value is represented by 10 bits. When the OBN pin is set "low", this 10-bit output is formatted using two's complement notation. When the OBN pin is set "high", this 10-bit output is formatted in offset binary notation (Table 2).

Input/Output Signals

The following are the pin configurations of the Q2220 DDS package (Figure 5) and a summary of the input/output signal pin assignments (Table 1):

FC0-FC22 (Input)

FC0-FC22 represents the 23-bit FC input. FC0 (pin 1) is the least significant bit (LSB), and FC22 (pin 21) is the MSB.

The value in the FC Register is 23 bits wide. This is then input to the 24-bit Phase Accumulator. The MSB of the Phase Accumulator input is internally set to "0".

RESET/ (Input)

RESET/ represents an active low asynchronous clear function. This sets the FC Register, Phase Accumulator, and Sine Computation Function to "0" when low. When unused, connect the RESET/ signal to a "high" setting.

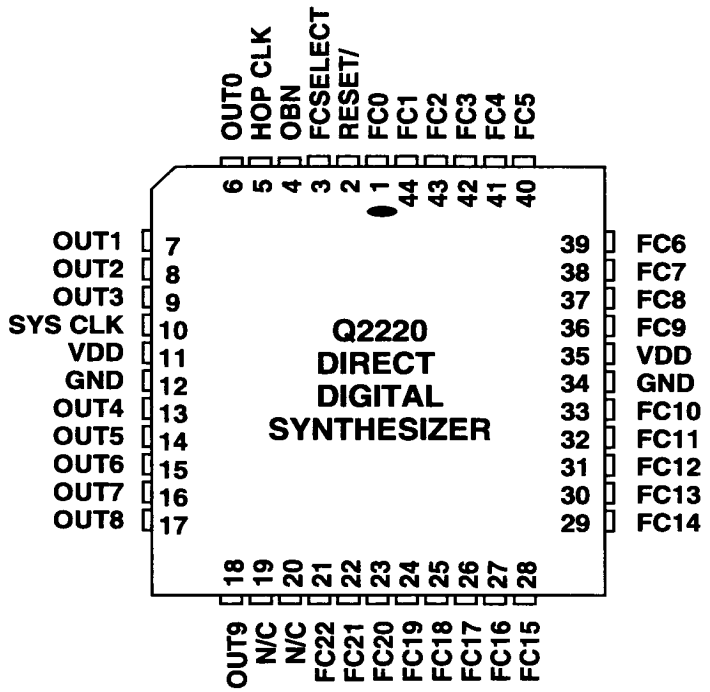
When the RESET/ function is activated, the FC Register, Phase Accumulator, and Sine Computation Function are set to "0". The output will remain at the reset level until the signal is disabled. When the RESET/ signal is disabled (i.e., set "high"), the FC value will change on the next HOP CLK or SYS CLK (depending on the setting of FCSELECT), and the accumulation process will begin again.

FCSELECT (Input)

When FCSELECT is set "high", the FC values are latched and activated into the FC Register by the rising edge of the internally synchronized HOP CLK signal (Figure 4).

The FC Register's contents also can be input synchronously with the system clock signal (SYS CLK). This mode is selected by setting FCSELECT to "low". In this case, the value for the FC value is activated by the rising edge of the SYS CLK signal.

Figure 5. Q2220 Package Pin Configuration



OBN (Input)

OBN represents the output format selection. If OBN is set "high", then the output format is offset binary. If OBN is set "low", then the output format is two's complement.

HOP CLK (Input)

When FCSELECT is set "high", the HOP CLK signal loads the FC Register

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with the value on the FC0 - FC22 inputs. The positive transition of the HOP CLK signal is internally synchronized to the SYS CLK signal and clocks FC0 - FC22 values to the FC Register. (Refer to the asynchronous load mode timing diagram under "Interface Timing", page 14.) The HOP CLK period (rising edge to rising edge) must be greater than or equal to three SYS CLK periods, and the HOP CLK signal can be asynchronous to the SYS CLK signal.

Table 1. Q2220 Input/Output Signals

PIN #	NAME	I/O TYPE	DESCRIPTION
1	FC0	INPUT	Frequency Control data bit 0 (LSB)
2	RESET/	INPUT	Clears FC Register, Phase Accumulator, and Sine Function when low
3	FCSELECT	INPUT	Selects which clock activates the FC value (0= SYS CLK , 1= HOP CLK)
4	OBN	INPUT	Output format select (0=Two's complement, 1=Offset Binary)
5	HOP CLK	INPUT	Rising edge clocks in the data bits when FCSELECT=1
6	OUT0	OUTPUT	Data Output Bit 0 (LSB)
7	OUT1	OUTPUT	Data Output Bit 1
8	OUT2	OUTPUT	Data Output Bit 2
9	OUT3	OUTPUT	Data Output Bit 3
10	SYS CLK	INPUT	System Clock
11	V_{DD}	INPUT	+5V power supply connection
12	GND	INPUT	Ground
13	OUT4	OUTPUT	Data Output Bit 4
14	OUT5	OUTPUT	Data Output Bit 5
15	OUT6	OUTPUT	Data Output Bit 6
16	OUT7	OUTPUT	Data Output Bit 7
17	OUT8	OUTPUT	Data Output Bit 8
18	OUT9	OUTPUT	Data Output Bit 9 (MSB)
19	N/C	N/C	Unused pin, do not connect
20	N/C	N/C	Unused pin, do not connect
21	FC22	INPUT	Frequency Control Data Input Bit 22 (MSB)
22	FC21	INPUT	Frequency Control Data Input Bit 21
23	FC20	INPUT	Frequency Control Data Input Bit 20
24	FC19	INPUT	Frequency Control Data Input Bit 19
25	FC18	INPUT	Frequency Control Data Input Bit 18
26	FC17	INPUT	Frequency Control Data Input Bit 17
27	FC16	INPUT	Frequency Control Data Input Bit 16
28	FC15	INPUT	Frequency Control Data Input Bit 15
29	FC14	INPUT	Frequency Control Data Input Bit 14
30	FC13	INPUT	Frequency Control Data Input Bit 13
31	FC12	INPUT	Frequency Control Data Input Bit 12
32	FC11	INPUT	Frequency Control Data Input Bit 11
33	FC10	INPUT	Frequency Control Data Input Bit 10
34	GND	INPUT	Ground
35	V_{DD}	INPUT	+5V power supply connection
36	FC9	INPUT	Frequency Control Data Input Bit 9
37	FC8	INPUT	Frequency Control Data Input Bit 8
38	FC7	INPUT	Frequency Control Data Input Bit 7
39	FC6	INPUT	Frequency Control Data Input Bit 6
40	FC5	INPUT	Frequency Control Data Input Bit 5
41	FC4	INPUT	Frequency Control Data Input Bit 4
42	FC3	INPUT	Frequency Control Data Input Bit 3
43	FC2	INPUT	Frequency Control Data Input Bit 2
44	FC1	INPUT	Frequency Control Data Input Bit 1

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If FCSELECT is set to "0", then HOP CLK has no function and should be set "low".

OUT0-OUT9 (Input)

OUT0-OUT9 represent digitized sine wave outputs encoded in offset binary or two's complement format, depending on the setting of OBN. One sample is generated during each period of the SYS CLK. OUT9 (pin 18) is the MSB.

SYS CLK (Input)

SYS CLK provides the fundamental sampling clock frequency of the synthesized sine waveform. Internal operations of the Phase Accumulator and FC Register are synchronized to this clock signal. The outputs change on the positive transitions of the SYS CLK.

V_{DD} (Input)

V_{DD} provides power to all Q2220 circuitry.

GND (Input)

GND provides electrical ground reference for signal and power inputs.

NO CONNECT

No electrical connections must be made to pins labelled NO CONNECT.

THROUGHPUT DELAY

When FCSELECT is set "low", the output frequency of the Q2220 device will reflect the change in frequency loaded by the SYS CLK signal in 5 SYS CLK cycles.

If FCSELECT is set "high", then the output frequency will change in 7 SYS CLK cycles measured from the first rising edge of SYS CLK after the rising edge of HOP CLK, as long as the HOP CLK signal follows the setup and hold times given on page 14.

PROGRAMMING THE Q2220 DDS

The Q2220 DDS outputs a digitized sine wave at a fixed frequency ranging from essentially DC to one-half the frequency of SYS CLK. Practical limitations on anti-alias filtering will limit the range of frequencies to an approximate maximum of 40% of the SYS CLK frequency.

Table 2. OUT [0:9] Output Formats

OUTPUT VALUE	OBN = 1 (OFFSET BINARY) MSB LSB	OBN = 0 (TWO'S COMPLEMENT) MSB LSB
Maximum Value	1111111111	0111111111
...	1111111110	0111111110
...	...	...
...	...	...
Half Maximum +1	1000000000	0000000000
Half Maximum -1	0111111111	1111111111
...	...	...
...	...	...
...	0000000001	1000000001
Minimum Value	0000000000	1000000000

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Programming Example

The following is an example of a step-by-step procedure to initialize the Q2220 to output a specific frequency. This procedure includes all necessary conditions to program the Q2220.

1. Establish the values for FS and the desired F_G. Using these values, determine the number to be loaded into the FC Register (Equation 1). This calculated value is loaded into the FC0-FC22 pins according to the timing specifications on page 12. (The activation of this value will depend on the setting of the FCSELECT pin.) The LSB of the 23-bit value is loaded into pin 1, and the MSB is loaded into pin 21.

2. Determine whether output format will be two's complement or offset binary. For offset binary format, set OBN (pin 4) "high". For two's complement output, set OBN "low".

3. Determine if frequency control data is to be loaded and activated in the Q2220 using the SYS CLK (i.e., synchronous) or the HOP CLK (i.e., asynchronous) signal. (Refer to "Internal Architecture, FC Register Activation", page 6.) If the data is to be loaded synchronously, then set FCSELECT (pin 3) "low". (Refer to "Technical Specifications, Interface Timing", page 12.) If the data is asynchronously loaded and synchronously activated, then set FCSELECT "high". When FCSELECT is set "high", the HOP CLK signal is the asynchronous signal that loads the data. (Refer to "Technical Specifications, Interface Timing", page 12.)

Specific Example

Following is a step-by-step procedure for outputting a specific frequency. In the subsequent example, the following values apply: F_S = 50 MHz; F_G =12.5 MHz; offset binary output format; and asynchronous loading of the FC Register.

1. Substitute these values in equation number 1:

   $F_G = (F_S \bullet \Delta f)/2^{24}$ (1)

   $12.5\ MHz = (50\ MHz \bullet \Delta f)/2^{24}$

   $\Delta f = 4{,}194{,}304$

   $= 0100\ 0000\ 0000\ 0000\ 0000\ 0000_2$

   (MSB) (LSB)

   Load this binary value into the FC0-FC22 pins (1, 44, 43, 42, 41, 40, 39, 38, 37, 36, 33, 32, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, and 21) according to timing specifications on page 12. FC22 (pin 21) is set "high", while the rest of the pins are set "low".

2. Set OBN (pin 4) "high" for offset binary output format.

3. To have the data asynchronously loaded, set FCSELECT "high". None of the settings will be loaded into the FC Registers until the assertion of a HOP CLK signal. This may be performed by pulsing the HOP CLK signal to an active high level, according to the timing requirements on page 12. This will cause the Q2220 device to begin synthesizing a sine wave at 12.5 MHz. Note that prior to loading the FC value, the output of the Q2220 will depend upon the value in the FC Register at power up, unless the RESET/ signal has been pulsed "low". In this case, the output will be all zeros until the FC Register is loaded.

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TECHNICAL SPECIFICATIONS

Absolute Maximum Ratings

		Q2220I-50		Q2220M-40L		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Storage Temperature	T_S	-40.0	+125.0	-65.0	+150.0	°C
Operating Temperature	T_A	-40.0	+85.0	-55.0	+125.0	°C
Supply Voltage	V_{DD}	-0.3	+7.0	-0.3	+7.0	V
Voltage on any Input Pin		-0.3	V_{DD}+0.3	-0.3	V_{DD}+0.3	V

NOTE: Stresses exceeding those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

		Q2220I-50N			Q2220M-40L			
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage	V_{DD}	4.5	5.0	5.5	4.5	5.0	5.5	V
High-level Input Voltage	V_{IH}	2.0		V_{DD}	2.0		V_{DD}	V
Low-level Input Voltage	V_{IL}	0		0.8	0		0.8	V
Input Current	I_{IN}			10.0			10.0	µA
High-level Output Voltage	V_{OH}	2.4	4.5		2.4	4.5		V
Low-level Output Voltage	V_{OL}		0.2	0.4		0.2	0.4	V
Quiescent Current	I_Q		100.0	200.0		100.0	200.0	µA
Input Capacitance	C_{IN}			5.0			5.0	pF
Power Dissipation @ maximum SYS CLK	P_D			250.0			200.0	mW

NOTE: To calculate the power dissipation associated with other clock frequencies, use the following equation: Power = (5.0 mW/MHz) • (Clock Frequency). To calculate the current, use the following equation: I = (1.0 mA/MHz) • (Clock Frequency).

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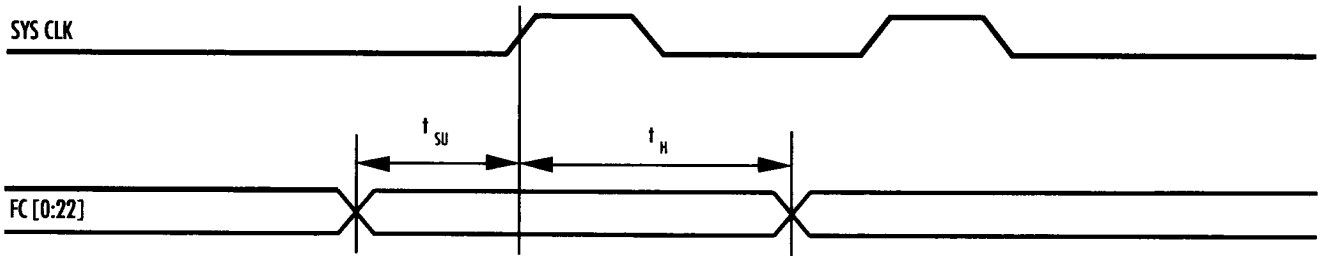
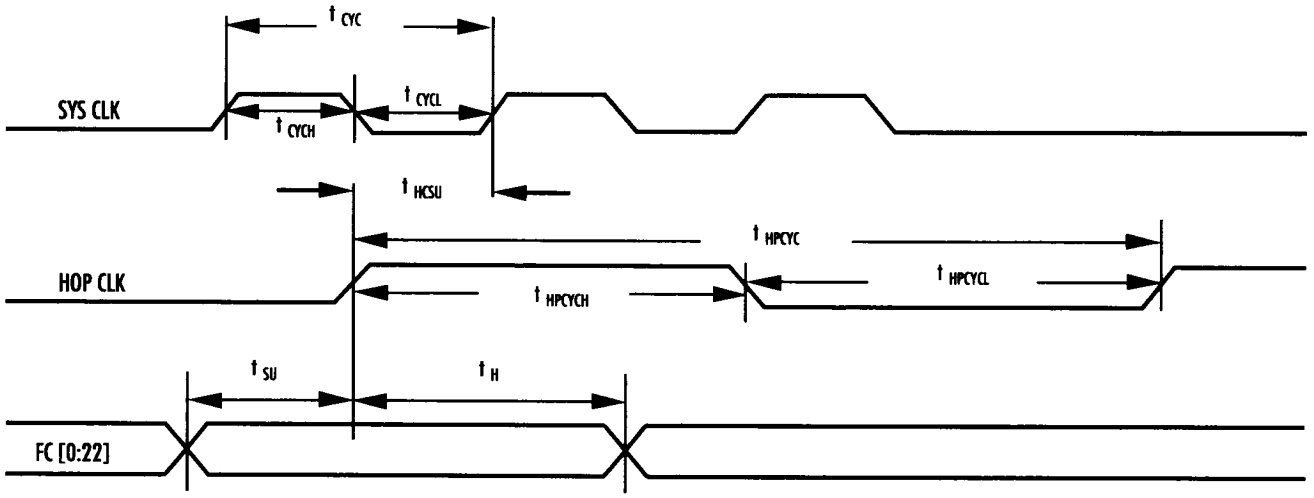
Interface Timing

FCSELECT = "0"



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{SU}	FC data setup to SYS CLK rising	2	-	ns
t_H	FC data hold after SYS CLK rising	4	-	ns

FCSELECT = "1" (Asynchronous Load Mode)



		Q2220I-50N		Q2220M-40L		
SYMBOL	DESCRIPTION	MIN	MAX	MIN	MAX	UNITS
t_{SU}	FC data setup to HOP CLK rising	2	-	2	-	ns
t_H	FC data hold after HOP CLK rising	t_{CYC} + 10	-	t_{CYC} + 10	-	ns
t_{CYC}	SYS CLK cycle period	20	-	25	-	ns
t_{CYCL}	SYS CLK low period	8	-	10	-	ns
t_{CYCH}	SYS CLK high period	8	-	10	-	ns
t_{HPCYC}	HOP CLK cycle period	3 • t_{CYC}	-	3 • t_{CYC}	-	ns
t_{HPCYCL}	HOP CLK cycle low period	10	-	10	-	ns
t_{HPCYCH}	HOP CLK cycle high period	10	-	10	-	ns
t_{HCSU}	HOP CLK rising to SYS CLK rising	5	-	5	-	ns

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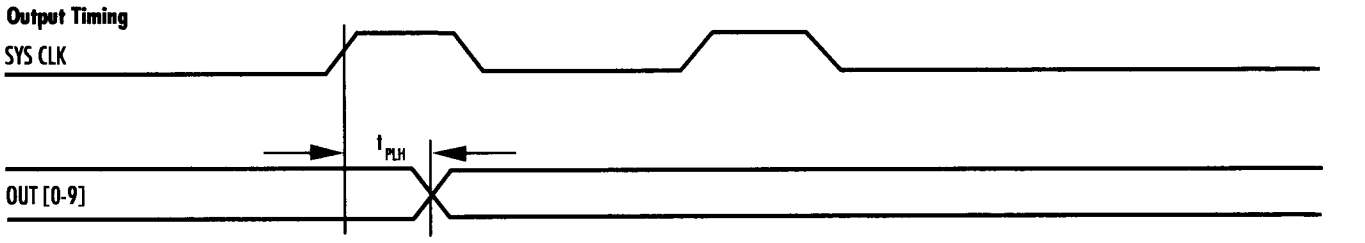
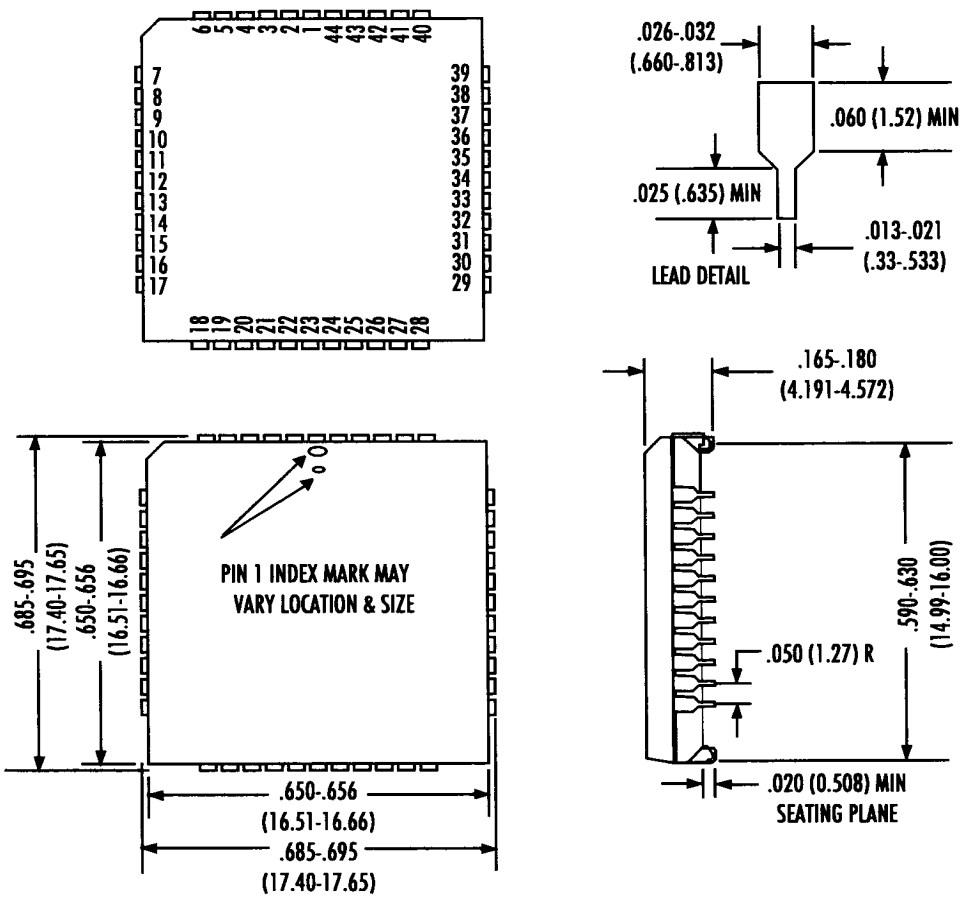


SYMBOL	DESCRIPTION	Q2220I-50N MIN	Q2220I-50N MAX	Q2220M-40L MIN	Q2220M-40L MAX	UNITS
t_{PLH}	SYS CLK rising to data bit output	3	17	3	21	ns

PLCC PACKAGING (Q2220I-50N)

The Q2220I-50N is packaged in a 44-pin plastic leaded chip carrier (PLCC) (Figure 6). Dimensions are given in inches (mm).

Figure 6. PLCC Packaging



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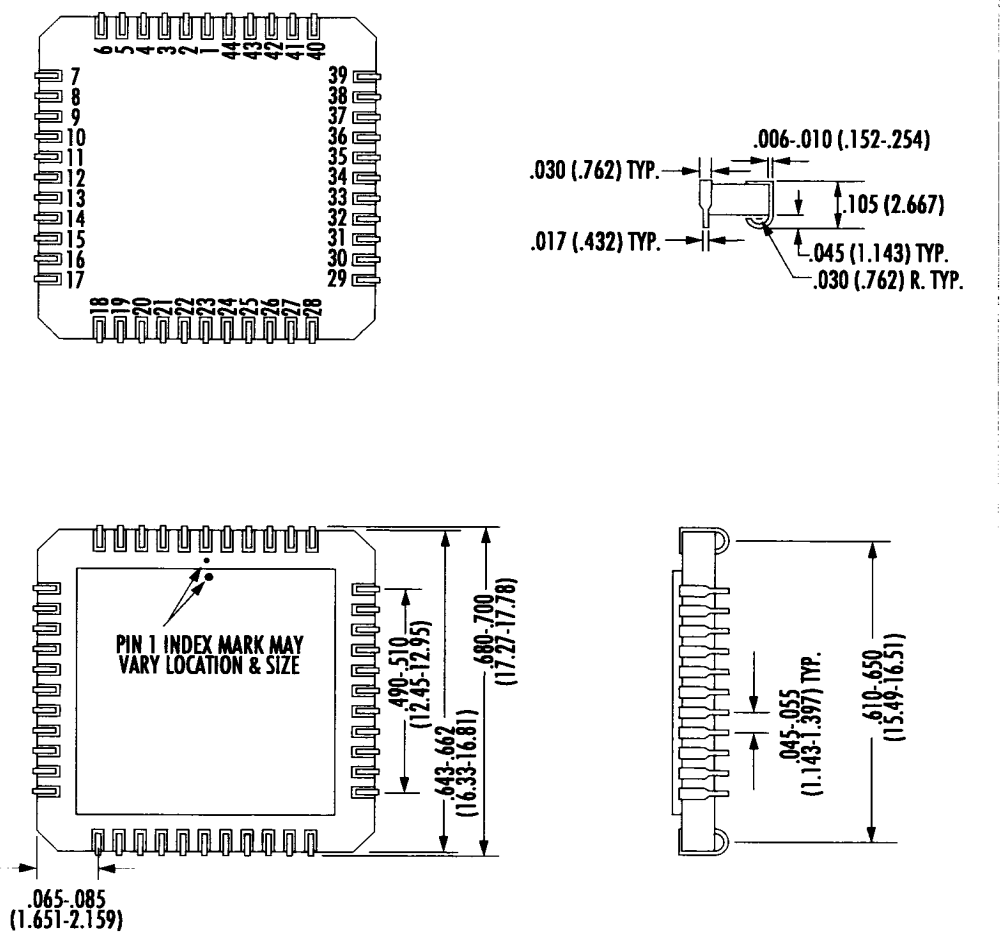
CLDCC PACKAGING (Q2220M-40L)

The Q2220M-40L is packaged in a 44-pin ceramic leaded chip carrier (CLDCC) (Figure 7). Dimensions are given in inches (mm).

Figure 7. CLDCC Packaging



Q0320 DDS SYNTHESIZER BOARD

The QUALCOMM Q0320 DDS Board (Figure 8) is a complete DDS system based upon the Q2220I-50N DDS. The Q0320 system includes a printed circuit card (3"x 3") with a Q2220I-50N coupled with a DAC and an anti-alias filter. This card also includes a 33.554 MHz clock source that provides an exact 2.0 Hz frequency resolution.

The Q0320 system is controlled through a DIL header or via manual dip switches. If desired, an external reference source can be input to the Q0320 system. Frequencies from DC to 14 MHz can be generated when using the on-board reference and anti-alias filter.

The Q0320 User's Guide is included with the Q0320 system.

RECOMMENDED SOCKETS

Several sockets are recommended for the Q2220 DDS. They are the AMP 821575-1 44-pin PLCC Socket, (through-hole board mounting); the Burndy QILE44P-410T PLCC Socket (through-hole board mounting); and the Methode Electronics 213-044-602 Low-Profile Surface Mount Chip Carrier Socket (surface mount).

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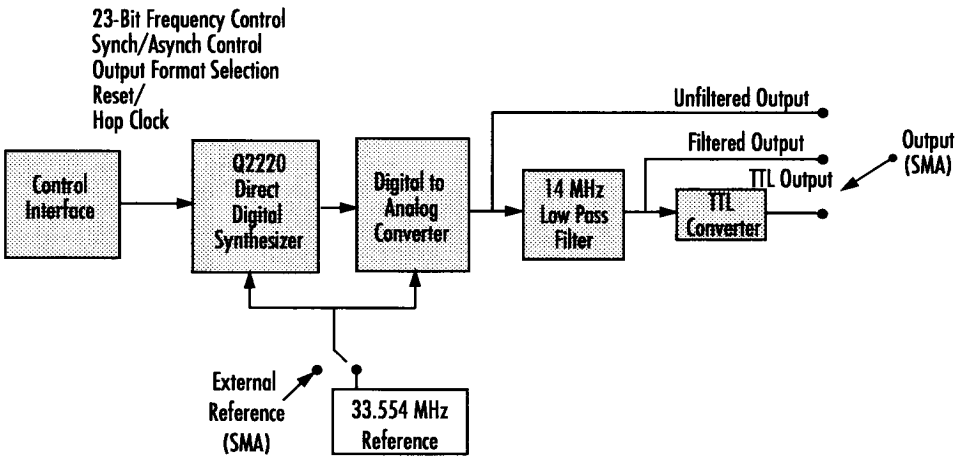
Figure 8. Q0320 Block Diagram



RECOMMENDED DACS

QUALCOMM Q2500 Series of 10-bit and 12-bit, 100 MHz Digital-to-Analog Converters (DACs). See QUALCOMM Q2500 Technical Data Sheet.

RELATED QUALCOMM LITERATURE

AN2334-3 "Direct Digital Synthesis, 21 Questions & Answers for RF Engineers," QUALCOMM, 1992.

AN2334-4 "Hybrid PLL/DDS Frequency Synthesizers," QUALCOMM, 1990.

Q0320-1 Direct Digital Synthesizer Board Information Sheet.

Q2510 Digital-to-Analog Converter Technical Data Sheet

ORDERING INFORMATION

Component Products

PRODUCT NUMBER	MAXIMUM CLOCK SPEED	PACKAGE	TEMPERATURE RANGE	V_{DD} INPUT	NOTES
Q2220I-50N	50 MHz	44 PLCC	-40°C to +85°C	4.5V to 5.5V	1
Q2220M-40L	40 MHz	44 CLDCC	-55°C to +125°C	4.5V to 5.5V	1, 2

Board-Level Products

PRODUCT NUMBER	DESCRIPTION
Q0320-1	Q2220 DDS Stand-alone Synthesizer Board with head
Q0320-2	Q2220 DDS Stand-alone Synthesizer Board with frequency select switches

NOTES:

1. For more information, refer to "Technical Specifications", page 12.
2. The Q2220M-40L is screened to MIL-STD-883C, Method 5004. Quality Conformance Inspection (QCI) Groups A and B to MIL 883C, level B, method 5005.

GLOSSARY

CLDCC	Ceramic Leaded Chip Carrier
DAC	Digital-to-Analog Converter
DDS	Direct Digital Synthesizer
FC	Frequency Control
F_G	Generated Frequency
F_S	System Clock Frequency
HOP CLK	Hop Clock
LPF	Low Pass Filter
LSB	Least Significant Bit
MSB	Most Significant Bit
PLCC	Plastic Leaded Chip Carrier

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10555 Sorrento Valley Road, San Diego, CA 92121-1617, USA, Telephone: (619) 597-5005, Fax: (619) 452-9096

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QUALCOMM Incorporated, VLSI Products
10555 Sorrento Valley Road, San Diego, CA 92121-1617, USA, Telephone: (619) 597-5005, Fax: (619) 452-9096

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