

## APPENDIX A ELECTRICAL CHARACTERISTICS

**Table A-1. Maximum Ratings**

Rating	Symbol	Value	Unit
Supply Voltage	$V_{DD}$	- 0.3 to + 7.0	V
Input Voltage	$V_{in}$	- 0.3 to + 7.0	V
Operating Temperature Range MC68HC(7)11Ex MC68HC(7)11ExC MC68HC(7)11ExV MC68HC(7)11ExM MC68HC811E2 MC68HC811E2C MC68HC811E2V MC68HC811E2M MC68L11E9	$T_A$	$T_L$ to $T_H$ 0 to + 70 - 40 to + 85 - 40 to + 105 - 40 to + 125 0 to + 70 - 40 to + 85 - 40 to + 105 - 40 to + 125 - 20 to + 70	°C
Storage Temperature Range	$T_{stg}$	- 55 to + 150	°C
Current Drain per Pin* Excluding $V_{DD}$ , $V_{SS}$ , $AV_{DD}$ , $V_{RH}$ , and $V_{RL}$	$I_D$	25	mA

\*One pin at a time, observing maximum power dissipation limits.

Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or  $V_{DD}$ ) enhances reliability of operation.

**Table A-2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Average Junction Temperature	$T_J$	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient Temperature	$T_A$	User-determined	°C
Package Thermal Resistance (Junction-to-Ambient) 48-Pin Plastic DIP (MC68HC811E2 only) 56-Pin Plastic SDIP 52-Pin Plastic Leaded Chip Carrier 52-Pin Plastic Thin Quad Flat Pack (TQFP) 64-Pin Quad Flat Pack	$\Theta_{JA}$	50 50 50 85 85	°C/W
Total Power Dissipation (Note 1)	$P_D$	$P_{INT} + P_{I/O}$ $K / (T_J + 273^\circ\text{C})$	W
Device Internal Power Dissipation	$P_{INT}$	$I_{DD} \times V_{DD}$	W
I/O Pin Power Dissipation (Note 2)	$P_{I/O}$	User-determined	W
A Constant (Note 3)	K	$P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JA} \times P_D^2$	W·°C

**NOTES:**

1. This is an approximate value, neglecting  $P_{I/O}$ .
2. For most applications  $P_{I/O} \ll P_{INT}$  and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known  $T_A$  and a measured  $P_D$  (at equilibrium). Use this value of K to solve for  $P_D$  and  $T_J$  iteratively for any value of  $T_A$ .



### Table A-3. DC Electrical Characteristics

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ , unless otherwise noted

Characteristics	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, RESET, and MODA $I_{Load} = \pm 10.0 \mu\text{A}$	$V_L$ $V_{OH}$	— $V_{DD} - 0.1$	0.1 —	V
Output High Voltage (Note 1) All Outputs Except XTAL, RESET, and MODA $I_{Load} = -0.8 \text{ mA}$ , $V_{DD} = 4.5 \text{ V}$	$V_{OH}$	$V_{DD} - 0.8$	—	V
Output Low Voltage $I_{Load} = 1.6 \text{ mA}$	$V_{OL}$	—	0.4	V
Input High Voltage All Inputs Except RESET RESET	$V_{IH}$	$0.7 \times V_{DD}$ $0.8 \times V_{DD}$	$V_{DD} + 0.3$ $V_{DD} + 0.3$	V
Input Low Voltage All Inputs	$V_{IL}$	$V_{SS} - 0.3$	$0.2 \times V_{DD}$	V
I/O Ports, Three-State Leakage $V_{in} = V_{IH}$ or $V_{IL}$ PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/LIR, RESET	$I_{OZ}$	—	$\pm 10$	$\mu\text{A}$
Input Leakage Current (Note 2) $V_{in} = V_{DD}$ or $V_{SS}$ $V_{in} = V_{DD}$ or $V_{SS}$ PA[2:0], IRQ, XIRQ MODB/VSTBY	$I_{in}$	— —	$\pm 1$ $\pm 10$	$\mu\text{A}$ $\mu\text{A}$
RAM Standby Voltage Power down	$V_{SB}$	4.0	$V_{DD}$	V
RAM Standby Current Power down	$I_{SB}$	—	10	$\mu\text{A}$
Input Capacitance PA[2:0], PE[7:0], IRQ, XIRQ, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/LIR, RESET	$C_{in}$	— —	8 12	pF pF
Output Load Capacitance All Outputs Except PD[4:1] PD[4:1]	$C_L$	— —	90 100	pF pF
Maximum Total Supply Current (Note 3)				
<b>RUN:</b>				
Single-Chip Mode				
2 MHz	$I_{DD}$	—	15	mA
3 MHz		—	27	mA
Expanded Multiplexed Mode				
2 MHz		—	27	mA
3 MHz		—	35	mA
<b>WAIT:</b> (All Peripheral Functions Shut Down)				
Single-Chip Mode				
2 MHz	$W_{IDD}$	—	6	mA
3 MHz		—	15	mA
Expanded Multiplexed Mode				
2 MHz		—	10	mA
3 MHz		—	20	mA
<b>STOP:</b>				
Single-Chip Mode, No Clocks				
- 40 to + 85	$S_{IDD}$	—	25	$\mu\text{A}$
> + 85 to + 105		—	50	
> +105 to + 125		—	100	
Maximum Power Dissipation				
Single-Chip Mode				
2 MHz	$P_D$	—	85	mW
3 MHz		—	150	mW
Expanded Multiplexed Mode				
2 MHz		—	150	mW
3 MHz		—	195	mW

**NOTES:**

- $V_{OH}$  specification for RESET and MODA is not applicable because they are open-drain pins.  $V_{OH}$  specification not applicable to ports C and D in wired-OR mode.
- Refer to A/D specification for leakage current for port E.
- EXTAL is driven with a square wave, and  
 $t_{cyc} = 500 \text{ ns}$  for 2 MHz rating;  
 $t_{cyc} = 333 \text{ ns}$  for 3 MHz rating;  $V_{IL} \leq 0.2 \text{ V}$ ;  
 $V_{IH} \geq V_{DD} - 0.2 \text{ V}$ ; No dc loads.



**Table A-3a. DC Electrical Characteristics (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ , unless otherwise noted

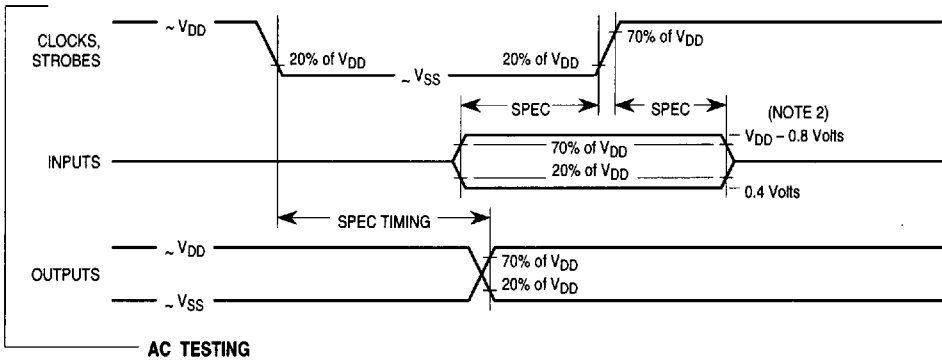
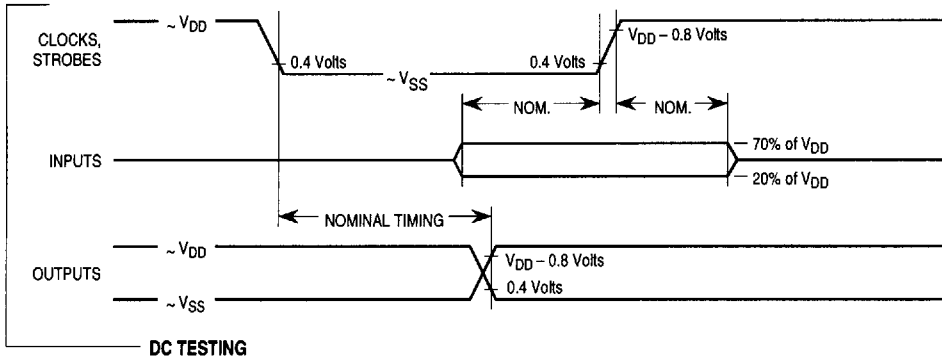
Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, RESET, and MODA $I_{Load} = \pm 10.0 \mu\text{A}$	$V_{OL}$ $V_{OH}$	— $V_{DD} - 0.1$	0.1 —	V V
Output High Voltage (Note 1) All Outputs Except XTAL, RESET, and MODA $I_{Load} = -0.5 \text{ mA}$ , $V_{DD} = 3.0 \text{ V}$ $I_{Load} = -0.8 \text{ mA}$ , $V_{DD} = 4.5 \text{ V}$	$V_{OH}$	$V_{DD} - 0.8$	—	V
Output Low Voltage All Outputs Except XTAL $I_{Load} = 1.6 \text{ mA}$ , $V_{DD} = 5.0 \text{ V}$ $I_{Load} = 1.0 \text{ mA}$ , $V_{DD} = 3.0 \text{ V}$	$V_{OL}$	—	0.4	V
Input High Voltage All Inputs Except $\overline{\text{RESET}}$ RESET	$V_{IH}$	$0.7 \times V_{DD}$ $0.8 \times V_{DD}$	$V_{DD} + 0.3$ $V_{DD} + 0.3$	V V
Input Low Voltage All Inputs	$V_{IL}$	$V_{SS} - 0.3$	$0.2 \times V_{DD}$	V
I/O Ports, Three-State Leakage PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/LIR, RESET $V_{in} = V_{IH} \text{ or } V_{IL}$	$I_{OZ}$	—	$\pm 10$	$\mu\text{A}$
Input Leakage Current (Note 2) $V_{in} = V_{DD} \text{ or } V_{SS}$ $V_{in} = V_{DD} \text{ or } V_{SS}$	$I_{in}$	— —	$\pm 1$ $\pm 10$	$\mu\text{A}$ $\mu\text{A}$
RAM Standby Voltage Power down	$V_{SB}$	2.0	$V_{DD}$	V
RAM Standby Current Power down	$I_{SB}$	—	10	$\mu\text{A}$
Input Capacitance PA[2:0], PE[7:0], IRQ, XIRQ, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/LIR, RESET	$C_{in}$	— —	8 12	pF pF
Output Load Capacitance All Outputs Except PD[4:1] PD[4:1]	$C_L$	— —	90 100	pF pF

Characteristic	Symbol	1 MHz	2 MHz	Unit
Maximum Total Supply Current (Note 3) <b>RUN:</b>				
Single-Chip Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$	$I_{DD}$	8 4	15 8	$\text{mA}$ $\text{mA}$
Expanded Multiplexed Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$		14 7	27 14	$\text{mA}$ $\text{mA}$
<b>WAIT:</b> (All Peripheral Functions Shut Down)				
Single-Chip Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$	$W_{IDD}$	3 1.5	6 3	$\text{mA}$ $\text{mA}$
Expanded Multiplexed Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$		5 2.5	10 5	$\text{mA}$ $\text{mA}$
<b>STOP:</b>				
Single-Chip Mode, No Clocks $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$	$S_{IDD}$	50 25	50 25	$\mu\text{A}$ $\mu\text{A}$
Maximum Power Dissipation				
Single-Chip Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$	$P_D$	44 12	85 24	$\text{mW}$ $\text{mW}$
Expanded Multiplexed Mode $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 3.0 \text{ V}$		77 21	150 42	$\text{mW}$ $\text{mW}$

**NOTES:**

- $V_{OH}$  specification for  $\overline{\text{RESET}}$  and MODA is not applicable because they are open-drain pins.  $V_{OH}$  specification not applicable to ports C and D in wired-OR mode.
- Refer to A/D specification for leakage current for port E.
- EXTAL is driven with a square wave, and  
 $t_{cyc} = 1000 \text{ ns}$  for 1 MHz rating;  
 $t_{cyc} = 500 \text{ ns}$  for 2 MHz rating;  $V_{IL} \leq 0.2 \text{ V}$ ;  
 $V_{IH} \geq V_{DD} - 0.2 \text{ V}$ ; No dc loads.





**NOTES:**

1. Full test loads are applied during all DC electrical tests and AC timing measurements.
2. During AC timing measurements, inputs are driven to 0.4 volts and  $V_{DD} - 0.8$  volts while timing measurements are taken at the 20% and 70% of  $V_{DD}$  points.

TEST METHODS 2

**Figure A-1. Test Methods**



**Table A-4. Control Timing**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	$f_o$	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	$t_{cyc}$	1000	—	500	—	333	—	ns
Crystal Frequency	$f_{XTAL}$	—	4.0	—	8.0	—	12.0	MHz
External Oscillator Frequency	$4 f_o$	dc	4.0	dc	8.0	dc	12.0	MHz
Processor Control Setup Time $t_{PCSU} = 1/4 t_{cyc} + 50 \text{ ns}$	$t_{PCSU}$	300	—	175	—	133	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	$PWRSTL$	8 1	— —	8 1	— —	8 1	— —	$t_{cyc}$
Mode Programming Setup Time	$t_{MPS}$	2	—	2	—	2	—	$t_{cyc}$
Mode Programming Hold Time	$t_{MPH}$	10	—	10	—	10	—	ns
Interrupt Pulse Width, IRQ Edge-Sensitive Mode $PW_{IRQ} = t_{cyc} + 20 \text{ ns}$	$PW_{IRQ}$	1020	—	520	—	353	—	ns
Wait Recovery Startup Time	$t_{WRS}$	—	4	—	4	—	4	$t_{cyc}$
Timer Pulse Width Input Capture Pulse Accumulator Input $PW_{TIM} = t_{cyc} + 20 \text{ ns}$	$PW_{TIM}$	1020	—	520	—	353	—	ns

NOTES:

1. RESET is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.

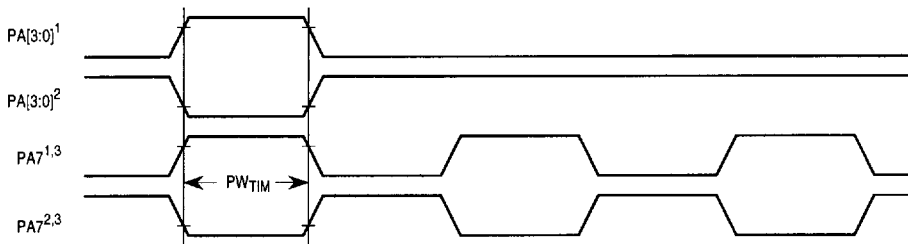
**Table A-4a. Control Timing (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation	$f_o$	dc	1.0	dc	2.0	MHz
E-Clock Period	$t_{cyc}$	1000	—	500	—	ns
Crystal Frequency	$f_{XTAL}$	—	4.0	—	8.0	MHz
External Oscillator Frequency	$4 f_o$	dc	4.0	dc	8.0	MHz
Processor Control Setup Time $t_{PCSU} = 1/4 t_{cyc} + 75 \text{ ns}$	$t_{PCSU}$	325	—	200	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	$PW_{RSTL}$	8 1	— —	8 1	— —	$t_{cyc}$ $t_{cyc}$
Mode Programming Setup Time	$t_{MPS}$	2	—	2	—	$t_{cyc}$
Mode Programming Hold Time	$t_{MPH}$	10	—	10	—	ns
Interrupt Pulse Width, IRQ Edge-Sensitive Mode $PW_{IRQ} = t_{cyc} + 20 \text{ ns}$	$PW_{IRQ}$	1020	—	520	—	ns
Wait Recovery Startup Time	$t_{WRS}$	—	4	—	4	$t_{cyc}$
Timer Pulse Width, Input Capture Pulse Accumulator Input $PW_{TIM} = t_{cyc} + 20 \text{ ns}$	$PW_{TIM}$	1020	—	520	—	ns

**NOTES:**

1. RESET is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.



**NOTES:**

1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

TIMER INPUTS TIM

**Figure A-2. Timer Inputs**



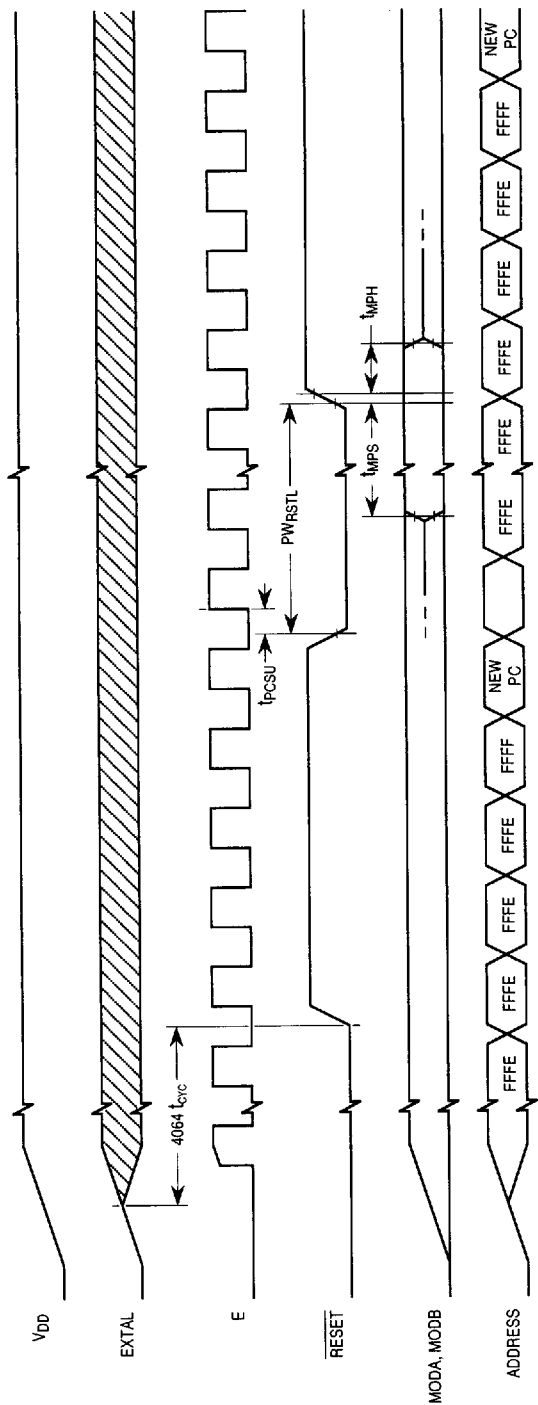
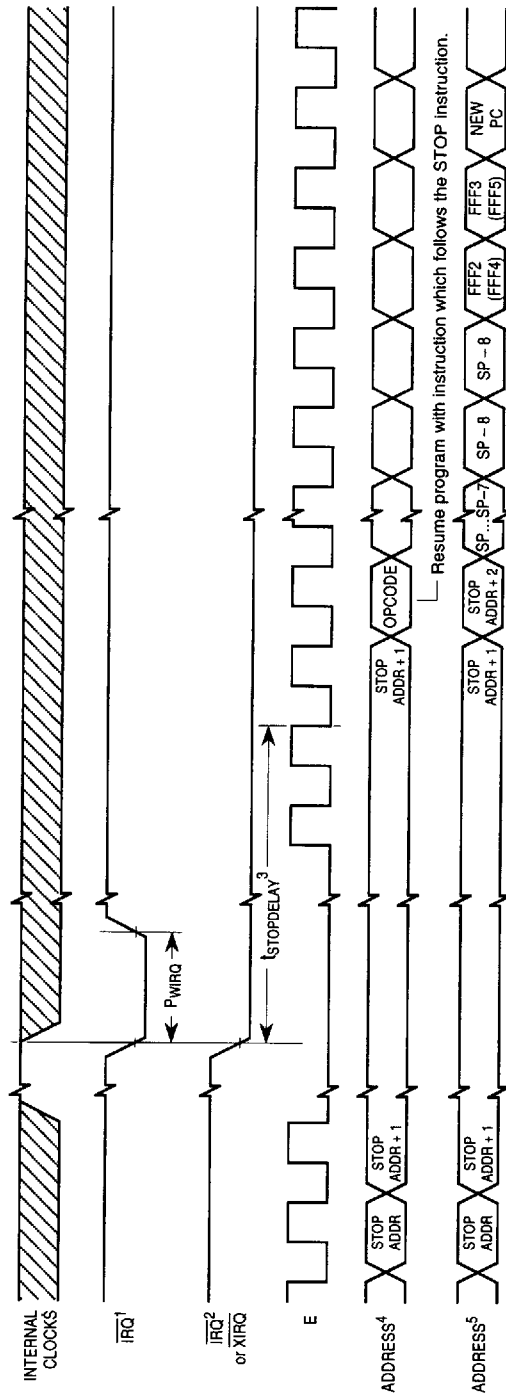


Figure A-3. POR External Reset Timing Diagram

POR EXT RESET TIM



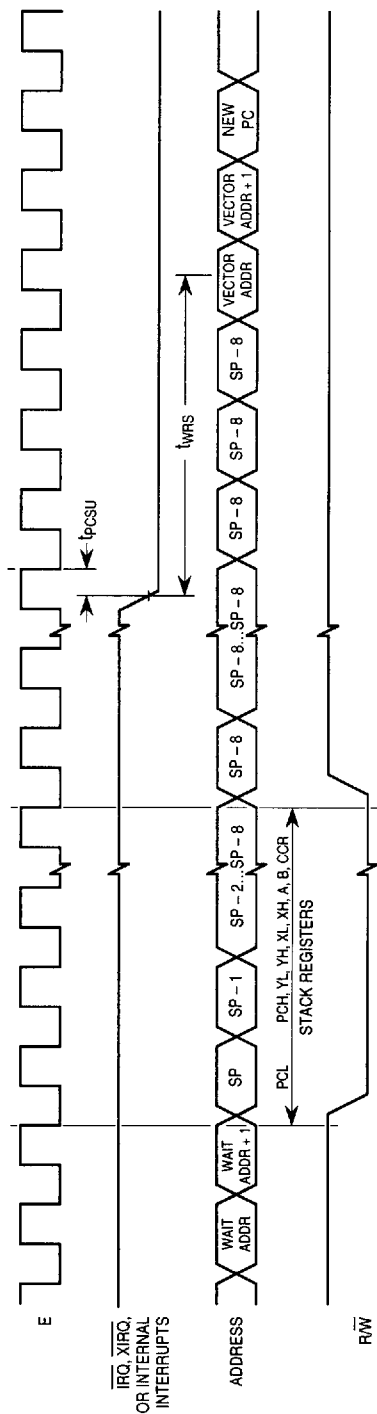


NOTES:

1. Edge Sensitive  $\overline{IRQ}$  pin (IRQE bit = 1)
2. Level sensitive  $\overline{IRQ}$  pin (IRQE bit = 0)
3.  $t_{STOPDELAY} = 4064 t_{CYC}$  if DLY bit = 1 or  $4 t_{CYC}$  if DLY = 0.
4.  $\overline{XIRQ}$  with X bit in CCR = 1.
5.  $\overline{IRQ}$  or  $\overline{XIRQ}$  with X bit in CCR = 0.

Figure A-4. STOP Recovery Timing Diagram

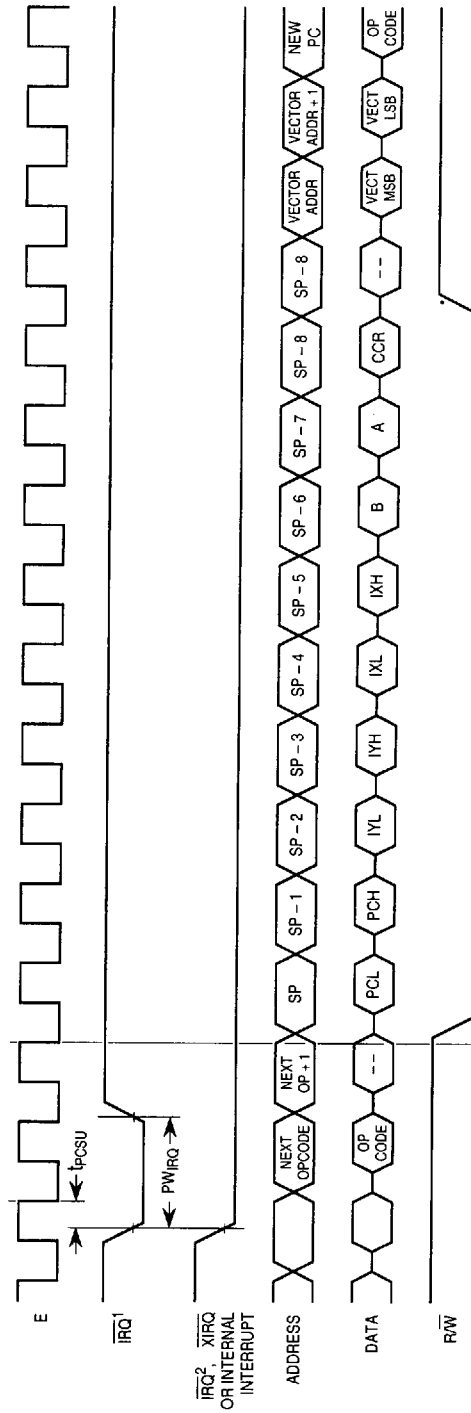




NOTE:  $\overline{\text{RESET}}$  also causes recovery from WAIT.

Figure A-5. WAIT Recovery from Interrupt Timing Diagram

WAIT RECOVERY TIM



NOTES:

1. Edge sensitive  $\overline{IRQ}$  pin (IRQE bit = 1)
2. Level sensitive  $\overline{IRQ}$  pin (IRQE bit = 0)

Figure A-6. Interrupt Timing Diagram

**Table A-5. Peripheral Port Timing**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	$f_o$	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	$t_{cyc}$	1000	—	500	—	333	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	$t_{PDSU}$	100	—	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	$t_{PDH}$	50	—	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D $t_{PWD} = 1/4 t_{cyc} + 100 \text{ ns}$	$t_{PWD}$	—	200	—	200	—	200	ns
		—	350	—	225	—	183	ns
Input Data Setup Time (Port C)	$t_{IS}$	60	—	60	—	60	—	ns
Input Data Hold Time (Port C)	$t_{IH}$	100	—	100	—	100	—	ns
Delay Time, E Fall to STRB $t_{DEB} = 1/4 t_{cyc} + 100 \text{ ns}$	$t_{DEB}$	—	350	—	225	—	183	ns
Setup Time, STRA Asserted to E Fall (Note 1)	$t_{AES}$	0	—	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	$t_{PCD}$	—	100	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	$t_{PCH}$	10	—	10	—	10	—	ns
Three-State Hold Time	$t_{PCZ}$	—	150	—	150	—	150	ns

**NOTES:**

1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.



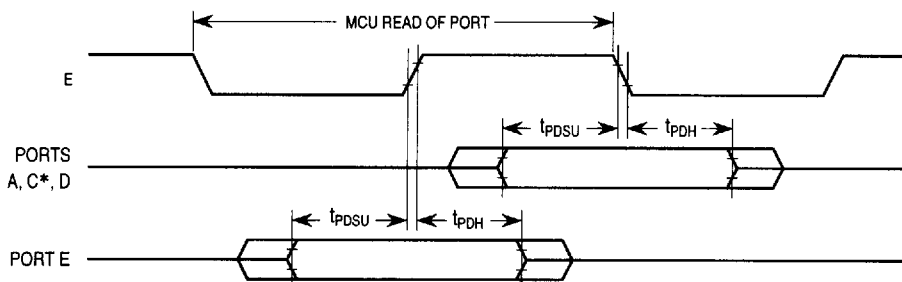
**Table A-5a. Peripheral Port Timing (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	$f_o$	dc	1.0	dc	2.0	MHz
E-Clock Period	$t_{cyc}$	1000	—	500	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	$t_{PDSU}$	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	$t_{PDH}$	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D $t_{PWD} = 1/4 t_{cyc} + 150 \text{ ns}$	$t_{PWD}$	—	250	—	250	ns
		—	400	—	275	ns
Input Data Setup Time (Port C)	$t_{IS}$	60	—	60	—	ns
Input Data Hold Time (Port C)	$t_{IH}$	100	—	100	—	ns
Delay Time, E Fall to STRB $t_{DEB} = 1/4 t_{cyc} + 150 \text{ ns}$	$t_{DEB}$	—	400	—	275	ns
Setup Time, STRA Asserted to E Fall (Note 1)	$t_{AES}$	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	$t_{PCD}$	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	$t_{PCH}$	10	—	10	—	ns
Three-State Hold Time	$t_{PCZ}$	—	150	—	150	ns

**NOTES:**

1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.

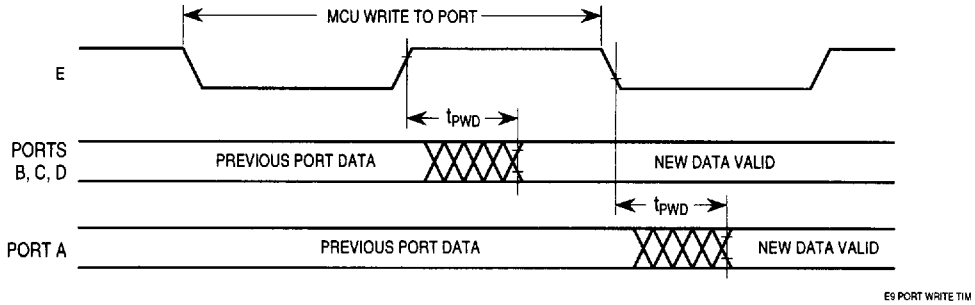


\* FOR NON-LATCHED OPERATION OF PORT C

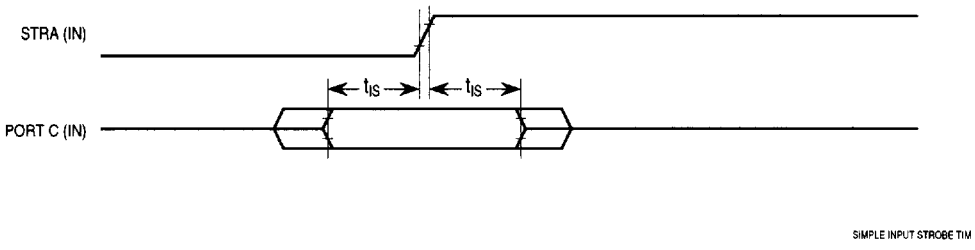
E9 PORT READ TIM

**Figure A-7. Port Read Timing Diagram**

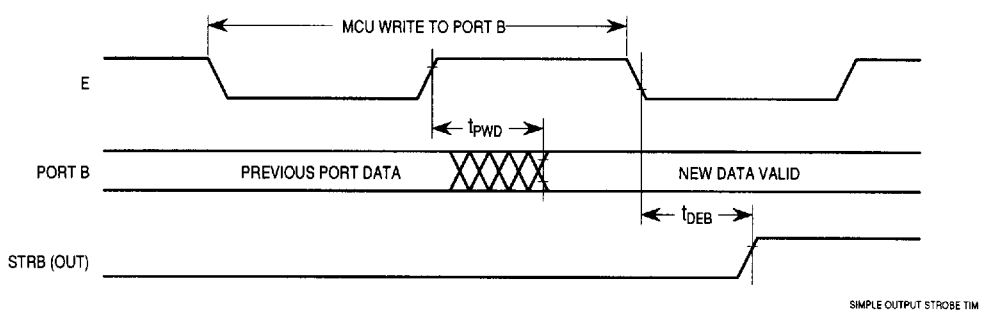




**Figure A-8. Port Write Timing Diagram**

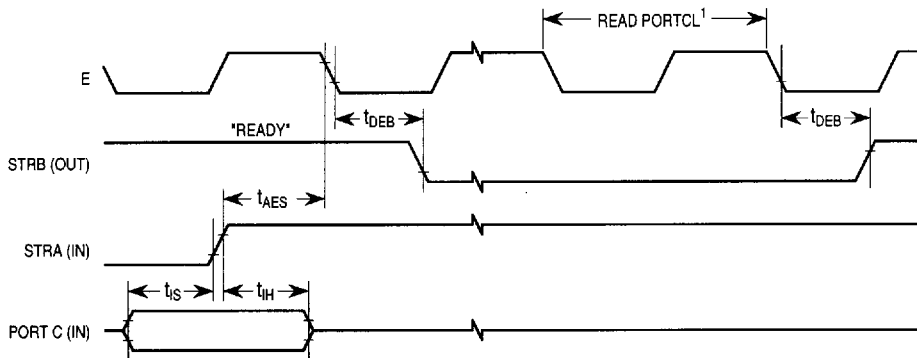


**Figure A-9. Simple Input Strobe Timing Diagram**



**Figure A-10. Simple Output Strobe Timing Diagram**



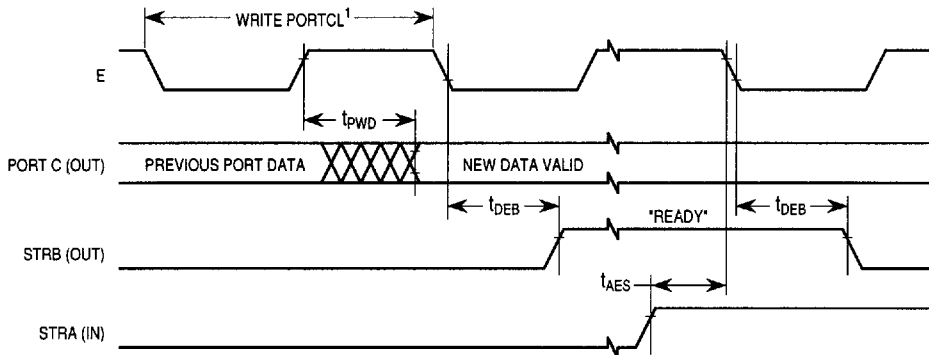


NOTES:

1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C INPUT HANDSHK TIM

Figure A-11. Port C Input Handshake Timing Diagram



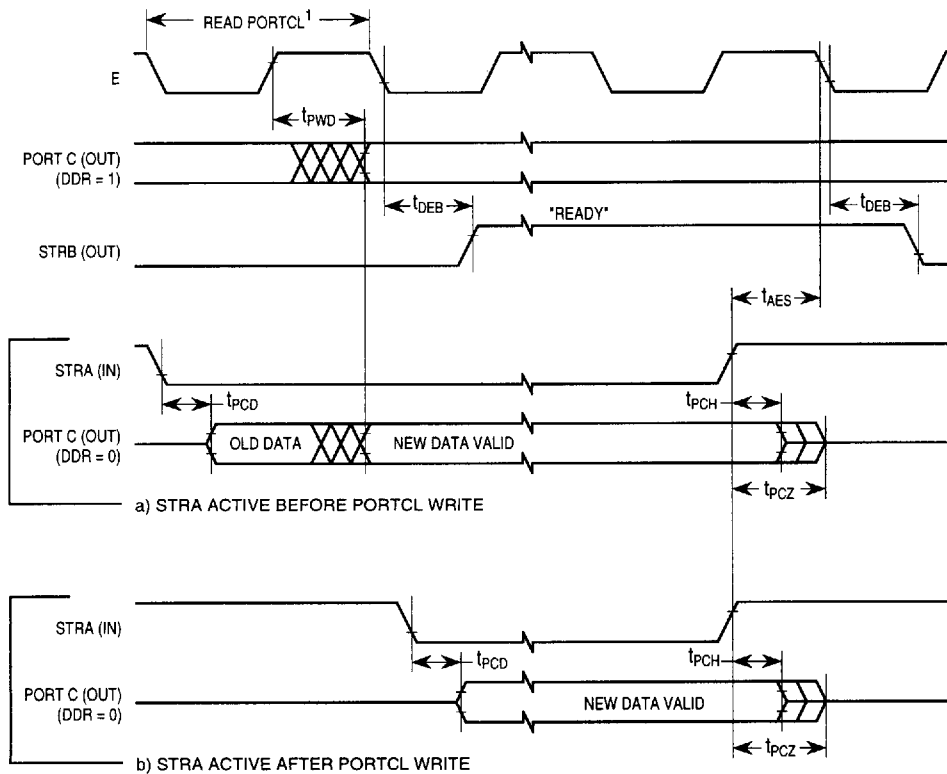
NOTES:

1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C OUTPUT HANDSHK TIM

Figure A-12. Port C Output Handshake Timing Diagram





NOTES:

1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

3-STATE VAR OUTPUT HANDSHK TIM

**Figure A-13. Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)**



**Table A-6. Analog-To-Digital Converter Characteristics**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$ ,  $750 \text{ kHz} \leq E \leq 3.0 \text{ MHz}$ , unless otherwise noted

Characteristic	Parameter	Min	Absolute	2.0 MHz	3.0 MHz	Unit
				Max	Max	
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	$\pm 1/2$	$\pm 1$	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	$\pm 1/2$	$\pm 1$	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	$\pm 1/2$	$\pm 1$	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	$\pm 1/2$	$\pm 1 1/2$	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	$\pm 1/2$	$\pm 1/2$	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	$\pm 1$	$\pm 2$	LSB
Conversion Range	Analog Input Voltage Range	$V_{RL}$	—	$V_{RH}$	$V_{RH}$	V
$V_{RH}$	Maximum Analog Reference Voltage (Note 2)	$V_{RL}$	—	$V_{DD} + 0.1$	$V_{DD} + 0.1$	V
$V_{RL}$	Minimum Analog Reference Voltage (Note 2)	$V_{SS} - 0.1$	—	$V_{RH}$	$V_{RH}$	V
$\Delta V_R$	Minimum Difference between $V_{RH}$ and $V_{RL}$ (Note 2)	3	—	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:  E Clock  Internal RC Oscillator	—	32	—	—	$t_{cyc}$
		—	—	$t_{cyc} + 32$	$t_{cyc} + 32$	$\mu s$
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—	—
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:  E Clock  Internal RC Oscillator	—	12	—	—	$t_{cyc}$
		—	—	12	12	$\mu s$
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]  $V_{RL}, V_{RH}$	—	—	400	400	nA
		—	—	1.0	1.0	$\mu A$

NOTES:

1. Source impedances greater than 10 k $\Omega$  affect accuracy adversely because of input leakage.
2. Performance verified down to 2.5 V  $\Delta V_R$ , but accuracy is tested and guaranteed at  $\Delta V_R = 5 \text{ V} \pm 10\%$ .





**Table A-6a. Analog-To-Digital Converter Characteristics (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc}$  to  $5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L$  to  $T_H$ ,  $750 \text{ kHz} \leq E \leq 2.0 \text{ MHz}$ , unless otherwise noted

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	$\pm 1$	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	$\pm 1$	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	$\pm 1$	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	$\pm 1 \frac{1}{2}$	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	$\pm \frac{1}{2}$	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	$\pm 2$	LSB
Conversion Range	Analog Input Voltage Range	$V_{RL}$	—	$V_{RH}$	V
$V_{RH}$	Maximum Analog Reference Voltage	$V_{RL}$	—	$V_{DD} + 0.1$	V
$V_{RL}$	Minimum Analog Reference Voltage	$V_{SS} - 0.1$	—	$V_{RH}$	V
$\Delta V_R$	Minimum Difference between $V_{RH}$ and $V_{RL}$	3.0	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:				
		E Clock	32	—	$t_{cyc}$
	Internal RC Oscillator	—	—	$t_{cyc} + 32$	$\mu s$
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:				
		E Clock	12	—	$t_{cyc}$
	Internal RC Oscillator	—	—	12	$\mu s$
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]	—	—	400	nA
		$V_{RL}, V_{RH}$	—	—	1.0

**NOTES:**

1. Source impedances greater than 10 k $\Omega$  affect accuracy adversely because of input leakage.



**Table A-7. Expansion Bus Timing**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	$f_o$	dc	1.0	dc	2.0	dc	3.0	MHz
1	Cycle Time	$t_{cyc}$	1000	—	500	—	333	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2 t_{cyc} - 23 \text{ ns}$ (Note 1)	$PW_{EL}$	477	—	227	—	146	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2 t_{cyc} - 28 \text{ ns}$ (Note 1)	$PW_{EH}$	472	—	222	—	141	—	ns
4a	E and AS Rise Time	$t_r$	—	20	—	20	—	20	ns
4b	E and AS Fall Time	$t_f$	—	20	—	20	—	15	ns
9	Address Hold Time $t_{AH} = 1/8 t_{cyc} - 29.5 \text{ ns}$ (Note 1, 2a)	$t_{AH}$	95.5	—	33	—	26	—	ns
12	Nonmultiplexed Address Valid Time to E Rise $t_{AV} = PW_{EL} - (t_{ASD} + 80 \text{ ns})$ (Note 1, 2a)	$t_{AV}$	281.5	—	94	—	54	—	ns
17	Read Data Setup Time	$t_{DSR}$	30	—	30	—	30	—	ns
18	Read Data Hold Time (Max = $t_{MAD}$ )	$t_{DHR}$	0	145.5	0	83	0	51	ns
19	Write Data Delay Time $t_{DDW} = 1/8 t_{cyc} + 65.5 \text{ ns}$ (Note 1, 2a)	$t_{DDW}$	—	190.5	—	128	—	71	ns
21	Write Data Hold Time $t_{DHW} = 1/8 t_{cyc} - 29.5 \text{ ns}$ (Note 1, 2a)	$t_{DHW}$	95.5	—	33	—	26	—	ns
22	Multiplexed Address Valid Time to E Rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90 \text{ ns})$ (Note 1, 2a)	$t_{AVM}$	271.5	—	84	—	54	—	ns
24	Multiplexed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} - 70 \text{ ns}$ (Note 1)	$t_{ASL}$	151	—	26	—	13	—	ns
25	Multiplexed Address Hold Time $t_{AHL} = 1/8 t_{cyc} - 29.5 \text{ ns}$ (Note 1, 2b)	$t_{AHL}$	95.5	—	33	—	31	—	ns
26	Delay Time, E to AS Rise $t_{ASD} = 1/8 t_{cyc} - 9.5 \text{ ns}$ (Note 1, 2a)	$t_{ASD}$	115.5	—	53	—	31	—	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4 t_{cyc} - 29 \text{ ns}$ (Note 1)	$PW_{ASH}$	221	—	96	—	63	—	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8 t_{cyc} - 9.5 \text{ ns}$ (Note 1, 2b)	$t_{ASED}$	115.5	—	53	—	31	—	ns
29	MPU Address Access Time (Note 2a) $t_{ACCA} = t_{cyc} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	$t_{ACCA}$	744.5	—	307	—	196	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} - t_{DSR}$	$t_{ACCE}$	—	442	—	192	—	111	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30 \text{ ns}$ (Note 1, 2a)	$t_{MAD}$	145.5	—	83	—	51	—	ns

**NOTES:**

- Formula only for dc to 2 MHz.
- Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of  $1/8 t_{cyc}$  in the above formulas, where applicable:

(a)  $(1-DC) \times 1/4 t_{cyc}$

(b)  $DC \times 1/4 t_{cyc}$

Where:

DC is the decimal value of duty cycle percentage (high time).

- All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.



**Table A-7a. Expansion Bus Timing (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	$f_o$	dc	1.0	dc	2.0	MHz
1	Cycle Time	$t_{cyc}$	1000	—	500	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2 t_{cyc} - 25 \text{ ns}$	$PW_{EL}$	475	—	225	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2 t_{cyc} - 30 \text{ ns}$	$PW_{EH}$	470	—	220	—	ns
4A	E and AS Rise Time	$t_r$	—	25	—	25	ns
4B	E and AS Fall Time	$t_f$	—	25	—	25	ns
9	Address Hold Time $t_{AH} = 1/8 t_{cyc} - 30 \text{ ns}$ (Note 1a)	$t_{AH}$	95	—	33	—	ns
12	Nonmultiplexed Address Valid Time to E Rise $t_{AV} = PW_{EL} - (t_{ASD} + 80 \text{ ns})$ (Note 1a)	$t_{AV}$	275	—	88	—	ns
17	Read Data Setup Time	$t_{DSR}$	30	—	30	—	ns
18	Read Data Hold Time (Max = $t_{MAD}$ )	$t_{DHR}$	0	150	0	88	ns
19	Write Data Delay Time $t_{DDW} = 1/8 t_{cyc} + 70 \text{ ns}$ (Note 1a)	$t_{DDW}$	—	195	—	133	ns
21	Write Data Hold Time $t_{DHW} = 1/8 t_{cyc} - 30 \text{ ns}$ (Note 1a)	$t_{DHW}$	95	—	33	—	ns
22	Multiplexed Address Valid Time to E Rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90 \text{ ns})$ (Note 1a)	$t_{AVM}$	265	—	78	—	ns
24	Multiplexed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} - 70 \text{ ns}$	$t_{ASL}$	150	—	25	—	ns
25	Multiplexed Address Hold Time $t_{AHL} = 1/8 t_{cyc} - 30 \text{ ns}$ (Note 1b)	$t_{AHL}$	95	—	33	—	ns
26	Delay Time, E to AS Rise $t_{ASD} = 1/8 t_{cyc} - 5 \text{ ns}$ (Note 1a)	$t_{ASD}$	120	—	58	—	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4 t_{cyc} - 30 \text{ ns}$	$PW_{ASH}$	220	—	95	—	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8 t_{cyc} - 5 \text{ ns}$ (Note 1b)	$t_{ASED}$	120	—	58	—	ns
29	MPU Address Access Time (Note 1a) $t_{ACCA} = t_{cyc} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	$t_{ACCA}$	735	—	298	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} - t_{DSR}$	$t_{ACCE}$	—	440	—	190	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30 \text{ ns}$ (Note 1a)	$t_{MAD}$	150	—	88	—	ns

**NOTES:**

- Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of  $1/8 t_{cyc}$  in the above formulas, where applicable:

(a)  $(1-DC) \times 1/4 t_{cyc}$

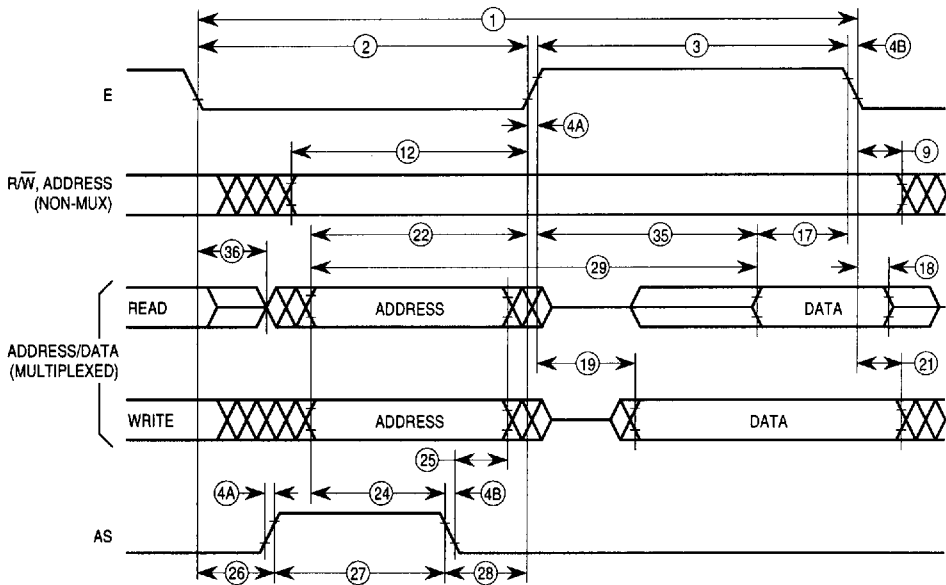
(b)  $DC \times 1/4 t_{cyc}$

Where:

DC is the decimal value of duty cycle percentage (high time).

- All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.





NOTE: Measurement points shown are 20% and 70% of  $V_{DD}$ .

MUX BUS TIM

**Figure A-14. Multiplexed Expansion Bus Timing Diagram**



**Table A-8. Serial Peripheral Interface Timing**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 2.0	dc dc	0.5 3.0	$f_{op}$ MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 500	— —	2.0 333	— —	$t_{cyc}$ ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 250	— —	— 240	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 250	— —	— 240	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	340 190	— —	227 127	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	340 190	— —	227 127	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	$t_a$	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	$t_{dis}$	—	240	—	167	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_v(s)$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	$t_{ho}$	0	—	0	—	ns
12	Rise Time (20% $V_{DD}$ to 70% $V_{DD}$ , $C_L = 200 \text{ pF}$ ) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and SS)	$t_{rm}$ $t_{rs}$	— —	100 2.0	— —	100 2.0	ns $\mu\text{s}$
13	Fall Time (70% $V_{DD}$ to 20% $V_{DD}$ , $C_L = 200 \text{ pF}$ ) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and SS)	$t_{fm}$ $t_{fs}$	— —	100 2.0	— —	100 2.0	ns $\mu\text{s}$

**NOTES:**

1. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on SCK, MOSI, and MISO pins.



**Table A–8a. Serial Peripheral Interface Timing (MC68L11E9)**

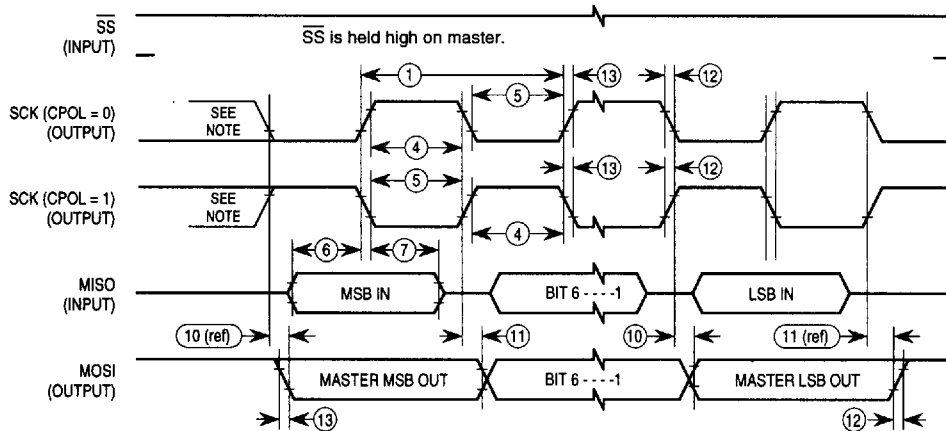
$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 1.0	dc dc	0.5 2.0	$f_{op}$ MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 1000	— —	2.0 500	— —	$t_{cyc}$ ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 500	— —	— 250	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 500	— —	— 250	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	680 380	— —	340 190	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	680 380	— —	340 190	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Imp. State) Slave	$t_a$	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	$t_{dis}$	—	240	—	240	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_v(s)$	—	240	—	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	$t_{ho}$	0	—	0	—	ns
12	Rise Time (20% $V_{DD}$ to 70% $V_{DD}$ , $C_L = 200 \text{ pF}$ ) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and SS)	$t_{rm}$ $t_{rs}$	— —	100 2.0	— —	100 2.0	ns $\mu\text{s}$
13	Fall Time (70% $V_{DD}$ to 20% $V_{DD}$ , $C_L = 200 \text{ pF}$ ) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and SS)	$t_{fm}$ $t_{fs}$	— —	100 2.0	— —	100 2.0	ns $\mu\text{s}$

NOTES:

1. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless otherwise noted.
2. Signal production depends on software.
3. Assumes 100 pF load on all SPI pins.

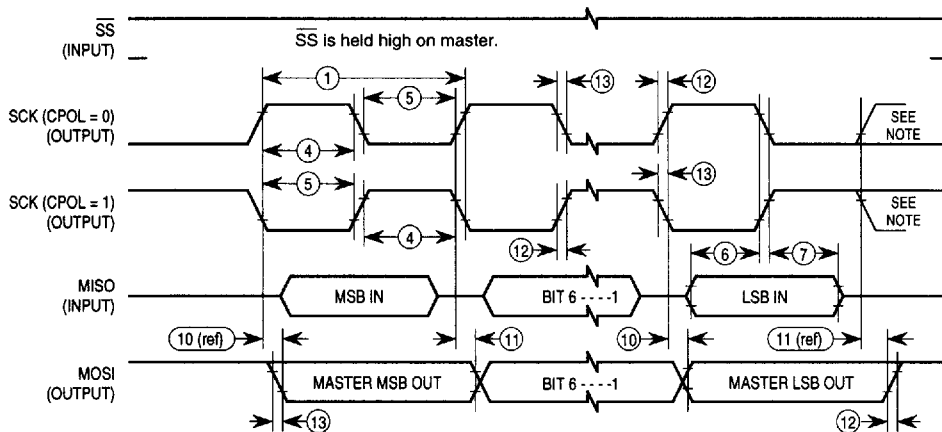




NOTE: This first clock edge is generated internally but is not seen at the SCK pin.

SPI MASTER CPHA0 TIM

### a) SPI Master Timing (CPHA = 0)

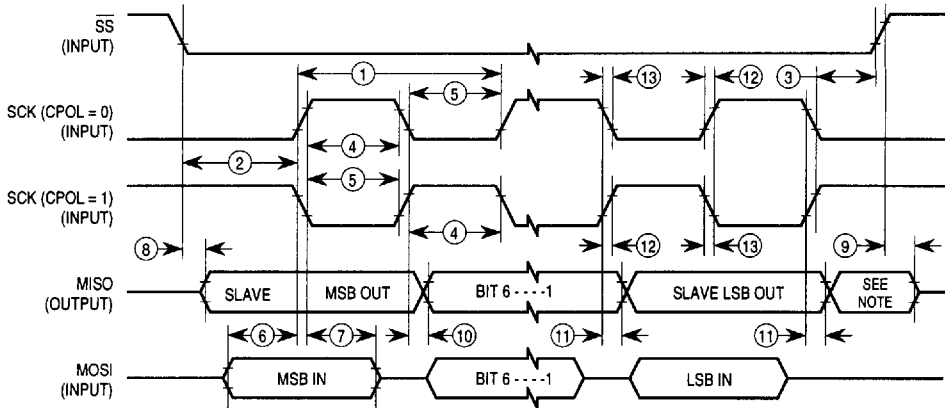


NOTE: This last clock edge is generated internally but is not seen at the SCK pin.

SPI MASTER CPHA1 TIM

### b) SPI Master Timing (CPHA = 1)

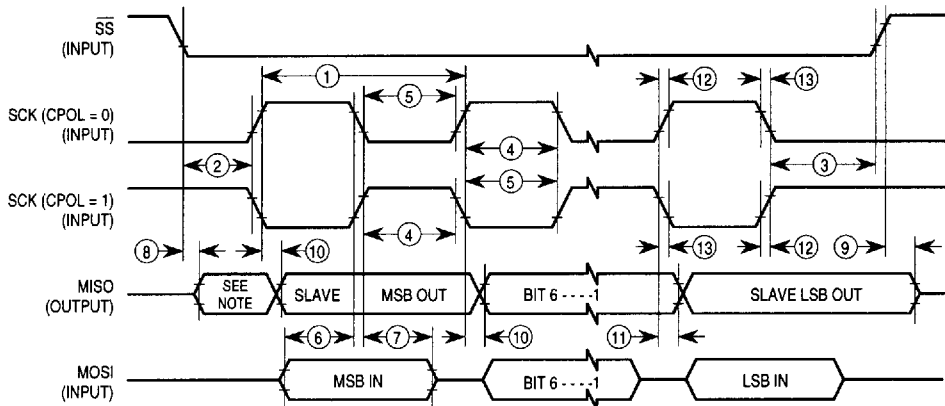
Figure A-15. SPI Timing Diagram (1 of 2)



NOTE: Not defined but normally MSB of character just received.

SPI SLAVE CPHA0 TIM

### a) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character previously transmitted.

SPI SLAVE CPHA1 TIM

### b) SPI Slave Timing (CPHA = 1)

Figure A-15. SPI Timing Diagram (2 of 2)





**Table A-9. EEPROM Characteristics**

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic	Temperature Range			Unit	
	- 40 to 85° C	- 40 to 105° C	- 40 to 125° C		
Programming Time (Note 1)	<1.0 MHz, RCO Enabled	10	15	ms	
	1.0 to 2.0 MHz, RCO Enabled	20	Must use RCO		
	≥ 2.0 MHz (or Anytime RCO Enabled)	10	15		
Erased Time (Note 1)	Byte, Row and Bulk	10	10	10	ms
Write/Erase Endurance (Note 2)		10,000	10,000	10,000	Cycles
Data Retention (Note 2)		10	10	10	Years

NOTES:

1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

**Table A-9a. EEPROM Characteristics (MC68L11E9)**

$V_{DD} = 3.0 \text{ Vdc to } 5.5 \text{ Vdc}$ ,  $V_{SS} = 0 \text{ Vdc}$ ,  $T_A = T_L \text{ to } T_H$

Characteristic		Temperature Range	Unit
		- 20 to 70° C	
Programming Time (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled	25	ms
	5 V, E ≤ 2.0 MHz, RCO Enabled	10	ms
Erased Time (Byte, Row and Bulk) (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled	25	ms
	5 V, E ≤ 2.0 MHz, RCO Enabled	10	ms
Write/Erase Endurance (Note 2)		10,000	Cycles
Data Retention (Note 2)		10	Years

NOTES:

1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

