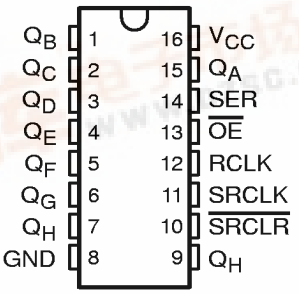
# SN54HC595, SN74HC595
# 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

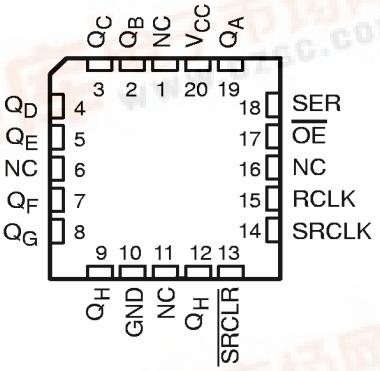
SCLS041B – DECEMBER 1982 – REVISED MAY 1997

- **8-Bit Serial-In, Parallel-Out Shift**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54HC595 . . . J OR W PACKAGE**
**SN74HC595 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54HC595 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

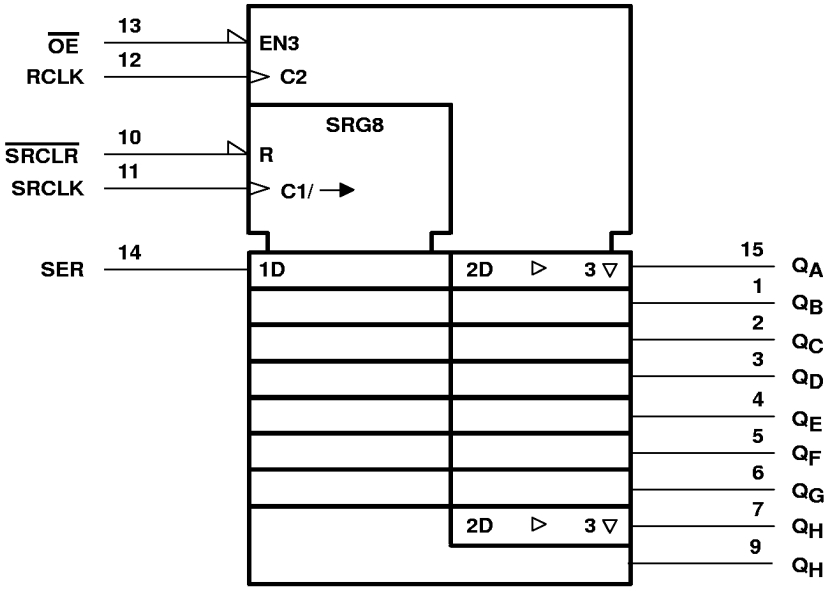
## description

The ’HC595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading.

Both the shift register clock (RCLK) and storage register clock (SRCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

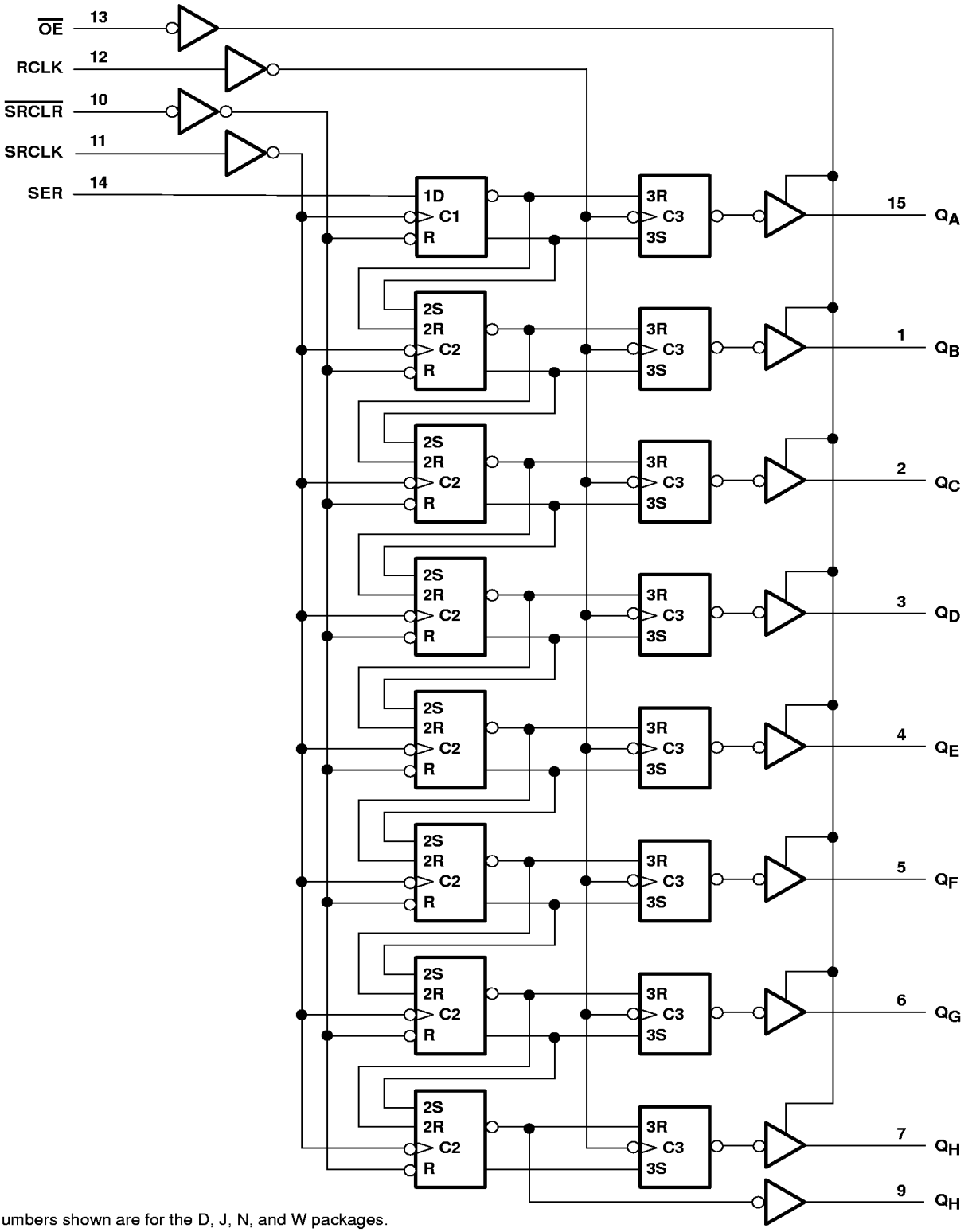
The SN54HC595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC595 is characterized for operation from –40°C to 85°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 113°C/W
N package . . . . . 78°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

| | | | SN54HC595 | | | SN74HC595 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | 0 | | 0.5 | 0 | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | 0 | | 1.35 | 0 | | 1.35 | |
| | | $V_{CC}$ = 6 V | 0 | | 1.8 | 0 | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$‡ | Input transition (rise and fall) time | $V_{CC}$ = 2 V | 0 | | 1000 | 0 | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | 0 | | 500 | 0 | | 500 | |
| | | $V_{CC}$ = 6 V | 0 | | 400 | 0 | | 400 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

‡ If this device is used in the threshold region (from $V_{IL}$max = 0.5 V to $V_{IH}$min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t$ = 1000 ns and $V_{CC}$ = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $Q_H$ , $I_{OH}$ = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $Q_A$–$Q_H$, $I_{OH}$ = –6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $Q_H$ , $I_{OH}$ = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | $Q_A$–$Q_H$, $I_{OH}$ = –7.8 mA | | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $Q_H$ , $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $Q_A$–$Q_H$, $I_{OL}$ = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $Q_H$ , $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| | | $Q_A$–$Q_H$, $I_{OL}$ = 7.8 mA | | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6 V | | | ±0.1 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or 0 | | 6 V | | | ±0.01 | | ±10 | | ±5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, | $I_O$ = 0 | 6 V | | | 8 | | 160 | | 80 | μA |
| $C_i$ | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC595 | | SN74HC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 2 V | 0 | 6 | 0 | 4.2 | 0 | 5 | MHz |
| | | | 4.5 V | 0 | 31 | 0 | 21 | 0 | 25 | |
| | | | 6 V | 0 | 36 | 0 | 25 | 0 | 29 | |
| $t_w$ | Pulse duration | SRCLK or RCLK high or low | 2 V | 80 | | 120 | | 100 | | ns |
| | | | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 17 | | |
| | | $\overline{\text{SRCLR}}$ low | 2 V | 80 | | 120 | | 100 | | |
| | | | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 17 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | SRCLK↑ before RCLK↑† | 2 V | 75 | | 113 | | 94 | | |
| | | | 4.5 V | 15 | | 23 | | 19 | | |
| | | | 6 V | 13 | | 19 | | 16 | | |
| | | $\overline{\text{SRCLR}}$ low before RCLK↑ | 2 V | 50 | | 75 | | 65 | | |
| | | | 4.5 V | 10 | | 15 | | 13 | | |
| | | | 6 V | 9 | | 13 | | 11 | | |
| | | $\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑ | 2 V | 50 | | 75 | | 60 | | |
| | | | 4.5 V | 10 | | 15 | | 12 | | |
| | | | 6 V | 9 | | 13 | | 11 | | |
| $t_h$ | Hold time, SER after SRCLK↑ | | 2 V | 0 | | 0 | | 0 | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | |
| | | | 6 V | 0 | | 0 | | 0 | | |

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 2 V | 6 | 26 | | 4.2 | | 5 | | MHz |
| | | | 4.5 V | 31 | 38 | | 21 | | 25 | | |
| | | | 6 V | 36 | 42 | | 25 | | 29 | | |
| $t_{pd}$ | SRCLK | $Q_H$ | 2 V | | 50 | 160 | | 240 | | 200 | ns |
| | | | 4.5 V | | 17 | 32 | | 48 | | 40 | |
| | | | 6 V | | 14 | 27 | | 41 | | 34 | |
| | RCLK | $Q_A$–$Q_H$ | 2 V | | 50 | 150 | | 225 | | 187 | |
| | | | 4.5 V | | 17 | 30 | | 45 | | 37 | |
| | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_H$ | 2 V | | 51 | 175 | | 261 | | 219 | ns |
| | | | 4.5 V | | 18 | 35 | | 52 | | 44 | |
| | | | 6 V | | 15 | 30 | | 44 | | 37 | |
| $t_{en}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | 2 V | | 40 | 150 | | 225 | | 187 | ns |
| | | | 4.5 V | | 15 | 30 | | 45 | | 37 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| $t_{dis}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | 2 V | | 42 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 20 | 34 | | 51 | | 43 | |
| $t_t$ | | $Q_A$–$Q_H$ | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |
| | | $Q_H$ | 2 V | | 28 | 75 | | 110 | | 95 | |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

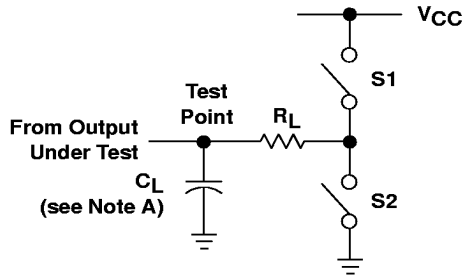
**switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | RCLK | $Q_A$–$Q_H$ | 2 V | | 60 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 22 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| $t_{en}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | 2 V | | 70 | 200 | | 298 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| $t_t$ | | $Q_A$–$Q_H$ | 2 V | | 45 | 210 | | 315 | | 265 | ns |
| | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | 6 V | | 13 | 36 | | 53 | | 45 | |

**operating characteristics, $T_A$ = 25°C**

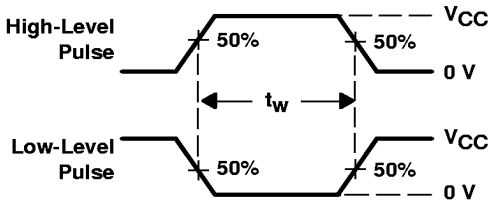
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 400 | pF |

## PARAMETER MEASUREMENT INFORMATION

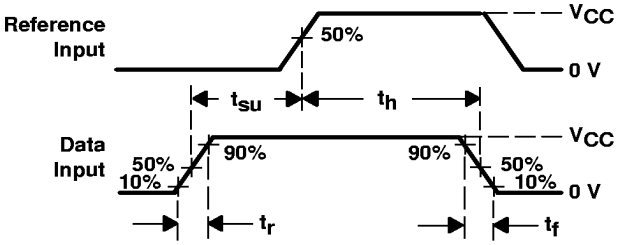



LOAD CIRCUIT

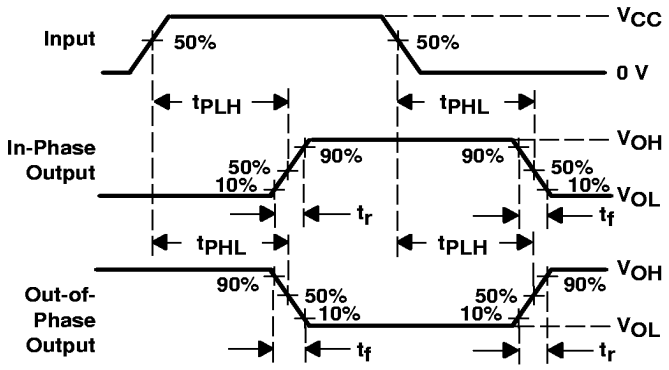
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | — | 50 pF or 150 pF | Open | Open |



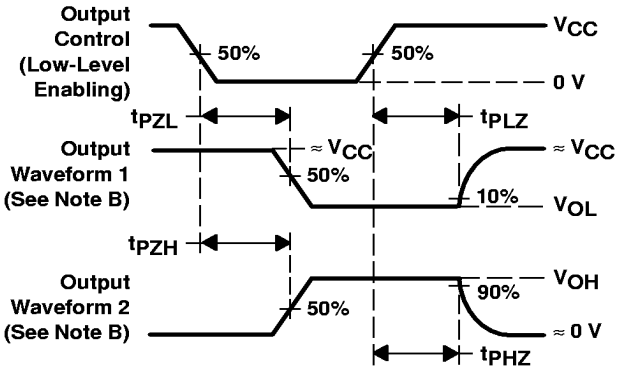

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**