F-MOD - 300 MHz[1] to 4000 MHz Quadrature Modulator Family

Preliminary Technical Data **ADL5373/ADL5374**

FEATURES

Output frequency range: 300 MHz[1] to 4000 MHz
Modulation bandwidth: >500 MHz (3 dB)
1 dB output compression: 12 dBm @ 2140 MHz
Noise floor: -158 dBm/Hz
Sideband Suppression: < -40 dBc
LO Leakage: < - 40 dBm
Single supply: 4.75 V to 5.5 V
24-Lead LFCSP package

APPLICATIONS

Cellular/PCS communication systems infrastructure
WCDMA/CDMA2000/GSM/EDGE, WiMax
Wi-Max/broadband wireless access systems

[1] 300 MHz to 1000 MHz, 600 MHz to 1300 MHz, and 1500 MHz to 2500 MHz coverage provided by the already-released ADL5370, ADL5371 and ADL5372 members of the family respectively. Refer to the Rev0 datasheets available at www.analog.com for more information.

FUNCTIONAL BLOCK DIAGRAM

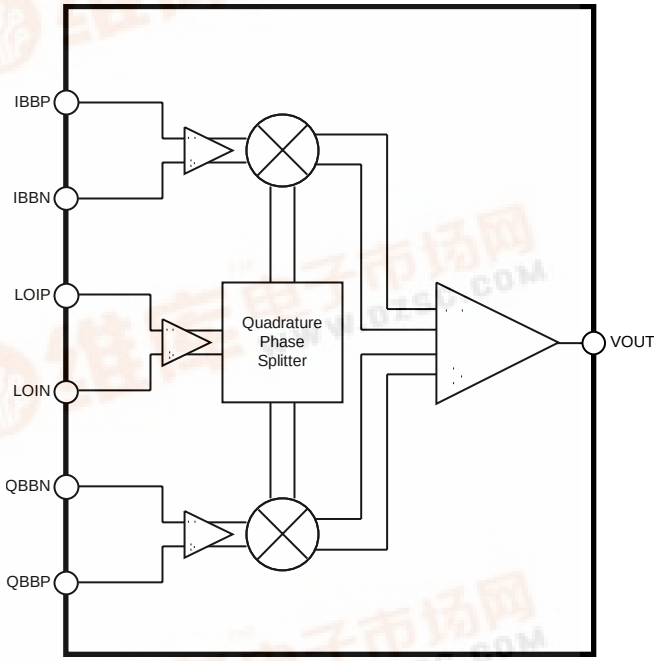

Figure 1.

PRODUCT DESCRIPTION

The F-MOD family of monolithic, RF quadrature modulators is designed for use from 300 MHz to 4000 MHz. Excellent phase accuracy and amplitude balance enable high performance direct RF modulation for communication systems..

The F-MOD family can be used as direct-to-RF modulators in digital communication systems such as GSM, CDMA, and WCDMA base stations, and QPSK or QAM broadband wireless access transmitters. A 3 dB baseband bandwidth in excess of 500 MHz makes it ideal in broadband Zero-IF or Low-IF-to-RF applications and in broadband Digital Pre-Distortion transmitters.

The F-MOD family is fabricated using Analog Devices' advanced Silicon-Germanium bipolar process, and are available in a 24-lead exposed-paddle LFCSP package. Performance is specified over a –40°C to +85°C temperature range.

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SPECIFICATIONS

Table 1. V_S = 5 V; T_A = 25°C; LO = 0 dBm[1] single-ended; Baseband I/Q Amplitude = 1.4 V p-p differential sine waves in quadrature with a 500 mV dc bias; Baseband I/Q Frequency (f_{BB}) = 1 MHz, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Operating Frequency Range	Frequency Range covered by F-Mod family				MHz
	Low Frequency		300		
	High Frequency		4000		MHz
ADL5373	LO = 2500 MHz				
Operating Frequency Range					
	Low Frequency (3dB Bandwidth)		2300		MHz
	High Frequency		3000		MHz
Output Power	V_{IQ}=1.4Vpp differential		6.5		dBm
Output P1 dB			13		dBm
Carrier Feedthrough			-34.5		dBm
Sideband Suppression			-33.3		dBc
Second Harmonic	$P_{OUT} - (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-48.8		dBc
Third Harmonic	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-45.4		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -3 dBm per tone		25		dBm
Noise Floor	Baseband inputs biased to 500 mV, P_{LO} = +6 dBm		-156		dBm/Hz
ADL5374	LO = 3500 MHz				
Operating Frequency Range					
	Low Frequency (3 dB Bandwidth)		2800		MHz
	High Frequency		4000		MHz
Output Power	V_{IQ}=1.4Vpp differential		4.8		dBm
Output P1 dB			11		dBm
Carrier Feedthrough			-32.1		dBm
Sideband Suppression			-35.9		dBc
Second Harmonic	$P_{OUT} - (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-36.9		dBc
Third Harmonic	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-43.1		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -3 dBm per tone		21.5		dBm
Noise Floor	Baseband inputs biased to 500 mV, P_{LO} = +6 dBm		-155		dBm/Hz
LO INPUTS					
LO Drive Level[1]	Characterization performed at typical level	-3	0	3	dBm
Nominal Impedance			50		Ω
Input Return Loss				-10	dB
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level		400	500	600	mV
Bandwidth (3 dB)			>500		MHz
POWER SUPPLIES	Pins VPS1 and VPS2				
Voltage		4.75		5.5	V
Supply Current	ADL5371, ADL5372, ADL5373, ADL5374		175		mA

Notes

1 LO drive in excess of +3 dBm can be provided to further reduce noise at 6 MHz and 20 MHz carrier offsets in GSM and WCDMA applications respectively.

ABSOLUTE MAXIMUM RATINGS

Table 2. F-MOD Absolute Maximum Ratings

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V to 2 V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1155 mW
θ_{JA} (Exposed Paddle Soldered Down)	54°C/W
Maximum Junction Temperature	147°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

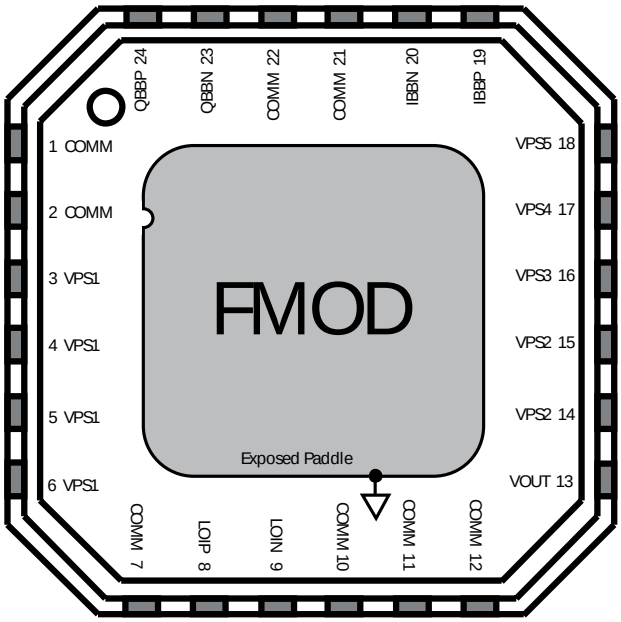


Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 7, 10 to 12, 21, 22	COM1, COM2, COM3, COM4	Input Common Pins. Connect to ground plane via a low impedance path.
3 to 6, 14 to 18	VPS1, VPS2, VPS3, VPS4, VPS5	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see Figure 3).
19, 20, 23, 24	IBBP, IBBN, QBBN, QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to 500 mV dc, and must be driven from a low-impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin. This results in a differential drive of 1.4 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased.
8, 9	LOIP, LOIN	50 Ω Single-Ended Local Oscillator Input. Internally dc-biased. Pins must be ac-coupled. AC-couple LOIN to ground and drive LO through LOIP.
13	VOUT	Single-Ended Device RF Output. Pin should be ac-coupled to the load.
	Exposed Paddle	The device package has an exposed paddle on the underside. This exposed paddle must be soldered to a low impdeance ground pad on the board . If the pcb has multiple ground planes, these should be stitched together with vias to optimize thermal conductivity (see drawing of evalution board top layer in Figure 16).

BASIC CONNECTIONS

Figure 3 shows the basic connections for the F-MOD.

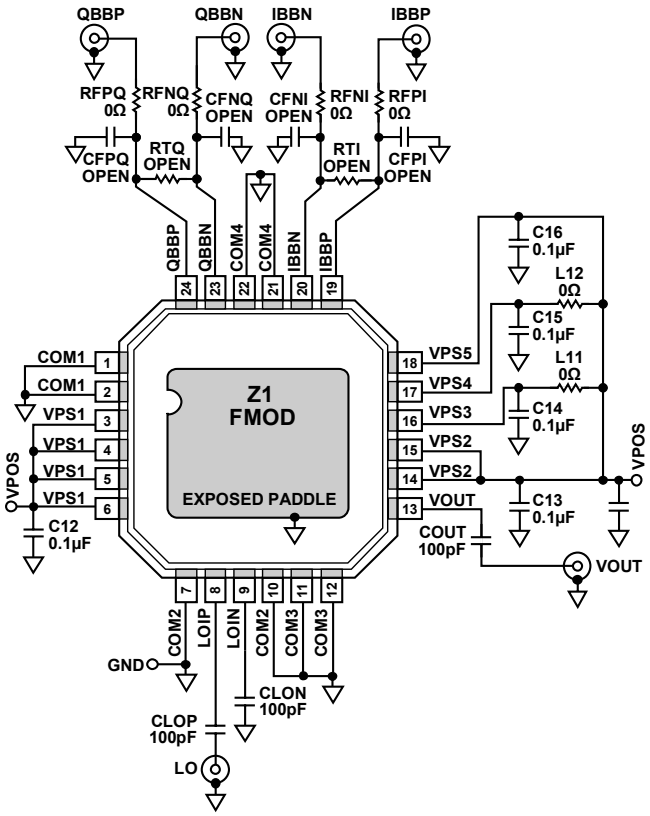


Figure 3. Basic Connections for the F-MOD

Power Supply and Grounding

All the VPS pins must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled with a 0.1 µF capacitor. These capacitors should be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1 pin, COM2 pin, and COM3 pin should be tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. The Analog Devices AN-772 application note discusses the thermal and electrical grounding of the LFCSP_VQ in greater detail.

Baseband Inputs

The baseband inputs QBBP, QBBN, IBBP, and IBBN must be driven from a differential source. The nominal drive level of 1.4 V p-p differential (700 mV p-p on each pin) should be biased to a common-mode level of 500 mV dc.

The dc common-mode bias level for the baseband inputs may range from 400 mV to 600 mV. This results in a reduction in the usable input ac swing range. The nominal dc bias of 500 mV allows for the largest ac swing, limited on the bottom end by the F-MOD input range and on the top end by the output compliance range on most digital-to-analog converters (DAC) from Analog Devices.

LO Input

A single-ended LO signal should be applied to the LOIP pin through an ac-coupling capacitor. The recommended LO drive power is 0 dBm. The LO return pin, LOIN, should be ac-coupled to ground through a low impedance path.

The nominal LO drive of 0 dBm can be increased to up to 7 dBm.

RF Output

The ground-referenced RF output is available at the VOUT pin (Pin 13). This pin should be ac-coupled to the load.

EVALUATION BOARD

Populated RoHS-compliant evaluation boards are available for evaluation of the F-MOD. The F-MOD package has an exposed paddle on the underside. This exposed paddle must be soldered to the board.The evaluation board is designed without any components on the underside so heat can be applied to the underside for easy removal and replacement of the F-MOD.

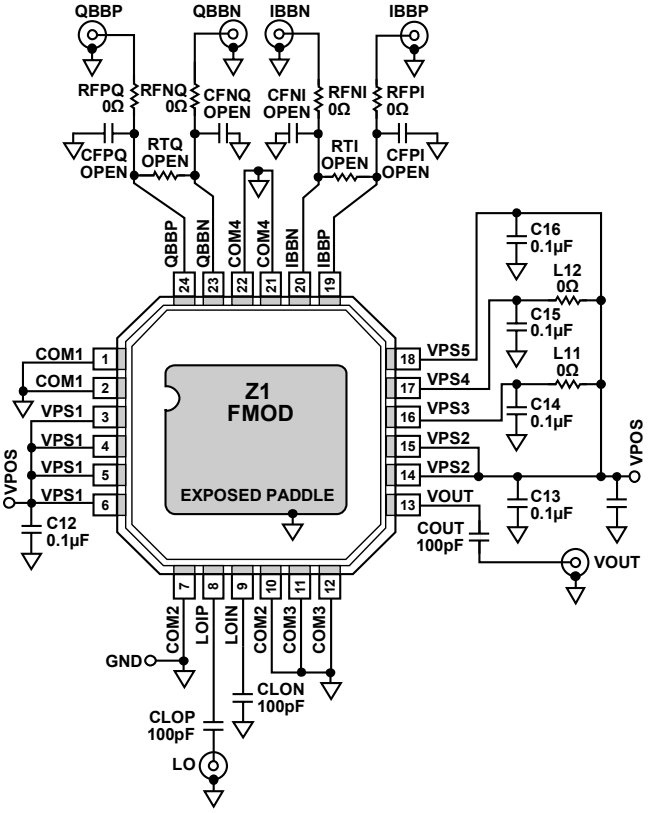


Figure 4. F-MOD Evaluation Board Schematic

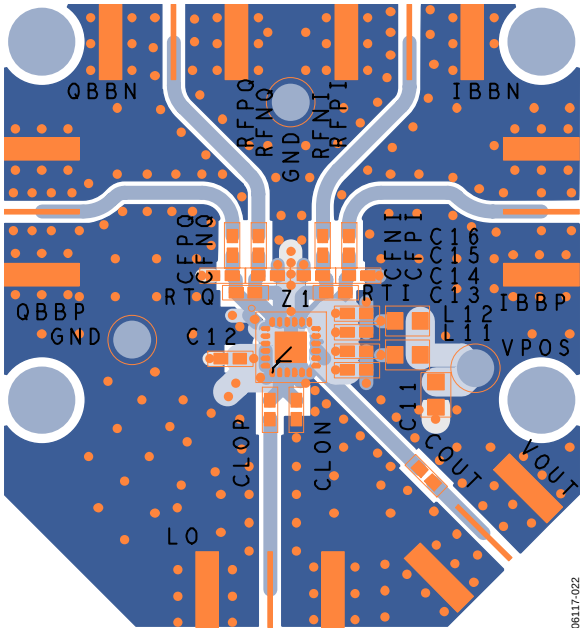
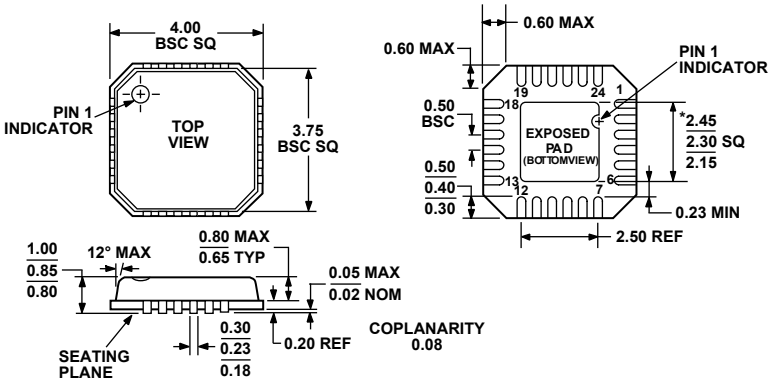


Figure 5. Evaluation Board Layout, Top Layer.

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Power Supply and Ground Clip Leads.	Not applicable
RFPI, RFNI, RFPQ, RFNQ, CFPI, CFNI, CFPQ, CFNQ, RTQ, RTI	Baseband Input Filters. These components can be used to implement a low-pass filter for the baseband signals.	RFNQ, RFPQ, RFNI, RFPI = 0 Ω (0402) CFNQ, CFPQ, CFNI, CFPI = Open (0402) RTQ, RTI = Open (0402)

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 6. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range (°C)	Package Description	Package Option
ADL5370ACPZ-R7[1]	–40 to +85	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2
ADL5370ACPZ-WP[1]	–40 to +85	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2
ADL5370-EVALZ[1]		Evaluation Board	
ADL5371ACPZ-R7[1]	–40 to +85	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2
ADL5371ACPZ-WP[1]	–40 to +85	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2
ADL537-EVALZ[1]		Evaluation Board	
ADL5372ACPZ-R7[1]	–40 to +85	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2
ADL5372ACPZ-WP[1]	–40 to +85	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2
ADL5372-EVALZ[1]		Evaluation Board	
ADL5373ACPZ-R7[1]	–40 to +85	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2
ADL5373ACPZ-WP[1]	–40 to +85	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2
ADL5373-EVALZ[1]		Evaluation Board	
ADL5374ACPZ-R7[1]	–40 to +85	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-2
ADL5374ACPZ-WP[1]	–40 to +85	24-Lead LFCSP_VQ, Waffle Pack	CP-24-2
ADL5374-EVALZ[1]		Evaluation Board	

[1] Z indicates Pb-free

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