Wideband high frequency amplifier

5205

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)
- No external components required
- Input and output impedances matched to 50/75Ω systems

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Fiber optics
- Modems
- Mobile radio
- Telecommunications

DESCRIPTION

The 5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz. The 5205 operates with a single supply of 6V, and only draws 33mA of supply current which is much less than comparable hybrid parts. The noise figure is typically 4.8dB in a 75Ω system and 6dB in a 50Ω system.

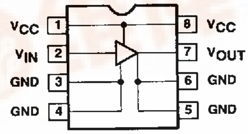
Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to fuse high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The 5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50Ω or 75Ω input and output impedances. The Standing Wave Rations in 50Ω and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 400MHz operating range.

No external components are needed other than AC coupling capacitors because the 5205 is internally compensated and matched to 50Ω and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz (typical values).

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional 5205s in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
8-Pin Ceramic DIP	5205/BPA	GDIP1-T8

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_I	AC input voltage	5	V_{PP}
T_{STG}	Storage temperature range	-65 to +150	°C

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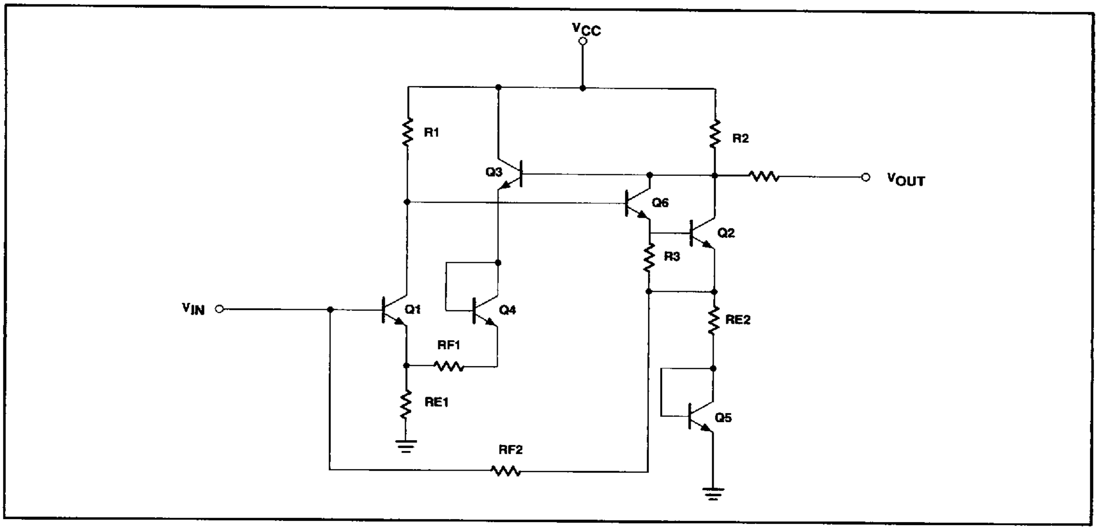
EQUIVALENT SCHEMATIC



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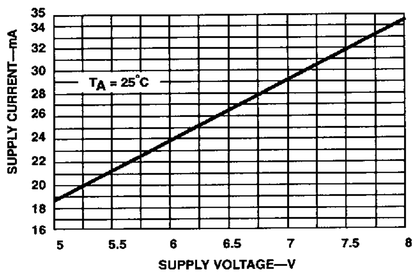

Figure 1. Supply Current vs Supply Voltage

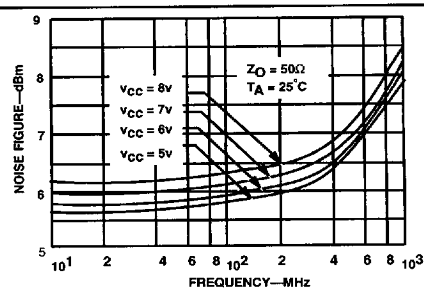

Figure 2. Noise Figure vs Frequency

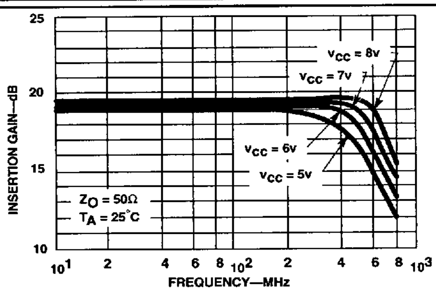

Figure 3. Insertion Gain vs Frequency (S_{21})

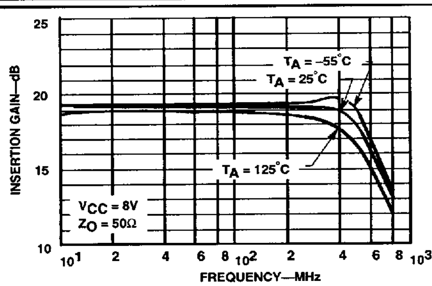

Figure 4. Insertion Gain vs Frequency (S_{21})

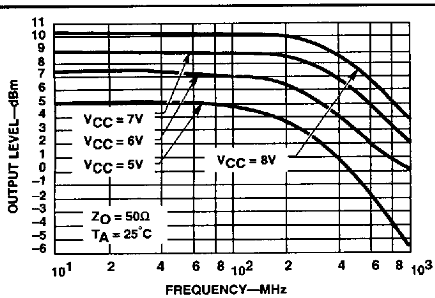

Figure 5. Saturated Output Power vs Frequency

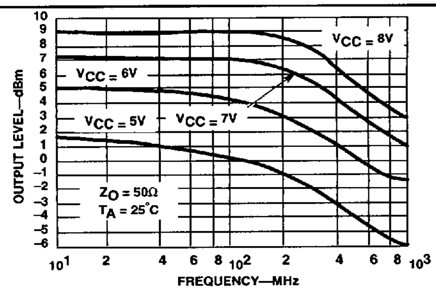

Figure 6. 1dB Gain Compression vs Frequency

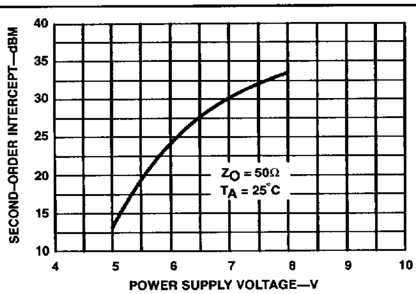

Figure 7. Second-Order Output Intercept vs Supply Voltage

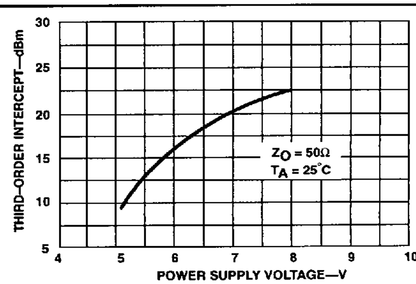

Figure 8. Third-Order Intercept vs Supply Voltage

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5205

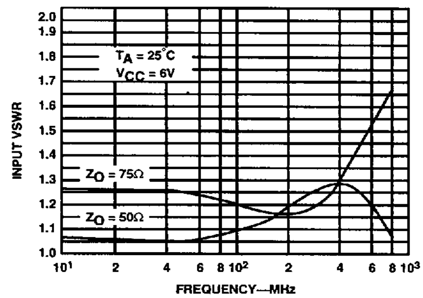


Figure 9. Input VSWR vs Frequency

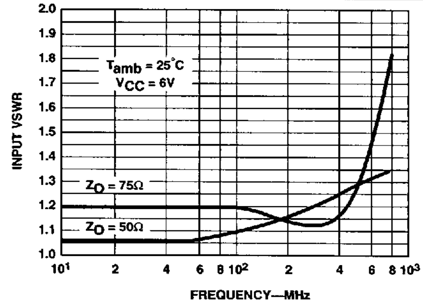


Figure 10. Output VSWR vs Frequency

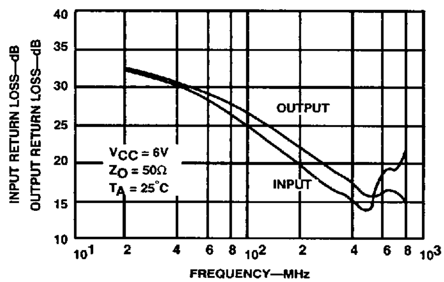


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

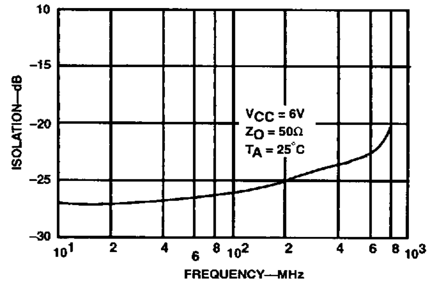


Figure 12. Isolation vs Frequency (S_{12})

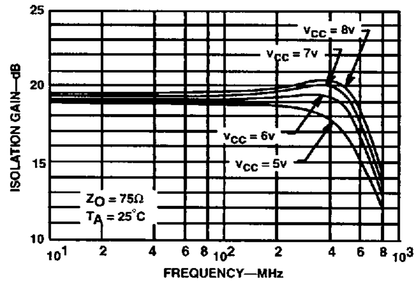


Figure 13. Insertion Gain vs Frequency (S_{21})

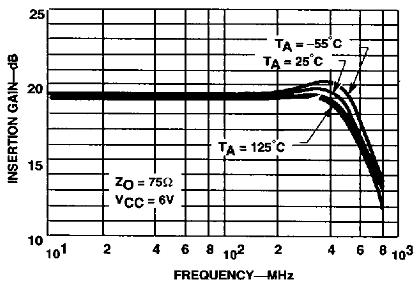


Figure 14. Insertion Gain vs Frequency (S_{21})

ELECTRICAL CHARACTERISTICS

V_{CC} = 6V, $Z_S = Z_L = Z_O$ = 50Ω, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 6.0V	20	24	32	19		33	mA
S_{21}	Insertion gain	f = 100MHz	17	19	21	16.5		21.5	dB
S_{11}	Input return loss[1, 2]	1 to 400MHz	12	29					dB
S_{11}	Input return loss[1]	1 to 300MHz				9			dB
S_{22}	Output return loss[1, 2]	1 to 400MHz	12	27					dB
S_{22}	Output return loss[1]	1 to 300MHz				9			dB
S_{12}	Isolation[1, 2]	1 to 400MHz	-18	-25					dB
S_{12}	Isolation[1]	1 to 300MHz				-18			dB
B_W	Bandwidth	±0.5dB		300					MHz
B_W	Bandwidth	-3dB	400	550		300			MHz
E_N	Noise figure	f = 100MHz		4.8					dB
E_N	Noise figure	f = 100MHz		6.0					dB
P_{SAT}	Saturated output power	f = 100MHz		+7.0					dBm
P_{SAT}	1dB gain compression	f = 100MHz		+4.0					dBm
IM_2	Second-order intermodulation intercept (output)	f = 100MHz		+24					dBm
IM_3	Third-order intermodulation intercept (output)	f = 100MHz		+17					dBm

NOTES:
1. This parameter/test condition is guaranteed but not tested.
2. Typical value is for 100MHz operation.

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wideband gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_O}{V_1} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\log\left\{1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_o}\right]\right\} dB$$

where I_{C1} = 5.5mA, R_{E1} = 12Ω, r_B = 130Ω, KT/q = 26mV at 25°C and R_O = 50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_1 can be determined by the equation:

$$V_1 = V_{BE1} + (I_{C1} + I_{C3})R_{E1} \qquad (3)$$

where R_{E1} = 12Ω, V_{BE} = 0.8V, I_{C1} = 5mA and I_{C3} = 7mA (currents rated at V_{CC} = 6V).

Under the above conditions, V_I is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. the value of R_{F1} = 140Ω is chosen to give the desired nominal gain. The DC output voltage V_O can be determined by:

$$V_O = V_{CC} - (I_{C2} + I_{C6}) R_2 \qquad (4)$$

where V_{CC} = 6V, R_2 = 225Ω, I_{C2} = 7mA and I_{C6} = 5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bandwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package. With this in mind, the following equation can be used to estimate the die temperature:

$T_J = T_{amb} + (P_D \times O_{JA})$

where T_{amb} = Ambient Temperature, T_J = Die Temperature, P_D = Power Dissipation = $I_{CC} \times V_{CC}$, O_{JA} = Package Thermal Resistance.

At the nominal supply voltage of 6V, the typical supply current is 25mA (33mA Max).

For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications.

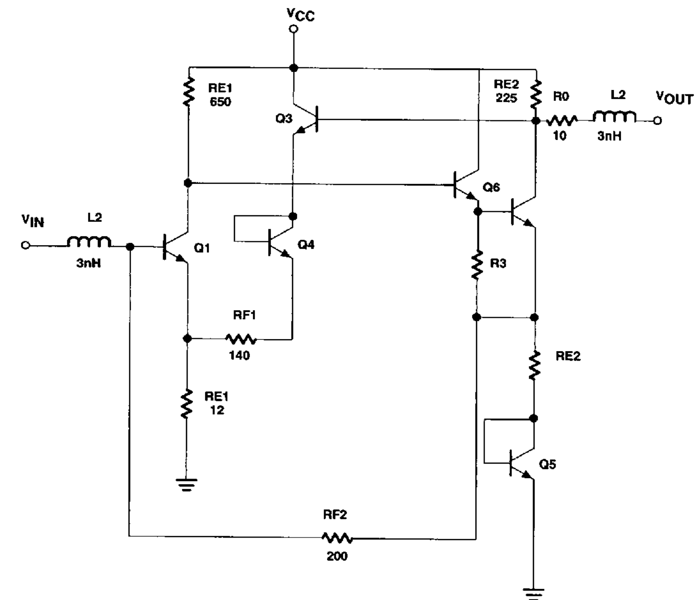


Figure 15. Schematic Diagram

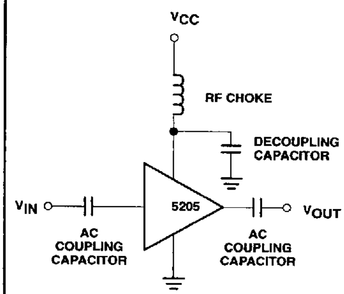


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

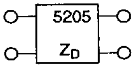
PC BOARD MOUNTING

In order to realize satisfactory mounting of the 5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC Bias on the output of the amplifier will be loaded down causing loss of output power. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_I = Z_O$ for the 5205

$P_I = \frac{V_I^2}{Z_D}$



$P_O = \frac{V_O^2}{Z_D}$

$$\frac{P_O}{P_I} = \frac{\frac{V_O^2}{Z_D}}{\frac{V_I^2}{Z_D}} = \frac{V_O^2}{V_I^2} = P_1$$

$P_I = V_I^2$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the 5205 = $|S_{21}|^2 = 100$

$$P_I = \frac{P_O}{P_I} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_O}{V_I} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

INPUT RETURN LOSS = S_{11} dB
$S_{11} \text{ dB} = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22} dB
$S_{22} \text{ dB} = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 18. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. these relationships are as follows:

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, and indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship ratio is illustrated in Figure 19, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_O + IMR_2$

$IP_3 = P_O + IMR_3/2$

where P_O is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operation range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the 5205 we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to:

- **High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.**
- **S-Parameter Techniques for Faster, More Accurate Network Design, H.P. App Note 95-1, Richard W. Anderson, 1967, HP Journal.**
- **S-Parameter Design, H.P. App Note 154, 1972.**

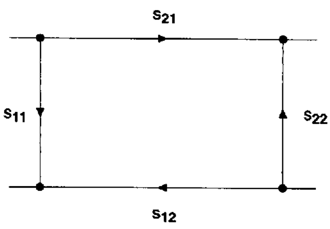
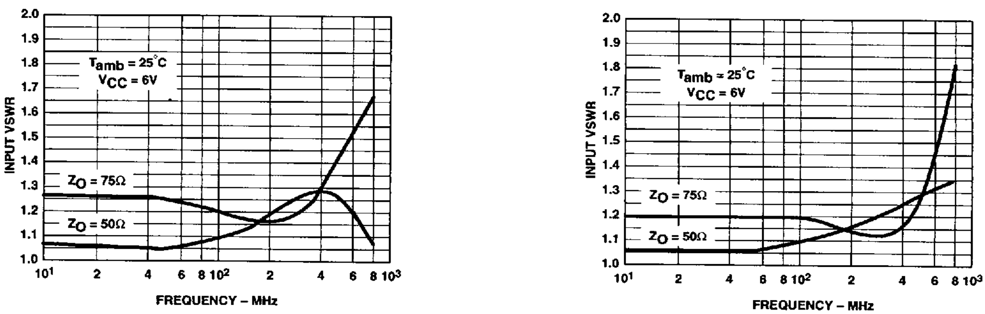


Figure 17. Two-Port Network Defined



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 18.

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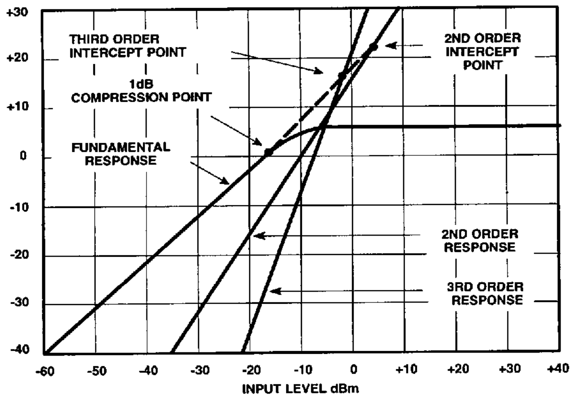

Figure 19. Output dBm vs Input dBm