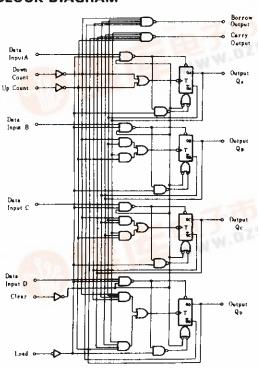
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; That is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been

provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

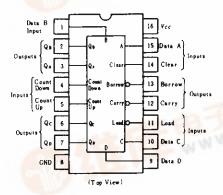
The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists.

The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

■BLOCK DIAGRAM



MPIN ARRANGEMENT

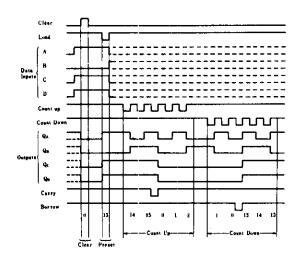


MRECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	
Clock frequency	frlack	0	-	25	MHz	
Pulse width	lu	20	_	_	ns	
Setup time (Clear)	fautclear)	40	_	_	ns	
Setup time	Lou	20	_	-	ns	
Hold time	th	3	_	-	ns	



ECOUNT SEQUENCES



Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to binary thirteen.
- 3. Count up to fourteen, fifteen, carry, zero, one, and two.
- Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75^{\circ}C$)

Item	Symbol	Test Conditions			typ*	max	Unit
Innua malanan	Vin		2.0	_	_	v	
Input voltage	VIL				_	0.8	v
Output voltage	Voн	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}, I_C$	2.7	-	_	V	
	Vol	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}$	$I_{OL} = 4 \text{mA}$	_	_	0.4	v
	VOL	VCC=4.75V, VIH=2V, VIL=0.8V	IoL = 8mA	_		0.5	·
Input current	IIH	$V_{CC} = 5.25 \text{V}, V_I = 2.7 \text{V}$		_	20	μA	
	IIL	$V_{CC} = 5.25 \text{V}, V_I = 0.4 \text{V}$		_	-0.4	mA	
	Ti Ii	$V_{CC} = 5.25 \text{V}, V_I = 7 \text{V}$		-	_	0.1	mА
Short-circuit output current	los	$V_{CC} = 5.25 \text{V}$	····	- 20	-	-100	mA
Supply current**	I cc	Vcc = 5.25 V			19	34	mA
Input clamp voltage	VIK	$V_{CC} = 4.75 \text{V}, I_{IN} = -18 \text{mA}$		_	-	-1.5	V

^{*} VCC=5V, Ta=25°C

ESWITCHING CHARACTERISTICS (Vcc = 5V, $Ta = 25^{\circ}C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	fmax				25	32		MHz
Propagation delay time	t PLH	Count-up	Carry	$C_L = 15 \text{pF}$ $R_L = 2 \text{k}\Omega$	_	17	26	ns
	ŧрні.					18	24	ns
	t PLH	Count-down	B			16	24	ns
	teni,	Count-down	Borrow		_	15	24	ns
	tplh	Either Count	Q			27	38	ns
	tphl				_	30	47	ns
	tpl.H				_	24	40	ns
	IPHL	Load	Q		-	25	40	ns
	tphi.	Clear	Q		_	23	35	ns

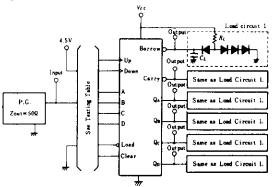


^{**} ICC is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

HD74LS193

TESTING METHOD

1) Test Circuit

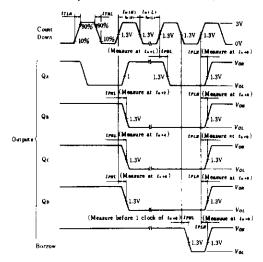


Notes) 1. C_L includes probe and jig capacitance.

2. All diodes are 1S2074 (B)

Input pulse: t_{TLH}, t_{THL}≤7ns
Duty Cycle≤50%, PRR=500kHz (Data input)
PRR=1MHz (except data input)

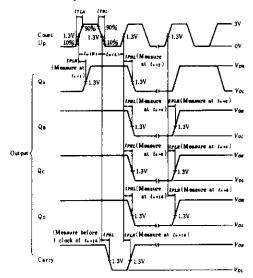
Waveform-2 fmax, tPLH, tPHL (Count Down)



Notes) 1. Input pulse: $t_{TLH} \le 7 \text{ns}$, $t_{THL} \le 7 \text{ns}$, PRR = 1 MHz, duty

- 2. for f_{max} , t_{TLH} , $t_{THL} \le 2.5$ ns
- 3. t_n is reference bit time when all outputs are high.

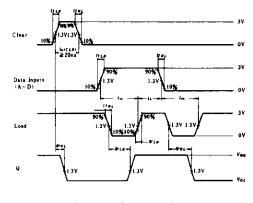
Waveform-1 fmax, tPLH, tPHL (Count Up)



Notes) 1. for f_{max} , $t_{TLH} = t_{THL} \le 2.5$ ns.

2. t_n is reference bit time when all outputs are low.

Waveform-3 tPLH, tPHL (Load, Clear→Q)

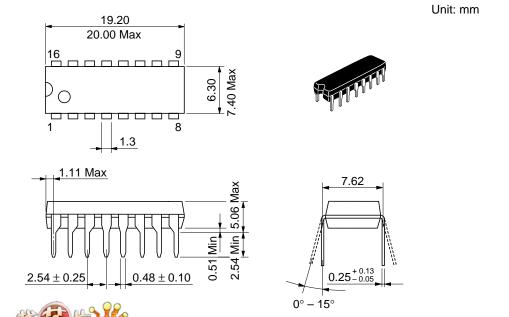


Note) Input pulse: $t_{TLH} \le 7 \text{ns}$, $t_{THL} \le 7 \text{ns}$

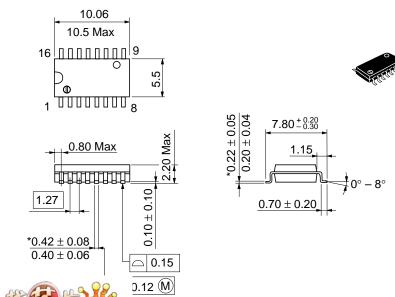
2) Testing Table

_	From input	Inputs							Outputs						
Item	to output	CLR	Load	Up	Down	A	В	С	D	QA	Qв	Qc	QD	Carry	Воггом
fmax	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	out	OUT	OUT	_
	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT		OUT
1	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	
t PLH	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	-	OUT
tphi.	Load→Q	GND	IN	GND	GND	IN	IN	IN	IN	OUT	OUT	OUT	OUT	_	-
	Clear→Q	IN	IN.	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	_	

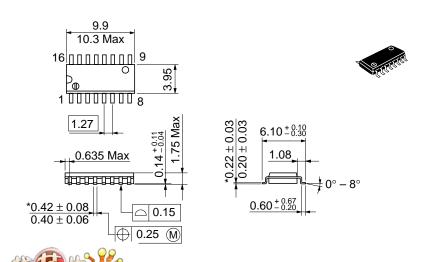
[•] for initialized







Unit: mm



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