



**ANALOG
DEVICES**

Complete, Voltage Output 12-Bit Buffered DAC

AD3860

1.1 Scope.

This specification covers the detail requirements for a hybrid, buffered, digital-to-analog converter with voltage output.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD3860SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-24B.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Single Voltage $+V_S$		+18 V max
$-V_S$		-18 V max
$+V_{\text{LOGIC}}$		+7 V max
V_{IN} Digital V_{INL}		0 to $+V_{\text{LOGIC}}$
Short Circuit Protection to GND		Continuous
Storage Temperature Range		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10 sec)		$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 8^\circ\text{C/W}$
θ_{JA}	$= 25^\circ\text{C/W}$



AD3860 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C (–55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1	2.0 (2.0)					V min
Digital Input Low Voltage	V _{IL}	–1	0.8 (0.8)					V max
Digital Input High Current	I _{IH}	–1	30 (30) 60 (60)			30	Data Inputs @ 2.0 V Register Input @ 2.0 V	μA max
Digital Input Low Current	I _{IL}	–1	600 (600) 1200 (1200)			600	Data Inputs @ 0.8 V Register Enable @ 0.8 V	μA max
Gain Error	A _E	–1	0.1	0.1			V _O = +FS, ±10 V Range	±% FSR max
Gain Error Temperature Coefficient	TCA _E	–1	(0.3)		0.3		V _O = +FS, ±10 V Range	±% FSR max
Unipolar Gain Error	V _{UGE}	–1	0.1	0.1			V _O = +FS 0 to 10 V Range	±% FSR max
Unipolar Gain Drift	V _{UGD}	–1	(0.3)		0.3		V _O = +FS 0 to 10 V Range	±% FSR max
Unipolar Offset Error	V _{OS}	–1	0.05	0.05			V _O = 0 V, ±10 V Range	±% FSR max
Unipolar Offset Error Temperature Coefficient	TCV _{OS}	–1	(0.1)		0.1		Over Operating Temperature	±% FSR max
Bipolar Gain Error	V _{BGE}	–1	0.1	0.1			V _O = ±FS, ±10 V Range	±% FSR max
Bipolar Gain Drift	V _{BGD}	–1	(0.3)		0.3		V _O = +FS, ±10 V Range	±% FSR max
Bipolar Offset Error	B _{POS}	–1	0.05	0.05			V _O = –FS, ±10 V Range	±% FSR max
Bipolar Offset Error Temperature Coefficient	TCB _{POS}	–1	(0.1)		0.1		V _O = –FS, ±10 V Range	±% FSR max
Bipolar Zero Error	B _{PZ}	–1	0.1				V _O = 0 V, ±10 V Range	±% FSR max
Bipolar Zero Error Temperature Coefficient	TCP _{PZ}	–1	(0.3)				V _O = 0 V, ±10 V Range	±% FSR max
Integral Nonlinearity	L _E	–1	1/2 (1/2)	1/2	1/2		Linearity ±10 V Range	±LSB max
Differential Nonlinearity Error	D _{LE}	–1	1 (1)	1	1		Monotonic Over Temperature	±LSB max
Output Voltage Range, Ideal	V _{OUT}	–1	+9.9952 (9.9952) –10.000 (–10.000)				±10 V Range	V Ideal
Output Current	I _{OUT}	–1	5.0 (5.0)			5.0	±10 V Range C _L = 250 pF, R _L = 2 kΩ	mA min
Input Resistance	R _{IN}	–1	N/A					
Reference Output Voltage Error	V _{REFER}	–1	126 126	126 126			Error @ No Load Error @ 2.5 mA Load	±mV max
Reference Output Voltage ² Temperature Coefficient	TCV _{REF}	–1	(126) (126)		126 126		Error @ No Load Error @ 2.5 mA Load	±mV max
Reference Output Current	I _{REF}	–1	2.5				For External Use	mA min
Slew Rate	V _{SL}	–1	10 (10)				±10 V Range	V/μs min
Output Voltage Settling Time	t _{SL}	–1	7 (7) 5 (5)				±10 V Range, 20 V Step ±5 V Range, 10 V Step	μs max
DC Feedthrough Error	FTE	–1	1	1			Latch @ +FS then Change to Offset	±mV max
DC Feedthrough Error Over Temperature	TCFTE	–1	(1)		1		Latch @ +FS then Change to Offset	±mV max

Table 1. (Continued on next page)

REV. C



Test	Symbol	Device	Design Limit @ +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Output Short Circuit Current	I _{SC}	-1	25 (25)					mA max
Power Supply Rejection Ratio	PSRR	-1	0.01 0.004	0.01 0.004	0.01 0.004		+15 V, ±0.5 V -15 V, ±0.5 V	±% FSR/% V _S max
Power Supply Current	I _{CC} I _{EE} I _{DD}	-1	+20 (+20) -30 (-30) +50 (+50)	+20 -30 +50	+20 -30 +50		+15 V _{CC} -15 V _{EE} +5 V _{LOGIC}	mA max
Power Dissipation	P _D	-1	1000 (1000)					mW max
Write Pulse Width	t _{NEPW}	-1	60					ns min
Data Setup Time	t _{SDE}	-1	40					ns min
Data Hold Time	t _{DH}	-1	10					ns min

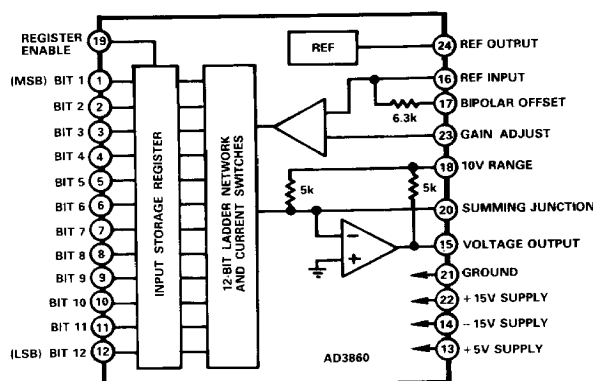
NOTES

¹Specified and tested at +25°C, ±15 V, +5 V, ±10 V range, no load conditions, internal reference unless noted otherwise in the table.

²V_{REF} = +6.300 V.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

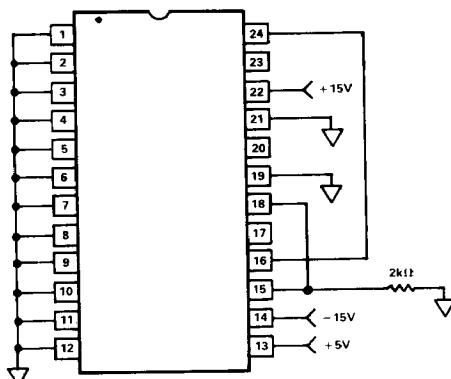


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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6.0 Output Range.

The analog input range is as specified in Table 2 when externally connected as shown in Table 3 below. The output range must be limited to ± 5 V full scale when operated with ± 12 V supplies.

OUTPUT VOLTAGE RANGE SELECTION

Output Range	0 to +10 V	± 5 V	± 10 V
Pin Connection			
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	NC
Connect Pin 20 to	NC	17	17

Table 2.

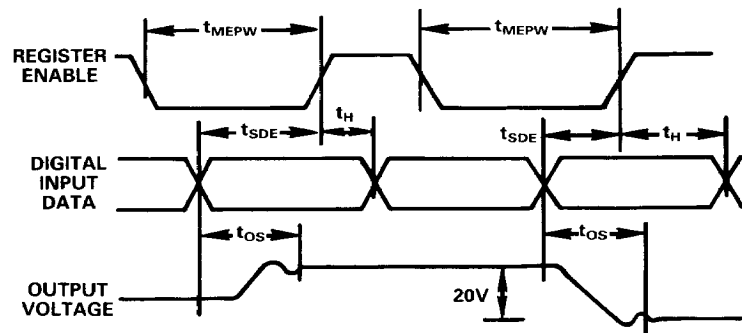
INPUT LOGIC CODING

Digital Input MSB LSB	Analog Output		
	0 to +10 V	± 5 V	± 10 V
0000 0000 0000	+9.9976 V	+4.9976 V	+9.9951 V
0000 0000 0001	+9.9951 V	+4.9951 V	+9.9902 V
0111 1111 1111	+5.0000 V	0.0000 V	0.0000 V
1000 0000 0000	+4.9976 V	-0.0024 V	-0.0049 V
1111 1111 1110	+0.0024 V	-4.9976 V	-9.9951 V
1111 1111 1111	0.0000 V	-5.0000 V	-10.0000 V

CODING NOTES:

1. For unipolar operation, the coding is complementary straight binary (CSB).
2. For bipolar operation, the coding is complementary offset binary (COB).
3. For FSR = 20 V, 1 LSB = 4.88 mV.
4. For FSR = 10 V, 1 LSB = 2.44 mV.

Table 3.



TIMING NOTES:

- t_{MEPW} MINIMUM ENABLE PULSE WIDTH IS 60 ns.
- t_{SDE} MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40 ns.
- t_H HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA AND IS 10 ns.
- t_{OS} OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO $\pm 1/2$ LSB IS 7 μ s MAX.

Figure 1. Input Register Timing Diagram

