ANALOG DEVICES

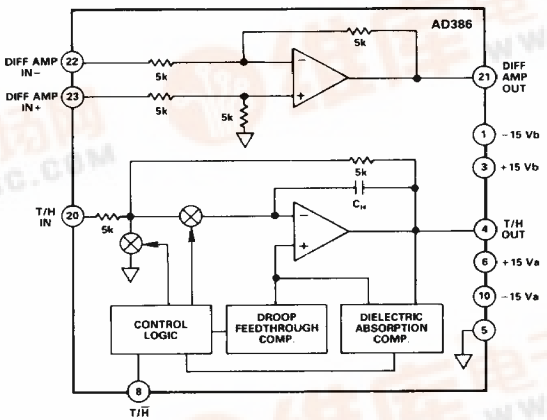
True 16-Bit Track-and-Hold Amplifier

AD386

FEATURES
Companion to True 16-Bit A/D Converters
16-Bit Linear (−40°C to +85°C)
14-Bit Linear (−55°C to +125°C)
Fast Acquisition Time: 3.6 μs to 0.00076%
Low Droop Rate: 20 μV/ms
Differential Amplifier for Ground Sense
Low Aperture Jitter: 40 ps

APPLICATIONS
Medical and Analytical Instrumentation
Signal Processing
Multichannel Data Acquisition Systems
Automatic Test Equipment
Guidance and Control
Sonar

FUNCTIONAL BLOCK DIAGRAM

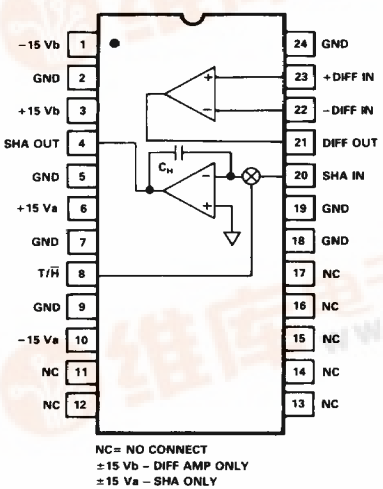


PRODUCT DESCRIPTION

The AD386 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (3.6 μs to 75 μV) and low aperture jitter (40 ps) make it ideal for use with fast A/D converters.

The AD386 is complete with an internal hold capacitor, and it incorporates a compensation network which minimizes the track-to-hold charge offset and dielectric absorption. The AD386 also includes an internal differential amplifier for very high accuracy applications.

Typical applications for the AD386 include sampled data system, peak hold function, strobe measurement system and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer true 16-bit performance (0.00076% linearity) over the industrial temperature range, and 14-bit performance (0.003% linearity) over the military temperature range.



AD386 Pin Configuration

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD386BD	0.00076% FSR	−40°C to +85°C	DH-24B
AD386TD	0.003% FSR	−55°C to +125°C	DH-24B
AD386TD/883B	0.003% FSR	−55°C to +125°C	DH-24B

*DH-24B = Ceramic DIP. For outline information see Package Information section.

AD386—SPECIFICATIONS (@ +25°C unless otherwise noted, V_S = ±15 V ± 10%)

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
DIFFERENTIAL AMPLIFIER								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Common-Mode Range		±10			±10			V
Input Resistance[1]								
Signal			5			5		kΩ
Ground Sense			10			10		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
CMRR	V_{CM} = ±10	**80**	90		**80**	90		dB
PSRR[3]		**76**	85		**76**	85		dB
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
Noise (ENBW = 1.8 MHz)			32	45		32	45	μV rms
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			6			6		MHz
Slew Rate			65			65		V/μs
Settling Time[4]								
10 V Step to 1/2 LSB16			2.0	3.0				μs
10 V Step to 1/2 LSB14			0.8	1.5		0.8	1.5	μs
20 V Step to 1/2 LSB16			2.0	**3.0**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		2.0	3.0				μs
20 V Step to 1/2 LSB14			0.8	**1.5**		0.8	**1.5**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		0.8	1.5		0.8	1.5	μs
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			4.2	**5.0**		4.2	**5.0**	mA
TRACK-AND-HOLD								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Input Resistance[1]			5			5		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.00076**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
PSRR[3]		**76**	85		**76**	85		dB
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			2			2		MHz
Slew Rate			15			15		V/μs
TRACK-TO-HOLD SWITCHING								
Pedestal + Offset			0.5	**1.5**		0.5	**1.5**	mV
Pedestal + Offset	T_{min} to T_{max}			5.0			7.5	mV
Pedestal Linearity	T_{min} to T_{max}		0.0004	0.00076		0.0004	0.003	%
Aperture Delay			12			12		ns
Aperture Jitter			40			40		ps
Transient Settling[4]								
to 1/2 LSB16	T_{min} to T_{max}		600	**800**				ns
to 1/2 LSB14	T_{min} to T_{max}		400	**500**		400	**500**	ns

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
HOLD MODE								
Droop Rate			20	**100**		20	**100**	mV/s
Droop Rate	T_{max}		0.2	1.0		3.6	18	V/s
Feedthrough[5]			−99	**−94**		−99	**−94**	dB
Noise (ENBW = 1.7 MHz)			32	50		32	50	μV rms
PSRR[3]		**60**	66		**60**	66		dB
Dielectric Absorption[6]			7	**10**		7	**10**	ppm
HOLD-TO-TRACK DYNAMICS								
Acquisition Time[4]								
10 V Step to 1/2 LSB16			3.6	4.1				μs
10 V Step to 1/2 LSB14			3.1	3.6		3.1	3.6	μs
20 V Step to 1/2 LSB16			3.6	**4.1**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.0	4.5				μs
20 V Step to 1/2 LSB14			3.1	**3.6**		3.1	**3.6**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.5	4.0		4.0	4.5	μs
DIGITAL INPUTS								
V_{IH}	T_{min} to T_{max}	**3.5**			**3.5**			V
V_{IL}	T_{min} to T_{max}			**0.9**			**0.9**	V
I_{IH}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
I_{IL}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±8		±18	±8		±18	V
Quiescent Current								
Positive Supply			8.0	**12.0**		8.0	**12.0**	mA
Negative Supply		**−6.0**	−5.4		**−6.0**	−5.4		mA
SYSTEM								
Gain Linearity	T_{min} to T_{max}		0.0003	0.0012		0.0003	0.0012	%
Acquisition Time[4, 7]								
20 V Step to 1/2 LSB16			4.1	5.1				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.5	5.4				μs
20 V Step to 1/2 LSB14			3.2	3.9		3.2	3.9	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.6	4.3		4.1	4.8	μs
Power Dissipation			312	435		312	435	mW
TEMPERATURE RANGE								
Operating		−40		+85	−55		+125	°C
Storage		−60		+150	−60		+150	°C

NOTES
[1]Typical resistance tolerance is ±25%.
[2]After 5 minute warmup at +25°C.
[3]Test conditions: $+V_S$ = +15 V, $-V_S$ = −16 V to −14 V and $+V_S$ = +14 V to +16 V, $-V_S$ = −15 V.
[4]R_{LOAD} = 5 kΩ, C_{LOAD} = **10** pF, settling measured to 1/2 LSB at output.
[5]Measured at 1 kHz.
[6]Dielectric Absorption represents the magnitude of long-term settling artifacts for hold times up to 80 μs as a fraction of the difference in voltages between two successive held samples.
[7]Specifications also apply for 10 V step.

Specifications subject to change without notice.
Specifications in **bold** are 100% production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . .800 mW
Input Voltage[2] . . . . . ±18 V
T/$\overline{H}$ Input Voltage . . . . . −0.5 V, +16 V
Output Short Circuit Duration . . . . . .Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD386B . . . . . −40°C to +85°C
AD386T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

AD386—Typical Performance Characteristics

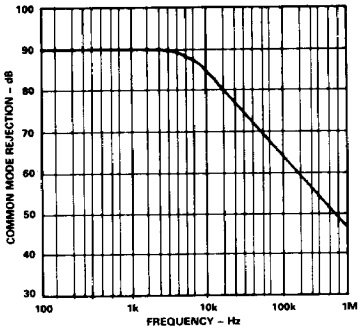


Figure 1. Differential Amplifier Common Mode Rejection vs. Frequency

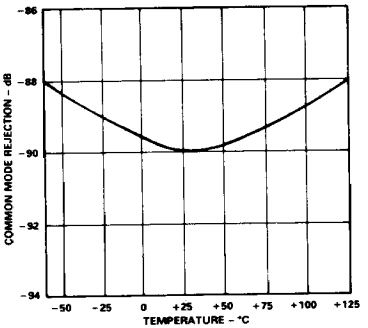


Figure 2. Differential Amplifier Common Mode Rejection vs. Temperature (100 Hz)

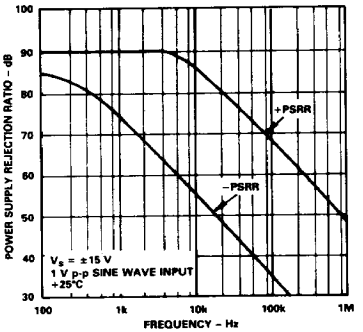


Figure 3. Differential Amplifier Power Supply Rejection vs. Frequency

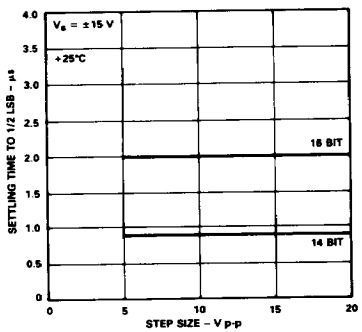


Figure 4. Differential Amplifier Settling Time vs. Step Size

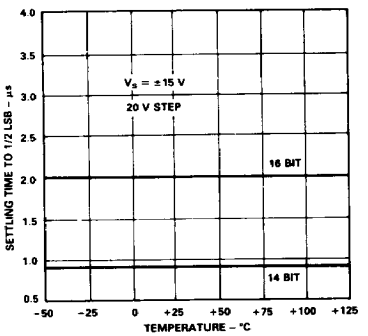


Figure 5. Differential Amplifier Settling Time vs. Temperature

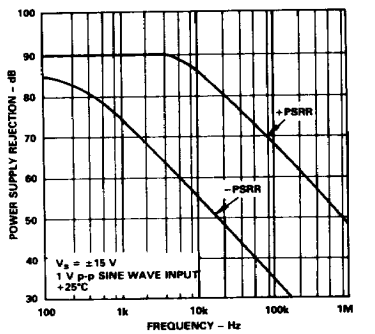


Figure 6. T/H Power Supply Rejection vs. Frequency, Track Mode

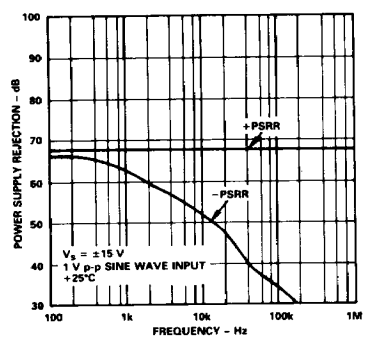


Figure 7. T/H Power Supply Rejection vs. Frequency, Hold Mode

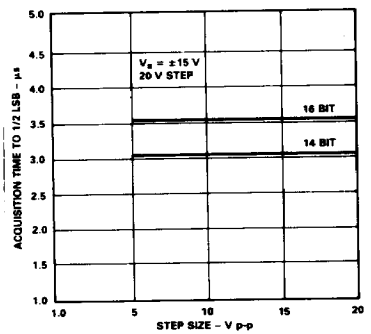


Figure 8. T/H Acquisition Time vs. Step Size

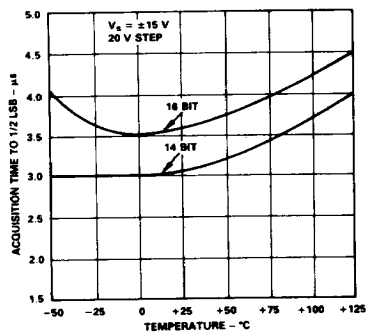


Figure 9. T/H Acquisition Time vs. Temperature

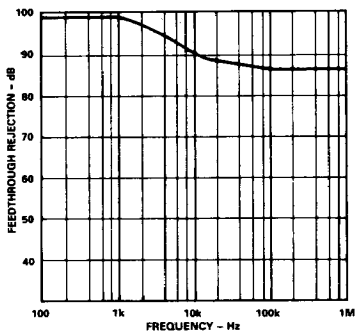


Figure 10. Feedthrough vs. Frequency

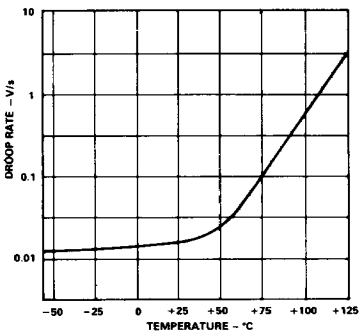


Figure 11. Droop Rate vs. Temperature

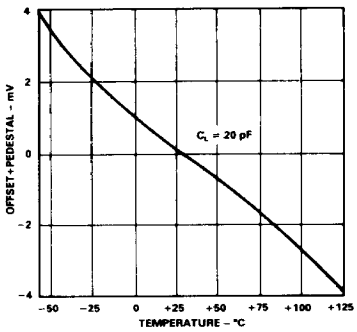


Figure 12. (Pedestal + Offset) vs. Temperature

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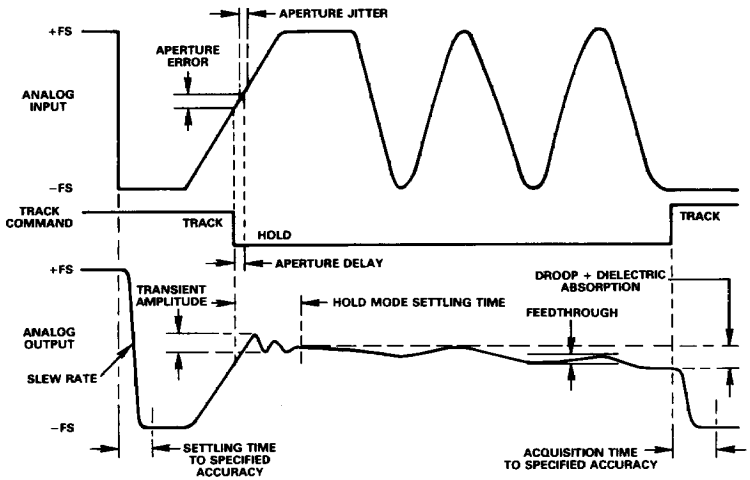


Figure 13. T/H Characteristic Features

TERMINOLOGY

Aperture Delay: the time required by the internal switch(es) to disconnect the hold capacitor from the input, which produces an effective delay in the sample timing.

Aperture Jitter: the uncertainty in Aperture Delay caused by internal noise and the variation of switching thresholds with signal level. The error caused by aperture jitter depends on the rate of change of the input and as such determines the maximum input frequency which can be sampled without error.

Pedestal: a step change in the output voltage which occurs when switching from track mode to hold mode.

Hold Mode Settling Time: the time required for the pedestal to reach its final value to within a specified fraction of full scale.

Droop: the change in the held output voltage resulting from leakage currents.

Feedthrough: the fraction of input signal variation which appears at the output in hold mode as a result of capacitive coupling.

Dielectric Absorption: the tendency of charges within a capacitor to redistribute themselves over time, resulting in "creep" in the voltage of an open circuit capacitor after a large rapid change.

Acquisition Time: the time required after entering track mode for the voltage on the hold capacitor to settle to within a specified fraction of full scale. This is usually specified for a full-scale step change in output voltage.

Settling Time: the time required in track mode for the output to reach its final value within a specified fraction of full scale following a step change in the input voltage.

Nonlinearity: the degree to which a plot of output versus input deviates from the straight line defined by the end points. It is usually specified as a percentage of full scale.

THEORY OF OPERATION

The architecture of the AD386 differs from that usually encountered in inverting Track-and-Hold (T/H) circuits. The hold capacitor in a conventional T/H (Figure 14) is always connected from the amplifier's output to its inverting input. In track mode switch A is open and switch B is closed. Since the summing junction is a virtual ground, the voltage across the capacitor follows the input. The switches change state in hold mode which disconnects the capacitor from the input and holds the output voltage constant. The clamping action of switch A reduces the variations across switch B, improving feedthrough performance.

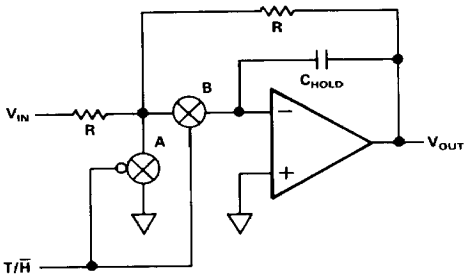


Figure 14. Conventional Inverting Integrator T/H

This circuit forces several tradeoffs. The hold capacitor's charging current is limited by the input resistor. Either the resistor or the capacitor, or both, must be made small to obtain fast acquisition times. A small resistor creates greater demands on the circuit which drives the T/H, while a small capacitor leads to increased pedestal and droop. In addition, the parallel combination of the feedback resistor and the hold capacitor acts as a low pass filter and constrains both bandwidth and acquisition time.

The AD386 uses a four-switch flyback architecture which removes the hold capacitor from the feedback loop during track mode (Figure 15). Switches A and C are open in track mode while switches B and D are closed. This maximizes bandwidth and provides minimum acquisition time because the charging current delivered to the hold capacitor is limited only by the amplifier's output capability. The hold capacitor can be made larger, subject to amplifier stability, since it no longer appears in parallel with the feedback resistor. This helps to reduce droop and pedestal. Switches A and C close in hold mode while switches B and D open, which connects the hold capacitor to the amplifier's inverting input.

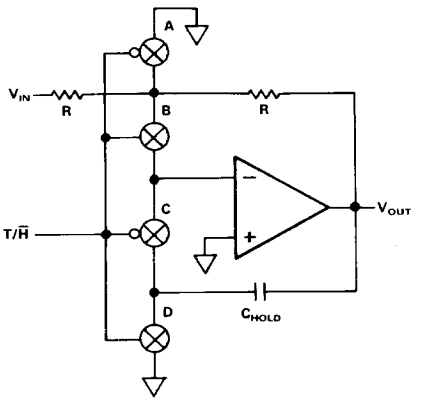


Figure 15. Four-Switch Inverting Flyback T/H

Additional switches and capacitors, not shown in the figure, provide first order cancellation of amplifier and switch leakage currents, switching charge injection, and switch feedthrough. Finally, a small amount of positive feedback is used to reduce dielectric absorption effects.

TRACK-AND-HOLD ERROR CONTRIBUTIONS IN SAMPLED-DATA SYSTEM

Any track-and-hold amplifier imposes performance limits on the system in which it is used. Some of these limits can be derived from the theory of sampled-data systems, some are intrinsic to the T/H, and some depend on details of the system design. Many subtle effects come into play as system resolution increases to 14 or 16 bits, and these can contribute significant errors. Understanding T/H error sources is critical to maintaining signal integrity in a high resolution data acquisition system.

FREQUENCY LIMITATIONS

Three factors set fundamental limits on system performance when digitizing high frequency signals. These are: T/H amplifier bandwidth, aperture uncertainty, and the maximum update rate of the T/H and A/D combination. The track mode bandwidth of the T/H must be significantly greater than the bandwidth of the signals being digitized to prevent the introduction of amplitude and phase errors. The 2 MHz small signal bandwidth of the AD386 attenuates a 35 kHz signal by 0.001 dB and shifts its phase by 1.0 degrees.

There are two different aperture related error terms. The first is aperture delay time, the delay between the HOLD command and the complete opening of internal switches in the T/H. This time amounts to a negative phase delay applied to the input signal because the T/H output can actually continue to track the input for a brief time after the HOLD command. Aperture delay time can be "tuned out" by advancing the assertion of HOLD.

Aperture jitter, the random variations in aperture delay time, causes errors which are directly related to the rate of change of the input signal and which cannot be eliminated by circuit adjustments.

A simple calculation provides the frequency at which aperture jitter produces an error of 1/2 LSB when the input is a full-scale sinusoid. The general result for an N-bit A/D converter is

$$F_{max} = \frac{V_{FS}}{V_{PP}} \times \frac{1}{2^{N+1} \times \pi \times Aperture\ Jitter}$$

where V_{FS} is the A/D converter's input range and V_{PP} is the peak-to-peak value of the input sinusoid. The worst case (minimum) value of F_{max} occurs when V_{PP} is equal to V_{FS}. If the T/H has an aperture jitter of 100 ps and is used with a 16-bit linear A/D, the maximum input frequency is 24.3 kHz.

The same T/H, when used with a 14-bit linear A/D, permits the processing of signals up to 97.1 kHz before aperture jitter-errors become observable. Figure 16 shows these errors as a function of frequency, assuming a full scale input sinusoid, for several values of aperture jitter.

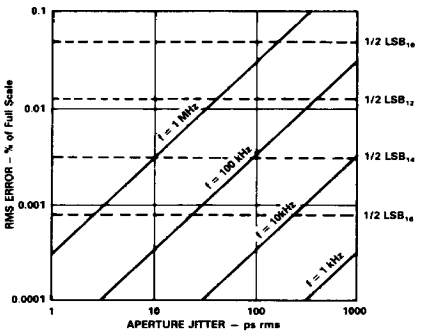


Figure 16. T/H Error vs. Aperture Jitter and Input Frequency

Aperture jitter is often expressed as an rms number. "Peak-to-peak" aperture jitter is usually defined as 6 times this rms value. This comes from probability theory, where 99.7% of the measurements of a random variable will be within 3 standard deviations of the variable's average value. Aperture jitter arises from broadband electrical noise, which is very nearly an ideal random process with a standard deviation equal to its rms value, so multiplication by 6 gives a good approximation to the noise's peak-to-peak value.

A second limit on the input frequency is imposed by the finite time required for signal acquisition and conversion. It is possible to reconstruct any uniformly sampled signal without loss of information provided the sampling rate is at least twice the bandwidth of the input signal; this is the Nyquist criterion, a fundamental result in sampling theory. This limits input frequency to

$$F_{max} = \frac{1}{2 \times (t_{ACQ} + t_{CONV} + t_{AP})}$$

where t_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{AP} is the aperture delay of the T/H. The last term is usually very small and can be ignored. A system composed of a 3.6 μs T/H and a 10 μs A/D can be used successfully to digitize signals with frequency components up to 36.76 kHz. This limit is independent of input signal amplitude. Throughput rates and input frequency ranges for the AD386 in combination with various A/D converters are shown in Table I.

A/D	Conversion Time	Minimum Throughput
ADADC71	50 μs max	18.7 kHz
AD1376/78	17 μs max	48.8 kHz
AD1377	10 μs max	73.5 kHz

Table I. Throughput for AD386 with Various A/D Converters

NONLINEARITIES

Two phenomena directly affect the fidelity of a T/H's transfer function and can degrade system linearity. One of these error sources is track mode nonlinearity. It arises primarily from gain nonlinearity in the T/H's internal amplifier(s). Mismatches in the temperature coefficients of internal resistors may also contribute, but usually do so only for very low frequency signals. The AD386's track mode nonlinearity is about 1/6 16-bit LSB (Figure 17), as is the nonlinearity of the AD386's differential amplifier.

System linearity will also be reduced if the pedestal varies nonlinearly with signal level. Pedestal nonlinearity in the AD386 is below 8 microvolts per volt of input signal, or about 1/2 16-bit LSB.

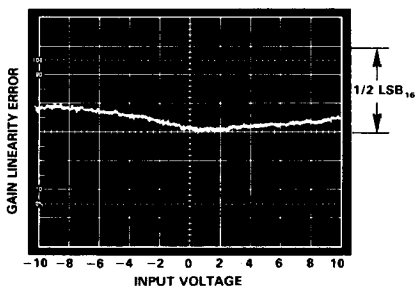


Figure 17. AD386 Track Mode Nonlinearity

FEEDTHROUGH, DROOP, AND DIELECTRIC ABSORPTION

Errors resulting from signal feedthrough and droop must be less than 1/2 LSB in order for the system's linearity to be maintained. The AD386 uses a symmetrical, compensated architecture to minimize both these effects. Feedthrough varies slightly with input frequency from −100 dB below 1 kHz to −86 dB above 100 kHz (Figure 10). This provides 16-bit accuracy for full-scale inputs up to at least 5 kHz and 14-bit performance to beyond 100 kHz.

The circuit's symmetry causes the droop rate to depend on differences in leakage currents between identical junctions under nearly identical bias conditions. The resulting droop is less than 1/2 16-bit LSB (10 V scale) at temperatures up to 85°C and 1/2 14-bit LSB (10 V scale) over the full military temperature range for hold times up to 100 μs.

Capacitors exhibit a memory phenomenon, dielectric absorption (DA), in fast charge, long hold applications. This arises from nonideal behavior of the dielectric material which allows charge storage in the bulk of the dielectric. This bulk charge cannot be removed rapidly because of the long time constant associated with the dielectric's high resistance. A capacitor with dielectric absorption can be modeled as an ideal capacitor in parallel with a series R-C circuit as shown in Figure 18. When such a capacitor is used as the hold capacitor in a T/H the held voltage will tend to creep back towards the voltage held for the previous conversion cycle. The degree and time constant of this behavior depends on the capacitor's dielectric material, as well as on the charge and hold time of the circuit.

Dielectric absorption will cause a variable "offset" if a T/H is used to sample multiple channels with widely varying signals. This causes an apparently nonlinear pedestal because the difference between the currently measured voltage and the previously measured voltage determines the magnitude of the DA error. The AD386 uses a high quality hold capacitor with low intrinsic DA. Residual DA errors are further reduced by laser trimming a compensation network during the manufacturing process. The trimming is performed under typical system timing conditions of 5 μs track, 45 μs hold. The post-trim dielectric absorption error is less than 1/2 16-bit LSB for full-scale changes between samples and hold times between 10 μs and 100 μs.

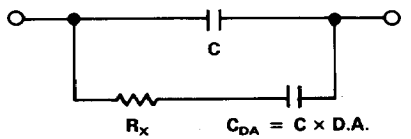


Figure 18. Capacitor Model with Dielectric Absorption

NOISE

Noise generated in a T/H adds to the held signal and causes variations in the output code of an A/D. This noise has two components, one which arises during track mode and another contributed during hold mode. The rms sum of these terms determines the noise performance of the T/H in the system.

Track noise is the noise which gets sampled when entering hold mode. An inverting T/H architecture such as that used in the AD386 has a noise gain of 2. This noise is low pass filtered in the R-C network comprised of the hold capacitor and the switch on resistance (see Figure 19a). The rms value of the track noise is

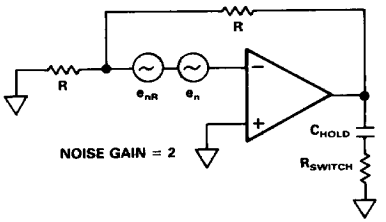
$$<e_{nT}> = (op\ amp\ noise) \times (noise\ gain) \times (ENBW)^{1/2}$$

Op amp noise is the rms sum of the amplifier's broadband voltage noise and the thermal noise contributions of the input and feedback resistors, about 17 nV/$\sqrt{\text{Hz}}$. Other noise sources, including amplifier current noise and switch thermal noise, are negligible. ENBW, the equivalent noise bandwidth, is

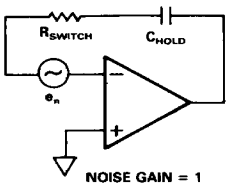
$$ENBW = \frac{\pi}{2} \times \frac{BW1 \times BW2}{BW1 + BW2}$$

where BW1 is the small signal bandwidth of the T/H in track mode (2 MHz for the AD386) and BW2 is the corner frequency of the R_{SWITCH}–C_{HOLD} combination (2.7 MHz). The resulting track noise in the AD386 is at most 46 μV rms.

Noise gain is reduced to 1 in hold mode, and input and feedback resistor thermal noise makes no contribution (Figure 19b). The equivalent noise bandwidth now depends on the T/H's small signal bandwidth and the characteristics of the A/D converter used in the system. This is because the signal at the input



a. Track Mode



b. Hold Mode

Figure 19. Dominant AD386 Noise Sources

of the comparator in a successive approximation A/D converter is filtered by the converter's input resistance and the summing junction capacitance. ENBW is calculated as before, but now BW1 is the T/H's small signal bandwidth in hold mode (4 MHz for the AD386), and BW2 is the bandwidth of the A/D's input R-C. BW2 is about 700 kHz in the AD ADC71 and AD1376 and roughly 1.7 MHz in the AD1377 and AD1378 (assuming a 10 V span). The respective values of ENBW are 940 kHz and 1.9 MHz. The hold noise contribution of the AD386 is about 16 μV rms when used with the AD ADC71 or AD1376 and 22 μV rms when used with the AD1377 or AD1378; this noise is 30% less for a 20 V span and 40% greater for a 5 V span because changes in the A/D's input resistance cause changes in BW2.

The total noise is the rms sum of these two results:

$$<e_n> = [<e_{nT}^2> + <e_{nH}^2>]^{1/2}$$

This yields 49 μV rms and 51 μV rms for the two cases. Track noise dominates in both instances.

When the AD386's differential amplifier is used, its noise contribution will be band limited and sampled by the T/H. The equivalent bandwidth for this noise is also 1.8 MHz and the contribution to the track noise is 46 μV rms. The total track noise is the rms sum of 46 μV and 46 μV, or 65 μV rms, and the overall noise for the complete AD386 used with any of the above A/D converters is at most 70 μV rms.

The rms value represents one standard deviation if the noise has a Gaussian distribution, which is usually the case for wideband electrical noise. If a constant noise-free voltage is sampled a large number of times, the held result will be within one standard deviation of the ideal value 32% of the time, within two standard deviations 95% of the time, and within three standard deviations 99.7% of the time. The entries in Table II were calculated using three standard deviations as the definition of the peak-to-peak noise.

Span	No. Bits	rms Noise LSBs	p-p Noise LSBs
10 V	14	0.11	0.66
20 V	14	0.06	0.36
10 V	16	0.45	2.7
20 V	16	0.23	1.4

Table II. AD386 Noise Contribution as a Function of A/D Span and Resolution

POWER SUPPLY REJECTION

Variations on the power supply lines, both dc and ac, can lead to unwanted changes in the voltage acquired by a T/H. Power supply variations in track mode cause the output voltage, and hence the voltage across the hold capacitor, to vary. PSRR decreases with increasing frequency, making well regulated, low noise linear power supplies and proper bypassing essential in a high resolution data acquisition system.

Equally important, but usually forgotten or omitted, is hold PSRR. This is frequently much worse than track PSRR because parasitic capacitances which are not significant in track mode couple into the extremely high impedance nodes which exist in a T/H during hold mode. This specification is essential to the system designer, as hold mode PSRR often determines the performance required from the system's power supplies. The power supply rejection of the AD386 is specified and characterized in both track and hold modes.

Pedestal arises from the transfer of charge from the internal switching circuitry to the hold capacitor during the transition from track mode to hold mode. Pedestal in some T/H circuits is extremely sensitive to changes in the high and low levels of the external control signal. The AD386 uses an internal +5 V supply and logic buffers to prevent this behavior.

GROUNDING

All voltage measurements in a data acquisition system are eventually referenced to ground. Variations in the "ground" potential through the system resulting from resistive drops of power supply and signal return currents as well as from interference from external sources may add to the signal being digitized and produce false results. The grounding scheme in a high resolution system cannot be left to chance and must be planned as carefully as any other aspect of the system's design. Proper grounding and the reduction of externally induced ground noise are discussed at length in the following Applications section.

Applications

GROUNDING. DECOUPLING, AND LAYOUT CONSIDERATIONS

Many data acquisition systems have two or more ground pins which are not connected together within the device(s). These "grounds" may be referred to as Logic Power Return, Digital Return, Analog Ground, Analog Power Return, Signal Ground, etc., and they must be connected together somewhere within the system to establish a measurement reference point. Good grounding practice dictates that these grounds be tied at a single point, sometimes called a star or "Mecca" ground. In high resolution systems the star point is often located at the A/D, with a single, short, low impedance trace leading from there to the analog supply "common" terminal. The ideal is to use a solid analog ground plane beneath the T/H and A/D as the star point.

Because circuit traces have resistance and inductance, currents in the various ground runs can create voltage differences of hundreds of millivolts between "ground" in different parts of the system. Power supply and signal ground traces should be separate to prevent summing power supply return currents with analog signal currents, which would lead to measurement errors. It is also important to avoid closed circuit loops in system ground connections. A loop can act as a very effective antenna, coupling voltages created by stray magnetic fields into the measurement system.

Each of the AD386's power supply terminals should be capacitively bypassed to the ground plane as closely as possible to the device. This is best done using 0.01 μF to 0.1 μF ceramic capacitors. High frequency supply noise rejection may be further improved by placing small (4.7 Ω to 10 Ω) carbon composition resistors in series with the supply leads. These resistors, in combination with the ceramic capacitors, act as local low pass filters and prevent crosstalk between system components. The bypassing scheme should also include solid Tantalum capacitors of 1 μF to 10 μF from each supply to ground in the critical areas of the board. Proper grounding and bypassing techniques are shown in Figure 20.

All AD386 ground pins (Pins 2, 5, 7, 9, 18, 19, and 24) should be connected to the analog ground plane.

WARNING: Improper bypassing can result in poor settling performance or high frequency oscillations.

The metal cover of the AD386 is internally grounded to provide additional shielding. Do not make any external connection to the cover.

DIFFERENTIAL AMPLIFIER

Many high resolution applications require the ability to sense ground at the signal source. This is especially true in systems with physical or thermal constraints that make it necessary to locate the T/H and A/D at some distance from the transducer. Under these conditions stray electromagnetic fields may cause "ground" at the signal source to be at a different potential from "ground" at the A/D despite the designer's best efforts. This will give rise to measurement errors because the potential difference will appear to be added to the true signal. The AD386's differential amplifier may be used to eliminate this type of ground noise as shown in Figure 21.

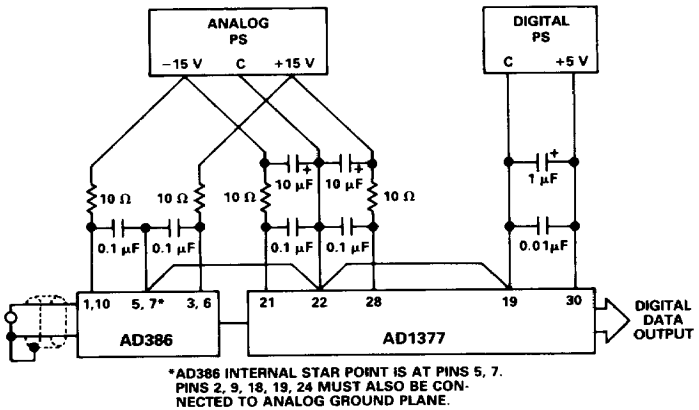
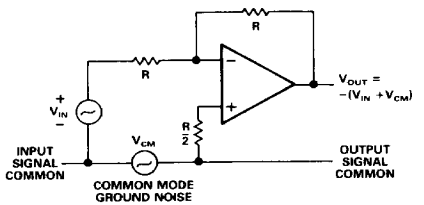
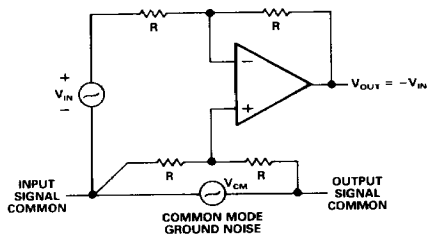


Figure 20. Proper Grounding and Supply Bypassing Techniques for a High Resolution Data Acquisition System



a. Without Differential Amplifier



b. With Differential Amplifier

Figure 21. Effects of Common Mode Noise

In extremely noisy environments it may be necessary to connect the differential amplifier to the signal source with shielded twisted pair cable. The shield should be connected to ground at the transducer and should be left floating at the AD386. This shielding technique is shown in Figure 22. The cable presents a capacitive load, and the signal source must be capable of driving this load without ringing or oscillations. The differential amplifier's noninverting input should be connected to Pin 24 if ground sensing is not required.

Another use of the differential amplifier is to restore signal polarity. Like most high resolution T/H amplifiers, the T/H in the AD386 operates in the inverting mode. The differential amplifier may be used to provide a second inversion so that the T/H output has the same polarity as the sensor output.

The differential amplifier also provides a low dynamic source impedance to the T/H section. This absorbs transients produced when the T/H switches from hold mode to track mode, providing optimal settling performance.

The T/H and differential amplifier have independent power supply connections. This permits a reduction in system power dissipation when the differential amplifier function is not needed.

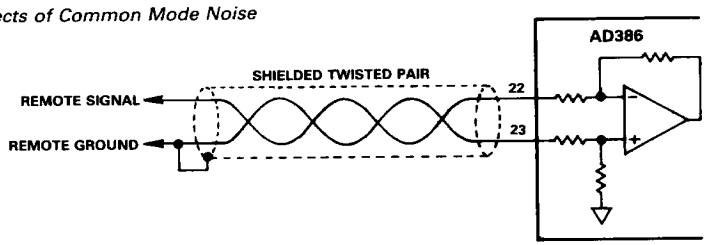


Figure 22. Remote Ground Sensing in a Noisy Environment

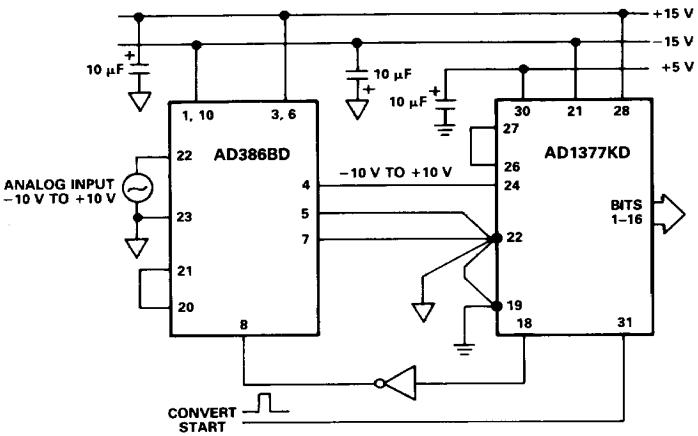


Figure 23. Basic Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

4

GAIN AND OFFSET ADJUSTMENT

The usual practice in the design of data acquisition systems is to incorporate a single system level trim for offsets and a second for gain errors, rather than to trim each element in the signal processing chain. Traditionally these trims involve potentiometers or fixed resistors. The trims should be designed so that nulling static errors does not introduce new errors such as noise, increased thermal drift, or nonlinearity.

The offset, drift, and gain errors of the AD386 are laser trimmed during manufacture and no external adjustment capabilities are provided. This prevents the introduction of noise through offset adjust terminals and preserves the excellent gain linearity and drift performance. Most A/Ds provide for nulling gain and offset errors with a range sufficient to include the contributions of the AD386. Of course, it is also possible to include calibration routines in the system's software to eliminate mechanical adjustments.

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 are shown in Figure 23. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the A/D's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode. The throughputs given in Table I were calculated based upon this circuit configuration.

One drawback of this connection becomes apparent if the system's grounding is marginal. The falling edge of CONVERT-START resets the successive approximation register within the A/D, causing transient currents in both the analog and digital return paths. These transients vary depending on the input signal and the prior conversion result. The same edge also drives the T/H into hold mode. The exact timing relationship of these two events depends upon differences in propagation delays. The T/H's held value may be affected if the A/D reset transient begins before the T/H has fully entered hold mode. The end result is system nonlinearity.

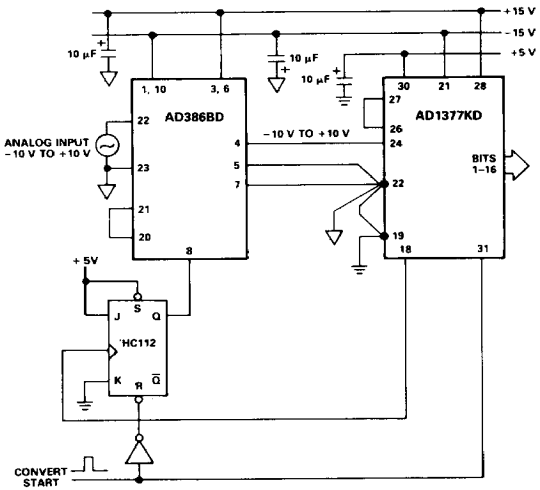


Figure 24. Improved Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

This problem can be avoided with the addition of a flip flop as shown in Figure 24. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

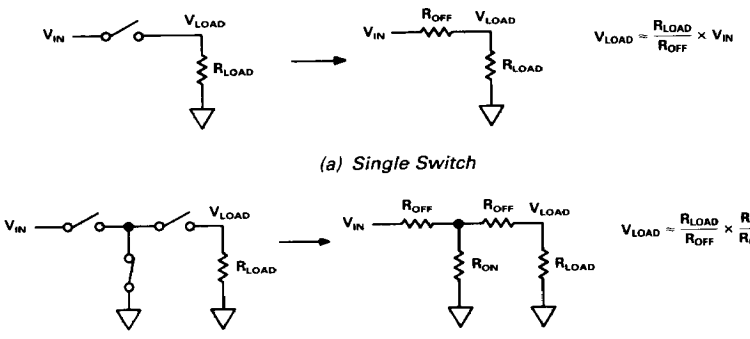


Figure 25. Single and "T" Analog Switches (Shown in OFF Position)

MULTICHANNEL SYSTEMS

The design of multiplexed data acquisition systems which maintain 14- or 16-bit signal fidelity is an extremely demanding task. One of the first difficulties encountered is the lack of adequate analog switches. The specified feedthrough performance of most switches and multiplexers is seldom better than −80 dB. This is an order of magnitude too high for a 16-bit system with its 8 parts-per-million sensitivity. A "T" switch configuration can be used to reduce feedthrough as shown in Figure 25. The improvement in "off" isolation relative to a single switch is substantial.

A few monolithic video T-switch ICs are now available and provide the necessary isolation in the dc-50 kHz frequency range. Unfortunately, these devices have voltage limitations which restrict their utility. It will usually be necessary to design a multiplexer using analog multiplexer and switch ICs. Figure 26 shows a simple 4-channel single-ended T-switch multiplexer and includes a high performance buffer (see below).

The on-resistance of analog switches and multiplexers is a nonlinear function of signal voltage. This will produce severe nonlinearity in a system in which a multiplexer supplies signals

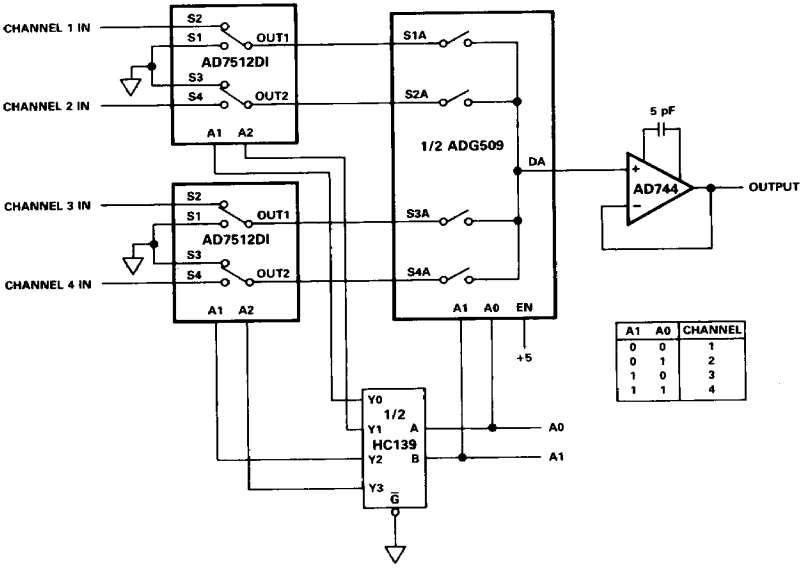


Figure 26. Four-Channel T-Switch Multiplexer(Power Supply Connections Not Shown)

directly to an AD386. A high-impedance buffer between the multiplexer and the T/H's input can solve this problem but may introduce several others.

An op amp in the noninverting gain-of-1 configuration is the obvious candidate for a buffer. The amplifier must settle quickly to maximize system throughput and must be extremely linear to maintain system performance. The linearity of this configuration depends upon the linearity of both the amplifier's open loop gain and common-mode rejection (linear errors in these parameters result only in system gain error, but nonlinear gain and CMRR produce system nonlinearity). Neither of these parameters is specified by most amplifier manufacturers.

A buffer may also increase system noise. Applications which require ground- sensing will require two buffers, resulting in 40% more noise than a one-buffer system.

Finally, a buffer will add its own offset to the signal being measured. Software calibration of the error and its drift is possible using a permanently grounded multiplexer channel.

The AD744 is a nearly ideal buffer for multiplexed systems. This amplifier provides offsets as low as 250 μV and an offset drift of 3 μV/°C while maintaining 16-bit linearity over the −40°C to +85°C temperature range. Typical settling times at room temperature are 2.3 μs (14 bits) and 3.5 μs (16 bits) for the AD744 combined with the AD386's differential amplifier. The increase in noise at the differential amplifier's output will be about 6 μV rms in a one-buffer system and roughly 12 μV rms in a two buffer system (recall that a 16-bit LSB in a 20 volt system is 305 μV). The AD744 is not unity-gain stable, and compensation is required. A 5 pF compensating capacitor is sufficient to ensure stability. The settling times listed above were measured using a 9 pF compensation capacitor which provides greater stability with moderate capacitive loads.

The NE5534 can also be used as a buffer to deliver 16-bit linearity. This amplifier also requires slight compensation to achieve unity-gain stability; 10 pF is sufficient. Settling is somewhat slower than the AD744, about 5 μs to 14 bits and 6 μs to 16 bits, including the AD386's differential amplifier when measured at room temperature. The 5534 has lower voltage noise and will cause only a 1 or 2 μV rms increase in the total noise at the differential amplifier's output. The NE5534 lacks the precision offset and drift performance of the AD744.

Multiplexed throughput can be improved with the proper choice of system timing. If the new input channel is selected while the AD386 is in Hold mode, then multiplexer, buffer, and differential amplifier settling can occur during the A/D conversion. In this case throughput is determined only by the sum of the T/H acquisition and A/D conversion times. The effects of T/H feedthrough must be considered when using this type of overlap in system timing.

There is another solution to many of the problems of multiplexed systems when the speed of channel switching is not critical: relays. Relays should be selected for good shielding, low thermal EMF, and low on-resistance. The only significant drawback of this approach, other than switching speed and size, is power dissipation. In all other respects relays offer a near-perfect solution to the problems of high resolution system design discussed above.

DYNAMIC PERFORMANCE

Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) are important in many signal processing applications. SNR and THD are affected by both the T/H and A/D. The errors contributed by the T/H are generally dependent upon the input signal frequency, while those contributed by the A/D converter usually are not. The dynamic performance of a T/H-A/D pair is characterized using Fast Fourier Transform (FFT) techniques.

Figures 27–31 show the results of several 1024-point FFTs which demonstrate the exceptional distortion and noise performance of the AD386 when combined with the AD1377. These FFTs were obtained using a circuit similar to that of Figure 24. The input signal was processed by both the differential amplifier and T/H sections of the AD386 and was sampled at an 83.333 kHz rate. The AD1377's clock was adjusted to yield an 8.0 μs conversion time, which provided 4.0 μs for the AD386 to acquire each new sample. The vertical scale for these figures is based on a full-scale input referenced as 0 dB. The system was configured for a 10 volt span.

Figures 27 and 28 illustrate the system's low frequency noise and distortion performance. The input frequency is 1.546 kHz. When the input is −0.3 dB, nearly full scale, the largest harmonic component is −102.8 dB (Figure 27). Total harmonic distortion, the rms sum of the second through fifth harmonics, is −99.9 dB. The signal to noise ratio is 89.9 dB. The ultimate noise floor can be determined using a lower level input. Reducing the input level about 20 dB, as in Figure 28, decreases the

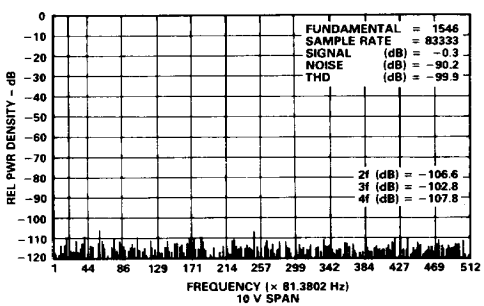


Figure 27.

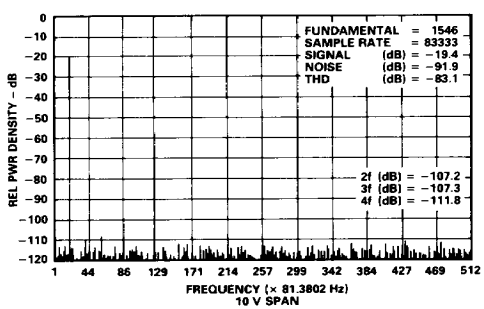


Figure 28.

noise floor by 1.8 dB to −91.9 dB. This corresponds to a total AD386 noise contribution of about 45 μV rms. The FFT noise floor would improve about 2 dB with the system configured for a 20 volt span because the effect of noise contributed by the AD386 is reduced as a result of the increased LSB size.

System performance just beyond the high end of the audio band is shown in Figure 29. Here the input is a −0.3 dB sinusoid at 21.24 kHz. The only significant harmonic component, the second harmonic, is −91.9 dB with respect to the fundamental, and THD is −91.1 dB. The noise floor is 0.5 dB greater than in Figure 27. The additional noise is contributed by higher-order harmonics; the second through fifth harmonics have been excluded from the noise floor calculations, but higher harmonics are considered to be "noise". These harmonics arise from the AD386's aperture jitter. The additional noise is consistent with an rms jitter of 40 ps.

In Figures 30 and 31, −0.3 dB and −20.1 dB inputs at 40.61 kHz show system performance near the Nyquist frequency. Even at this high frequency a full-scale input produces THD of only −84.6 dB, dominated by the second harmonic at −85.1 dB (Figure 31). In Figure 31 the harmonics have been eliminated by reducing the input level by a factor of 10.

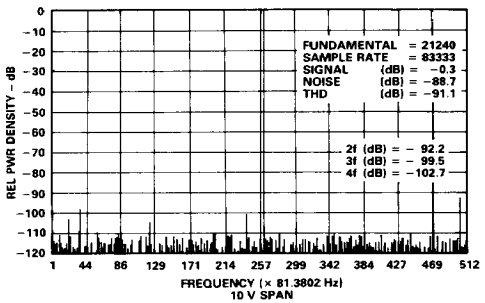


Figure 29.

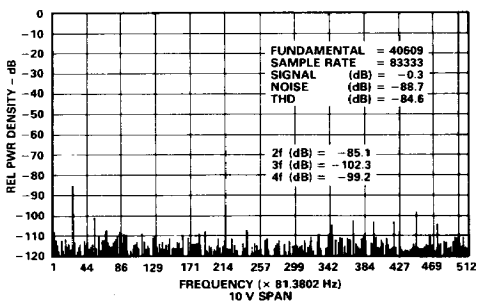


Figure 30.

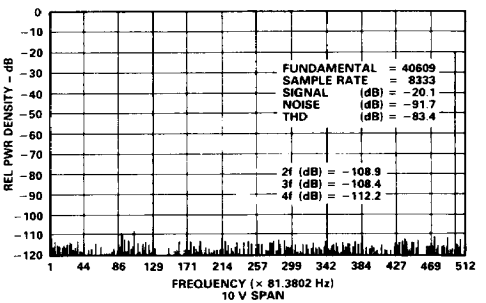


Figure 31.