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NEXFLASH® Technologies, Inc.

NX29F010

1M-BIT (128K x 8-bit) CMOS, 5.0V Only ULTRA-FAST SECTORED FLASH MEMORY

JUNE 2000

FEATURES

- **Ultra-fast Performance**
  - 35, 45, 55, 70, and 90 ns max. access times
- **Temperature Ranges**
  - Commercial 0°c-70°c
  - Industrial -40°c-85°c
- **Single 5V-only Power Supply**
  - 5V ± 10% for Read, Program, and Erase
- **CMOS Low Power Consumption**
  - 20 mA (typical) active read current
  - 30 mA (typical) Program/Erase current
- **Compatible with JEDEC-Standard Pinouts**
  - 32-pin DIP, PLCC, TSOP
- **Program/function Compatible with AM29F010**
  - No system firmware changes
  - Uses same PROM programer algorithm
- **Flexible sector architecture**
  - Erase any of eight uniform sectors or full chip erase
  - Sector protection/unprotection using PROM programming equipment
- **100,000 Program/Erase cycles**
- **Embedded algorithms**
  - Automatically programs and verifies data at specified address
  - Auto-programs and erases the chip or any designated sector
- **Data/Polling and Toggle Bits**
  - Detect program or erase cycle completion

DESCRIPTION

The *NexFlash* NX29F010 is a 1 Megabit (131,072 bytes) single 5.0V-only Sectored Flash Memory. The NX29F010 provides in-system programming with the standard system 5.0V-only Vcc supply and can be programmed or erased in standard PROM programmers.

The NX29F010 offers access times of 35, 45, 55, 70, and 90 ns allowing high-speed controller and DSPs' to operate without wait states. Byte-wide data appears on DQ0-DQ7. Separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls eliminates bus contention.

Power consumption is greatly reduced when the system places the device into the Standby Mode.

The device is offered in 32-pin PLCC, TSOP, and PDIP packages.

Principles of Operation

Only a single 5.0V power supply is required for both read and write functions. Program or erase operations do not require 12.0V V_{PP}. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the JEDEC single power supply Flash standard. Commands are written to the command register using standard micro-processor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Executing the Program Command Sequence invokes the Embedded Program Algorithm, an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

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Executing the Erase Command Sequence invokes the Embedded Erase Algorithm, an internal algorithm that automatically pre-programs the array to all zeros (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin during erase.

By reading the DQ7 ($\overline{\text{Data}}$ Polling) and DQ6 (toggle) status bits, the host system can detect whether a program or erase operation is complete. After completion, the device is ready to read array data or accept another command.

The sector erase architecture is designed to allow memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is erased before it is shipped to customers.

The hardware data protection includes a low Vcc detector that automatically inhibits write operations during power transitions. The hardware sector protection feature will disable both program and erase operations in any combination of the sectors of memory, and is implemented using standard EPROM programming algorithm.

The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. Data are programmed one byte at a time using the EPROM programming algorithm of hot electron injection.

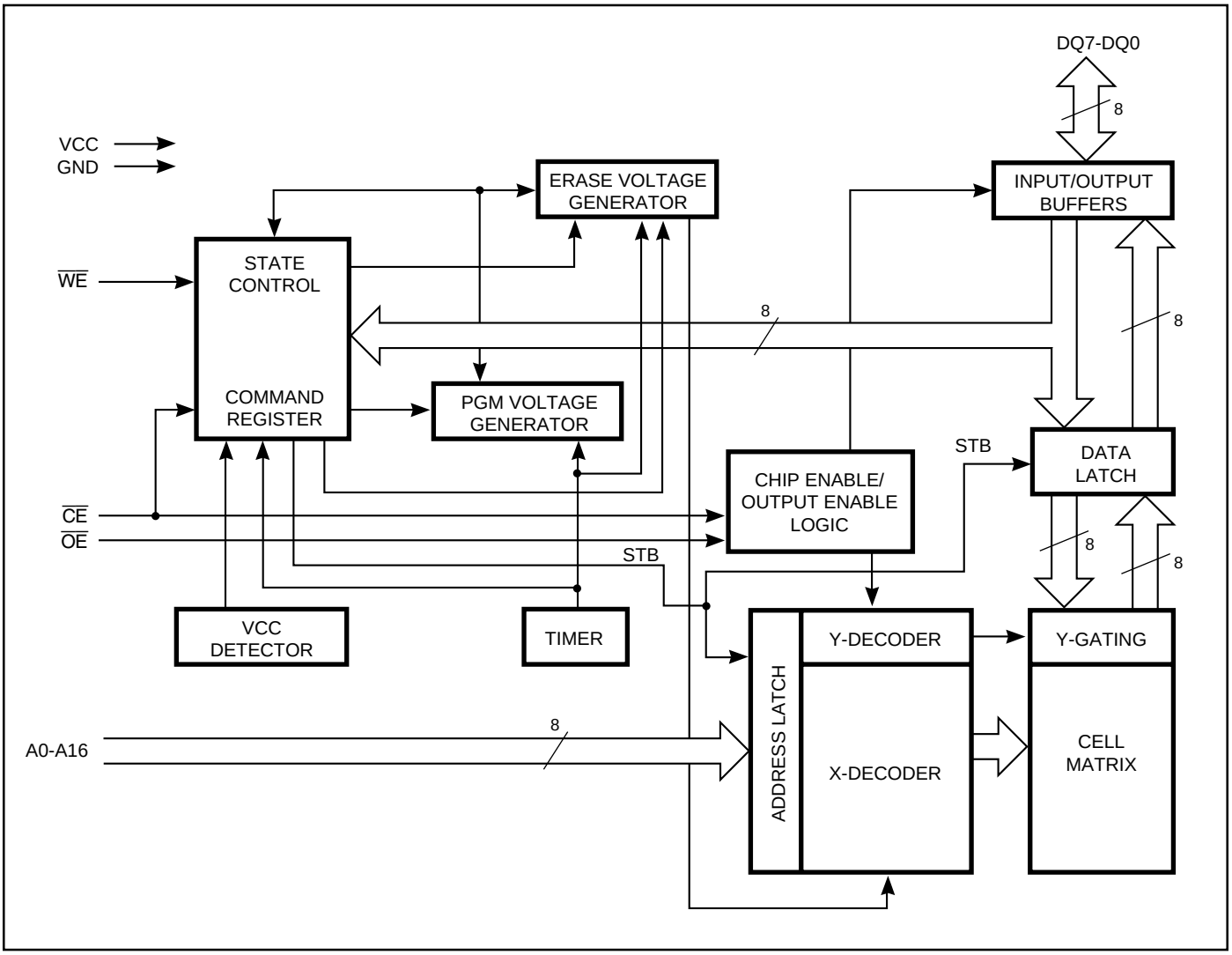


Figure 1. NX29F010 Block Diagram

PIN CONFIGURATIONS

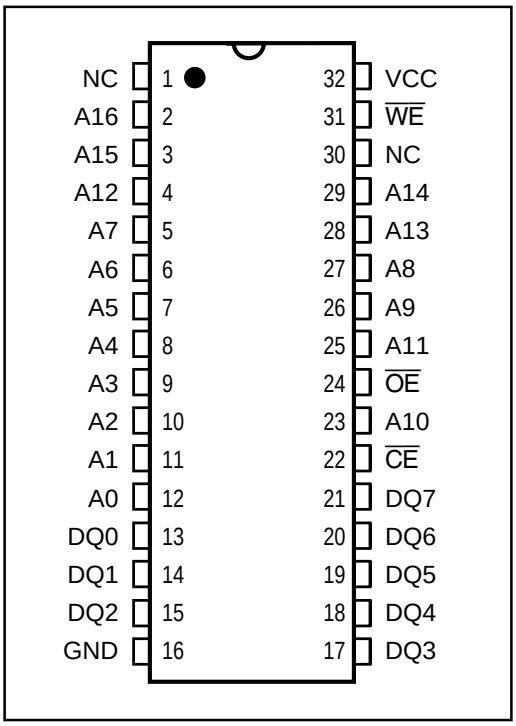


Figure 2. NX29F010 32-pin Plastic DIP

Table 1. Pin Descriptions

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
Vcc	Power Supply Voltage
GND	Ground
NC	No Internal Connection

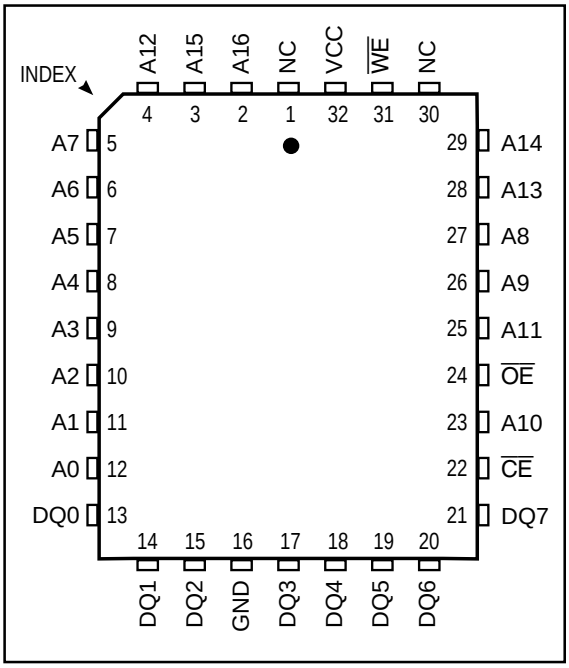


Figure 3. NX29F010 32-pin PLCC

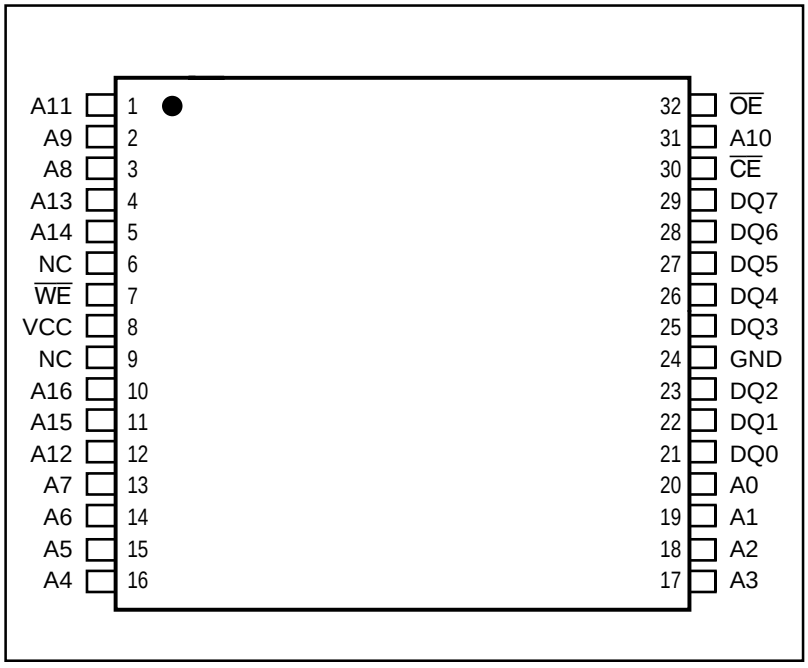


Figure 4. NX29F010 32-pin TSOP

BUS OPERATIONS

Table 2. Device Bus Operations(1, 2)

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Address (A16-A0)	DQ0-DQ7
Read	L	L	H	A_{IN}	Data Out
Write	L	H	L	A_{IN}	Data In
Standby	V_{CC} ± 0.5V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z

Notes:
1. L = V_{IL} , H = V_{IH} , X = Don't care, AIN = Address In.
2. The sector protect and sector unprotect functions must be implemented via programming equipment. See the Sector Protection/Unprotection section.

Requirements for Reading Array Data

Upon device power-up, or after a hardware reset, the internal state machine is set for reading array data. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

The system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL} to read array data from the outputs. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control that passes array data to the output pins. During a READ operation, $\overline{WE}$ must remain at V_{IH}.

Write Commands/Command Sequences

The system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH} to write a command or command sequence (which includes programming data to the device and erasing sectors of memory).

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Table (see Table 3) indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip.

Table 3. Sector Addresses Table

Sector	A16	A15	A14	Address Range
Sector A0	0	0	0	00000H-03FFFH
Sector A1	0	0	1	04000H-07FFFH
Sector A2	0	1	0	08000H-0BFFFH
Sector A3	0	1	1	0C000H-0FFFFH
Sector A4	1	0	0	10000H-13FFFH
Sector A5	1	0	1	14000H-17FFFH
Sector A6	1	1	0	18000H-1BFFFH
Sector A7	1	1	1	1C000H-1FFFFH

After the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on DQ7-DQ0. Standard read cycle timings apply in this mode. Refer to the "Auto-select Mode and Auto-select Command Sequence" sections for more information.

Program and Erase Operation Status

By reading the status bits on DQ7-DQ0, the system may check the status of the operation during an erase or program operation.

Standby Mode

In the Standby Mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{OE}$ input. The system can place the device in the standby mode when it is not reading or writing to the device.

The device enters the CMOS standby mode when the $\overline{CE}$ pin is held at $V_{CC} \pm 0.5V$. The device enters the TTL standby mode when $\overline{CE}$ is held at V_{IH}. The device requires the standard access time (t_{CE}) before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Output Disable Mode

When the $\overline{OE} = V_{IH}$, the output from the device is disabled and the output pins are placed in the high-impedance state.

Auto-select Mode

The auto-select mode provides access to the manufacturer and device equivalent codes, as well as sector protection verification codes, via the DQ7-DQ0 pins. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the auto-select codes can also be accessed in-system through the command register.

When using programming equipment, the auto-select mode requires V_{ID} (11.5V to 12.5V) on address pin A9. Address pins A1 and A0 must be as shown in Auto-select Codes (High Voltage Method), Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Table (Table 3). The Command Definitions table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the auto-select codes in-system, the host system can issue the auto-select command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See "Command Definitions" for details on using the auto-select mode.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement. Contact an NexFlash representative to obtain a copy of the appropriate document.

The device is shipped with all sectors unprotected. NexFlash offers the option of programming and protecting sectors at its factory prior to shipping the device. Contact a NexFlash representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Auto-select Mode" for details.

Table 4. Auto-select Codes (High Voltage Method)

Description	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A16-A14	A13-A10	A9	A8-A2	A1	A0	DQ7-DQ0
Manufacturer Equivalent ID	L	L	H	X	X	V_{ID}	X	L	L	01 (Hex)
Device Equivalent ID	L	L	H	X	X	V_{ID}	X	L	H	20 (Hex)
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	H	L	01H (protected)
										00H (unprotected)

Note:

1. L = V_{IL} , H = V_{IH} , V_{ID} = 11.5 to 12.5V , SA = Address Sector , X = Don't care.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to the Command Definitions table). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

If $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ during power-up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definitions Table 5 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

The system must issue the reset command to re-enable the device for reading array data if the error status bit, DQ5, is set high after an erase or program operation, or while in the auto-select mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operation's table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Reset Command

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device for reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an auto-select command sequence.

Once in the auto-select mode, the reset command must be written to return to reading array data.

If the error status bit, DQ5, goes high during a program or erase operation, writing the reset command returns the device to reading array data.

Auto-select Command Sequence

The auto-select command sequence allows the host system to access the manufacturer and device equivalent codes, and determines whether or not a sector is protected. The Command Definitions Table 5 shows the address and data requirements. This method is an alternative to that shown in the Auto-select Codes (High Voltage Method) Table 4, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The auto-select command sequence is initiated by writing two unlock cycles, followed by the auto-select command. The device then enters the auto-select mode, and the system may read at any address any number of times, without initiating another command sequence.

Table 5. Command Definitions

Command[1] Sequence	Cycles	Bus Cycles [2] (Hexadecimal) 1st Addr	1st Data	2nd Addr	2nd Data	3rd Addr	3rd Data	4th Addr	4th Data	5th Addr	5th Data	6th Addr	6th Data
Read[3,4]	1	RA	RD										
Reset[5]	1	XXXX	F0										
Auto-select[6]													
Manufacturer Equiv. ID	4	5555	AA	2AAA	55	5555	90	XX00	01				
Device Equiv. ID	4	5555	AA	2AAA	55	5555	90	XX01	20				
Sector Protect Verify[7,8]	4	5555	AA	2AAA	55	5555	90	(SA) X02	00 01				
Program[9]	4	5555	AA	2AAA	55	5555	A0	PA	PD				
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA	30

Notes:
1. Bus Operations are described in Table 2.
2. All command bus cycles are write operations, except when reading array or auto-select data.
3. No unlock or command cycles are required when reading array data.
4. RA = Address of the memory location to be read; RD = Data read from location RA during read operation
5. The Reset command is required to return to reading array data when device is in the auto-select mode, or if DQ5 goes high (while the device is providing status data).
6. The fourth cycle of the "Auto-select Command Sequence" is a read operation.
7. The data is 00H for an unprotected sector and 01h for a protected sector. See "Auto-select Command Sequence" for more information.
8. SA = Address of the sector to be verified (in auto-select mode) or erased. Address bits A16-A14 uniquely select any sector
9. PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens later; PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever happens first.
10. Address bit A16 and A15 =x (don't care) for all address commands except for Program Address (PA), Read Address (RA) and Sector Address (SA).
11. X = Don't Care.

A read cycle at address XX00H or retrieves the manufacturer code. A read cycle at address XX01H returns the device code. A read cycle containing a sector address (SA) and the address 02H in returns 01H if that sector is protected, or 00H if it is unprotected. Refer to the Sector Address tables for valid sector addresses.

The system must write the reset command to exit the auto-select mode and return to reading array data.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program setup command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. The Command Definitions Table (Table 5) shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See "Write Operation Status" for information on these status bits.

Commands written to the device while the Embedded Program Algorithm is in progress are ignored.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a '0' back to a '1'.** Attempting to do so may halt the operation and set the error status bit, DQ5, to '1', or cause the $\overline{\text{Data}}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still '0'. Only erase operations can convert a '0' to a '1'.

Note: See Command Definitions (Table 5) for program command sequence.

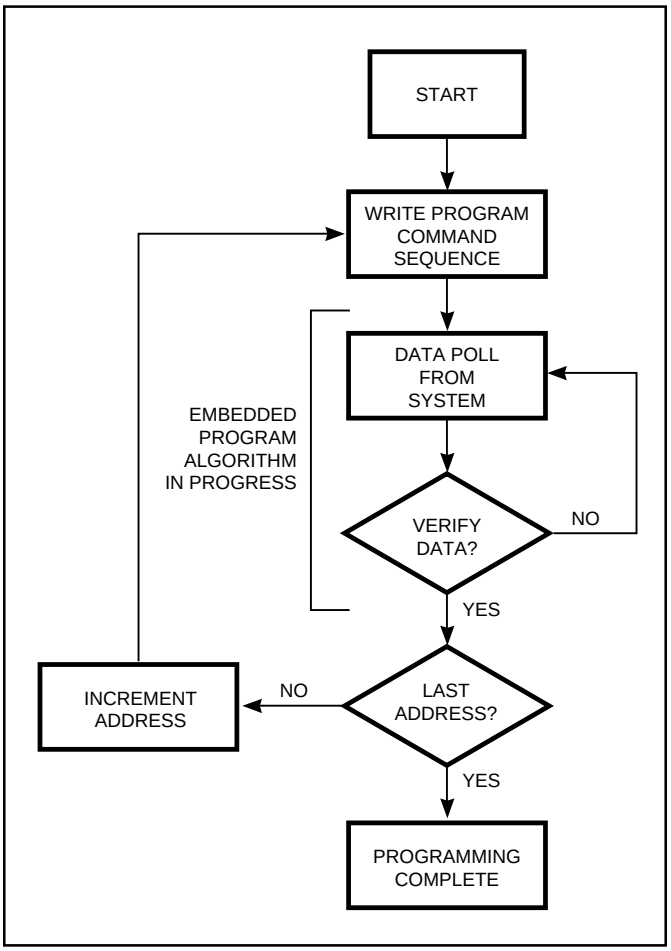


Figure 5. Program Operation

Chip Erase Command Sequence

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a setup command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Commands written to the chip while the Embedded Erase Algorithm is in progress are ignored.

The system can determine the status of the erase operation by using DQ7 or DQ6. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 6 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a setup command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions Table (Table 5) shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The embedded erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

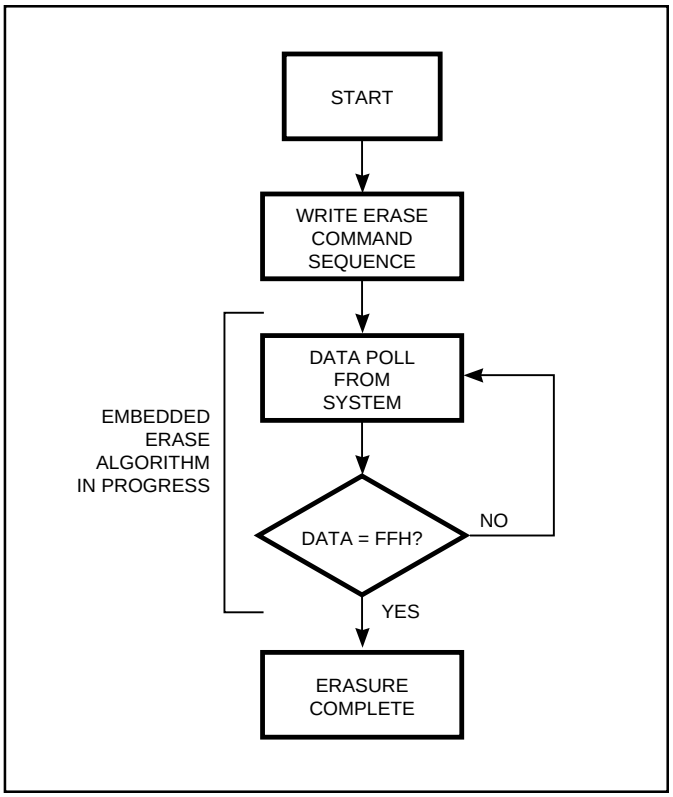


Figure 6. Erase Operation

Notes:
1. For Erase Command Sequence. See Command Definitions table.
2. See "DQ3: Sector Erase Timer" for more information.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. Any command during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Once the sector erase operation has begun, all other commands are ignored.

When the embedded erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6. Refer to "Write Operation Status" for information on these status bits.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ3, DQ5, DQ6, and DQ7. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. Table 6 and the following subsections describe the functions of these bits.

DQ7: $\overline{\text{Data}}$ Polling

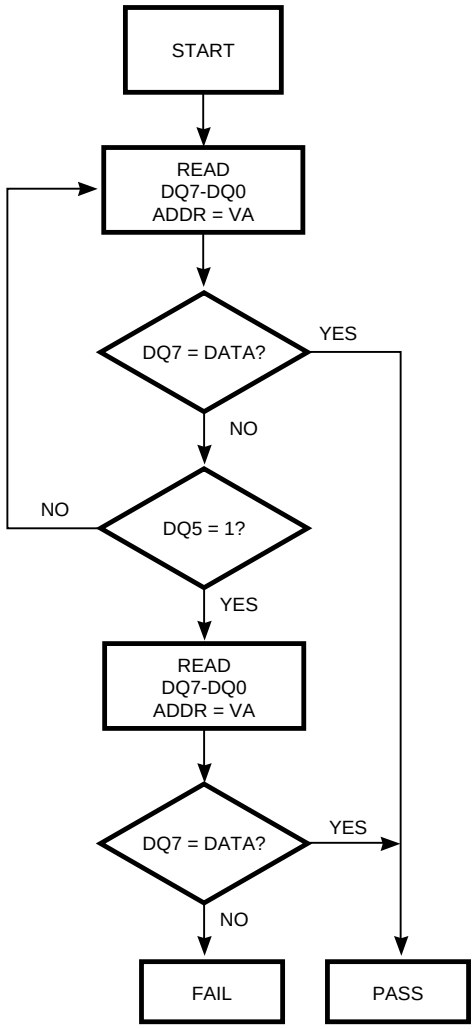
The $\overline{\text{Data}}$ Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed. $\overline{\text{Data}}$ Polling is valid after the rising edge of the final $\overline{\text{WE}}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. When the Embedded Program algorithm is complete, the device outputs the true datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ7 is active for approximately 2 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{\text{Data}}$ Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, $\overline{\text{Data}}$ Polling produces a "1" on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7-DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0-DQ6 while Output Enable ($\overline{\text{OE}}$) is asserted low. The $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithms) figure in the "AC Characteristics" section illustrates this.



Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 ="1" because DQ7 may change simultaneously with DQ5.

Figure 7. $\overline{\text{Data}}$ Polling Algorithm

Table 6 shows the outputs for $\overline{\text{Data}}$ Polling on DQ7. Figure 7 shows the $\overline{\text{Data}}$ Polling algorithm.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

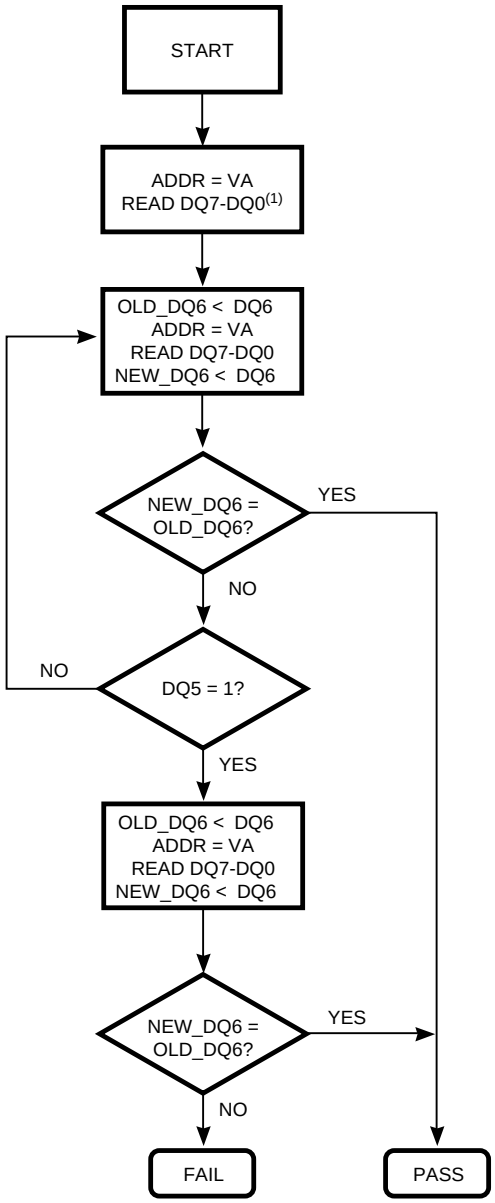
If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

The Write Operation Status table shows the outputs for Toggle Bit I on DQ6. Refer to Figure 8 for the toggle bit algorithm, and to the Toggle Bit Timings figure in the "AC Characteristics" section for the timing diagram.

Reading Toggle Bit DQ6

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7-DQ0 at least twice in a row to determine whether a toggle bit is toggling.

Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7-DQ0 on the following read cycle.



Notes:
1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as DQ5 changes to '1'. See text.
3. VA = Valid Address.

Figure 8. Toggle Bit Algorithm

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle as not successfully completed.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on DQ7 ($\overline{\text{Data}}$ Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for DQ3.

Table 6. Write Operation Status

Operation	DQ7[1]	DQ6	DQ5[2]	DQ3
Embedded Program Algorithm	DQ7#	Toggle	0	N/A
Embedded Erase Algorithm	0	Toggle	0	1

Notes:
1. DQ7 requires a valid address when reading status information.
2. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND		
	Any Pin Except A9	–2.0 to +7.0[2]	V
	A9	–2.0 to +12.5[2]	V
	V_{CC}	–2.0 to +7.0[2]	V
I_{SC}	Output Short Circuit Current (Max. Limit)	200	mA
T_A	Commercial Operating Temperature	0 to +70	°C
T_A	Industrial Operating Temperature	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +125	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC inputs, I/O, and A9 pins voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods less than 20 ns. Maximum DC voltage on output pins is Vcc + 0.5V, which may overshoot to Vcc + 2.0V for periods less than 20 ns. Maximum DC voltage on A9 is +12.5V that may overshoot to +12.5V for periods less than 20 ns.
3. No more than one output shorted at one time. Duration of short shall not exceed one second.

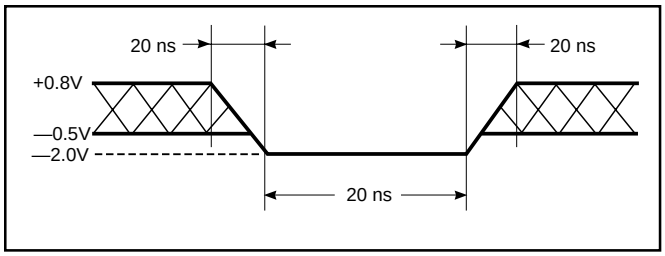


Figure 9. Maximum Negative Overshoot Waveform

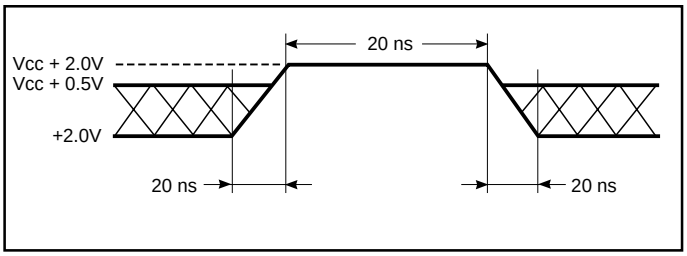


Figure 10. Maximum Positive Overshoot Waveform

OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	–40°C to +85°C	5V ± 10%

Note:
1. Operating ranges define those limits between which the functionally of the device is guaranteed.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3	6	pF
$C_{OC/C}$	Output and Control Capacitance	V_{OUT} = 0V	7	12	pF

DC CHARACTERISTICS: TTL/NMOS COMPATIBLE

Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ to GND	—	±1.0	µA
I_{LI2}	A9 Input Current	$V_{CC} = V_{CC}$ Max., A9 = 12.5V	—	50	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., V_{OUT} = GND to V_{CC}	—	±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max., $\overline{CE}$ and $\overline{OE} = V_{IH}$	—	1.0	mA
I_{CC1}	V_{CC} Active Current(1)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	30	mA
I_{CC2}	V_{CC} Active Current(2,3)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	50	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage For Auto-select and Temporary Sector Unprotect	V_{CC} = 5.0V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	2.4	—	V

Notes:
1. The I_{CC} current listed is typically less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Program or Embedded Erase Algorithm is in progress.
3. Not 100% tested.

DC CHARACTERISTICS: CMOS COMPATIBLE

Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or GND	—	±1.0	µA
I_{LI2}	A9 Input Current	$V_{CC} = V_{CC}$ Max., A9 = 12.5V	—	50	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., V_{OUT} = GND to V_{CC}	—	±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max., $\overline{CE}$ = Vcc ± 0.5V, $\overline{OE} = V_{IH}$	—	100	µA
I_{CC1}	V_{CC} Active Current(1)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	30	mA
I_{CC2}	V_{CC} Active Current(2,3)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	50	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.5	V
V_{ID}	Voltage For Auto-select and Temporary Sector Unprotect	V_{CC} = 5.0V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min.	—	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	0.85 x V_{CC}	—	V
V_{OH2}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min.	V_{CC} – 0.4	—	V

Notes:
1. The I_{CC} current listed is typically less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Program or Embedded Erase Algorithm is in progress.
3. Not 100% tested.

AC CHARACTERISTICS: READ ONLY (Over Operating Range)

Std. Symbol	Parameter	-35 Min.	-35 Max.	-45 Min.	-45 Max.	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-90 Min.	-90 Max.	Unit
t_{RC}	Read Cycle Time[1]	35	—	45	—	55	—	70	—	90	—	ns
t_{CE}	Chip Enable Access Time[2]	—	35	—	45	—	55	—	70	—	90	ns
t_{ACC}	Address Access Time[3]	—	35	—	45	—	55	—	70	—	90	ns
t_{OE}	Output Enable Access Time	—	25	—	25	—	30	—	30	—	35	ns
t_{DF}	Chip Enable to Output High Z[1,4]	—	10	—	10	—	15	—	20	—	20	ns
t_{DF}	Output Enable to Output High Z[1,4]	—	10	—	10	—	15	—	20	—	20	ns
t_{OEH}	Output Enable Hold Time[1] Read	0	—	0	—	0	—	0	—	0	—	ns
	Toggle & Data Polling	10	—	10	—	10	—	10	—	10	—	
t_{OH}	Output Hold from First of Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurs First	0	—	0	—	0	—	0	—	0	—	ns

Notes:
1. Not 100% tested.
2. $\overline{OE} = V_{IL}$.
3. $\overline{CE}$ and $\overline{OE} = V_{IL}$.
4. Output Driver Disable Time.
5. See Figure 12 and Table 6 for test specifications.

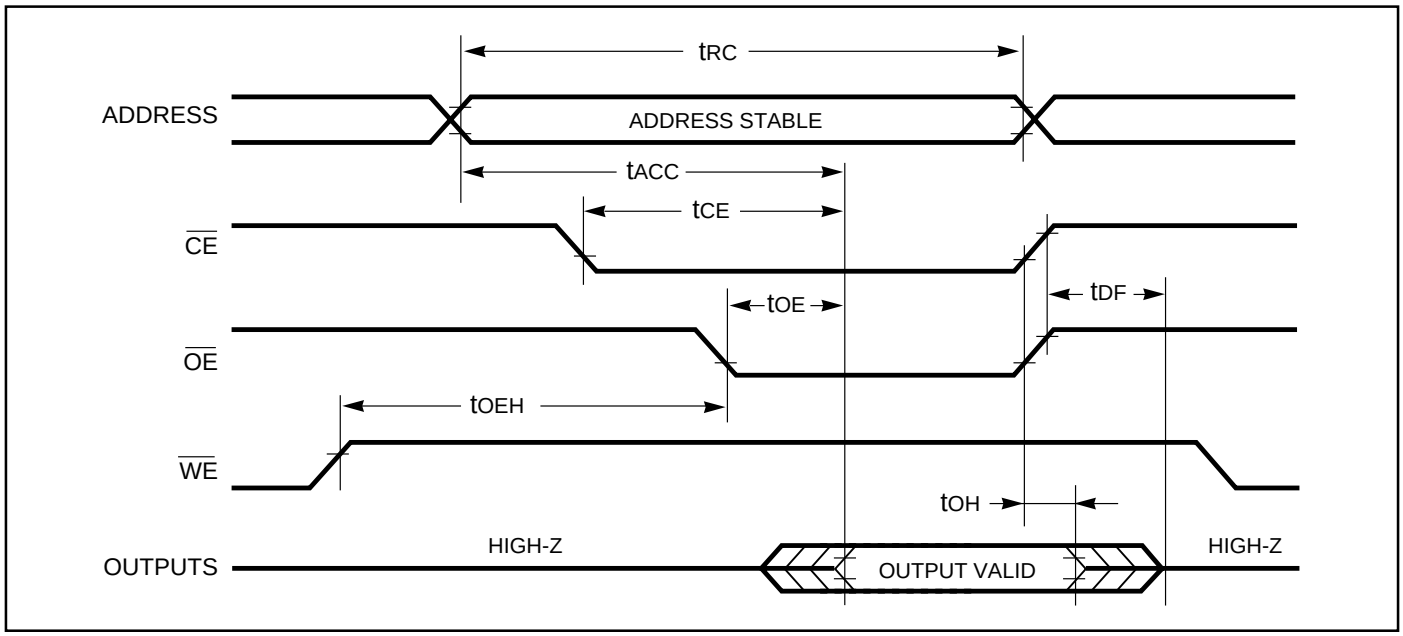


Figure 11. AC Waveform: READ Only

TEST CONDITIONS

Table 6. AC Test Specifications

Test Conditions	35 ns	All Others	Unit
Output Load		1 TTL Gate	
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Pulse Levels	0 to 3.0	0.45 to 2.4	V
Input Timing Measurement Reference Levels	1.5	0.8	V
Output Timing Measurement Reference Levels	1.5	2.0	V

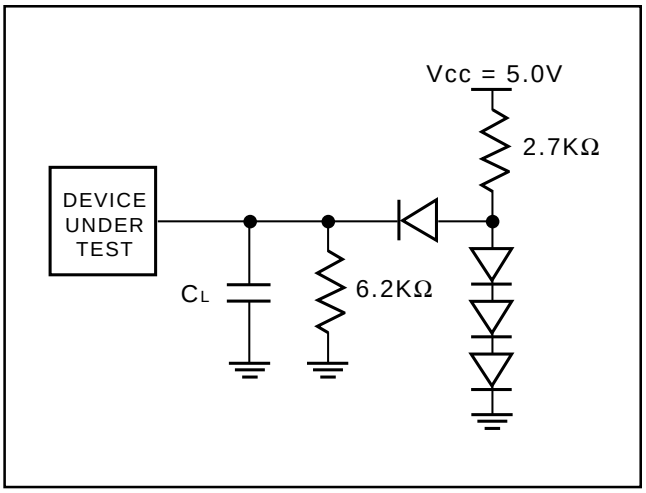


Figure 12. Test Setup

AC CHARACTERISTICS: ERASE AND PROGRAM

Std. Symbol	Parameter	-35 Min.	-35 Max.	-45 Min.	-45 Max.	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-90 Min.	-90 Max.	Unit
t_{WC}	Write Cycle Time[1]	35	—	45	—	45	—	45	—	90	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{AH}	Address Hold Time	30	—	35	—	45	—	45	—	45	—	ns
t_{DS}	Data Setup Time	15	—	20	—	20	—	30	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{GHWL}	Read Recovery Time before Write ($\overline{OE}$ HIGH to $\overline{WE}$ LOW)	0	—	0	—	0	—	0	—	0	—	ns
t_{CS}	$\overline{CE}$ Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{CH}	$\overline{CE}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	45	—	ns
t_{WPH}	Write Pulse Width HIGH	20	—	20	—	20	—	20	—	20	—	ns
t_{WHWH1}	Byte Programming Operation[2]	20	—	20	—	20	—	20	—	20	—	µs
t_{WHWH2}	Sector Erase Operation[2]	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	sec
t_{VCS}	V_{CC} Setup Time[1]	50	—	50	—	1.0	—	1.0	—	1.0	—	µs

Note:
1. Not 100% tested.

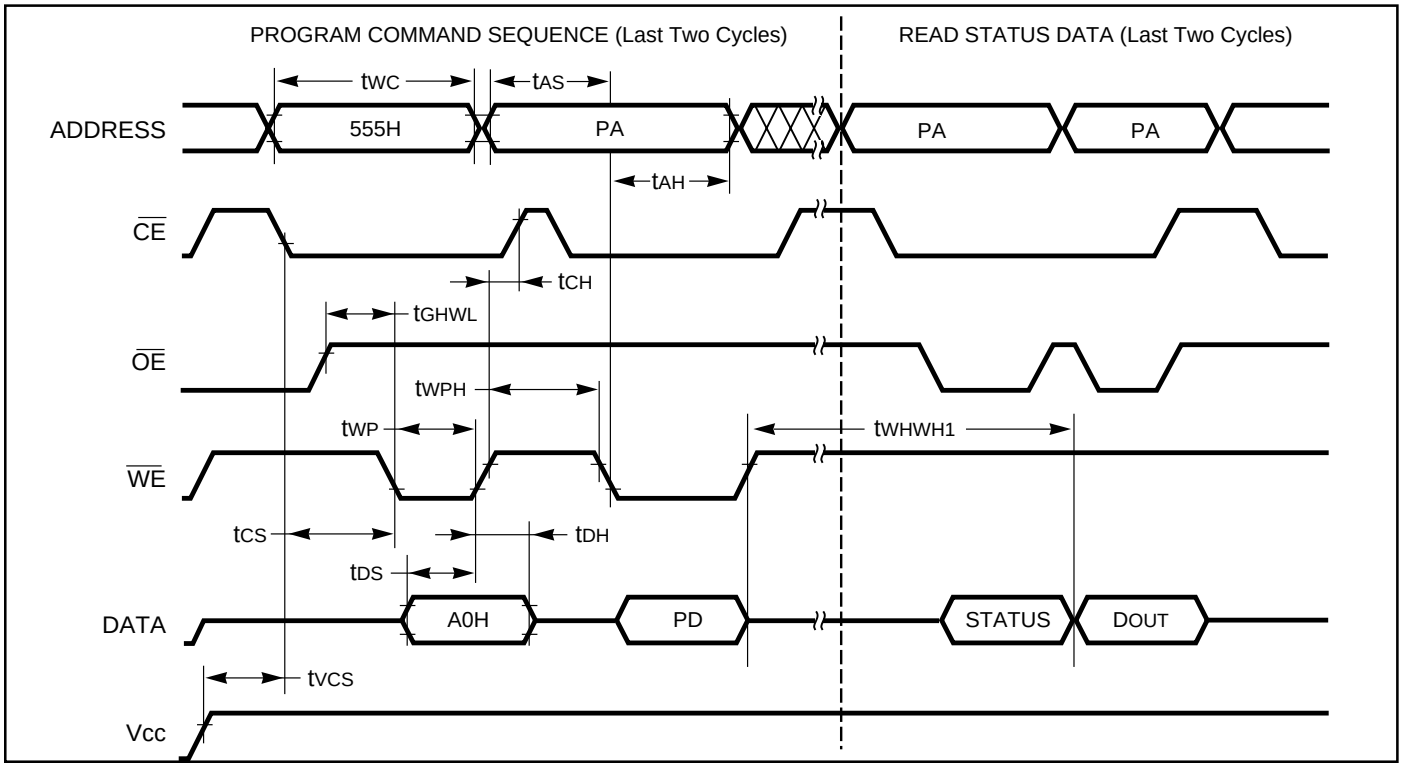


Figure 13. AC Waveform: Program Operation

Note:
1. PA = Program Address, PD = Program Data, DOUT is the true data at the Program Address.

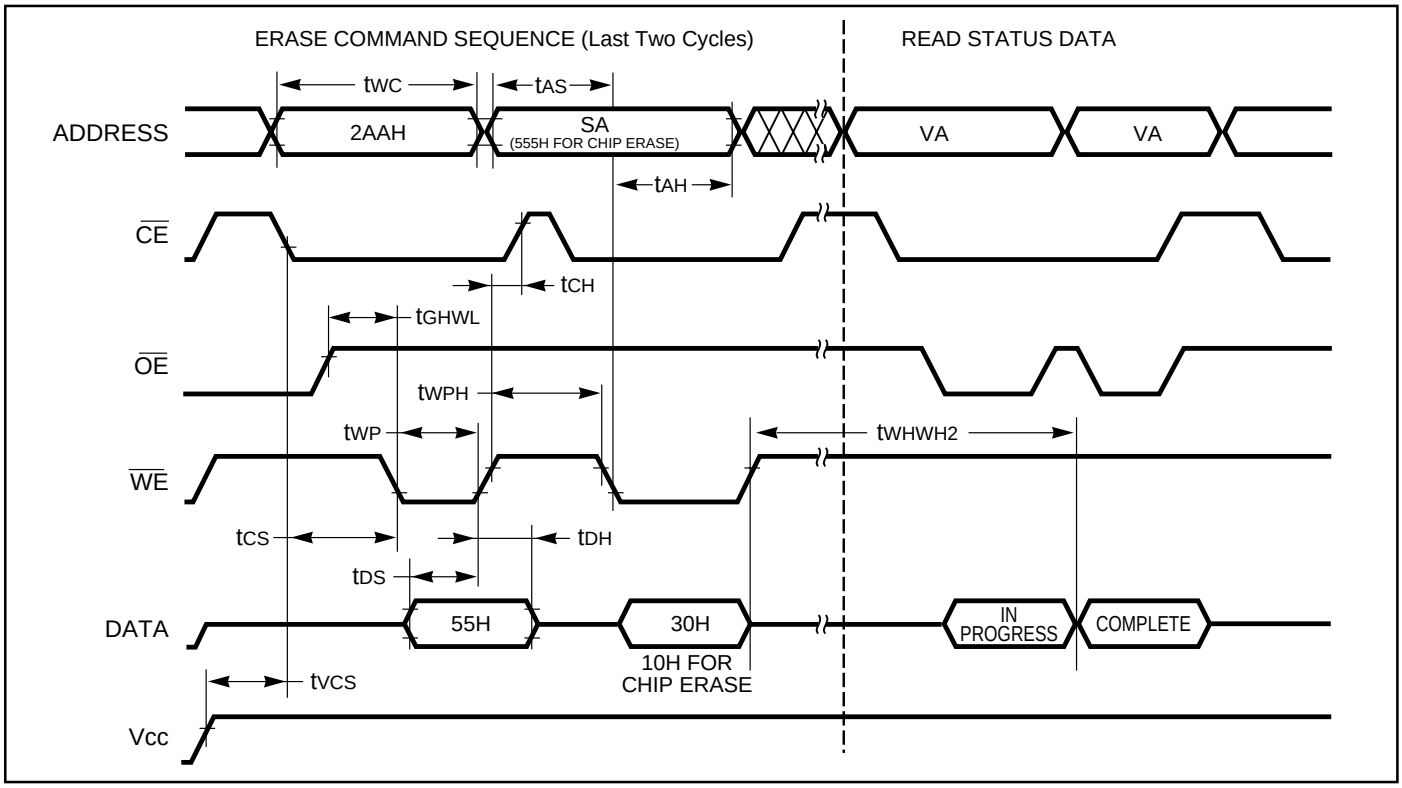


Figure 14. AC Waveform: Erase Operation

Note:
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").

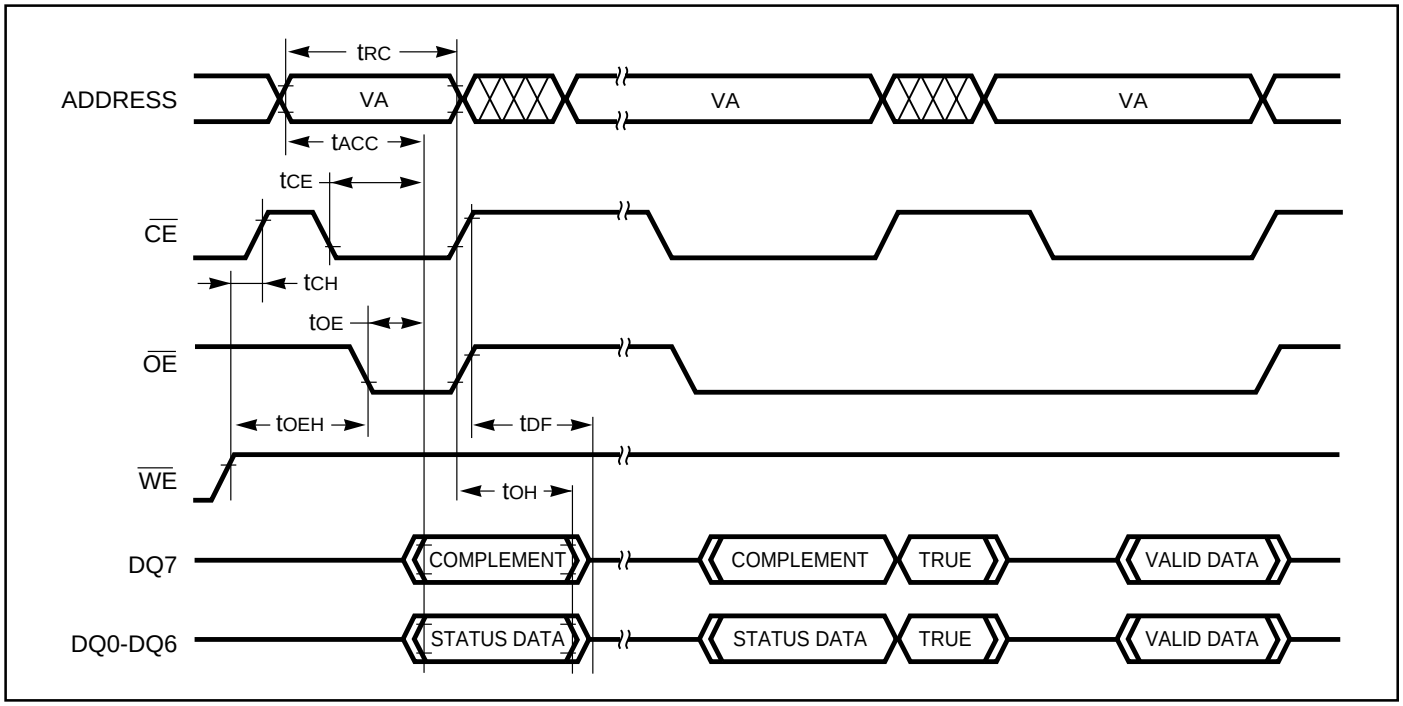


Figure 15. AC Waveform:

Note:
1. VA = Valid Address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

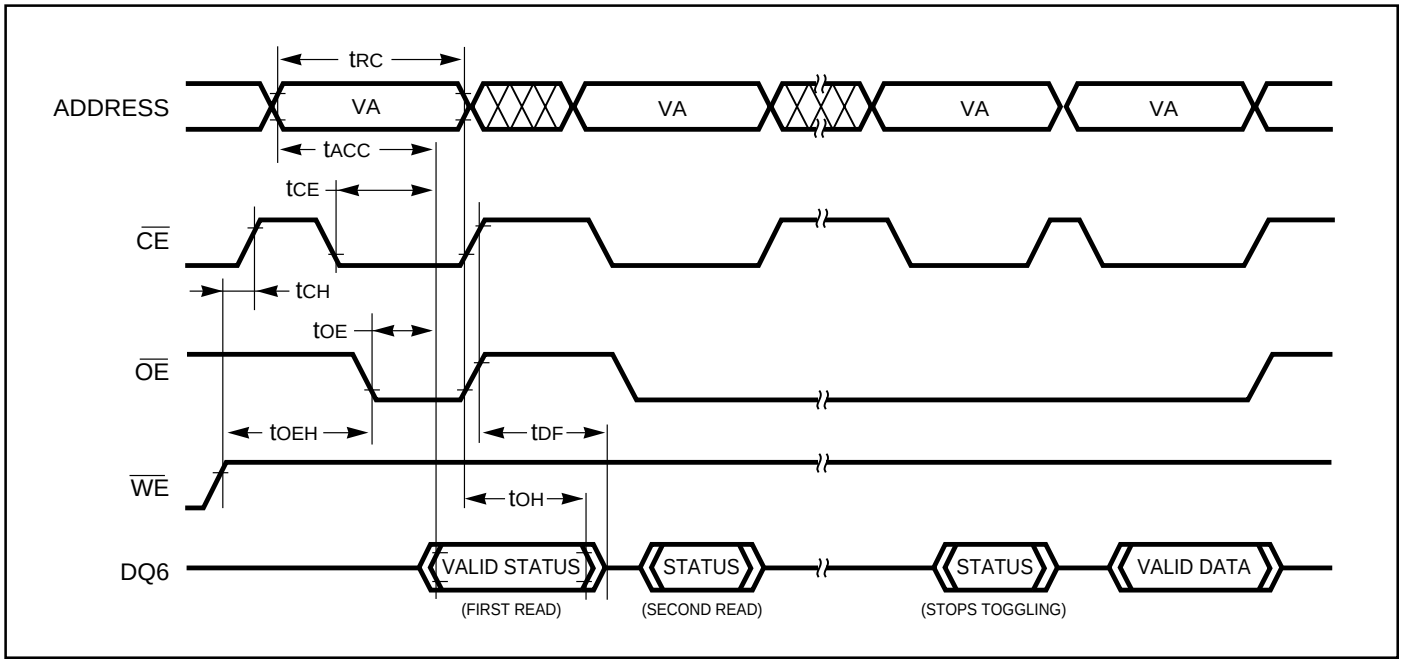


Figure 16. AC Waveform: Erase and Program Operations, Alternate $\overline{CE}$ Controlled Writes

Note:
1. VA = Valid Address, not required for DQ6. Illustration shows first two status cycles after command sequence, last status read cycle, and array data read cycle.

AC ELECTRICAL CHARACTERISTICS

Std. Symbol	Parameter	-35 Min.	-35 Max.	-45 Min.	-45 Max.	-55 Min.	-55 Max.	-70 Min.	-70 Max.	-90 Min.	-90 Max.	Unit
t_{WC}	Write Cycle Time[1]	35	—	45	—	55	—	70	—	90	—	ns
t_{AS}	Addess Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{AH}	Address Hold Time	30	—	35	—	45	—	45	—	45	—	ns
t_{DS}	Data Setup Time	20	—	20	—	20	—	30	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OES}	Output Enable Setup Time[1]	0	—	0	—	0	—	0	—	0	—	ns
t_{GHWL}	Read Recovery Time Before Write	0	—	0	—	0	—	0	—	0	—	ns
t_{WS}	Write Enable Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{CP}	Chip Enable Pulse Width	20	—	25	—	30	—	35	—	45	—	ns
t_{CPH}	Chip Enable Pulse Width HIGH	20	—	20	—	20	—	20	—	20	—	ns
$t_{WHWH}1$	Byte Programming Operation[2]	20	—	20	—	20	—	20	—	20	—	µs
$t_{WHWH}2$	Sector Erase Operation[2]	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	sec

Note:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

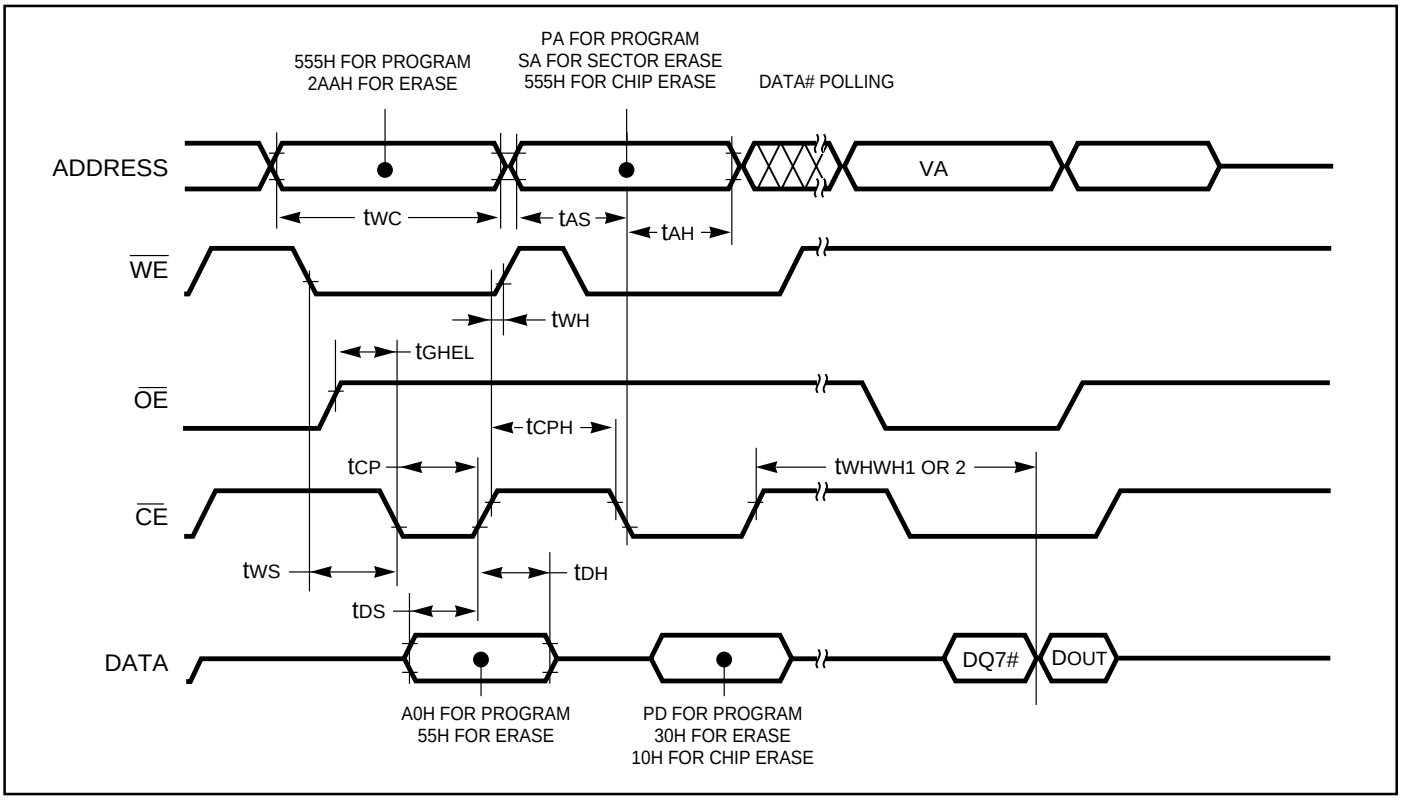


Figure 17. AC Waveform:

Note:
1. PA = Program Address, PD = Program Data, SA = Sector Address, DQ7# = Complement of Data Input, DOUT = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ.[1]	Max.[2]	Unit	Comments
Chip/Sector Erase Time	1.0	15	sec	Excludes 00H Programming Prior to Erase[4]
Byte Programming Time	27	300/1000	µs	Commercial / Industrial Temperature Excludes System Level Overhead[5]
Chip Programming Time[3]	3.5	12.5	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 5.0V Vcc, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.
2. Under worst case conditions for Commercial and Industrial temperature ranges, Vcc = 4.5V (4.75V for –35), 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed. If the maximum byte program time given is exceeded, only then does the device set DQ5 = 1. See the section on DQ5 for further information.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 2 for further information on command definitions.
6. The device has a typical erase and program cycle endurance of 1,000,000 cycles. 100,000 cycles are guaranteed.

LATCHUP CHARACTERISTIC

Parameter	Min.	Max.[2]
Input Voltage with Respect to GND on I/O Pins	–1.0V	V_{CC} + 1.0V
Vcc Current	–100 mA	+100 mA

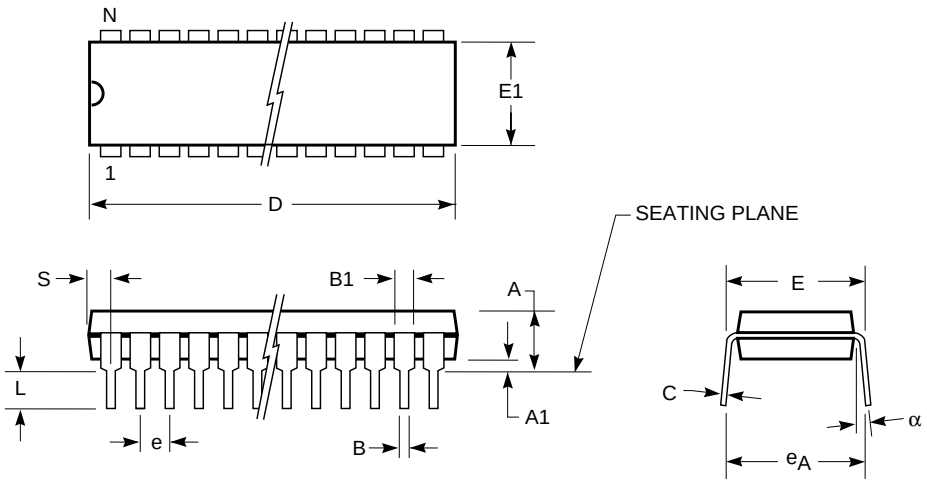
Note:
1. Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.

DATA RETENTION

Parameter	Test Conditions	Min.	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
Vcc Current	125°C	20	Years

PACKAGING INFORMATION

600-mil Plastic DIP
Package Code: W

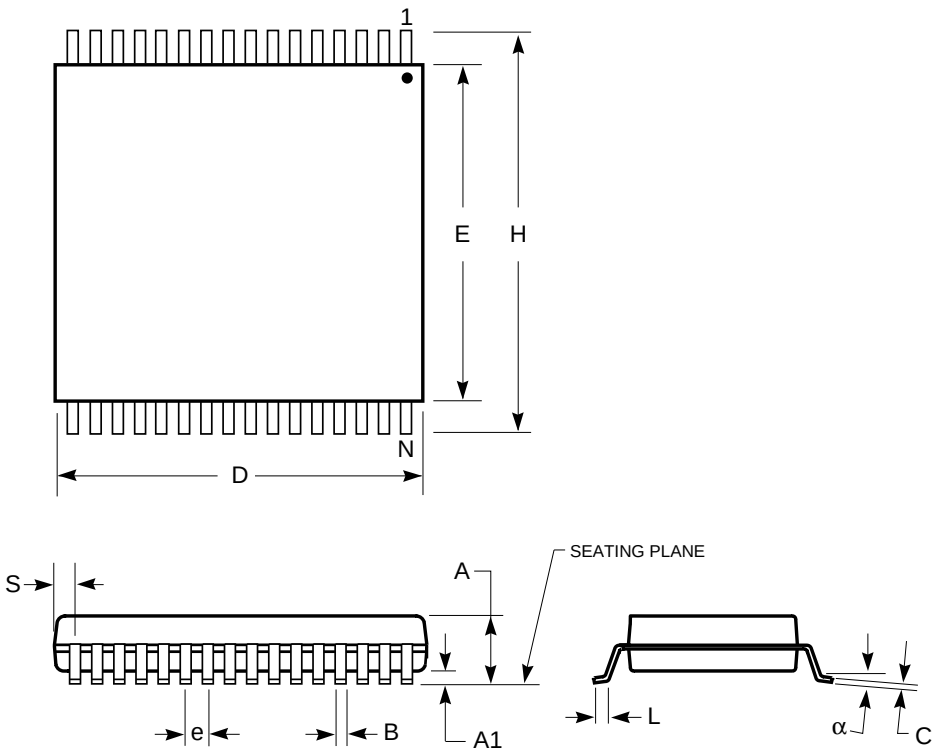


600-mil Plastic DIP (W)						
	Inches					
Symbol	Min	Max	Min	Max	Min	Max
Ref. Std.						
N	28		32		40	
A	0.160	0.185	0.165	0.180	0.165	0.200
A1	0.020	0.030	0.010	—	0.020	0.045
B	0.015	0.020	0.018		0.015	0.022
B1	0.050	0.065	0.050		0.045	0.067
C	0.008	0.012	0.010		0.008	0.015
D	1.420	1.460	1.645	1.655	2.045	2.055
E	0.600	0.620	0.590	0.610	0.600	0.620
E1	0.530	0.555	0.540	0.555	0.530	0.560
e_A	0.610	0.660	0.620	0.680	0.600	0.680
e	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.120	0.150	0.120	0.140	0.120	0.138
S	0.055	0.080	0.065	0.085	0.055	0.085
a	0°	15°	2°	8°	—	—

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Plastic TSOP - 32-pins
Package Code: T (Type I)

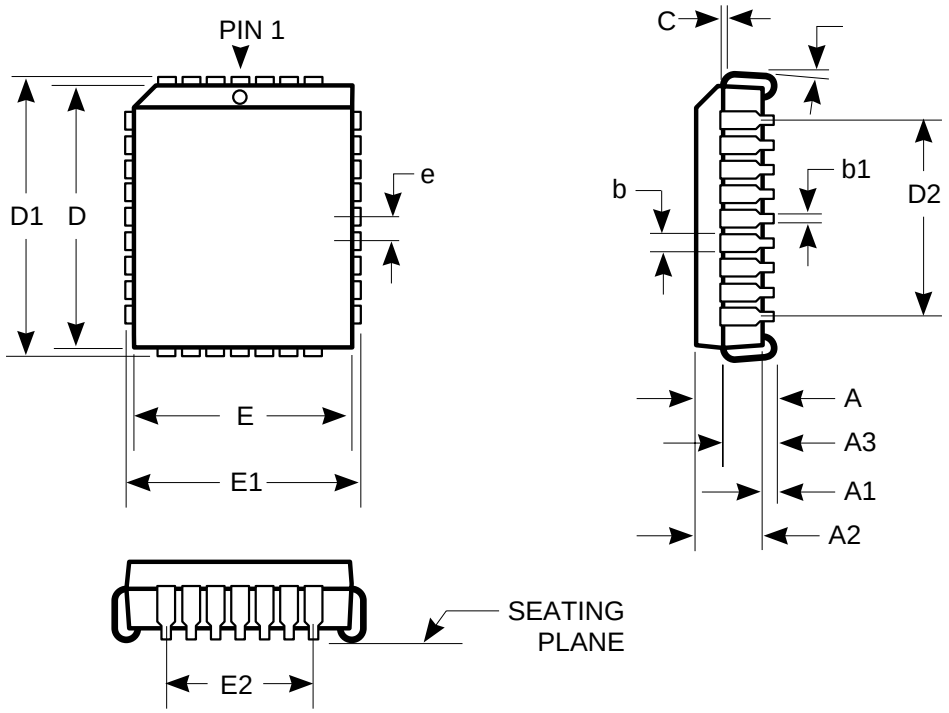


Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	32			
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.005
B	0.17	0.27	0.007	0.009
C	0.10	0.21	0.004	0.008
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.50	0.70	0.016	0.024
a	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

PLCC (Plastic Leaded Chip Carrier)
Package Code: PL



Plastic Leaded Chip Carrier (PL)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	3.33	3.56	0.131	0.140
A1	0.50	–	0.020	–
A2	2.67	2.93	0.105	0.115
A3	1.91	0.81	0.026	0.032
b	0.66	8.10	0.311	0.319
b1	0.33	0.54	0.013	0.021
C	0.20	0.35	0.008	0.014
D	13.89	14.05	0.547	0.553
D1	14.86	15.10	0.585	0.595
D2	–	7.62	–	0.400
E	11.35	11.51	0.447	0.453
E1	12.32	12.57	0.485	0.495
E2	–	7.62	–	0.300
e	1.27 BSC		0.050 BSC	
	0°	10°	0°	10°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.
5. ND and NE represent the number of leads in D and E directions, respectively.
6. D1 and E1 should be measured from the bottom of the package.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
35	NX29F010-35W NX29F010-45PL NX29F010-35T	600-mil Plastic DIP PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
45	NX29F010-45W NX29F010-45PL NX29F010-45T	600-mil Plastic DIP PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
55	NX29F010-55W NX29F010-55PL NX29F010-45T	600-mil Plastic DIP PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
70	NX29F010-70W NX29F010-70PL NX29F010-70T	600-mil Plastic DIP PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
90	NX29F010-90W NX29F010-90PL NX29F010-90T	600-mil Plastic DIP PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)

Note: Contact NexFlash Marketing for availability of DIP packages

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	NX29F010-45PLI NX29F010-45TI	PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
55	NX29F010-55PLI NX29F010-55TI	PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
70	NX29F010-70PLI NX29F010-70TI	PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)
90	NX29F010-90PLI NX29F010-90TI	PLCC – Plastic Leaded Chip Carrier TSOP (Type 1)

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The “Preliminary” designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

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(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

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