

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	LED ON Voltage Set Input	8	GND
2	Non Inverting Input(1)	9	LED1 Output
3	Inverting Input	10	LED2 Output
4	Non Inverting Input(2)	11	LED3 Output
5	Ref. Voltage	12	LED4 Output
6	LED Current Set Input	13	LED5 Output
7	V _{CC}	14	Amp. Output

■ Absolute Maximum Ratings (Ta = 25°C)

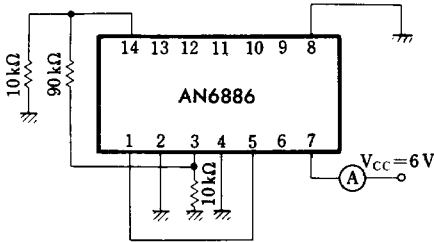
Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V _{CC}	18	V
	Circuit Voltage	V ₁₄₋₈	12	V
	Operational Amp. Input Voltage	V _{2,3,4-8}	-0.5 V _{CC}	V
	LED-ON Set Voltage	V ₁₋₈	V _{CC}	V
	LED Output Pin Voltage	V ₉₋₁₃₋₈	V _{CC}	V
Current	Supply Current	I _{CC}	15	mA
	LED Output Pin Current	I ₉₋₁₃	30	mA
	Reference Voltage Output Current	I ₅	-5	mA
	RA Pin Input Current	I ₆	10	mA
Power Dissipation (Ta ≤ 75°C)		P _D	480	mW
Temperature	Operating Ambient Temperature	T _{opr}	-30 ~ +75	°C
	Storage Temperature	T _{stg}	-55 ~ +150	°C

■ Electrical Characteristics (Ta = 25°C, V_{CC} = 6V)

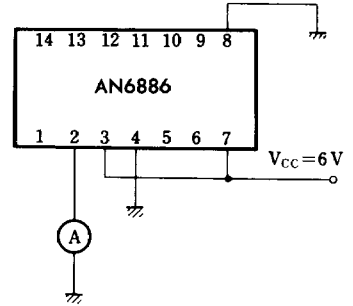
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Current Consumption	I _{tot}	1	V _{2,4-8} = 0V, R _A = Open		4	8	mA
Input Bias Current	I _{Bias2}	2		-1		0	μA
	I _{Bias4}	3		-1		0	μA
	I _{Bias3}	4		-2		0	μA
	I _{Bias14}	5		-5		0	μA
Output Offset Voltage	V _{O(Offset)}	6	V ₂₋₈ = 30mV, V ₄₋₈ = 0V, G _v = 20dB	200		400	mV
	V _{O(Offset)}	6	V ₄₋₈ = 30mV, V ₂₋₈ = 0V, G _v = 20dB	200		400	mV
Reference Voltage	V _{REF}	7		2.6	2.8	3	V
Output Sink Current	I _{SINK9-13}	8	R _A = Open	4		9	mA
	I _{SINK9-13}	9	R _A = 5.6kΩ	11		21	mA
Voltage Gain	G _{V1}	10	V ₂₋₈ = 0.1V, V ₄₋₈ = 0V	19	20	21	dB
	G _{V2}	11	V ₄₋₈ = 0.1V, V ₂₋₈ = 0V	19	20	21	dB
Comparator Level	GD ₁	8	Pin ⑨	-11	-10	-9	dB
	GD ₂	8	Pin ⑩	-5.5	-5	-4.5	dB
	GD ₃	8	Pin ⑪	-0.5	0	0.5	dB
	GD ₄	8	Pin ⑫	2.5	3	3.5	dB
	GD ₅	8	Pin ⑬	5	6	7	dB



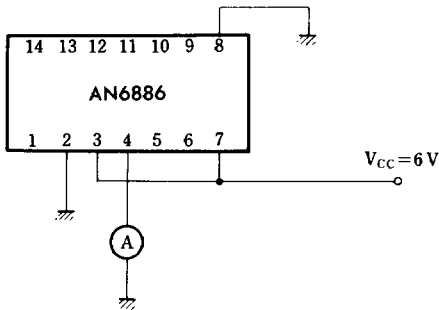
Test Circuit 1 (I_{Tot})



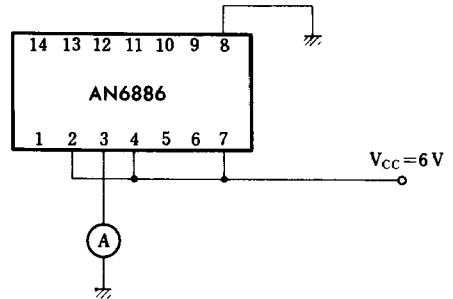
Test Circuit 2 (I_{Bias2})



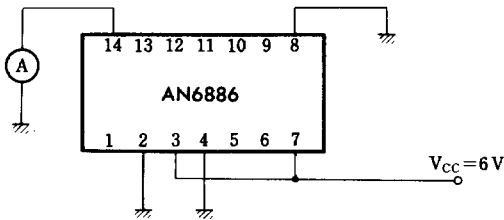
Test Circuit 3 (I_{Bias4})



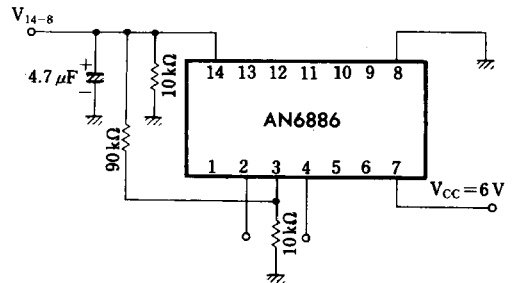
Test Circuit 4 (I_{Bias3})



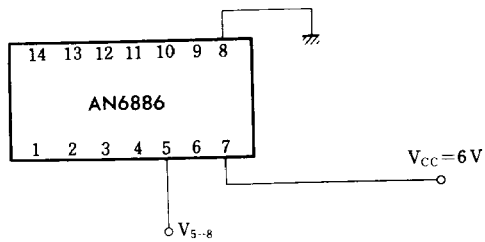
Test Circuit 5 (I_{Bias14})



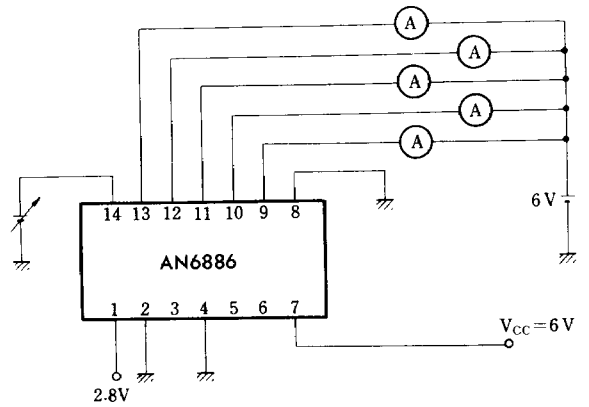
Test Circuit 6 ($V_{O(offset)}$)



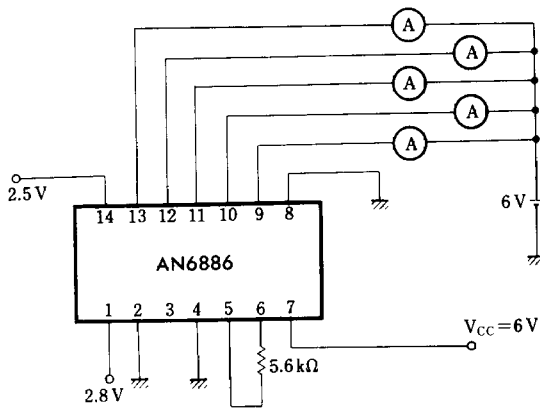
Test Circuit 7 (V_{REF})



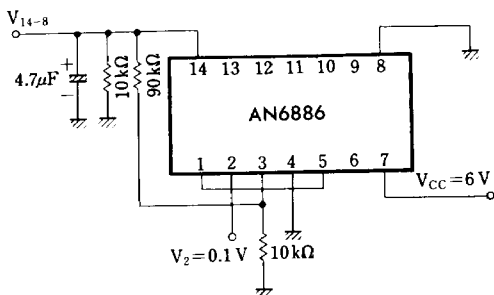
Test Circuit 8 ($I_{(SINK)9-13}$, $GD_1 \sim GD_5$)



Test Circuit 9 ($I_{(SINK)9-13}$)



Test Circuit 10 (G_{V1})



Test Circuit 11 (G_{V2})

