ADVANCE INFORMATION

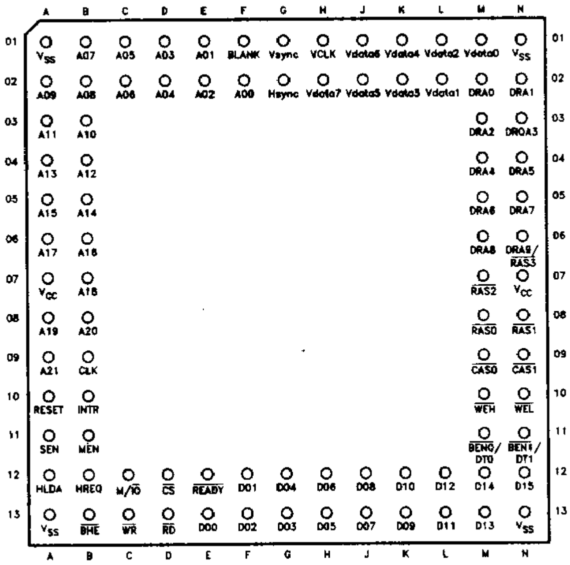
M82786
CHMOS GRAPHICS COPROCESSOR

Military

- **High Performance Graphics**
- **Fast Polygon and Line Drawing**
- **High Speed Character Drawing**
- **Advanced DRAM/VRAM Controller for Graphics Memory up to 4 Mbytes**
- **Supports up to 160 MHz CRTs**
  — up to 640 by 480 by 8 Bits (DRAMs) or 1400 by 1400 by 1 Bit (DRAMs)
  — 8 by 2048 by 8 Bits (VRAMs)
- **Up to 256 Simultaneous Colors**
- **Integral DRAM/VRAM Controller, Shift Registers and DMA Channel**
- **International Character Support**
- **Interface Designed for Device-Independent Standards**
- **Hardware Windows**
- **Fast Bit-Block Copies Between System and Bitmap Memories**
- **Third-Party Software Support**
- **Multi-tasking Support**
- **Provides Support for Rapid Filling with Patterns**
- **Programmable Video Timing**
- **Advanced CHMOS Technology**
- **Supports Dual Port Video DRAMs & Sequential Access DRAMs**
- **88-Pin Grid Array Hermetic Package**
- **Military Temperature Range: −55°C to +125°C (T_C)**

The M82786 is a powerful, yet simple component designed for microcomputer graphics applications including personal computers, engineering workstations, terminals, laser printers and a multitude of high resolution military displays. Its advanced software interface makes applications and systems level programming efficient and straight-forward. Its performance and high-integration make it a cost-effective component while improving the performance of nearly any design. Hardware windows provide instantaneous changes of display contents and support multiple graphics applications from multiple graphics bitmaps. Applications programs written for the IBM Personal Computer can be run within one or more windows of the display when used with Intel CPUs.

The M82786 works with all Intel microprocessors, and is a high-performance replacement for sub-systems and boards which have traditionally used discrete components and/or software for graphics functions. The M82786 requires minimal support circuitry for most system configurations, and thus reduces the cost and board space requirements of many applications. The M82786 is based on Intel's advanced CHMOS III process.


A B C D E F G H J K L M N
01 Vss A07 A05 A03 A01 BLANK Vsync VCLK Vdata6 Vdata4 Vdata2 Vdata0 Vss
02 A09 A08 A06 A04 A02 A00 Hsync Vdata7 Vdata5 Vdata3 Vdata1 DRA0 DRA1
03 A11 A10 DRA2 DROA3
04 A13 A12 DRA4 DRA5
05 A15 A14 DRA6 DRA7
06 A17 A16 DRA8 DRA9/RAS3
07 Vcc A18 RAS2 Vcc
08 A19 A20 RAS0 RAS1
09 A21 CLK CAS0 CAS1
10 RESET INTR WEH WEL
11 SEN MEN BEN0/DT0 BEN1/DT1
12 HLDA HREQ M/IO CS READY D01 D04 D06 D08 D10 D12 D14 D15
13 Vss BHE WR RD D00 D02 D03 D05 D07 D09 D11 D13 Vss

271071-27

Figure 1. M82786 Pinout—Bottom View

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INTRODUCTION

The M82786 is an intelligent peripheral capable of both drawing and refreshing raster displays. It has an integrated drawing engine with high level VDI like graphics commands. Multiple character sets (fonts) can be used simultaneously for text display applications. The M82786 provides hardware support for fast manipulation and display of multiple windows on the screen. It supports high resolution displays with a 20 MHz pixel clock and can display up to 256 colors simultaneously. Using multiple M82786s and/or in conjunction with dual port video DRAMs (VRAMs), the M82786 is virtually unlimited in terms of color support and resolution.

Table 1. M82786 Pin Description

Symbol	Pin Number	Type	Description
A21:0	A09,B08,A08,B07, A06,B06,A05,B05, A04,B04,A03,B03, A02,B02,B01,C02, C01,D02,D01,E02, E01, F02	I/O	Address lines for the External Bus. Inputs for Slave Mode accesses of the M82786 supported Graphics memory array or M82786 internal memory or I/O mapped registers. Driven by the M82786 when it is the External Bus Master.
D15:0	N12,M12,M13,L12, L13,K12,K13,J12, J13,H12,H13,G12, G13,F13,F12,E13	I/O	Data Bus for the M82786 Graphics memory array and the External Bus.
$\overline{\text{BHE}}$	B13	I/O	Byte High Enable. An input of the M82786 Slave Interface; driven LOW by the M82786 when it is Bus Master. Determines asynchronous vs. synchronous operation for $\overline{\text{RD}}$, $\overline{\text{WR}}$ and HLDA inputs at the falling (trailing) edge of RESET. A HIGH state selects synchronous operation.
$\overline{\text{RD}}$	D13	I/O	Read Strobe. An input of the M82786 Slave Interface; driven by the M82786 when it is Bus Master. Selects normal/test mode at falling RESET.
$\overline{\text{WR}}$	C13	I/O	Write Strobe. An input of the M82786 Slave Interface; driven by the M82786 when it is Bus Master. Selects normal/test mode at falling edge of RESET.
M/$\overline{\text{IO}}$	C12	I/O	Memory or I/O indication. An input of the M82786 Slave Interface; driven HIGH by the M82786 when it is the Bus Master. Determines synchronous M80286 or M80186 interface at the falling edge of RESET. A LOW state selects a synchronous M80286 interface.
$\overline{\text{CS}}$	D12	I	Chip Select. Slave Interface input qualifying the access.
MEN	B11	O	Master Enable. Driven HIGH when the M82786 controls the External Bus. (i.e., HLDA received in response to a M82786 HREQ.) Used to steer the data path and select source of bus cycle status commands.
SEN	A11	O	Slave Enable. Driven HIGH when the M82786 is executing a Slave bus cycle for an External Master into the M82786 graphics memory or registers. Used to enable the data path and as a READY indication to the External Bus Master.
$\overline{\text{READY}}$	E12	I	Synchronous input to the M82786 when executing External Bus cycles. Identical to M80286 $\overline{\text{READY}}$.

Table 1. M82786 Pin Description (Continued)

Symbol	Pin Number	Type	Description
HREQ	B12	O	Hold Request. Driven HIGH by the M82786 when an access is being made to the External Bus by the Display or Graphics Processors. Remains HIGH until the M82786 no longer needs the External Bus.
HLDA	A12	I	Hold Acknowledge. Input in response to a HREQ output. Asynchronous vs. synchronous input determined by state of $\overline{\text{BHE}}$ pin at falling RESET.
INTR	B10	O	Interrupt. The logical OR of a Graphics Processor and Display Processor interrupt. Cleared with an access to the BIU Control Register.
RESET	A10	I	Reset input, internally synchronized, halts all activity on the M82786 and brings it to a defined state. The leading edge of RESET synchronizes the M82786 clock to phase 2. The trailing edge latches the state of $\overline{\text{BHE}}$ to establish the type of Slave Interface. It also latches $\overline{\text{RD}}$, $\overline{\text{WR}}$ and MIO to set certain test modes.
CLK	BO9	I	Double frequency clock input. Clock input to which pin timings are referenced. 50% duty cycle.
$\overline{\text{CAS0}}$	M09	O	Column Address Strobe 0. Drives the CAS inputs of the even word Graphics memory bank if interleaved; identical to $\overline{\text{CAS1}}$ if non interleaved Graphics memory. Capable of driving 16 DRAM/VRAM CAS inputs.
$\overline{\text{CAS1}}$	N09	O	Column Address Strobe 1. Drives the CAS inputs of the odd word Graphics memory bank if interleaved; identical to $\overline{\text{CAS0}}$ if non-interleaved Graphics memory. Capable of driving 16 DRAM/VRAM CAS inputs.
$\overline{\text{RAS2:0}}$	M07,N08,M08	O	Row Address Strobe. Drives the RAS input pins of up to 16 DRAMs/VRAMs. Drives the first three rows of both banks of Graphics memory.
DRA9/$\overline{\text{RAS3}}$	N06	O	Multiplexed most significant Graphics memory address line and $\overline{\text{RAS3}}$. DRA9 when using 1 Mb DRAMS; $\overline{\text{RAS3}}$ otherwise.
$\overline{\text{WEL}}$	N10	O	Write Enable Low Byte. Active LOW strobe to the lower order byte of Graphics memory.
$\overline{\text{WEH}}$	M10	O	Write Enable High Byte. Active LOW strobe to the higher order byte of Graphics memory.
DRA8:0	M06,N05,M05, N04,M04,N03, M03,N02,M02	O	Multiplexed Graphics memory Address. Graphics memory row and column address are multiplexed on these lines. Capable of driving 32 DRAMs/VRAMs.
$\overline{\text{BEN1:0}}$ DT1:0	N11,M11	O	Multiplexed Bank Enable and Data Transfer Line. In normal memory cycle enables the output of the Graphics memory array on to the M82786 data bus, D15:0. In data transfer cycle, loads the serial register in dual port video DRAMs (VRAMs). $\overline{\text{BEN1}}$/DT1 and $\overline{\text{BEN0}}$/DT0 control Bank1 and Bank0 respectively.
BLANK	F01	I/O	Output used to blank the display at particular positions on the screen. May also be configured as input to allow the M82786 to be synchronized with external sources.

Table 1. M82786 Pin Description (Continued)

Symbol	Pin Number	Type	Description
$V_{DATA}7{:}0$	H02,J01,J02, K01,K02,L01, L02,M01	O	Video data output.
V_{CLK}	H01	I	Video Clock input used to drive the display section of the M82786. Maximum frequency of 20 MHz.
H_{SYNC}/WS0	G02	I/O	Horizontal Sync. Window status is multiplexed on this pin. May also be configured as input to allow the M82786 to be synchronized with external sources. May also be configured to output Window status.
V_{SYNC}/WS1	G01	I/O	Vertical Sync. Window status is multiplexed on this pin. May also be configured as input to allow the M82786 to be synchronized with external sources. May also be configured to output Window status.
V_{SS}	A01,N01,A13, N13	P	4 V_{SS} pins.
V_{CC}	N07,A07	P	2 V_{CC} pins.

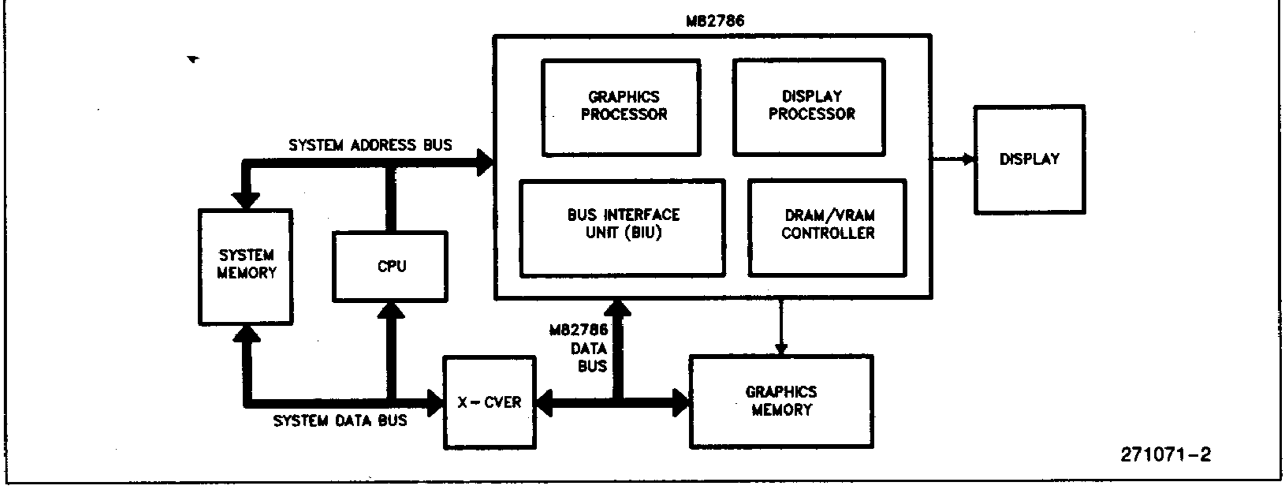


Figure 2

ARCHITECTURE

The M82786 is a high integration device which contains three basic modules (Figure 2):

1. Display Processor (DP)
2. Graphics Processor (GP)
3. Bus Interface Unit (BIU) with DRAM/VRAM Controller.

Display Processor

The M82786 Display Processor controls the CRT timings and generates the serial video data stream for the display. It can assemble several windows on the screen from different bitmaps scattered across the memory accessible to the M82786.

Graphics Processor

The M82786 Graphics Processor executes commands from a Graphics Command Block (GCMB) (placed in memory by the host CPU) and updates the bitmap memory for the Display Processor. The Graphics Processor has high level VDI like commands and can draw graphical objects and text at high speeds.

Bus Interface Unit (BIU)

The BIU controls all communication between the M82786, external CPU and memory. The BIU includes an integrated DRAM/VRAM controller that can take advantage of the high speed burst access modes of page mode and fast page mode DRAMs to perform block transfers. The Display Processor and Graphics Processor use the BIU to access the bitmaps in memory.

Memory Structure and Internal Registers

The M82786 address range is 4 Mbytes. This is divided between the graphics memory directly supported by the M82786 and external system memory. The M82786 distinguishes between graphics memory and external system memory by assuming graphics memory space starts at address 0H and goes up to whatever amount of graphics memory is configured. External system memory occupies the rest of the address space. The amount of graphics memory configured, and therefore the graphics memory/external system memory boundary, is controlled by the "DRAM/VRAM Control Register" in the BIU. The upper limit of configured graphics memory is 4 Mbytes.

A 128 byte block (contiguous) of internal control registers is distributed throughout the three modules on the M82786. This block can be either memory or I/O mapped in the CPU address space. The base address and memory or I/O mapped for this register block is programmable through the "Internal Relocation Register" in the BIU.

External Memory Access (Master Mode)

The M82786 initiates "Master Mode" AUTOMATICALLY whenever access to a memory address beyond the upper limit of configured graphics memory is attempted. This memory is typically external memory shared between the M82786 and the external CPU. The bus timings in this mode are similar to the M80286 style bus timings.

An M82786 request for the bus is indicated by a high level on the HREQ line. The M82786 drives the external bus (A21:0, D15:0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, MIO and $\overline{\text{BHE}}$) only after receiving a HLDA (acknowledge) from the external master. The HLDA line could be externally synchronized (M82786 synchronous mode) or internally synchronized (M82786 asynchronous mode). The M82786 will deactivate the HREQ line when it no longer needs to access external memory or when it senses an inactive HLDA. The M82786 indicates that it is in control of the external bus by a high level on the MEN output. Screen corruption can occur if the external CPU is not configured to handshake with the M82786. In this case, the M82786 will wait indefinitely for the HLDA, in response to its HREQ, and no DRAM refresh will be generated.

CAUTION: The external CPU should be configured to handshake with the M82786, including HREQ/HLDA. Any attempts at accessing memory beyond the limit of graphics memory will AUTOMATICALLY send the M82786 into "Master Mode". If the M82786 does not receive a HLDA in response to its HREQ, it will wait indefinitely—no DRAM refresh will be generated and screen corruption will occur.

Slave Mode

The M82786 Slave Interface allows an external CPU access into the graphics memory array or the M82786 Internal Registers. The external CPU directs a (read/write) slave access to the M82786 by asserting the M82786 $\overline{\text{CS}}$ input. When the M82786 is not driving the external bus, the A21:0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, MIO and $\overline{\text{BHE}}$ lines are inputs. The $\overline{\text{RD}}$, $\overline{\text{WR}}$, MIO and $\overline{\text{CS}}$ lines are constantly monitored by the M82786 to detect a CPU cycle directed at the M82786. After beginning a slave access to the M82786, the external CPU must go into a wait state. The M82786 will not process new slave commands from the CPU before the previous command has been serviced. The M82786 initiates a slave access by a high level on the SEN output and terminates the slave access when SEN is low. The data bus transceivers can be enabled by SEN.

SEN as Slave Ready Indication

Inverted SEN should be connected to the M82C284 ARDY input when the Slave Interface is set in synchronous M80286 mode. The number of wait states for a read cycle is a function of the DRAM/VRAM speed. Write cycles execute with 2 wait states because the M82786 issues SEN with different timing during write cycles.

The M82786 supports byte accesses to graphics memory. The combination of $\overline{\text{BHE}}$ and A0 generate the proper $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ signals. $\overline{\text{BHE}}$ and A0 are ignored for read cycles. Since the Display and Graphics Processors always generate word addresses, the slave cycles directed to graphics memory are the only time $\overline{\text{WEL}}$ may not exactly follow $\overline{\text{WEH}}$.

The M82786 will acknowledge a slave access from an external CPU while waiting for an acknowledge (HLDA) to its own request for the external bus. This prevents a potential deadlock situation.

Synchronous/Asynchronous Operation

The synchronous/asynchronous mode is selected by the state of the $\overline{\text{BHE}}$ input at the falling edge of reset. A high state selects synchronous operation. The synchronous interface requires that the M82786 and the M80286/M80186 clock inputs are shared. For the M80286 case, a common RESET ensures that the M82786 and the M80286 initialize to the same state. With the M80186, external hardware must ensure that the M82786 phase1 is coincident with the M80186 CLKOUT LOW. In the Master Mode, the HLDA line is sampled synchronously or asynchronously. The M82786 slave interface provides for synchronous or asynchronous sampling of the command lines ($\overline{\text{RD}}$ and $\overline{\text{WR}}$).

EIGHT AND SIXTEEN BIT HOST

On reset, the M82786 always assumes an 8 bit host interface. The first few accesses to the M82786 must be 8 bit accesses. The M82786 can be switched to a 16 bit interface by setting the "BCP" bit in the "BIU Control Register".

In 16 bit mode, the Internal Register Block is only word addressable. Odd word or odd byte accesses to the internal locations will not produce the desired result. Even byte access, however will work as desired. The least significant address bit, A0, is ignored in 16 bit mode.

In 8 bit mode, the internal registers must be accessed by two successive bus cycles. This is not necessary for reads, but is necessary for writes to the internal registers. The low byte (A0 = 0) must be written first, followed by the high byte (A0 = 1) of the register. A21:1 must be the same for both bus cycles. The register is not changed until the second byte (the high byte) is written to the M82786. There is no restriction on the time between the two bus cycles, but if successive low bytes are written before a high byte is written, the last low byte is the one written to the register. The BIU latches even bytes (A0 = 0) of write data in a temporary register. When an odd byte is subsequently written to location address + 1, this byte and the even byte in the temporary register are written to the desired location. A lock out mechanism prevents a high byte write to modify an internal register if there is no valid word in the temporary register.

There is no crossing done by the M82786 in 8 bit mode: low bytes are transferred on the low data lines D7:0 and the high bytes on D15:8. An external crossover creates the 8 bit bus for the host. This is not additional hardware since a crossover is needed for an 8-bit host accessing of the memory array anyway.

MEMORY ACCESS ARBITRATION

The BIU receives requests to access the graphics memory from the Display Processor, the Graphics Processor and the External CPU. Additionally the internal DRAM/VRAM Controller also generates refresh requests. The DRAM/VRAM refresh requests are always highest priority. The other requests are arbitrated with programmable priorities. A higher priority request can interrupt lower priority memory cycles. Block transfers however can only be interrupted on doubleword boundaries.

There are two priority levels for requests from the Display and Graphics Processors: a First Priority (FPL) and a Subsequent Priority (SPL). The First Priority is the priority at which the first request of a bus cycle is arbitrated with. The Subsequent Priority is the priority associated with subsequent requests of a block transfer bus cycle. This allows for block transfers to execute with a different priority level. If a higher priority request occurs while a block transfer is executing, the BIU suspends the current block transfer and acknowledges the higher priority request. After completion of that higher priority memory access, the requests are arbitrated again. The suspended block transfer is arbitrated with its SPL priority since it is still executing a block transfer. The External Request has no Subsequent Priority level since it cannot execute block transfers. It does have an Altered Priority, though, which is the priority it assumes once every 42 CLK's (maximum bus latency for IBM PCs). The default priorities from highest to lowest following RESET are:

External	APL	7
External	FPL	7
Display	FPL	6
Graphics	FPL	5
Displays	SPL	3
Graphics	SPL	2

Three bits describe the priorities; 7 is the highest and 0 is the lowest. If two priority registers are programmed with the same value, a default priority chain is used. The default order is, from highest to lowest priority:

1. Display Processor
2. Graphics Processor
3. External

Graphics Memory Interface

The M82786 directly supports up to 32 DRAMs without additional external logic. This capability allows the use of cost effective memory devices and can result in significant performance improvement through the use of either standard Page Mode or the newer Fast Page Mode/Static Column Decode sequential access RAMs. The Fast Page Mode/Static

Column Decode parts enable the M82786 to cycle the DRAMs in 100 ns instead of the 200 ns used for Page Mode parts. The M82786 also allows the memory to consist of either standard single port memory devices or dual port Video RAM devices (VRAMs).

The M82786 supports a wide range of DRAM/VRAM configurations. The choices include interleaving or non-interleaving (1 or 2 banks - one CAS line/bank), number of rows per bank (1, 2, 3 or 4 - one RAS line/row), width (x1, x4 or x8), height (16k, 64k, 256k or 1M) and performance (Page Mode or Fast Page Mode/Static Column Mode). The only limitation is the address space limit of 4Mbytes. The M82786 DRAM/VRAM address lines (DRAx) can directly drive 32 memory devices while the RAS, CAS, WE and BEN lines can directly drive 16 devices. When the memory array consists of more than 32(16) devices then external drivers must be used to drive the memory array.

DRAMs with a HEIGHT of 64k are not allowed in the graphics memory of a system in which Master Mode will be used. There is no limitation on the total DRAM density (64k x 4 DRAMs cannot be used; 256k x 1 DRAMs are okay).

There are some special DRAM configurations:

i) When 1 Mb x 1 DRAMs are used, $\overline{\text{RAS3}}$ is used as DRA9.

ii) When only one interleaved row is configured (32 devices), $\overline{\text{RAS1}}$ is identical to $\overline{\text{RAS0}}$. Additional buffering on $\overline{\text{RAS0}}$ is therefore not required.

iii) When two non interleaved rows are configured (32 devices), $\overline{\text{CAS1}}$ is identical to $\overline{\text{CAS0}}$. Additional buffering on $\overline{\text{CAS0}}$ is therefore not required.

DRAM Cycle Types

The M82786 supports two fundamental memory cycle types: single and block. A single cycle involves a single 16 bit word, while a block transfer is a minimum of 2 16 bit words with no maximum length. The single cycle types supported and their cycle times are given below. The cycle times are counted in system clocks, $1/2$ the CLK input frequency.

1. Single Reads	3 cycles	600 ns @ 5 MHz
2. Single Writes	3 cycles	600 ns @ 5 MHz
3. Read-Modify-Writes	4 cycles	800 ns @ 5 MHz

The block cycles use the high speed sequential access modes of page mode, fast page mode (ripple mode) and static column DRAMs. Typical performance numbers for this case are:

1. Page Mode, Non-Interleaved	2 cycles 5 Mb/s @ 5 MHz
2. Page Mode, Interleaved	1 cycle 10 Mb/s @ 5 MHz
3. Fast Page Mode, Non-Interleaved	1 cycle 10 Mb/s @ 5 MHz
4. Fast Page Mode, Interleaved	0.5 cycles 20 Mb/s @ 5 MHz

All accesses into the graphics memory by the Display Processor use the high speed sequential access mode whenever possible. The Graphics Processor uses a single Read-Modify-Write cycles for all pixel drawing operations. Block copy operations by the Graphics Processor use the high speed sequential access modes. External CPU access into graphics memory is always a single read or write cycle. When configured to interface with dual port VRAMs, the M82786 generates Page Mode and Fast Page Mode style control signals for memory access through the normal random access port. It also executes a data transfer cycle when the video shift register in the VRAMs have to be loaded.

Graphics Memory Refresh

The BIU has an internal DRAM/VRAM refresh controller. The refresh period is programmable through the "DRAM/VRAM Refresh Control" Register in the BIU. All configured rows are refreshed simultaneously by activating the corresponding $\overline{\text{RAS}}$ lines periodically ($\overline{\text{RAS}}$ only refresh). The refresh row address (10 bits) is generated internally. On power up, the refresh row address is undefined. On normal reset, the refresh row address is not affected. It is initialized only if the M82786 is reset into the "BIU Test Mode". Not modifying the refresh address during RESET allows for a "warm RESET" implementation: contents of DRAM/VRAM can be insured to remain valid if RESET is short enough (less than three DRAM/VRAM refresh cycles). DRAM/VRAM refresh will continue at the proper row after RESET goes inactive again.

The graphics memory refresh cycles are always the highest priority cycles. There is some latency possible between the internal refresh request and the actual refresh cycle. This latency is critical only in one case: The M82786 is in a wait state while executing a bus cycle on the External Bus.

The worst case is a refresh request occurring just after the M82786 receives a HLDA from the host CPU to execute a block transfer on the external bus. Refresh requests can interrupt block transfers, but only on doubleword boundaries — the M82786 must execute 2 full bus cycles on the external bus before the refresh cycle is run. The possibility of many wait states when executing these two bus cycles creates a need for a large refresh latency tolerance. The M82786 can queue up to 3 refresh requests internally. In the default mode (a refresh request occurs every 30.4 microseconds and at 10 MHz clock), this implies that each bus cycle to external memory should not have more than 225 wait states.

There is no warm up logic on the M82786. The system must either wait for sufficient number of refresh cycles to execute or the boot software on the host can quickly access the memory array for the required number of cycles.

The default value of the DRAM/VRAM Control Register configures the array as 4 rows of Non-Interleaved Page Mode 256k × 1 with refresh requests generated every 30.4 micro seconds.

Internal Register and Graphics Memory Slave Access

The external master can access either M82786 internal memory I/O mapped registers or the Graphics memory. The M82786 internal address space consists of a contiguous 128-byte block that starts on an even byte address. It is mapped to memory or I/O space depending on the state of the M/$\overline{IO}$ bit in the "Internal Relocation Register". If the MIO bit is set to one, the Internal Register Block is memory mapped. If the MIO bit is zero, the Internal Register Block is I/O mapped. An address comparison is done between the Internal Relocation Register and the incoming address to determine if the CPU access is directed to internal memory/IO mapped registers.

Intel reserves the right to add functions to future versions of the M82786. Users should not use reserved locations in order to ensure future compatibility.

PERFORMANCE

Slave performance is measured here by assuming a request is made to an idle M82786. A synchronous interface is assumed.

Minimum M80286 Wait States = 3
(10 MHz M80286 and M82786)

Minimum M80386 Wait States = 8
(16 MHz M80386, 8 MHz M82786)

Minimum M80C186 Wait States = 3
(10 MHz M80C186 and M82786, $\overline{WT}$ = 1)

Minimum M80C186 Wait States = 2
(10 MHz M80C186 and M82786, $\overline{WT}$ = 0)

The values mentioned above are for read cycles. In some cases, write cycles can operate with fewer wait states. For instance, the M80286 can execute 2 wait state synchronous write cycles. The M80C186 can execute write cycles with one less wait state than mentioned above.

For asynchronous interfaces, if the CPU is operating at the same frequency as the M82786, the number of wait states are typically 1 more than those indicated above. For CPUs operating at a slower frequency than the M82786, the number of wait states are, on the average, less than 1 greater than those given above. In some cases, (eg. a 6 MHz M80286) an asynchronous interface acutally has less wait states than those quoted above for the synchronous interface.

INTERNAL REGISTERS

The M82786 Internal Register block is relocatable by programming an even byte address in the "Internal Relocation Register" in the BIU. The register block can be memory or I/O mapped based on the state of the MIO bit. The Register Block is physically distributed between the three M82786 modules, BIU, Graphics Processor and Display Processor.

Accesses to reserved locations have no effect; they execute normally but may produce indeterminate read data. No register is altered when a write is executed to a reserved location.

Location of Internal Registers within 128 byte block:

Byte Address			
'00–0F H		BIU Registers	8 words
'10–1F H		reserved	
'20–2B H		GP Registers	6 words
'2C–3F H		reserved	
'40–49 H		DP Registers	5 words
'4A–7F H		reserved	

The BIU register map is as follows:

Byte Address	
BASE + 0H	Internal Relocation
BASE + 2H	Reserved
BASE + 4H	BIU Control
BASE + 6H	Refresh Control
BASE + 8H	DRAM Control
BASE + AH	Display Priority
BASE + CH	Graphics Priority
BASE + EH	External Priority

The field definitions for the BIU Registers are as follows:

Internal Relocation

	15 14 13 12 ··· 4 3 2 1	0
Addr = BASE + 0H	Base Address	MIO

Reset values: xxx0

The Base Address determines the location of the 128 byte Internal Register Block. The MIO bit selects between memory or I/O mapping. If it is set (1), the Register Block is memory mapped. At RESET, the Base Address is set so that the Internal Relocation Register is located at every 128-byte address in the entire I/O space whenever $\overline{CS}$ is asserted. The Base Address must be written into this register before any other registers can be accessed.

BIU Control

	6	5	4	3	2	1	0
Addr = BASE + 4H	VR	WT	BCP	GI	DI	WPI	WP2
RESET value:	0	1	0	0	0	0	0

VR: If set (1) then the M82786 generates dual port video DRAM (VRAM) type memory cycles for display data fetch. If reset (0) then conventional page mode type memory cycles are performed to fetch display data.

WT: Determines the minimum number of wait states possible in a synchronous M80186 interface. If set (1), there is a minimum of 2 (3) wait states during memory write (read) cycles.

BCP: Determines whether the Internal Register block is accessed as bytes or words by the external CPU. If set (1), a 16 bit interface is selected.

GI: Graphics Processor Interrupt. Set when the Graphics Processor issues an Interrupt. Cleared with RESET or a read of this register.

DI: Display Processor Interrupt. Set when the Display Processor issues an Interrupt. Cleared with RESET or a read of this register.

WP1: Write Protection One. When set (1), all BIU Register contents except for the WP1 and WP2 bits of this register are write protected.

WP2: Write Protection Two. When set (1), all BIU Register contents are write protected, including WP1 and this bit, WP2. The only way to regain write access to the BIU registers after this bit is set, is to RESET the M82786.

Refresh Control

	6	5	4	3	2	1	0
Addr = BASE + 6H		Refresh Scalar					
RESET value:		0	1	0	0	1	0

The Refresh Scalar is a 6 bit quantity that determines the frequency of refresh cycles to the Graphics memory.

Refresh interval = (Scalar + 1) * 16 * Input clock period

DRAM/VRAM Control

	6	5	4	3	2	1	0
Addr = BASE + 8H	RW1	RW0	DC1	DC0	HT2	HT1	HT0
RESET value:	1	1	0	0	1	0	1

RW1:0: Number of Graphics memory Rows. One of the variables in defining the Graphics memory/External system boundary. Also disables RAS signals not driving any DRAMs/VRAMs.

RW1	RW0		
0	0	:	1 Rows
0	1	:	2 Rows
1	0	:	3 Rows
1	1	:	4 Rows

DC1:0: DRAM/VRAM Configuration. Controls the rate of block transfers and orientation of CAS1 and CAS0.

DC1	DC0		
0	0	:	Page Mode, Non-Interleaved
0	1	:	Page Mode, Interleaved
1	0	:	Fast Page Mode, Non-Interleaved
1	1	:	Fast Page Mode, Interleaved

HT2:0: DRAM/VRAM Height. Defines the HEIGHT (not size) of each DRAM/VRAM chip in the system. All DRAMs/VRAMs must be the same size.

HT2	HT1	HT0		
0	0	0	:	8K Devices
0	0	1	:	16K Devices
0	1	0	:	32K Devices
0	1	1	:	64K Devices
1	0	0	:	128K Devices
1	0	1	:	256K Devices
1	1	0	:	512K Devices
1	1	1	:	1M Devices

Display Processor Priority

	6	5	4	3	2	1	0
Addr = BASE + AH		FPL			SPL		
RESET value:		1	1	0	0	1	1

Graphics Processor Priority

Addr = BASE + CH

	FPL			SPL		
RESET value:	1	0	1	0	1	0

External CPU Priority

Addr = BASE + EH

	FPL			APL		
RESET value:	1	1	1	1	1	1

Specifies the priorities of the Display Processor, Graphics Processor and External CPU requests for the first request (FPL) and subsequent requests for block transfers (SPL). Code 111 is highest priority. Code 000 is lowest priority.

RESET AND INITIALIZATION

The state of $\overline{BHE}$ at trailing RESET determines synchronous vs. asynchronous operation. In Master mode, synchronous/asynchronous operation affects the sampling of the HLDA signal only. In Slave mode, synchronous/asynchronous operation affects the sampling of $\overline{RD}/\overline{WR}$ signals. Synchronous operation is set if $\overline{BHE}$ is sensed HIGH at trailing RESET. This enables direct connection of the M80286 $\overline{BHE}$ pin in synchronous systems since it is driven HIGH during RESET. The M80186 "tristates" its $\overline{BHE}$ during RESET so a small static load on this line can select asynchronous operation.

All internal registers are set to their default values on reset. The first slave I/O write access to the M82786 will always be directed at the Internal Registers (ignoring the upper fifteen address bits). The Internal Relocation Register must be programmed before any other Internal registers can be accessed. The DRAM/VRAM configuration registers must also be programmed to conform to any specific environment.

The M82786 assumes an 8 bit external CPU interface on reset. The graphics memory interface is always 16 bits wide. The BCP bit in the "BIU Control Register" must be set to 1 to enable a 16 bit external interface. Interrupts are cleared on reset.

GRAPHICS PROCESSOR

Introduction

The Graphics Processor (Graphics Processor) is an independent processor within the M82786. Its primary task is to draw bitmap graphics. It executes commands residing in the memory, accessing the memory through the Bus Interface Unit (BIU). The Graphics Processor addresses 4 MB of linear memory (22 bit addresses).

The Graphics Processor draws into a predefined area in the memory which is referred to as a "bitmap". A bitmap can be thought of as a rectangular drawing area composed of pixels. A coordinate system is defined for this bitmap with the origin at the upper left corner, the x-coordinate increasing from left to right and the y-coordinate increasing from top to bottom. A bitmap can be up to 32K pixels wide and 32K pixels high.

The M82786 can draw several graphics primitives such as points, lines, arcs, circles, rectangles, polygons and characters. During the figure drawing process, the M82786 follows several programmable attributes.

The graphics attributes supported by the M82786 are:

color
depth (bits/pixel)
texture
logical operation
color bit mask
clipping rectangle

Each graphics primitive can be drawn in any one of 2, 4, 16 or 256 "Colors". The color details (bits/pixel and exact color) are programmable. The "Texture" controls the appearance of any line (or figure). The texture pattern can be up to 16 bits long thus enabling drawing of solid, dashed, dotted, dot-dash etc. types of lines. Each bit in the Texture corresponds to one pixel. The M82786 supports all sixteen binary "Logical Operation" between a figure being drawn in bitmap memory and the existing contents of memory. It is thus possible to overlay a figure on a background. The "Color Bit Mask" restricts the drawing operation to only some "color planes". The clipping rectangle restricts the drawing operation to a specific area in the bitmap.

The pixel information is stored in the bitmap memory in a packed pixel format. Different color bits for the same pixel are stored in adjacent bit positions within the same byte. Each byte represents 1, 2, 4 or 8 pixels (in one of 256, 16, 4 or 2 colors).

The Graphics Processor fetches its commands directly from a linked list Memory-resident Graphics Processor Command Block (GCMB). The GCMB is created and maintained by the CPU. The initial address for the GCMB is contained in a Graphics Processor Opcode Register in the M82786. Addresses for subsequent (next) GCMBs are contained in the previous GCMBs. The Graphics Processor can be forced to stop by appropriate commands.

When the Graphics Processor is idle, it is said to be in the "Poll State". This is the default mode after reset. While in the Poll State, the Graphics Processor continuously monitors its internal "Opcode

Register". A valid command in this register starts the Graphics Processor. The first command placed in the internal Opcode Register must always be a "LINK" command directing the Graphics Processor to the main GCMB in memory.

Address	Register	Function	
BASE + 20h	GR0	OPCODE	GECL
BASE + 22h	GR1	Parameter 1	(Link Address Lower)
BASE + 24h	GR2	Parameter 2	(Link Address Upper)

Graphics Processor Internal Registers used in Poll State

Graphic Processor Command Format

The commands are placed (along with their parameters) sequentially in memory. Several GCMBs may be linked together through a LINK command. All commands have a standard format as described below:

15 8	7 1	0
OPCODE	0 0 0 0 0 0 0	GECL
Parameter 1		
• • •		
Parameter n		
etc.		

Each command to the Graphics Processor consists of an opcode, a Graphics End of Command List (GECL) bit and a list of parameters as required by the command. The opcode is 8-bits wide. The remaining 7-bits in the first word of the command must be all zeroes to ensure future compatibility. Also, whenever a parameter for the command is an address, 32-bits have been set aside but the M82786 uses only 22-bit addresses. The user must ensure that the higher 10-bits in the address parameter are always all zeroes All commands must lie at even byte addresses.

After fetching each command, the Graphics Processor checks the GECL bit. If the GECL bit is zero, the command executes and the next command is then fetched from the GCMB. If the GECL bit is set to one, the Graphics Processor does not execute the command and enters a POLL state.

Graphics Processor Status Register

One of the M82786 Internal Registers contains the Graphics Processor Status Byte. The bits in the Status Byte are represented as:

Address
BASE + 26H

GPOLL	GRCD	GINT	GPSC	GBCOV	GBMOV	GCTP	GIBMD

1. GPOLL - Poll State

   Indicates if the Graphics Processor is in a POLL state.
2. GRCD - Reserved Command

   This bit is set if the Graphics Processor encounters an illegal opcode.
3. GINT - This bit is set as a result of the INTR_GEN command.
4. GPSC - Pick Successful

   This bit is set or cleared while the Graphics Processor is in the PICK mode. The bit is set if the pick operation resulted in success on any command.
5. GBCOV - bitmap Overflow for BitBlt or CharBlt

   An attempt to execute a CHAR or a BitBlt command with any portion of the destination rectangle lying outside the clip rectangle causes this bit to be set.
6. GBMOV - bitmap Overflow for Geometric Commands

   An attempt to draw a pixel lying outside clip rectangle as a result of any geometric drawing commands (LINE, CIRCLE etc.) causes this bit to be set. The reason for separating these two bits is the difference between the clipping operations for the two types of commands.
7. GCTP - Character Trap

   This bit indicates that a character specified in the character string as a parameter for the CHAR command had its TRAP bit set.
8. GIBMD - Illegal Bit Map Definition

   This bit is set if the DEF__BIT__MAP command is executed with illegal parameters. The illegal parameters are bits per pixel defined to be other than 1, 2, 4 or 8, Xmax defined to be greater than 32k-1, or the following equation not being met: ((Xmax + 1) * Bpp) mod 16 = 0.

All the status bits except GPOLL are cleared upon reset. The GPOLL bit is set on reset.

Graphics Instruction Pointer

The Graphics Processor Instruction Pointer is a 22 bit quantity stored in two registers in the Graphics processor. It points to the current command in the GCMB.

Address	Register	Function
BASE + 28h	GCIPL	Instruction Pointer Lower
BASE + 2Ah	GCIPH	IP Upper

Clipping Rectangle

The M82786 can be instructed to restrict drawing to certain portion of the bitmap only. This portion is called the "Clipping Rectangle". The default clipping rectangle is the entire bitmap. The clipping rectangle must be redefined after a DEF_BIT_MAP command. For figures that are partially inside and partially outside the clipping rectangle, only the part inside the clipping rectangle is updated in the bitmap. Character clipping is supported for word mode.

In order for the clipping to have predictable results, there are some restrictions on the x,y coordinates of each pixel. The rules to be observed are:

1. For lines, circles, polygons, polylines, BitBlts and CharBlts, each pixel lying on the figure (both the visible and the invisible parts) must not have its x or y coordinate outside ± 32K range.
2. For circular arcs, the above restriction applies to the circle of which the arc is a part.
3. If the top of characters are to be clipped, the top row of pixels of the character must begin on an even-numbered scan line (scan lines are numbered from top to bottom beginning with number 0).

Pick Mode

The Graphics Processor can be put in "PICK Mode" by executing the ENTER_PICK command. In the PICK Mode, the Graphics Processor performs all pixel computations for all drawing, BitBlt and Character commands. However, the bitmap memory is not updated. Instead every computed pixel is compared against the clipping rectangle. If any computed pixel is found to lie within the clipping rectangle, the GPSC bit in the Graphics Processor Status Register is set. PICK Mode is not supported for circles and arcs.

Character Font Storage

The character fonts are stored in memory. Starting from an even address, the character information is stored in consecutive words of memory forming a character block. Each block can be of different lengths for different characters. A character font is selected by programming its base address into the M82786 through the DEF_CHAR_SET command. The font could be established for 8 or 16 bit character codes. Each character block within a font has the following format:

15	8	7	0
S	Width W	T	Height H
Dot Pattern for 1st row Dot Pattern for 2nd row — Dot Pattern for Hth row			

S - Character Space bit T - Trap Bit

Each character block must start at a word address and the dot patterns for each line of the font must reside in separate words. The height and width of each character cannot be more than 16 pixels. In case the width of a character is less than 16 pixels, the dot pattern for each line must be stored as right justified within the word.

Note that width and height of the character refer to the difference between their limiting x and y coordinates respectively. Thus width = 0 specifies a character one pixel wide and a height = 0 specifies a character one pixel high.

Graphics Processor Control and Context Registers

All Control and Context Registers in the Graphics Processor can be read from or written into, through the Graphics Processor commands DUMP_REG and LOAD_REG. Each register is identified by a 9-bit Register ID.

These registers are not directly addressable like the registers that are mapped into the M82786's On-Chip-Memory (I/O) space, i.e., they are accessible only through the DUMP_REG and the LOAD_REG commands. The four user accessible graphics control registers are listed below.

Step	Register Name	Register—ID (# of bits)	Register Function
	GPOEM	0003 (6)	Poll Mask
	GIMR	0004 (8)	Interrupt Mask
	GSP	010C (21)	Stack Pointer
C	GCNT	0015 (16)	Character Count while drawing characters in bitmap
D	GCNT	0014 (16)	

The Graphics Processor also has Context Registers, which are normally of no use to a user except in the event of saving and restoring them during a CPU context switch. Any other direct access to these registers must be avoided.

Name	ID	Bits	Function
GCOMM	0002	(16)	Command
GCHOR	0007	(2,2)	Character Orientation and Path*
GCHA	010B	(21)	Character Font Base Address~
GCA	010D	(21)	Memory Address of Current Position (X, Y)~
GBORG	010F	(21)	Bitmap Origin Address~
GCX	0010	(16)	Current X Position
GCY	0011	(16)	Current Y Position
GPAT	0012	(16)	Line Pattern
GSPAC	0013	(16)	Spacing between Characters and Bitblts
GN	0016	(16)	Number of 16-Bit Words Spanning Width of Bitmap
GVERS	0017	(16)	Version Number*** (D Step Value = 5)
TEMP	0019	(16)	Temporary Storage
GXMAX	0090	(16)	Maximum X for Clipping Rectangle
GYMAX	0091	(16)	Maximum Y for Clipping Rectangle
GXMIN	0094	(16)	Minimum X for Clipping Rectangle^
GYMIN	0095	(16)	Minimum Y for Clipping Rectangle^
GMASK	0099	(16)	Pixel Mask
GBGC	009B	(16)	Background Color
GFGC	009C	(16)	Foreground Color
GFCODE	009E	(4)	Function Code^^
GCIP	01AC	(21)	Current Instruction Pointer~
GBPP(RO)	009F	(4)	Used with Dump Register Command to Get Current Bits per Pixel Value^^^
GBPP(WO)	0008	(4)	Used with Load Register Command to Write Current Bits per Pixel Value^^^

~21-bit registers use 2 consecutive words.

*These bits are right justified in each byte of the word in which they are stored. Two bits are stored in bits 1 and 0 and two bits are stored in bits 8 and 9; the remaining upper bits in each byte are zeroed.

***In D-Step, valid after RESET and prior to drawing or drawing control commands.

^Correction to previous GXMIN ID 0096 and GYMIN 0097 assignments.

^^GFCODE ID reassigned from 001C to 009E in D-Step. This code is read out inverted. The value read out must be inverted in order to restore it properly.

^^^New D-Step Bpp Registers.

NOTE:
The following information is not saved by saving the state of these registers:

1) Type of character font, word, or byte.
2) Whether or not you are in pick mode.
3) Transparent or opaque drawing.

Graphics Processor Exception Handling

The status bits GPOLL, GRCD, GINT, GPSC, GBCOV, GBMOV, GCTP, and GIBMD are capable of generating an interrupt to the CPU depending upon the Interrupt Mask Register (GIMR). If the corresponding bit in the GIMR is a "0" an interrupt is generated. If another bit in the Graphics Processor Status Register is set before an acknowledgement for a previously generated interrupt, then another interrupt is not generated. Reading the Status Register and the BIU Control Register serves the purpose of an Interrupt Acknowledge to the Graphics Processor. Reading the Graphics Processor Status Register clears the offending status bit(s) - bits not masked out in the Interrupt Mask. If the interrupt is generated due to the GPOLL bit, then this bit is not cleared on an interrupt acknowledge. However this does not generate repeated interrupts.

The status bits GINT, GPSC, GBCOV, GBMOV, GTRP and GIBMD can also cause the Graphics Processor to stop its normal instruction fetch/execution and enter the POLL state. This is determined by the contents of the POLL On Exception Mask register (GPOEM). The GPOEM is 6 bits wide. If the corresponding bit in the GPOEM is a "0", POLL state is entered. On entering the POLL state, the GECL bit in the Opcode (GR0) register is automatically set. When the Graphics processor is in POLL state, it can be restarted by writing the appropriate opcode into the Opcode register (GR0) and writing a zero into the GECL bit. The act of clearing the GECL bit also causes the status bits that caused the POLL state to be cleared. Interrupt generation due to the GPOLL bit is enabled on exit from the POLL state.

The status bit GRCD when set, always causes the Graphics Processor to enter the Poll State. The Interrupt and the POLL mechanisms are two independent mechanisms. It is possible for the Graphics Processor to issue an interrupt and not POLL, or to issue an interrupt and POLL, or not to issue an interrupt and POLL or do none of them - all depending upon the GIMR and GPOEM Registers.

Initialization And Software Abort

The ABORT signal causes the Graphics Processor to enter POLL state after the execution of the currently executing command.

The two ways to initiate a software ABORT and force the Graphics Processor to enter POLL state are:

i) An attempt to write into the Graphics Processor Status Register

ii) An attempt to write into the Graphics Current Instruction Pointer.

Upon RESET, the Graphics Processor immediately enters a well defined state. The following events take place:

1. Command execution is halted and the Graphics Processor enters POLL state.
2. The GECL bit of the Opcode register (GR0) is set to one to indicate an End of Command List.
3. All status bits except GPOLL are cleared. GPOLL is set.
4. Interrupt Mask Register (GIMR) is set to all ones (disabled).
5. Poll on Exception Mask register (GPOEM) is set to all ones (disabled).
6. Graphics Processor exits pick mode.

The Graphics Processor command set is divided into the following classes:

1. Non-Drawing Commands
2. Drawing Control Commands
3. Geometric Commands
4. Bit Block Transfer (BitBlt) Commands
5. Character Block Transfer (CharBlt) Commands

List of Graphics Processor Commands
(Higher Byte - Hex)

Command	Opcode	Command	Opcode
LINK	02	POINT	53
NOP	03	LINE	54
DEF_TEXTURE_OPAQUE	06	LINE_OE	55
DEF_TEXTURE_TRANSPARENT	07	RECT	58
DEF_CHAR_SET_WORD	0A	BIT_BLT	64
DEF_CHAR_SET_BYTE	0B	ARC_EXCLUSION	68
INTR_GEN	0E	ARC_INCLUSION	69
CALL	0F	POLYGON	73
RETURN	17	POLYLINE	74
DEF_BIT_MAP	1A	CIRCLE	8E
DUMP_REG	29	CHAR_OPAQUE	A6
LOAD_REG	34	CHAR_TRANSPARENT	A7
DEF_COLOR	3D	CHAR_OPAQUE/REVERSE	A8
DEF_LOGICAL_OP	41	CHAR_TRANSPARENT/REVERSE	A9
ENTER_PICK	44	BIT_BLT_M	AE
EXIT_PICK	45	INCR_POINT	B4
DEF_CLIP_RECT	46	HORIZ_LINES	BA
DEF_SPACE	4D	BIT_BLT_EO	D4
DEF_CHAR_ORIENT	4E	BIT_BLT_ET	D5
ABS_MOVE	4F	BIT_BLT_ERO	D6
REL_MOVE	52	BIT_BLT_ERT	D7

NON-DRAWING COMMANDS

NOP = No Operation	0300h			
LINK = Link to Next Command	0200h	Link Address Low	Link Address High	
INTR__GEN = Generate Interrupt	0E00h			
DUMP__REG = Dump Register	2900h	Dump Address Low	Dump Address High	Register ID
LOAD__REG = Load Register	3400h	Load Address Low	Load Address High	Register ID
CALL = Call Subroutine	0F00h	Call Addr Low	Call Addr High	
RETURN = Return from Subroutine	1700h			
HALT = Enter Poll State	xx01h			

DRAWING CONTROL COMMANDS

DEF__BIT__MAP = Define bitmap	1A00h	Origin Addr Low	Origin Addr High	Xmax	Ymax	Bits/pixel
DEF__CLIP__RECT = Define Clip Rectangle	4600h	xmin	ymin	xmax	ymax	
DEF__COLORS = Define Colors	3D00h	Foreground Color	Background Color			
DEF__TEXTURE = Define Texture Opaque/Transparent	0600/0700h	Pattern				
DEF__LOGICAL__OP = Define Logic Operation	4100h	Color Bit Mask	Function Code (see table below)			

The functions performed and their codes are:

FCODE	FUNCTION	FCODE	FUNCTION
0000	0	1000	CMP (source) AND CMP (dest)
0001	source AND dest	1001	CMP (source) XOR dest
0010	CMP (source) AND dest	1010	CMP (source)
0011	dest	1011	CMP (source) OR dest
0100	source AND CMP(dest)	1100	CMP (dest)
0101	source	1101	source OR CMP (dest)
0110	source XOR dest	1110	CMP (source) OR CMP (dest)
0111	source OR dest	1111	1

DEF__CHAR__SET = Define Character Set (Word/Byte mode)	0A00/0B00h	Font Addr Low	Font Addr High
DEF__CHAR__ORIENT = Define Char Orientation	4000h	Path /Rotation	

There are four defined values for both the path and rotation. They are:

CODE	INCREMENT
00	0 degrees
01	90 degrees
10	180 degrees
11	270 degrees

DEF_CHAR = Define Inter Char and Bit Blt GCPP Update Space	4D00h	Space	
ABS_MOV = Move	4F00h	x coordinate	y coordinate
REL_MOV = Relative Move	5200h	dx	dy
ENTER_PICK = Enter Pick Mode	4400h		
EXIT_PICK = Exit Pick Mode	4500h		

GEOMETRIC COMMANDS

POINT = Draw Point	5300h	dx	dy	
INCR_POINT = Draw Incremental Points	B400h	Array Addr Low	Array Addr High	N (# of pts)

INCREMENTAL POINTS ARRAY

INC4	INC3	INC2	INC1
—	—	—	—
—	INCN	INCN-1	INCN-2

The largest allowable single array of incremental points is 32K points. The upper two bits of the "inc" field specify the increment for the x coordinate while the lower two bits specify the increment for the y coordinate. The encoding for the two bits is as follows:

CODE	INCREMENT
00	0
01	+1
10	−1
11	Unused

NOTE:
Transparent mode is not supported with the INCR_POINT command if the texture is non-solid.

LINE = Draw Line (With End Point/ without End Point)	5400/5500h	dx	dy	
CIRCLE = Draw Circle	8E00h	radius		
RECT = Draw Rectangle	5800h	dx	dy	
POLYLINE = Draw Polyline	7400h	Array Addr Low	Array Addr High	N (# of lines)
POLYGON = Draw Polygon	7300h	Array Addr Low	Array Addr High	N (# of lines)

POLYLINE/POLYGON ARRAY

dx1
dy1
—
dxN
dyN

HORIZONTAL LINE ARRAY

dxy
dyl
deltaX1
—
dxN
dyn
deltaXN

ARC = Draw Arc (Exclusion/Inclusion)	6800/6900h	dxmin	dymin	dxmax	dymax	radius
SCAN__LINES = Draw Series of Horizontal Lines	BA00/BA01h	Array Addr Low	Array Addr High	N (# of lines)		

NOTE:
Transparent mode is not supported with the CIRCLE and ARCommands if the texture is non-solid.

BITBLT COMMANDS

BIT__BLT = Bit Block Transfer within bitmap	6400h	Source x coord	Source y coord	dx	dy
BIT__BLT__M = Bit Block Transfer across bitmaps	AE00h	Source Addr Low	Source Addr High	Source Xmax	
	Source Ymax	Source x coord	Source y coord	dx	dy
BIT__BLT__E = Bit Block Transfer across bitmaps (opaque, transparent, opaque/reverse, transparent/reverse)	D400/D500/ D600/D700h	Source Addr Low	Source Addr High	Source Xmax	
	Source Ymax	Source x coord	Source y coord	dx	dy

CHARBLT COMMANDS

CHAR = Draw Character String (opaque, transparent, opaque/reverse, transparent/reverse)	A600/A700/ A800/A900h	String Ptr Low	String Ptr High	N(# of char)

CHARACTER STRING FORMAT

Word Mode

char1
char2
—
charN

Byte Mode

char2	char1
char4	char3
—	—
charN	charN-1

NOTE:
In byte mode, the character code of the first character to be drawn must reside at an even address.

DISPLAY PROCESSOR

Introduction

The Display Processor (Display Processor) is an independent processor responsible for controlling the display of video data on a CRT, laser printer and other display devices. Its functions include the generation of horizontal and vertical timing signals, blanking signal and the control of 8 Video Data output pins.

The M82786 can function in two distinct types of graphics memory environments – i) using single port DRAMs (normal display mode) and ii) using dual port video DRAMs (VRAM mode). When the M82786 is configured to interface with single port DRAMs, the Display Processor uses the BIU to fetch the screen parameters and display data from memory. The Display Processor then internally shifts the video data into the video stream for screen refresh. When configured to run with VRAMs, the Display Processor uses the BIU to load the shift registers in the VRAMs at the beginning of every scan line. The screen refresh is then done by the second port of the VRAMs. The BIU and Graphics Processor have the rest of the scan line time to access the graphics memory.

Bitmap Organization

The Display Processor is optimized to display data in packed bitmap form. The Graphics Processor writes pixel data in the memory in this form. The Display Processor supports display of 1, 2, 4 or 8 bits/pixel data, stored in sequential bitmap form, with the first (left-hand) pixel to be displayed occupying the Most Significant Bit(s) of a word in memory, and subsequent pixels occupying sequentially lower bits in the word. Ascending word addresses represent subsequent pixels, moving left to right and top to bottom on the screen.

Windows and Normal Display Mode

In the normal display mode, Windows may be displayed on the screen in a flexible format. There can be up to 16 window segments or tiles appearing on any single display line. There is no limit on the number of windows vertically (limited by the number of scan lines in the active display area). At the basic video rate (20 MHz, 8 bpp), these windows may be placed at pixel resolution on the screen, and mapped at pixel resolution into the bitmap. Windows can be made to overlap, by breaking the windows into tiles and assembling the tiles on the screen.

Cursor (Normal Display Mode)

The Display Processor supports a single hardware cursor which may be 8 x 8 pixels or 16 x 16 pixels. This cursor may be positioned anywhere on the screen with a pixel resolution. The cursor may be defined to be transparent or opaque, and may be either a block cursor with its hot-spot at the top-left of the cursor pattern, or a cross-hair cursor one pixel across, stretching the width and height of the screen with its hot-spot at the center of the cross. The cursor color and pattern (shape) are programmable. The cursor may be programmed off if not required, or to implement a blinking cursor.

Video Rates (Normal Display Mode)

The Display Processor is clocked from an external Video Clock. In this mode, the M82786 fetches video data from memory into an internal FIFO. An internal shift register then generates the serial video data stream to the display. The M82786 will support CRT screens of up to about 640 x 480 pixels at 8 bits/pixel and 60 Hz non-interlaced, or about 1024 x 640 x 8 at 60 Hz interlaced. The Display Processor supports Interlaced, non-interlaced and interlace-sync displays.

The Display Processor also has higher speed modes which enable the user to trade off bits/pixel for dot-rate. Thus it is possible to run at a maximum of 8 bpp with a 20 MHz dot-rate, 4 bpp at a 40 MHz dot-rate, 2 bpp at a 80 MHz dot-rate or 1 bpp at 160 MHz dot-rate; with corresponding increase in size and resolution. Note that in the high speed modes, horizontal window and cursor placement resolution is reduced to 2, 4 or 8 pixel resolution at 40 MHz, 80 MHz, or 160 MHz rates respectively.

VRAM Mode

In the VRAM mode, the first tile for every scan line is used to load the shift register in the VRAMs by executing a data transfer cycle. Subsequent tiles (if any) for all strips will still be available through the VDATA pins of the M82786. The window status bits can be used to internally multiplex the VRAM video stream and the M82786 generated video stream. The address for this data transfer cycle is determined from the Tile Descriptor. The M82786 $\overline{\text{BEN}}$ pin is used as a DT pin for this case. If the graphics memory banks are interleaved, then both banks are loaded in the transfer cycle. During the Blank period, Default VData appears on the VDATA pins.

CRT Controller

CRT timing signals HSYNC, VSYNC, and BLANK are each programmable at a pixel resolution, giving a maximum display size of 4096 x 4096 pixels. If High-Speed, Very-High-Speed, or Super High-Speed display modes are selected, the horizontal resolution of the CRT timing signals becomes 2 pixels, 4 pixels or 8 pixels at 40 MHz, 80 MHz and 160 MHz respectively.

Window Status

The HSync and VSync CRT timing pins may be configured to serve as Window Status output pins, which can be programmed to present a predefined code while the Display Processor is displaying a tile. This code is programmable as part of the Tile Descriptor, and may be used externally to multiplex in video data from another source, or select a pallette range for a particular window, etc. External logic must be used to enable VSync and HSync as CRT timing signals when Blank is high, and as encoded Window Status signals when Blank is low. This is valid in both DRAM and VRAM modes.

Zoom Support

The Display Processor allows windows to be zoomed in the normal display mode. The zoom factor is an integer between 1 and 64. There are independent zoom factors for the x and y direction. The zoom function results in pixel replication.

All zoomed windows on a display are zoomed by the same amount. A window is therefore either zoomed or not zoomed. Zoom offset is not supported—a pixel must either be fully displayed or not displayed at all. This places a restriction on window placement—a window may not be placed such that a zoomed pixel is partially obscured. VRAM displays can be zoomed vertically by using this feature. Horizontal zooming of VRAM windows requires external hardware support.

Only even zoom factors are supported in the Y direction with interlaced displays. In addition, when zooming, both descriptor lists (interlaced systems use two descriptor lists, one for each frame) must point to the same place in memory, i.e., they must be identical list.

Extended M82786 Systems

The CRT timing signal pins may be configured as output pins (for the normal stand-alone M82786 system), or as input pins for a system in which multiple M82786's are ganged in parallel to provide a greater number of bits/pixel, higher dot rates, larger display area, or more windows. In multiple M82786 systems, each of the Display Processors run in lock step, allowing the individual outputs to be combined on a single display. The HSync, VSync and Blank pins for the "Slave" M82786 are configured as inputs and are driven by the "Master" M82786.

When programmed as inputs, VSync and HSync still serve as outputs for Window Status while Blank is inactive.

External Video Source

The HSync and VSync pins on the M82786 can be configured as inputs to synchronize the M82786 to external video sources (VCR, broadcast TV etc.). In this case, the Blank pin is configured as output and the active M82786 display period is determined by the programmed M82786 parameters.

Memory Bandwidth Requirements

The memory bandwidth required by the Display Processor depends on the display size and mode of operation. The M82786 has a 40 Mbyte/sec maximum bandwidth during fast block accesses to graphics memory. In the normal display mode the Display Processor makes use of these fast block reads for screen refresh, thereby minimizing its use of the memory bus, which the other M82786 modules share. For worst-case displays, when the Display Processor is running at its maximum speed of 20 MHz and 8 bits/pixel, about 50% of the memory bandwidth is used for display refresh. Correspondingly, at only 1 bit/pixel the Display Processor's bus requirements are reduced to about one-eighth of its requirement at 8 bpp. In the VRAM mode, the Display Processor does not fetch any of the display data. The display data is passed directly from the graphics memory to the pixel logic. In this case about 1% of the graphics memory bandwidth is required by the Display Processor to fetch the Strip Descriptors.

Display Processor Registers

There are two different register sets for the Display Processor. Six of the M82786 Internal Registers are dedicated to the Display Processor. These registers are memory (or I/O) mapped in the external CPU address space. They can therefore be directly accessed by the external CPU. Another set of registers is totally local to the Display Processor. These are the display control registers and are used for display parameters.

M82786 Registers For Display Processor

There are six of these Registers. They are listed below:

Address	Function
Base + 40	Display Processor Opcode
Base + 42	Param1
Base + 44	Param2
Base + 46	Param3
Base + 48	Display Processor Status
Base + 4A	Default Video

The Display Processor Opcode and the three parameter registers are used to send a command to the Display Processor. The Display Processor Status Register contains the status for the Display Processor. This is described in more detail later. The Default Video Register contains the data that appears on the Video Out pins during the blanking intervals. The CPU can use this register to address an external pallette RAM while loading the pallette, thereby eliminating a separate address path and external logic.

Display Control Registers

The display control registers can be loaded under control of the Display Processor during the Vertical Blanking interval. This synchronizes parameter updates with display refresh and ensures that the display remains clean, with no updates occurring during data display.

The Display Processor may also be programmed to provide a Frame Interrupt once per certain number of frames. This may be used to facilitate blinking, scrolling, panning, animation or other periodic functions.

Command Execution

At the beginning of each Vertical Blanking time, the Display Processor checks the ECL bit in the Display Processor Opcode Register. If the ECL bit is 1, the Display Processor status remains unchanged. If the ECL bit is 0, the Display Processor executes the command. Only one command is executed per frame.

On completion of the command, the Display Processor sets its ECL bit back to 1, indicating to the CPU that a new command may be written into the Command Register. This handshake prevents the CPU from writing a new command before the old one has finished executing. The commands for the Display Processor are:

1. Load Register
2. Load All Registers
3. Dump Register
4. Dump All Registers

The command formats are:

LOAD REGISTER (LD—REG):

0	0	0	0	0	1	0	0	0	0	0	0	0	WP	LP	ECL
Memory Address Lower															
Mem Addr Upper															
Register ID															

This command loads a pair of display control registers with values stored in memory starting at the location given by Memory Address. The Memory Address must be an even byte address. The Register ID for the register pair is given in the register block description below. This command may be used to update individual pairs of registers (such as the Cursor Position registers). The register ID must be an even number for this command.

LOAD ALL (LD—ALL):

0	0	0	0	0	1	0	1	0	0	0	0	0	WP	LP	ECL
Mem Address Lower															
Mem Addr Upper															

This command loads the entire block of display control registers in a block read starting from the Memory Address given in the command. The Memory Address must be an even byte address. This command must be the first command executed and has to be executed after reset to enable the display operation. The registers are listed below.

DUMP (DMP—REG):

0	0	0	0	0	1	1	0	0	0	0	0	0	WP	LP	ECL
Memory Address Lower															
Mem Addr Upper															
Register ID															

This command causes the Display Processor to write the contents of the display control register pair specified by Register ID to the location in memory specified by Memory Address. The Memory Address must be an even byte address.

The register ID must be an even number for this command.

DUMP ALL (DMP—ALL):

0	0	0	0	0	1	1	1	0	0	0	0	0	WP	LP	ECL
Mem Address Lower															
Mem Addr Upper															

This command causes the Display Processor to write its entire display control register block out to a block in memory, starting at the Memory Address specified. The Memory Address must be an even byte address. The write occurs as a series of single write cycles.

For any of the Display Processor's four commands, setting the LP bit to 1 will cause that command to execute at the start of each VSYNC period. While in Loop Mode, the DP does not set the ECL bit back to 1 at the end of each execution. Exit Loop Mode by writing 0 to the LP bit.

The Write Protect bit (WP, bit 2 of the DP opcode register) allows the user to write protect the CRT Timing parameter registers (Display Control Register Block registers 06h–0Dh). Write protect is not enabled until after the first DP command has executed. This must be a LOAD ALL. Before changing the WP bit, the user should exit Loop Mode and wait for the ECL bit to return to 1.

Display Control Register Block

The display control register block is shown below. Each register is 16-bits wide. The numbers in parentheses are the number of bits per parameter.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	VStat:															C	D
01h		—								IntMsk							
02h		—								TripPt							
03h		—								Frint − 1							
04h		Reserved															
05h	CRTMode:	—									IL		W	S	B	AA	

C- CsrOn(1); D- DspOn(1)

IL - Interlace(2): 00 → Non-Interlace
01 → Reserved
10 → Interlace
11 → Interlace-Sync

W - Window Status Enable(1)

S - HSYNC, VSYNC Slave Mode(1)

B - Blank Slave Enable(1)

AA - Accelerated Video (High Speed Video, etc.)(2)
00 → Normal (20 MHz)
01 → High Speed (40 MHz)
10 → Very High Speed (80 MHz)
11 → Super High Speed (160 MHz)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
06h		—				HSynStp − 3											
07h		—				HFldStrt − 3											
08h		—				HFldStp − 3											
09h		—				LineLen − 3											
0Ah		—				VSynStp − 1											
0Bh		—				VFldStrt − 1											
0Ch		—				VFldStp − 1											
0Dh		—				FramLen − 1											
0Eh		Descriptor Addr. Pointer (L)															
0Fh		Descriptor Addr. Pointer (U)															
10h		Reserved															
11h		XZoom − 1								YZoom − 1							
12h		—								FldColor							
13h		—								BdrColor							
14h		—								1Bpp Pad							
15h		—								2Bpp Pad							
16h		—								4Bpp Pad							
17h	CsrMode:	S	X	T	CSt		CSC		—	CsrPad							

CsrStyle: S - CsrSize(1): 0 → 8 x 8 Csr
1 → 16 x 16 Csr

X - CsrX-Hair(1)

T - CsrTransparent(1)

CSt - CursorStatus (to Window Status output)(2)

CSC - CursorStatusControl(2): 00 → Current Window Status
01 → Foreground
10 → Background
11 → Block

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18	—				CsrPos X − 2											
19	—				CsrPos Y − 1											
1A	CsrPat0															
1B	CsrPat1															
1C	CsrPat2															
1D	CsrPat3															
1E	CsrPat4															
1F	CsrPat5															
20	CsrPat6															
21	CsrPat7															
22	CsrPat8															
23	CsrPat9															
24	CsrPatA															
25	CsrPatB															
26	CsrPatC															
27	CsrPatD															
28	CsrPatE															
29	CsrPatF															

The functions of the preceding registers are described in more detail below:

0. VStat:CsrOn(1) DspOn(1)

   If set, the internally generated display or cursor are turned on.

1. IntMsk

   Interrupt Mask Register. This register enables an M82786 interrupt whenever the corresponding bit in the Display Processor Status Register is set. A 0 for any bit enables the interrupt. This Interrupt Mask is different from the Interrupt Mask for the Graphics Processor. If using interrupts, mask bit 5 of this register.

2. TripPt

   The Trip Point register is a reserved field and must be programmed to 00h.

3. Frint

   Frame Interrupt Register. Enter the number of frames minus one elapsed between successive setting of the FRINT bit in the Display Processor Status Register.

4. Reserved field should always be set to zero.

5. CRTMode — IL(2) W(1) S(1) B(1) AA(2)

   These bits control the various modes of the CRT Controller.

   IL are the Interlace Control bits—if IL is 00, the display is Non-Interlaced. If IL is 10, the display is Interlaced (displaying the even lines (Field 1) of the frame and then the odd lines (Field 2)). If IL is 11, the display is interlace-sync (similar to interlace, except that the odd field display is identical to the even field display).

   W is the Window Status Enable bit. If W is 0, HSYNC and VSYNC will have normal operation. If W is 1, the Window Status Code programmed into the Tile Descriptors will be output on VSYNC and HSYNC pins while display data for that particular window is being displayed. VSYNC represents the MSB and HSYNC the LSB of the Window Status Code.

   S is the HSYNC/VSYNC Slave Mode bit. If S is 0, the VSYNC and HSYNC pins are outputs. If S is 1, they are inputs. In the Slave Mode, if Window Status is enabled, HSYNC and VSYNC will still be outputs while BLANK is low.

   B is the Blank Slave Mode bit. If B is 0, the BLANK pin is an output. If B is 1, it is an input.

NOTE:
Always program the slave M82786 first, then the master. The slave VSYNC, HSYNC and BLANK pins must be held high until they are programmed.

AA are the Accelerated Video Mode bits. By using an external latch or shift register, 40, 80 or 160 MHz video data rates can be generated. In the Accelerated Video Modes, each memory byte represents 2, 4 or 8 physical pixels. The upper bit(s) of each byte represent the pixels that appear on the left on the display medium. Used in DRAM display mode. Must be programmed to zero for the first tile in the VRAM Mode.

6. HSynStp

   Enter the HSYNC width in number of VClks minus 3. (For a graphical representation of all the CRT timing signals, see Figure 3).

7. HFldStrt

   Enter the number of VClks minus 3 between the rising edge of HSYNC and the falling edge of BLANK (the start of Video Data).

8. HFldStp

   Enter the number of VClks minus 3 between the rising edge of HSYNC and the rising edge of the next BLANK (the end of Video Data).

9. LineLen

   Enter the number of VClks minus 3 between the rising edge of HSYNC and the rising edge of the next HSYNC.

10. VSynStp

    The number of Horizontal Synchronizations (HSYNCS) between the beginning of Vertical Synchronization (VSYNC) and the end of VSYNC.

    Enter VSYNC width as the number of HSYNC periods minus one. In the non-interlaced mode, VSYNC rises and falls on the rising edge of HSYNC. In interlaced and interlace-sync mode, VSYNC has the same timing as in non-interlace mode at the start of each Even Field (lines 0, 2, 4, etc), but is delayed by half LineLen at the start of each Odd Field (lines 1, 3, 5, etc).

11. VFldStrt

    Enter the number of HSYNCs minus one between the beginning of VSYNC and the end of Vertical Blanking.

12. VFldStp

    Enter the number of HSYNCs minus one between the beginning of VSYNC and the beginning of the next Vertical Blanking.

13. FramLen

    Enter the number of HSYNCs minus one between the beginning of VSYNC and the beginning of the next VSYNC.

14. Descriptor Address Pointer (L)

    The address of the first Strip Descriptor for the display. After fetching the first descriptor the Display Processor uses the Link Address in the descriptor to fetch the next descriptor. The Descriptor address must be an even byte address.

15. Descriptor Address Pointer (U)

    The most significant bits of the Descriptor Address Pointer.

16. Reserved field should always be set to zero.

17. ZoomX, ZoomY

    Enter the x-zoom factor minus one and y-zoom factor minus one for the zoomed windows. The zoom factor can be any integer number between 1 and 64. In the VRAM mode, ZoomX is not used unless additional logic is added.

18. Field Color

    An 8-bit value indicating the color of the background field to be displayed in the absence of windows.

19. Border Color

    An 8-bit value indicating the color of the border to be displayed inside selected windows.

20. 1Bpp Pad

    An 8-bit value where the upper 7 bits represent the upper 7 bits of video data concatenated to the 1 bit video data from a 1 bit/pixel bitmap.

21. 2Bpp Pad

    An 8-bit value where the upper 6 bits represent the upper 6 bits of video data concatenated to the 2 bit video data from a 2 bit/pixel bitmap.

22. 4Bpp Pad

    An 8-bit value where the upper 4 bits represent the upper 4 bits of video data concatenated to the 4 bit video data from a 4 bit/pixel bitmap.

23. CsrStyle:S(1) X(1) T(1) CSt(2) CsrPad

    The Cursor Mode Register. The Cursor Pad is an 8-bit value where the upper 7 bits are the higher 7 bits for the cursor color.

    Cursor Style: S is the size bit. If S is 0 an 8 x 8 pixel cursor will be displayed. If S is 1, a 16 x 16 pixel cursor will be displayed.

    X is the CrossHair Mode bit. If X is 0, a block cursor will be displayed. The pattern for the cursor is specified in the Cursor Pattern registers. The cursor hot-spot is at the top-left of the cursor block. If X is 1, a crosshair cursor will be displayed. Its hot-spot is at the center of the cross, and it will stretch the full height and width of the display.

    T is the Transparent Mode bit. If T is 0, the cursor is opaque. Its forground color is determined by the concatenation of the cursor padding bits (7 MSB's) with 1. The background color is determined by the concatenation of the cursor padding bits with 0. If T is 1, the cursor background reverts to whatever bitmap data is being displayed "behind" the cursor.

    CSt is the Cursor Status. The code to be output onto the Window Status outputs while the Cursor is being displayed.

CSC is the Cursor Status Control (2 bits). The cursor status may be output whenever the cursor foreground color is being output, whenever the cursor background color is being output, or whenever the cursor block is active, whether it is displaying background color or foreground color or transparent pixels (useful for inverse video), or else the cursor status may default to the current Window Status. The code is shown in the Display Control Register Block. CsrPad: Cursor padding bits.

24. CsrPos X

This is the Cursor X-Position Register—the position of the cursor hot-spot relative to the beginning of the line (the rising edge of the previous HSYNC). Enter the value minus 2.

25. CsrPos Y

This is the Cursor Y-Position Register—the position of the cursor hot-spot relative to the beginning of the frame (the beginning of the previous VSYNC). Enter the value minus one.

26. CsrPat0:F

These 16 registers contain the pattern to be displayed as a cursor. CsrPat0 is the top row of the cursor, and the MSB is the left bit of the cursor. For an 8 x 8 cursor, the cursor pattern used is the higher byte of the first eight cursor registers.

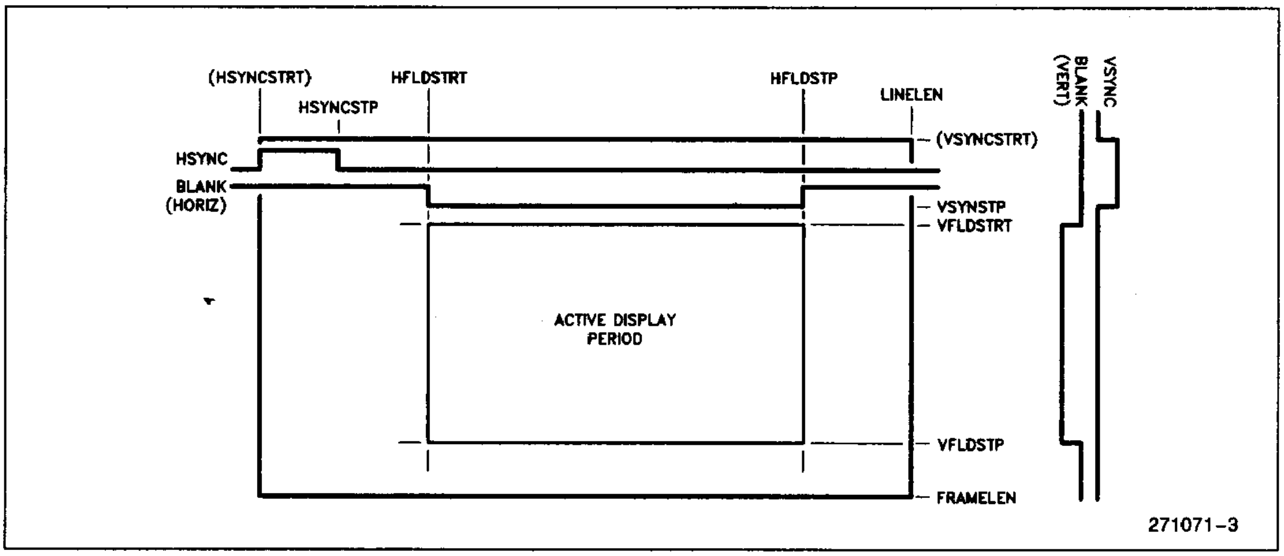


Figure 3. Timing Parameters

NOTE: In slave video mode, at least a 1-line vertical front porch and a 7-line vertical back porch are required.

Windows

The CPU creates Strip Descriptors in memory that describe windows for the Display Processor. The Strip Descriptors are organized as one Descriptor per strip of window segments (tiles) as shown in Figure 4. Each Descriptor contains information for the tiles within that strip in the order they are displayed on the screen (left to right). The Descriptor for a particular strip must be contiguous in memory. The Strip Descriptors for several strips are linked to each other in the order they are displayed (top to bottom). The linking is done through the Link to Next Strip Descriptor parameters in each Descriptor which points to the following Descriptor. The Descriptor for the first strip is accessed during the VBlank interval, using an address specified by the Descriptor Address Pointer, one of the Display Control Register pairs.

The Strip Descriptor consists of a header followed by one or more Tile Descriptors. The header and Tile Descriptors must occupy one contiguous block in memory.

The format of the Window Strip Descriptors is:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	Number of Lines in Strip − 1															
	Link to Next Strip Descr. (L)															
	Link to Next Strip Descr. (U)															
	C	Number of Tiles in Strip − 1														
1st Tile Descr.	Bitmap Width															
	Mem Start Address (L)															
	Mem Start Address (U)															
					Bpp				StartBit				StopBit			
	Fetch Count (bytes − 2)															
	T	B	L	R	WSt		—						PC		Z	F
2nd Tile Descr.	Bitmap Width															
	Mem Start Address (L)															
	Mem Start Address (U)															
					Bpp				StartBit				StopBit			
	Fetch Count (bytes − 2)															
	T	B	L	R	WSt		—						PC		Z	F

etc . . .

NOTE:
The first tile of any scan line must be greater than 1 pixel.

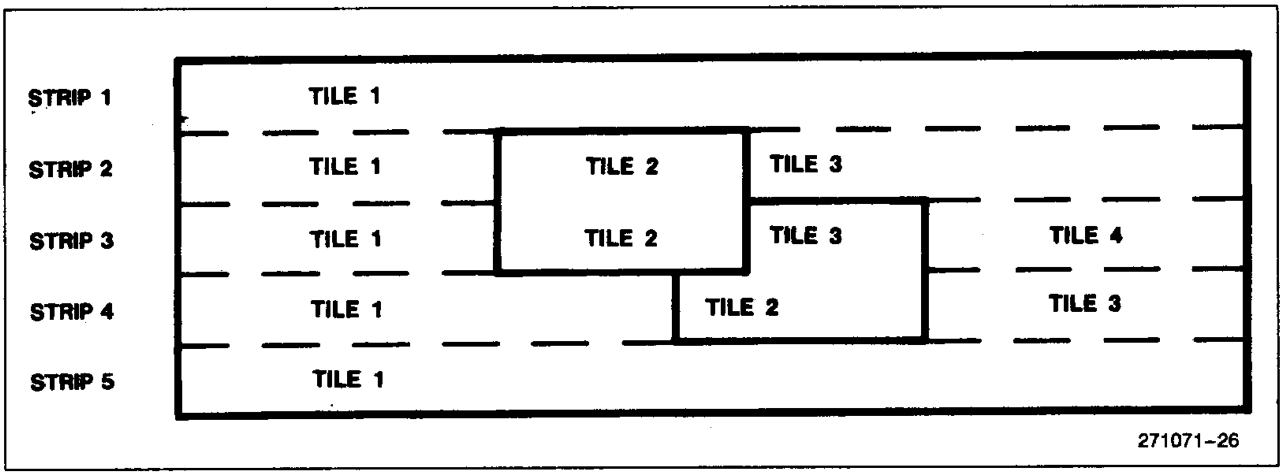


Figure 4. Display Shows Strips and Tiles with Two Overlapping Windows

The Strip Descriptor Header is programmed with values for the number of display lines minus one and the number of tiles in the strip minus one. There may be any number of lines in a strip, up to the number of lines on the display (within their restrictions imposed by zoom, if used). The first VRAM strip must be at least 2 lines. In DRAM mode there may be up to 16 tiles within a single strip. In the VRAM Mode the first tile is used to load the VRAM shift register, leaving up to 15 tiles to be used by the Display Processor. The header also contains Link to Next Strip Descriptor parameters.

NOTE:
You must only define in the strip descriptors the number of scan lines that will actually be displayed.

The C bit (the most significant bit) in the Number of Tiles in Strip parameter tells the DP to color the display area following the current strip with FldColor data or link to the next strip. If the C bit is set to one, the DP colors the remainder of the display with the background color defined in the FldColor Register of the Display Control Register Block. If the C bit is zero, the DP links to the next strip.

Each Tile Descriptor contains the following parameters:

1. Bitmap Width—the width of the bitmap in bytes. This must be an even byte address. Bitmap Width is added to the Memory Address for each scan line in the window (each HSync period within the strip) to get the start address of the next display line (if y-zoom inactive or counted out). In case of interlaced displays, the Memory Address is incremented by twice the bitmap width. In the VRAM Mode, the bitmap width of the first tile must be a power of 2 and must be less than the maximum width of the VRAM shift register.
2. Memory Start Address—the memory address for the window. This is an even byte address, corresponding to the address of the first word of bitmap data for the window tile (top left corner). In the VRAM mode the start address for the first tile must guarantee that the entire scan line is contained in a single row of the VRAM.
3. Bpp—The number of bits/pixel in the current window—must oe programmed to 1, 2, 4, or 8 in the normal mode. In the VRAM mode this field should be zero.
4. StartBit—The bit position in the corresponding memory word for the first bit of the first pixel in the window. Gives bit resolution to the Memory Start Address (and pixel resolution to the start of the window). In the normal mode this must be programmed to be consistent with the Bpp defined for that window. In the VRAM mode, this must be programmed to zero for the first tile.
5. StopBit—The bit position in the corresponding memory word for the last bit of the last pixel in the widow. Gives bit resolution to the window width. In the normal mode this must be programmed to be consistent with the Bpp defined for that window. An illegal value will result in incorrect display. In VRAM mode, this must be programmed to zero for the first tile.
6. Fetch Count—In the DRAM mode, this specifies the number of bytes minus two from the bitmap to be fetched for each scan line in the current window tile. This must be an even quantity. The value programmed in this field is 2 less than the number of bytes to be fetched rounded off to the next higher even number. In the VRAM mode, this must be programmed to zero for the first tile.
7. TBLR—Border Control Bits—When a bit is set to one, it turns on the border on Top, Bottom, Left or Right of window tile. This is a four bit field with one bit controlling each border. The most significant bit controls the top border and the least significant bit controls the right border. All four bits must be programmed to zero for the first tile in VRAM Mode.
8. WST—Window Status (2 bits)—The code to be presented on the Window Status pins while the window is being displayed.
9. PC—IBM PC Mode—Indicates that this window is being displayed from a bitmap created in IBM PC format. The Display Processor supports the IBM Color Graphics Adapter bitmap format in which the least significant byte of a word appears on the left of the most significant byte on the screen as opposed to the M82786 format in which the least significant byte appears to the right of the most significant byte. Also, the 2-bank and 4-bank bank oriented bitmaps used in the PC and PCjr systems are supported. These modes enable bitmaps created by IBM PC or PCjr (or compatible) systems to be upward compatible with M82786 displays, with the PC format bitmaps being displayed either as the whole screen, or as windows on a screen together with M82786 created bitmaps. The PC mode bitmaps can be zoomed or used with interlaced or accelerated displays. In the VRAM mode, this field must be programmed to zero for the first tile.

   Note that although the Display Processor can display bitmaps created in these formats, the Graphics Processor always draws bitmaps in M82786 format. The vertical mapping of IBM format bitmaps is restricted in that the Memory Start Address of an IBM format window must be in the first of the 2 or 4 banks.

The coding for IBM PC mode is given below:

00 → M82786 Mode
01 → Swapped Byte Mode
10 → Swapped Byte, 2 banks*
11 → Swapped Byte, 4 banks*

*Not supported in Interlaced Mode.

Bitmap formats in M82786 and PC Modes are shown below:

Pixel # (from left as displayed on screen):

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
M82786 Mode Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC Mode Bit #	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

10. Z—Zoom—This bit if set, indicates that in the normal display mode the window is to be zoomed using the zoom parameters programmed into the ZoomX and ZoomY registers.
11. F—Field—This bit if set, indicates that the window tile is background field. In the normal mode the field color is displayed for the window. The number of pixels of Field to be displayed should be programmed into what would normally be the Bpp, StartBit, StopBit fields. This bit must be set to zero for a the first tile in the VRAM mode.

If the Strip Descriptor list causes a window to be displayed that extends beyond the active display area, then only the upper left hand portion of the window is displayed and the rest of it is truncated.

In interlace mode, in order to maintain a line resolution on vertical positioning of windows, a double-length Descriptor Table must be used. The first part contains window position information for the even lines, the second part for the odd lines. Also note that in interlace mode, one frame takes two fields to display. Command execution occurs at frame boundaries, not field boundaries, so the instruction execution frequency will typically be 25/30 Hz instead of the non-interlaced 50/60 Hz.

Initialization

The Display Processor is reset during the main M82786 reset process. Upon reset it enters a well defined reset state described below:

1. Any command execution is immediately halted.
2. Parameter, Descriptor, or Display Data fetches are terminated.
3. Display Outputs VDATA7:0 are all reset to default video.
4. HSync, VSync, Blank are tristated (Display Processor defaults to Slave Operation). These stay tristated until the first LOAD_ALL instruction.
5. Display Processor Status Register is cleared.
6. Display Processor Interrupt Mask to set to all 1's (all interrupts disabled).
7. ECL bit is set to 1.

Display Processor Interrupts, Status Register and Exception Handling

The Display Processor Status Register is an 8-bit memory (or I/O) mapped register which indicates the current status of the Display Processor, and allows the generation of interrupts depending on the state of individual bits. Interrupts may be masked off using the Display Processor Interrupt Mask Register. The format of the Display Processor Status Register is:

ADDRESS	7	6	5	4	3	2	1	0
BASE + 48 h	FRI	RCD	R	FMT	BLK	EVN	ODD	ECL

Display Processor Status Register

The functions of each bit, and the action taken in the case of exceptions is described below:

FRI—Frame Interrupt. This bit is set every n frames, where n is a value between 1 and 256 loaded into the Frint Register. This may be used, for example, for timing in animation applications, or to time blink rates.

RCD—Reserved Command. This bit is set if the Display Processor does not recognize the Opcode it has been instructed to execute. The Display Processor will not execute the command.

Reserved (R)

FMT—FIFO Empty. This indicates that the Display FIFO has underrun. This forces an End of Line condition and the rest of the Display Line will display the FldColor defined in the Display Control Register Block. At the beginning of HBlank, the Display Processor uses the current Descriptor to start a new Display Data fetch. A FIFO underrun therefore does not necessarily mean that the whole field is lost—just the current display line is corrupted.

BLK—Blank. This indicates that the BLANK pin is currently active for Vertical Sync.

EVN—Even Field. In Interlace and Interlace-Sync modes, this bit is set during the even field (Field 1).

ODD—Odd Field. In Interlace and Interlace-Sync modes, this bit is set during the odd field (Field 2). The Even and Odd status bits assist in synchronizing the M82786 with other interlaced display systems.

ECL—End of Command List. This is set at the same time the ECL bit in the Opcode Register is set, and allows the Display Processor to inform the CPU as soon as it has completed execution of a command. In Loop Mode, the ECL bit is not set. It will be set upon exiting Loop Mode.

All active interrupts are OR'ed together to drive a single M82786 interrupt line. Once set, the interrupt line remains active until the Status Register is read. The active bits in the Status Register (bits with 0 in the corresponding bit in the Interrupt Mask) are reset to zeroes after the Status Register is read.

Test Modes

The M82786 implements several special modes of operation beyond normal use to aid in debug, characterization and production testing. When RESET goes inactive, the RD and WR pins are sampled. If either of these two pins is low, one of the special test modes is enabled according to the state of RD, WR and MIO pins.

A 16-bit Linear Feedback Shift Register signature analyzer is placed on the Video output bus to compress the video data stream into a single signature that is output onto the Video Data pins during Blank time. The signature is also readable by the CPU at the end of a Frame using the Dump_Reg command at Register ID 3D. This signature analyzer output onto the VDATA lines is activated in DP Test Mode. Once in DP Test Mode, the signature Analyzer is enabled by setting bit 14 of the DP Opcode register to 1.

The M82786 implements three global pin conditioning features. Specifically, the M82786 can drive all output and I/O pins high, or low, or can tristate all pins. The test modes are activated according to the following table:

$\overline{\text{RD}}$	$\overline{\text{WR}}$	MIO	Mode
0	0	0	Reserved
0	0	1	Reserved
0	1	0	DP Test Mode
0	1	1	Drive Output Pins High
1	0	0	Drive Output Pins Low
1	0	1	Tristate Pins
1	1	X	Normal Operation

NOTE:
All timing numbers in the parametric section are preliminary and are subject to change.

V_{OL}/V_{OH} Pin Conditioning

The M82786 has the capability to bring all its output pins to a constant logic high or low state. This feature can be used for testing the output buffers on the M82786.

Tristate Feature

The M82786 has the ability to tristate all of its I/O and output pins to effectively isolate the M82786 from any connected circuitry. This allows testing a completely assembled PC board by isolating the M82786. Leakage on all I/O pins can also be tested in this mode.

M82786 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Case Temperature Under Bias...	−55°C to +125°C
Voltage V_{CC}–V_{SS}	−0.5V to +6.5V
Voltage on Other Pins	−0.5V to V_{CC} + 0.5V

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Notes
V_{ILC}	Input Low Voltage	−0.5	+0.8	V	CLK Input
V_{IHC}	Input High Voltage	+2.2	V_{CC} + 0.5	V	CLK Input
V_{ILVC}	Input Low Voltage	−0.5	+0.8	V	V_{CLK} Input
V_{IHVC}	Input High Voltage	+3.9	V_{CC} + 0.5	V	V_{CLK} Input
V_{IL}	Input Low Voltage	−0.5	+0.8	V	All Other Pins
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.5	V	All Other Pins

D.C. CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Output Low Voltage	—	+0.45	V	All Pins I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.8	—	V	All Pins I_{OH} = −400 μA
I_{LI}	Input Leakage Current	—	±10	μA	0 <V_{IN} <V_{CC}
I_{LO}	Output Leakage Current	—	±10	μA	0.45 <V_{IN} <V_{CC}
I_{CC}	Power Supply Current	—	350	mA	@ −55°C Temp CLK @ 10 MHz V_{CLK} @ 20 MHz

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

CLOCK and RESET Timings

AC timings are referenced to 1.5V on clock input and 0.8V/2.0V on other pins

Symbol	Parameter	Min	Max	Units	Notes
T_C	CLK Period	100	200	ns	
T_{CL}	CLK Low Time	40	—	ns	
T_{CH}	CLK High Time	40	—	ns	
T_{CR}	CLK Rise Time	—	10	ns	0.8V–2.0V
T_{CF}	CLK Fall Time	—	10	ns	0.8V–2.0V
T_{R1}	Test Input Setup Time	10	—	ns	
T_{R2}	Test Input Hold Time	5	—	ns	
T_{R3}	Reset Active Hold Time	25	2 T_C	ns	
T_{R5}	Reset Inactive Hold Time	10	—	ns	
T_{R6}	Reset Active Setup Time	10	—	ns	
T_{R7}	Forced Output Delay	30	—	ns	
T_{R8}	Reset Width	10 T_C	—	ns	

θ_{JA} = 28°C/W, θ_{JC} = 2°C/W

DRAM Interface Timings

AC timings are referenced to 0.8V/2.4V on all pins and are valid for total DRAM capacitance on each pin between 30 pF and 200 pF

SINGLE READ, WRITE, READ MODIFY WRITE AND PAGE MODE CYCLES

Symbol	Parameter	Min	Max	Units
T_{RC}	Single Cycle Time	$6\,T_C - 5$	—	ns
T_{RAC}(1)	Access Time from $\overline{RAS}$	—	$4\,T_C - 30 - 0.050\,C_R$	ns
T_{CAC}(1)	Access Time from $\overline{CAS}$	—	$2\,T_C + T_{CH} - 20 - 0.050\,C_C$	ns
T_{CAA}(1)	Acc Time from Col Addr	—	$3\,T_C - 20 - 0.075\,C_A$	ns
T_{OAC}(1)	Access Time from $\overline{BEN}$	—	$2\,T_C - 25 - 0.050\,C_B$	ns
T_{RP}	$\overline{RAS}$ Precharge Time	$2\,T_C - 10$	—	ns
T_{RAS}	$\overline{RAS}$ Width	$4\,T_C - 30 - 0.025\,C_R$	—	ns
T_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	$T_C + T_{CL} - 25 + 0.050\,C_C - 0.050\,C_R$	—	ns
T_{RSH}	$\overline{RAS}$ Hold Time	$2\,T_C + T_{CH} - 15 + 0.025\,C_R - 0.050\,C_C$	—	ns
T_{CSH}	$\overline{CAS}$ Hold Time	$4\,T_C - 15 + 0.025\,C_C - 0.050\,C_R$	—	ns

SINGLE READ, WRITE, READ MODIFY WRITE AND PAGE MODE CYCLES (Continued)

Symbol	Parameter	Min	Max	Units
T_{CAS}	$\overline{CAS}$ Width	$2\,T_C + T_{CH} - 10 - 0.025\,C_C$	—	ns
T_{ASR}	Row Address Setup Time	$T_C - 10 + 0.075\,C_R - 0.075\,C_A$	—	ns
T_{RAH}	Row Address Hold Time	$T_C - 25 + 0.075\,C_A - 0.050\,C_R$	—	ns
T_{ASC}	Column Addr Setup Time	$T_{CL} - 17 + 0.075\,C_C - 0.075\,C_A$	—	ns
T_{CAR}	Col Addr Setup to $\overline{RAS}$	$3\,T_C - 10 + 0.025\,C_R - 0.075\,C_A$	—	ns
T_{OFF}	Data in Hold Time	10	—	ns
T_{BOV}	$\overline{BEN0}$ to $\overline{BEN1}$ Overlap	0	—	ns

SINGLE WRITE CYCLE

Symbol	Parameter	Min	Max	Units
T_{RWL}	$\overline{WE}$ to $\overline{RAS}$ Lead Time	$T_C - 14 + 0.025\,C_R - 0.050\,C_W$	—	ns
T_{WCH}	$\overline{WE}$ Hold Time	$3\,T_C - 15 + T_{CH} + 0.025\,C_W - 0.050\,C_C$	—	ns
T_{WP}	$\overline{WE}$ Width	$2\,T_C - 20 - 0.025\,C_W$	—	ns
T_{CWL}	$\overline{WE}$ to $\overline{CAS}$ Lead Time	$T_C - 13 + 0.025\,C_C - 0.050\,C_W$	—	ns
$T_{DS(W)}$	Data Out Setup Time	$T_C - 15 + 0.075\,C_W - 0.075\,C_D$	—	ns
T_{DH}	Data Out Hold Time	$T_C - 20 + 0.075\,C_D - 0.050\,C_W$	—	ns

READ MODIFY WRITE CYCLE

Symbol	Parameter	Min	Max	Units
T_{RWC}	RMW Cycle Time	$8\,T_C - 5$	—	ns
$T_{DS(RW)}$	Data Out (RMW) Setup Time	$T_{CH} - 20 + 0.075\,C_W - 0.075\,C_D$	—	ns
T_{DH}	Data Out (RMW) Hold Time	$T_C - 10 + 0.075\,C_D - 0.050\,C_W$	—	ns
$T_{OFF(RW)}$	Data In Hold/Data Out (RMW) Drive Time	10	$T_{CL} + 5 + 0.075\,C_D - 0.075\,C_B$	ns

PAGE MODE READ AND WRITE CYCLES

Symbol	Parameter	Min	Max	Units
T_{PC}	Page Mode Cycle Time	$4\,T_C - 5$	—	ns
T_{CP}	$\overline{CAS}$ Precharge Time	$T_C + T_{CL} - 15$	—	ns
T_{CAS}	$\overline{CAS}$ Width	$2\,T_C + T_{CH} - 10 - 0.025\,C_C$	—	ns
$T_{CAH(n)}$	Col Addr Hold (Non Interleaved)	$3\,T_C + T_{CH} - 20 + 0.075\,C_A - 0.050\,C_C$	—	ns
$T_{DS(n)}$	Data Out Setup (Non Interleaved)	$T_C + T_{CL} - 20 + 0.075\,C_C - 0.075\,C_D$	—	ns
$T_{DH(n)}$	Data Out Hold (Non Interleaved)	$2\,T_C + T_{CH} - 10 + 0.075\,C_D - 0.050\,C_C$	—	ns
$T_{CAH(i)}$	Col Addr Hold (Interleaved)	$T_C + T_{CH} - 20 + 0.075\,C_A - 0.050\,C_C$	—	ns
$T_{DS(i)}$	Data Out Setup (Interleaved)	$T_{CL} - 25 + 0.075\,C_C - 0.075\,C_D$	—	ns
$T_{DH(i)}$	Data Out Hold (Interleaved)	$T_C + T_{CH} - 10 + 0.075\,C_D - 0.050\,C_C$	—	ns

FAST PAGE MODE READ AND WRITE CYCLES

Symbol	Parameter	Min	Max	Units
T_{PC}	Fast Cycle Time	$2\ T_C - 5$	—	ns
T_{CP}	$\overline{CAS}$ Precharge Time	$T_{CL} - 10$	—	ns
T_{CAS}	$\overline{CAS}$ Width	$T_C + T_{CH} - 10 - 0.025\ C_C$	—	ns
T_{CAA}(1)	Col Address Access Time	—	$2\ T_C - 15 - 0.075\ C_A$	ns
T_{CAC}(1)	$\overline{CAS}$ Access Time	—	$T_C + T_{CH} - 15 - 0.050\ C_C$	ns
T_{CAP}(1)	Access Time from Col Precharge	—	$2\ T_C - 25 - 0.075\ C_C$	ns
$T_{OAC(i)}$	Access Time from $\overline{BEN}$ (Interleaved)	—	$T_C - 21 - 0.050\ C_B$	ns
$T_{CAH(n)}$	Col Addr Hold (Non Interleaved)	$T_C + T_{CH} - 20 + 0.075\ C_A - 0.050\ C_C$	—	ns
$T_{DS(n)}$	Data Out Setup Non Interleaved)	$T_{CL} - 25 + 0.075\ C_C - 0.075\ C_D$	—	ns
$T_{DH(n)}$	Data Out Hold (Non Interleaved)	$T_C + T_{CH} - 10 + 0.075\ C_D - 0.050\ C_C$	—	ns
$T_{CAH(i)}$	Col Addr Hold (Interleaved)	$T_{CH} - 12 + 0.075\ C_A - 0.050\ C_C$	—	ns
$T_{DS(i)}$	Data Out Setup (Interleaved)	$T_{CL} - 25 + 0.075C_C - 0.075\ C_D$	—	ns
$T_{DH(i)}$	Data Out Hold (Interleaved)	$T_{CH} - 10 + 0.075\ C_D - 0.050\ C_C$	—	ns

DUAL PORT DRAM DATA TRANSFER CYCLE

Symbol	Parameter	Min	Max	Units
T_{DTR}	DT High to $\overline{RAS}$ High Setup	$T_C - 10 + 0.025\ C_R - 0.075\ C_B$	—	ns
T_{DTH}	DT High from $\overline{RAS}$ High Hold	$T_C - 10 + 0.075\ C_B - 0.075\ C_R$	—	ns
T_{RDHN}	DT High from $\overline{RAS}$ Low Hold	$3\ T_C - 10 + 0.025\ C_B - 0.050\ C_R$	—	ns
T_{RDHP}	DT High from $\overline{RAS}$ Low Hold	$7\ T_C - 10 + 0.025\ C_B - 0.050\ C_R$	—	ns
T_{RDHF}	DT High from $\overline{RAS}$ Low Hold	$5\ T_C - 10 + 0.025\ C_B - 0.050\ C_R$	—	ns
T_{DLS}	DT Low to $\overline{RAS}$ Low Setup	$T_C - 10 + 0.075\ C_R - 0.050\ C_B$	—	ns
T_{CDH}	DT Low from $\overline{CAS}$ Low Hold	$T_C + T_{CH} - 10 + 0.025\ C_B - 0.050\ C_C$	—	ns
T_{DTC}	DT High to $\overline{CAS}$ High Setup	$T_C - 10 + 0.025\ C_C - 0.075\ C_B$	—	ns

MASTER MODE TIMINGS $C_L = 100$ pF on all output pins
AC timings are referenced to 1.5V on clock input and 0.8V/2.0V on other pins

Symbol	Parameter	Min	Max	Units
T_{M1A}(2)	CLK to MEN Delay	—	40	ns
T_{M1B}(3)	HLDA to MEN Delay	—	45	ns
T_{M2A}(2)	CLK to A21:0, MIO, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ Drive	—	60	ns
T_{M2B}(3)	HLDA to A21:0, MIO, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$ Drive	—	65	ns
T_{M3}	HREQ, MEN Inactive Delay	—	45	ns
T_{M4}	A21:0, D15:0 Float Delay	—	40	ns
T_{M5}	Async HLDA Setup	5	—	ns
T_{M8}	Read Data Setup Time	10	—	ns

MASTER MODE TIMINGS C_L = 100 pF on all output pins (Continued)
AC timings are referenced to 1.5V on clock input and 0.8V/2.0V on other pins

Symbol	Parameter	Min	Max	Units
T_{M9}	Read Data Hold Time	10	—	ns
T_{M10}	READY Setup Time	20	—	ns
T_{M11}	READY Hold Time	5	—	ns
T_{M12}	Command Valid Delay	—	35	ns
T_{M13}	Address Valid Delay	—	40	ns
T_{M14}	Write Data Valid Delay	—	40	ns
T_{M15}	Write Data Hold Time	—	40	ns
T_{M16}	Sync HLDA Setup : 01	5	—	ns
T_{M17}	Sync HLDA Setup : 02	20	—	ns
T_{M18}	CLK to HREQ Delay	—	35	ns

SLAVE INTERFACE TIMINGS C_L = 100 pF on all output pins
AC timings are referenced to 1.5V on clock input and 0.8V/2.0V on other pins

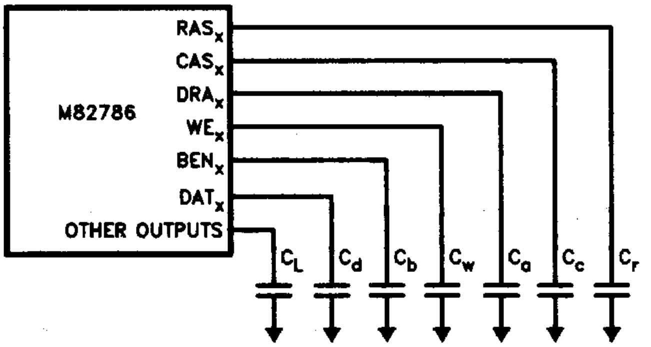
Symbol	Parameter	Min	Max	Units
T_{S1}	Active Input Setup	5	—	ns
T_{S2}	Active Input Hold Time	10	—	ns
T_{S3}	Inactive Input Setup	5	—	ns
T_{S4}	Inactive Hold Time	10	—	ns
T_{S14}	Active Command Width	$2\,T_C + 30$	—	ns
T_{S16}	A21:0, MIO, $\overline{CS}$, $\overline{BHE}$ Hold Time	$2\,T_C + 30$	—	ns
T_{S17}	A21:0, MIO, $\overline{CS}$, $\overline{BHE}$ Delay	—	$T_C - 20$	ns
T_{S18}	SEN Active Delay	0	35	ns
T_{S19}	Write Data Delay	0	$2\,T_C - 25$	ns
T_{S20}(4)	Write Data Hold (Memory Write)	$3\,T_C + T_{DH} + 30$	—	ns
T_{S20}	Write Data Hold (Int. Write)	$4\,T_C$	—	ns
T_{S21}	SEN Inactive Delay	0	45	ns
T_{S22}(5)	Read Data Delay (Memory Read)	0	(Note 5)	ns
T_{S22}	Read Data Delay (Int. Read)	0	$T_C + 40$	ns
T_{S23}	Read Data Hold	$5\,T_C - 15$	—	ns
T_{S24}(6)	RD/WR to SEN Delay (Mem Write)	$4\,T_C + 20$	—	ns
T_{S24}(6)	RD/WR to SEN Delay (Int. Write)	$4\,T_C + 20$	—	ns
T_{S24}(6)	RD/WR to SEN Delay (Mem Read)	$5\,T_C + 20$	—	ns
T_{S24}(6)	RD/WR to SEN Delay (Int. Read)	$7\,T_C + 35$	—	ns
T_{S25}	SEN Width (Write Cycle)	$4\,T_C - 25$	$4\,T_C + 35$	ns
T_{S25}	SEN Width (Read Cycle)	$5\,T_C - 25$	$5\,T_C + 35$	ns

VIDEO INTERFACE C_L = 50 pF on all output pins
AC timings are referenced to 1.5V on clock input and 0.8V/2.0V on other pins

Symbol	Parameter	Min	Max	Units	Notes
T_{VCYC}	VCLK Cycle Time	50	—	ns	@ 1.5V
T_{VCL}	VCLK Low Time	23	—	ns	@ 1.5V
T_{VCH}	VCLK High Time	19	—	ns	@ 1.5V
T_{VDL}	Delay VCLK to Output Valid	0	25	ns	
T_{VDH}	Output Valid Hold from VCLK	4	—	ns	@ 1.5V
T_{VS}	Input Setup Time	5	—	ns	
T_{VH}	Input Hold Time	8	—	ns	

NOTES:
1. Subtract transceiver delay from these numbers for by-1 DRAM devices.
2. Valid for asynchronous interface or for synchronous interface when TM16 is satisfied. Synchronous interface requires same clock and reset input for M82786 and M80286.
3. Valid for synchronous interface when TM16 is not satisfied.
4. TS20 (memory write) is dependent on DRAM specs.
5. TS22 (memory read) is dependent on DRAM specs. This is the maximum of:
   i) $T_{RAC} - T_C + 10$
   ii) $T_C - T_{CH} + T_{CAC} + 10$
   iii) $T_C - T_{OAC} + 10$
6. TS24 timings are the absolute minimum values for a synchronous M80286/M82786 type interface (or synchronous M80186/M82786 interface with WT = 0). Add T_C to get corresponding minimum number for an asynchronous interface. Add T_C for M80186 interface with WT = 1. Typical delay from Command to SEN active will be greater than the minimum value, depending on level of activity of the M82786 and priority for external access.

AC TEST LOADS (Use capacitance values in pico farads in the timing equations)

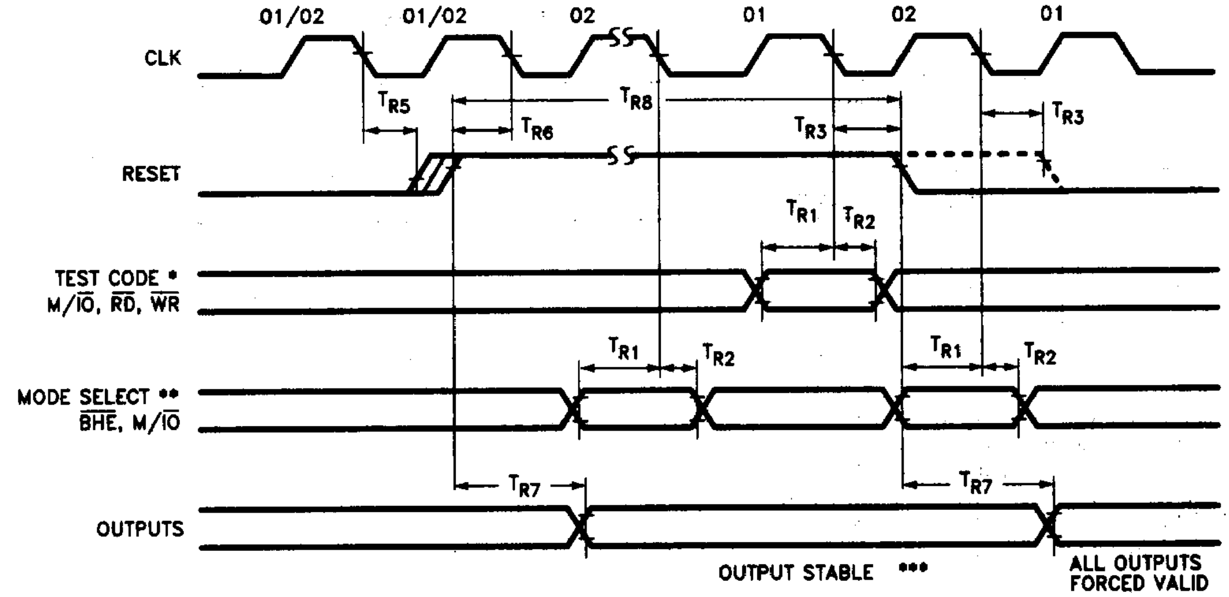


271071-4

C_d, C_b, C_w, C_a, C_c, C_r in the range 30 pF-200 pF

16

RESET TIMINGS



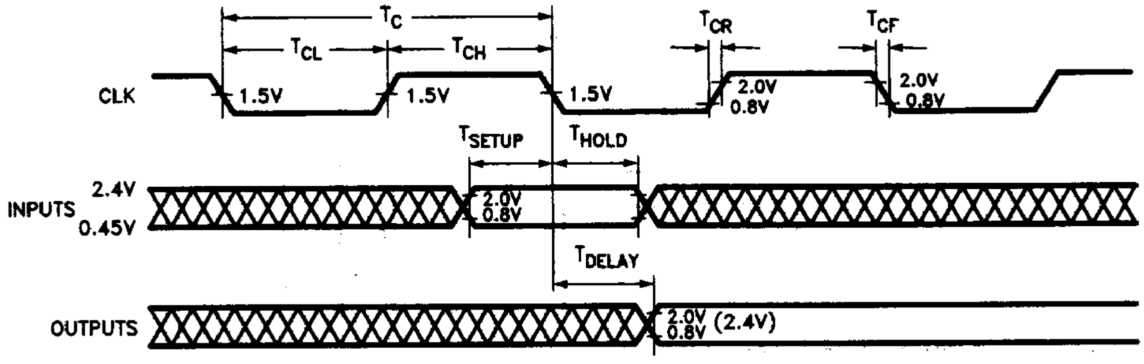
271071-5

*Test code sampled at end of 01 preceding falling edge of RESET

**Mode select sampled at end of 02 preceding falling edge of RESET

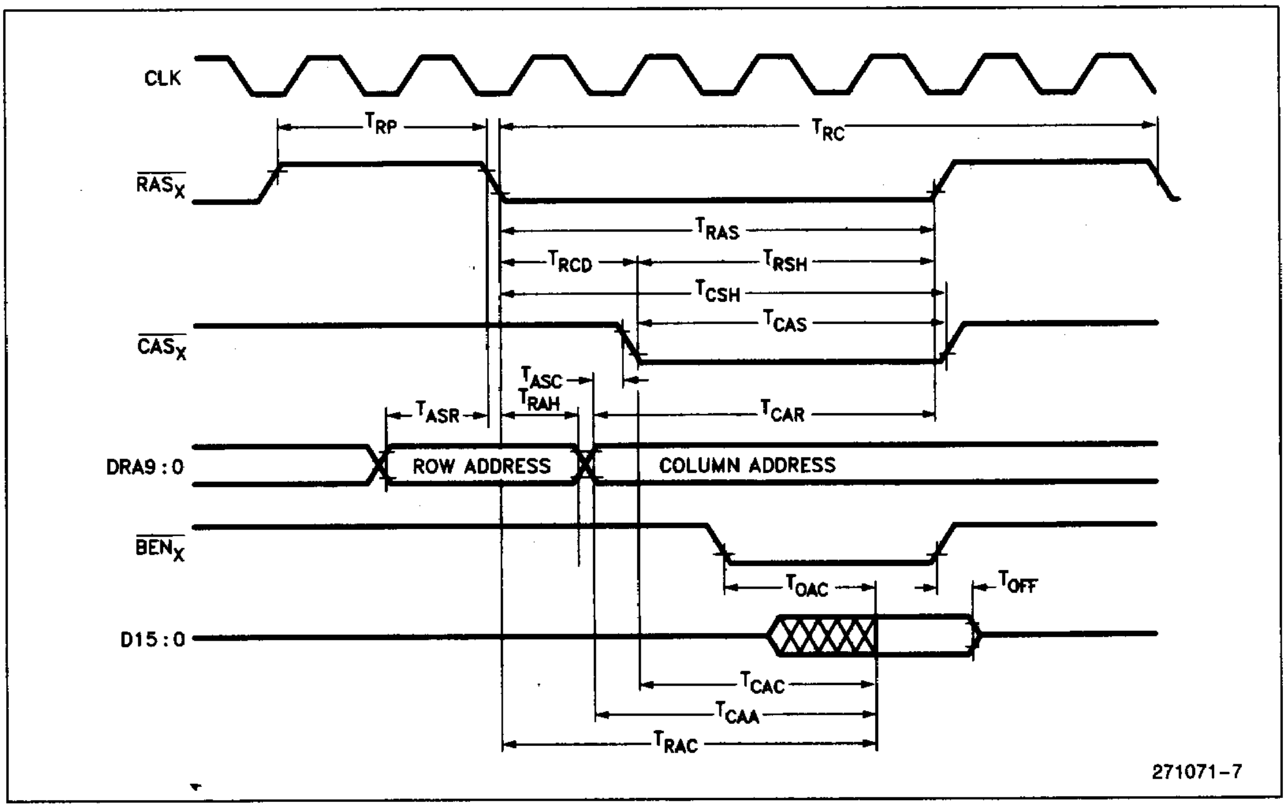
***$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, MIO, A21:0, D15:0, BLANK, HSYNC, VSYNC—TRISTATED
MEN, SEN, HREQ, INTR—LOW
$\overline{\text{CAS}}_x$, $\overline{\text{RAS}}_x$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$, $\overline{\text{BEN}}_x$—HIGH
DRA8:0, VDATA7:0—Indeterminate

CLOCK AND AC TEST CONDITIONS



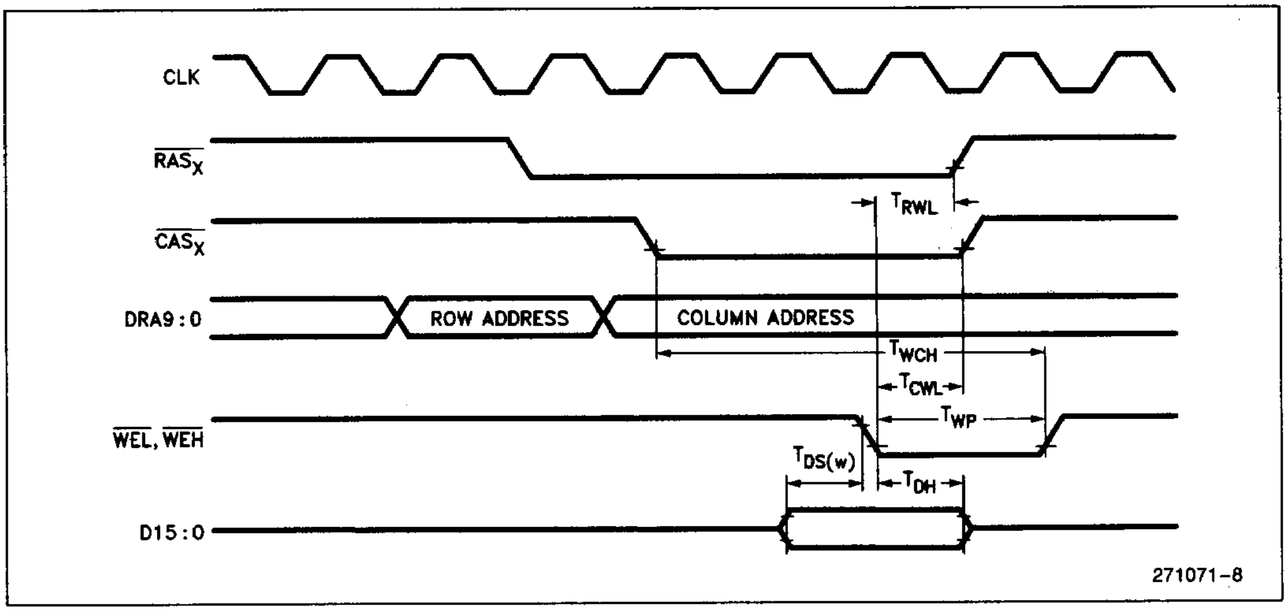
271071-6

DRAM SIGNALS—SINGLE READ CYCLE



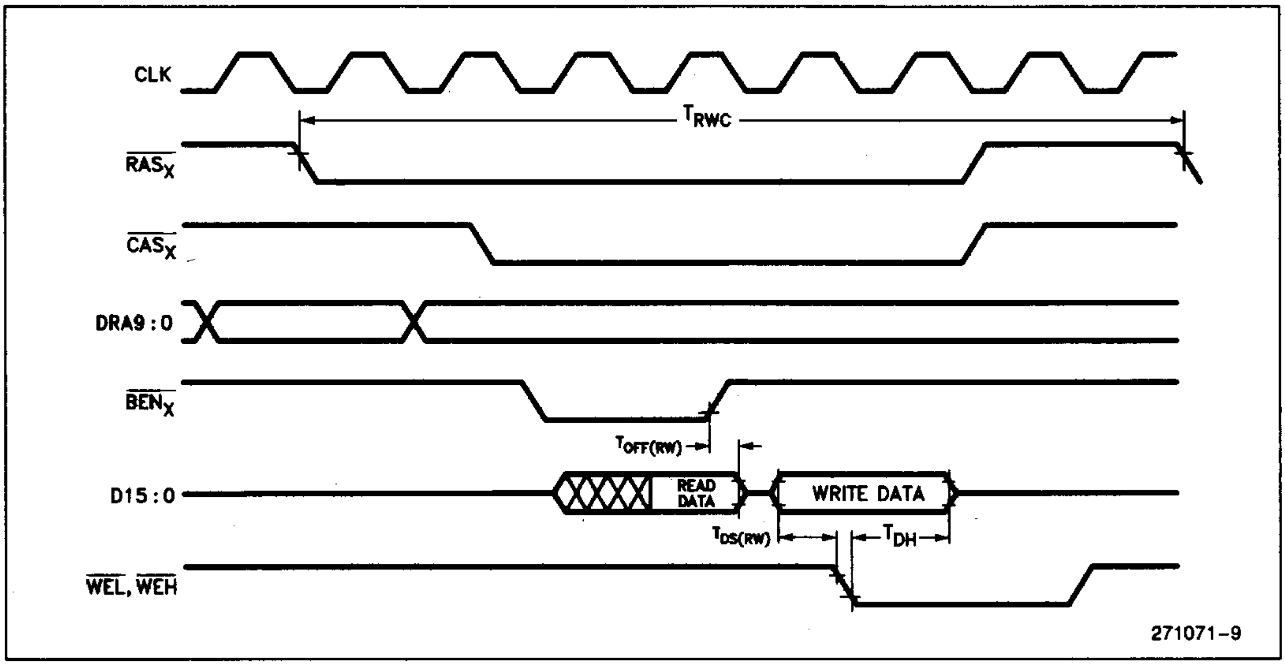
271071-7

DRAM SIGNALS—SINGLE WRITE CYCLE



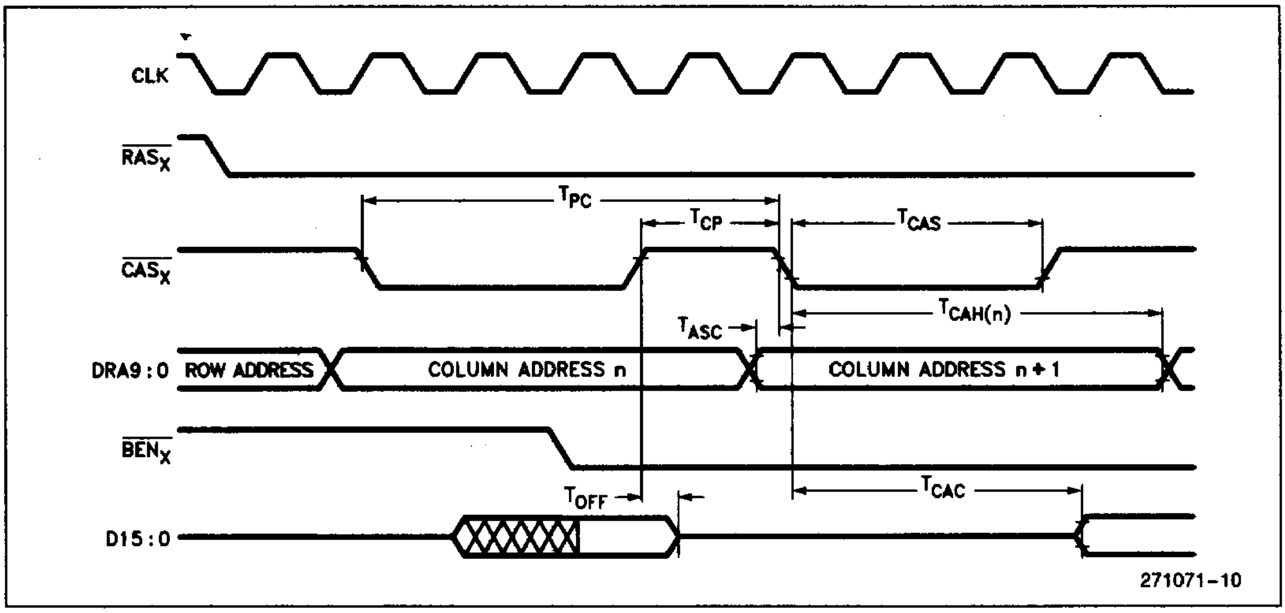
271071-8

DRAM SIGNALS—READ MODIFY WRITE CYCLE



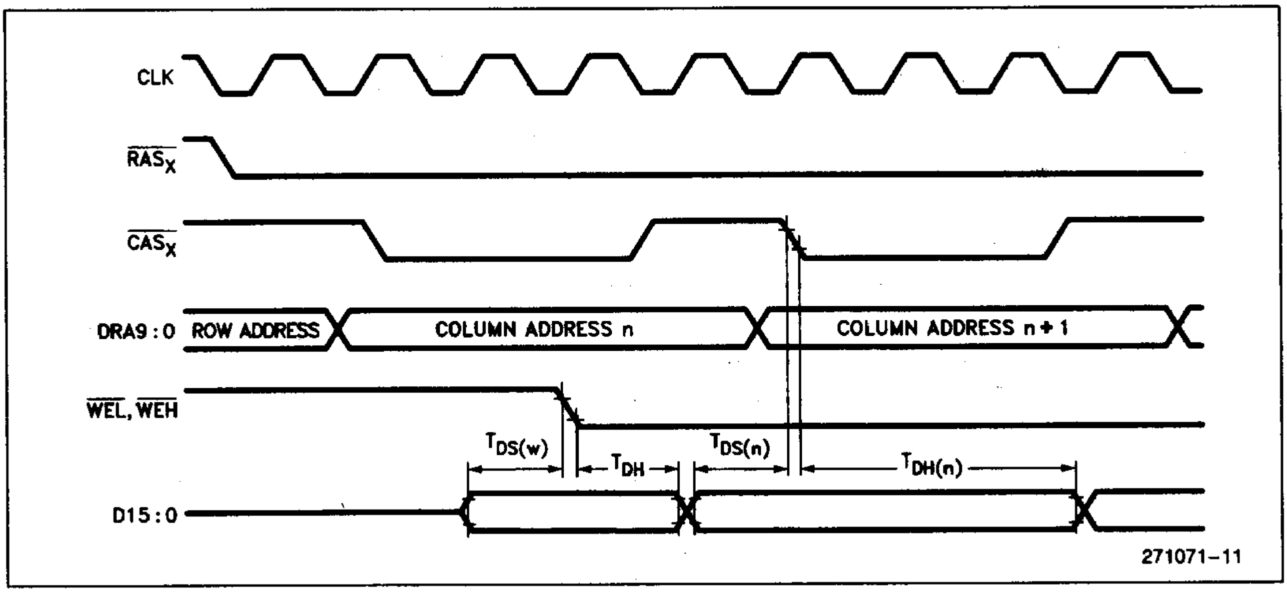
271071–9

DRAM SIGNALS—NON-INTERLEAVED PAGE MODE READ



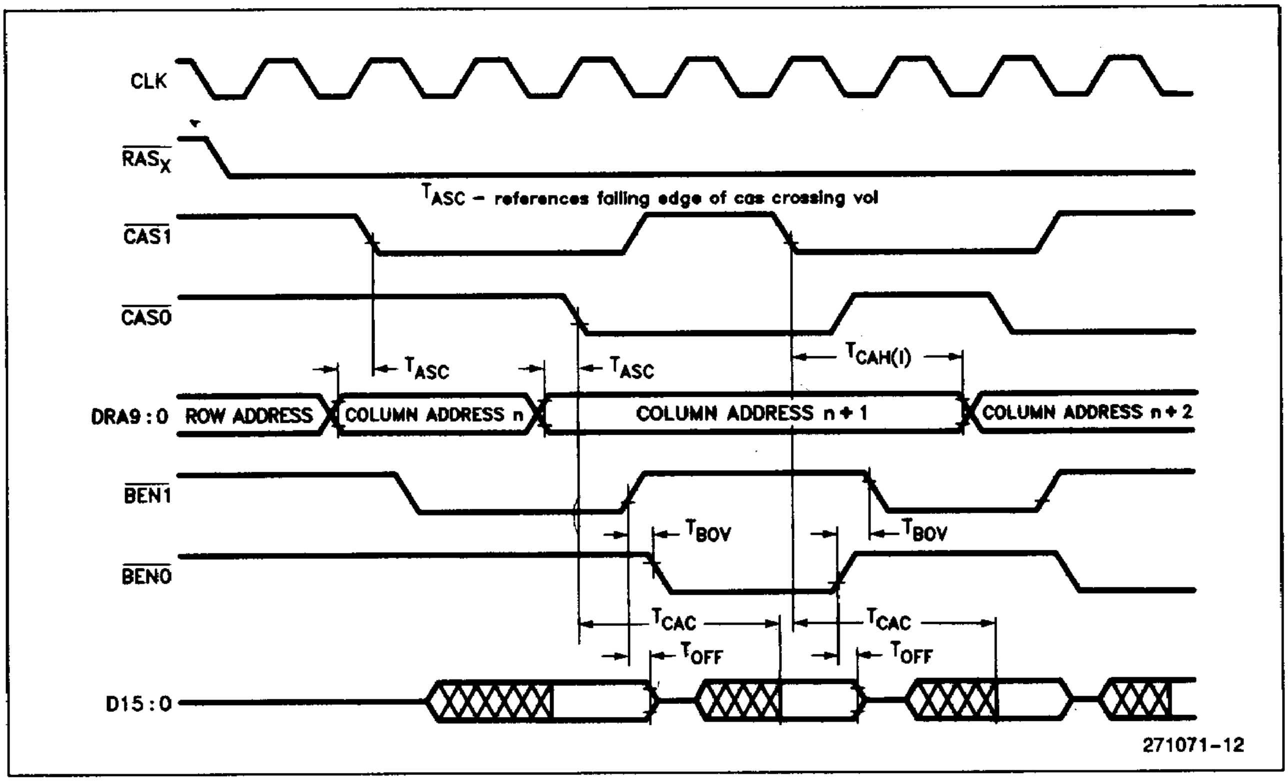
271071–10

DRAM SIGNALS—NON INTERLEAVED PAGE MODE WRITE



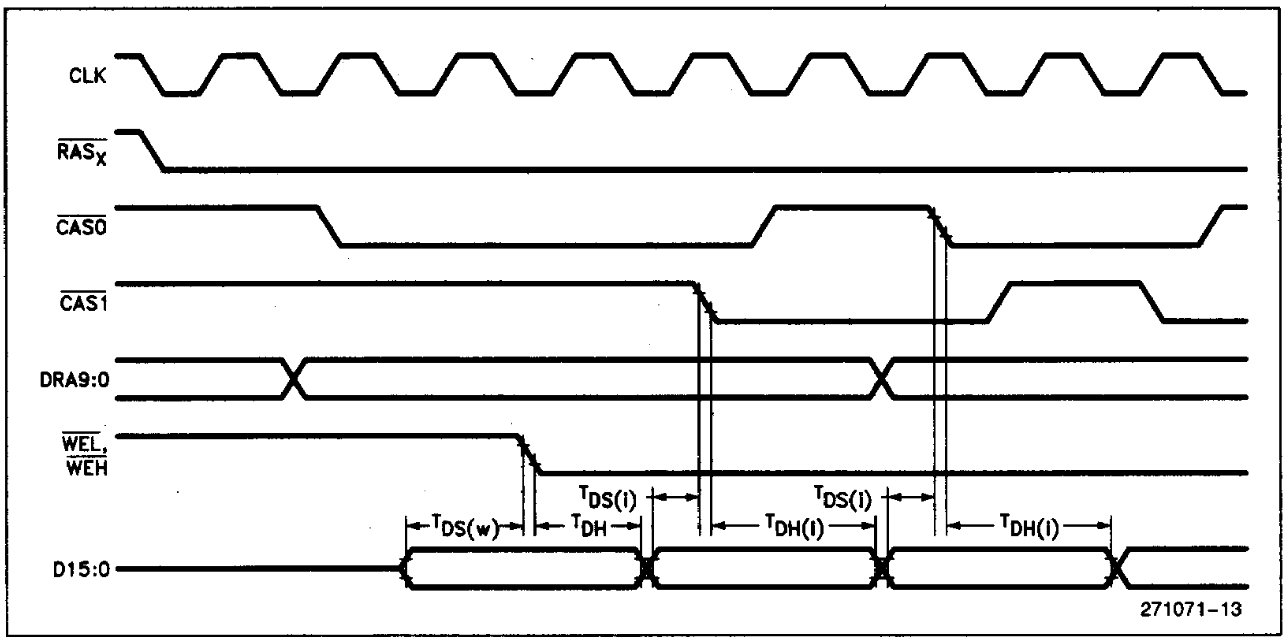
271071–11

DRAM SIGNALS—INTERLEAVED PAGE MODE READ

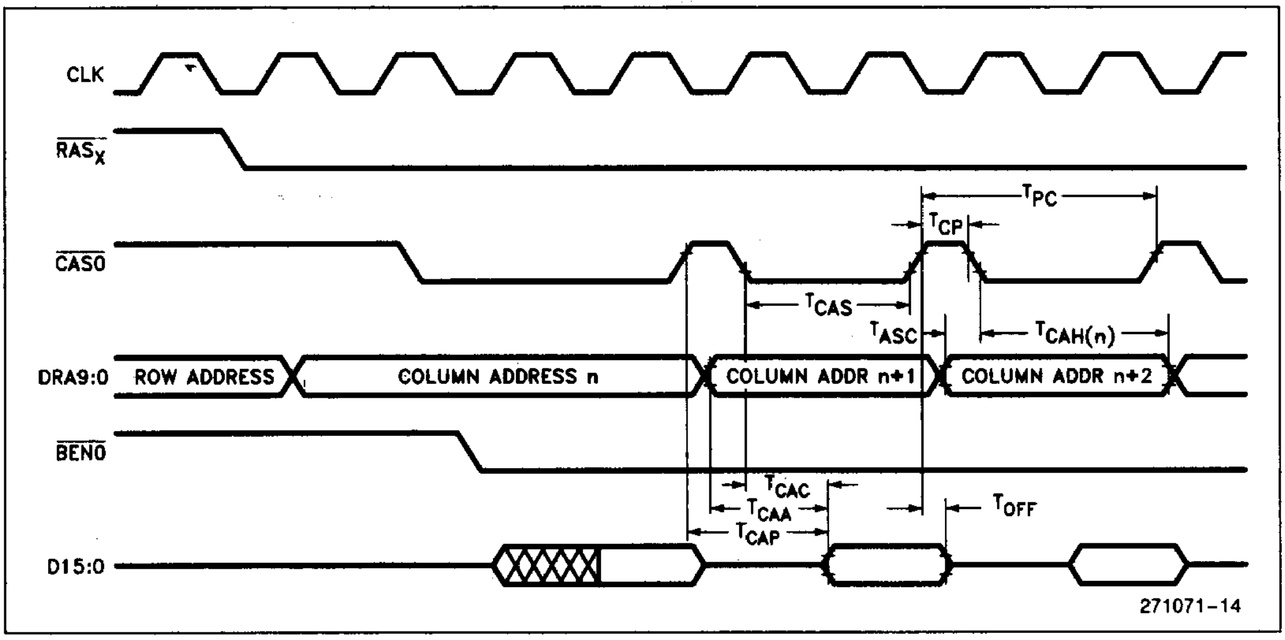


271071–12

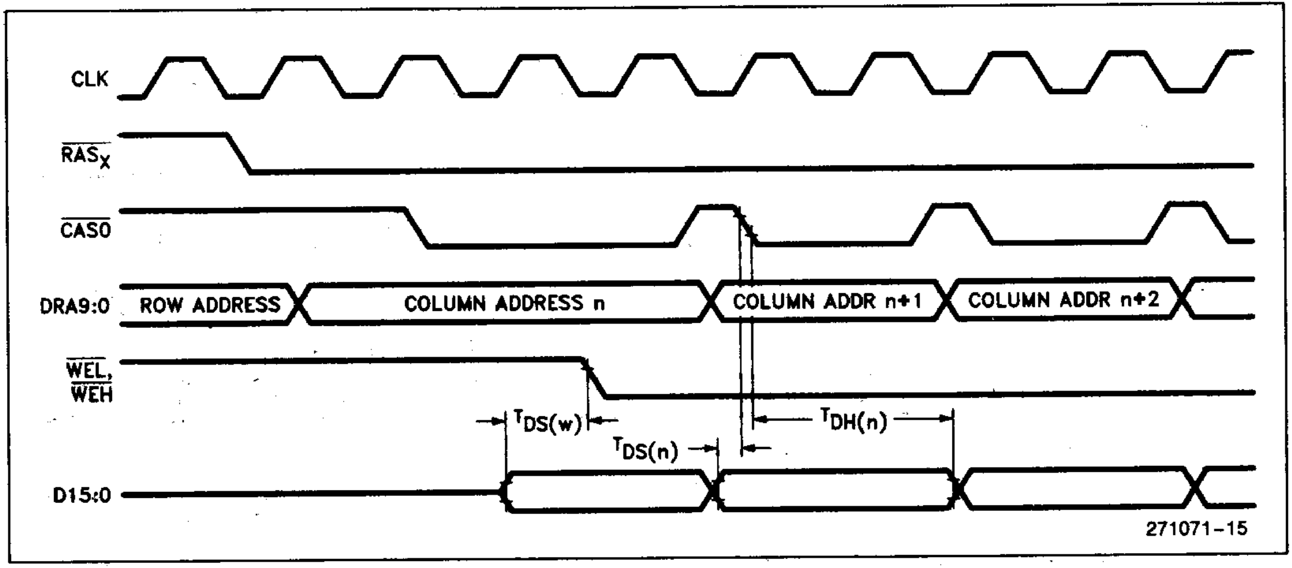
DRAM SIGNALS—INTERLEAVED PAGE MODE WRITE



DRAM SIGNALS—NON-INTERLEAVED FAST PAGE MODE READ

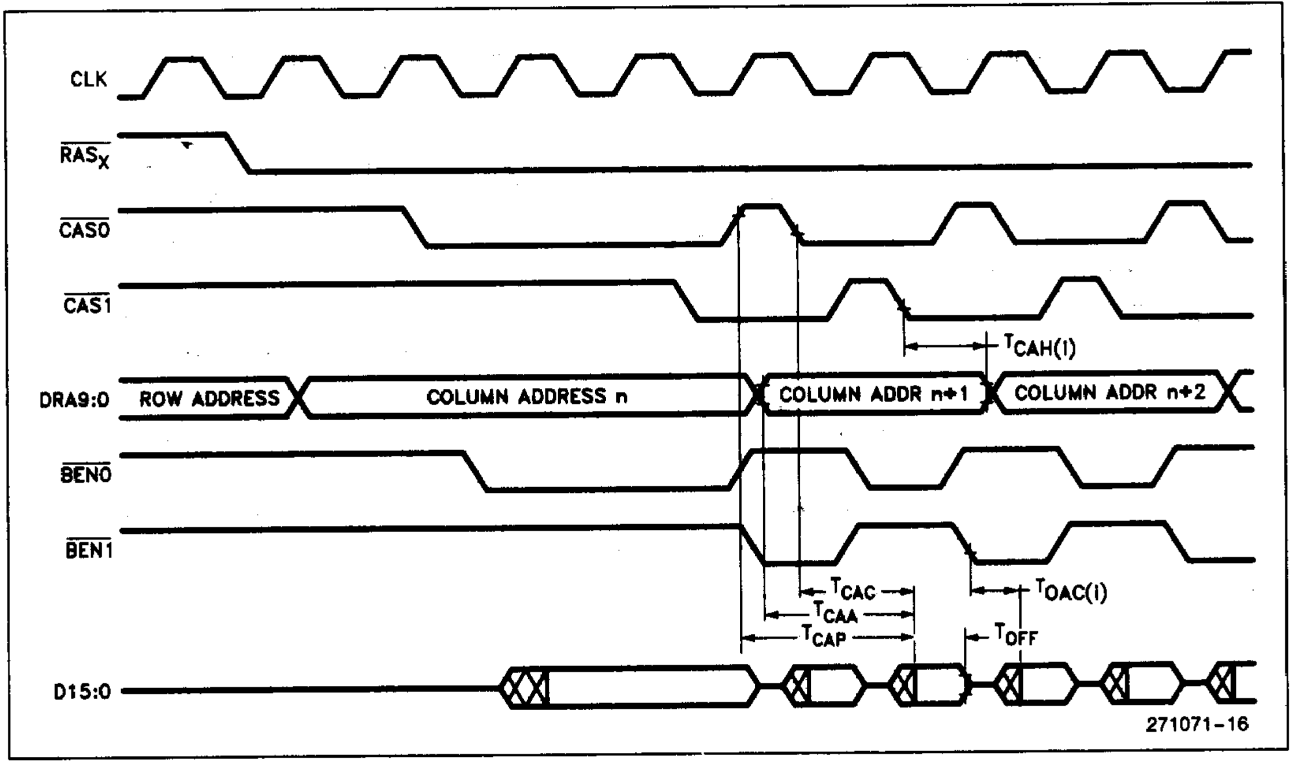


DRAM SIGNALS—NON-INTERLEAVED FAST PAGE MODE WRITE



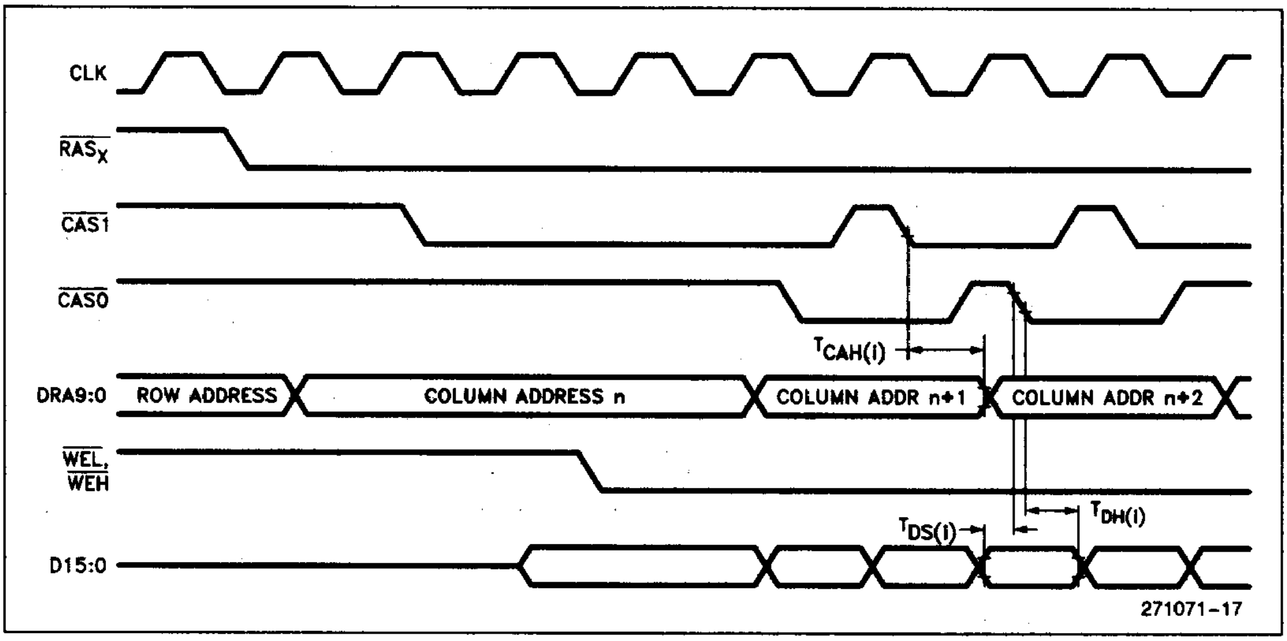
271071-15

DRAM SIGNALS—INTERLEAVED FAST PAGE MODE READ

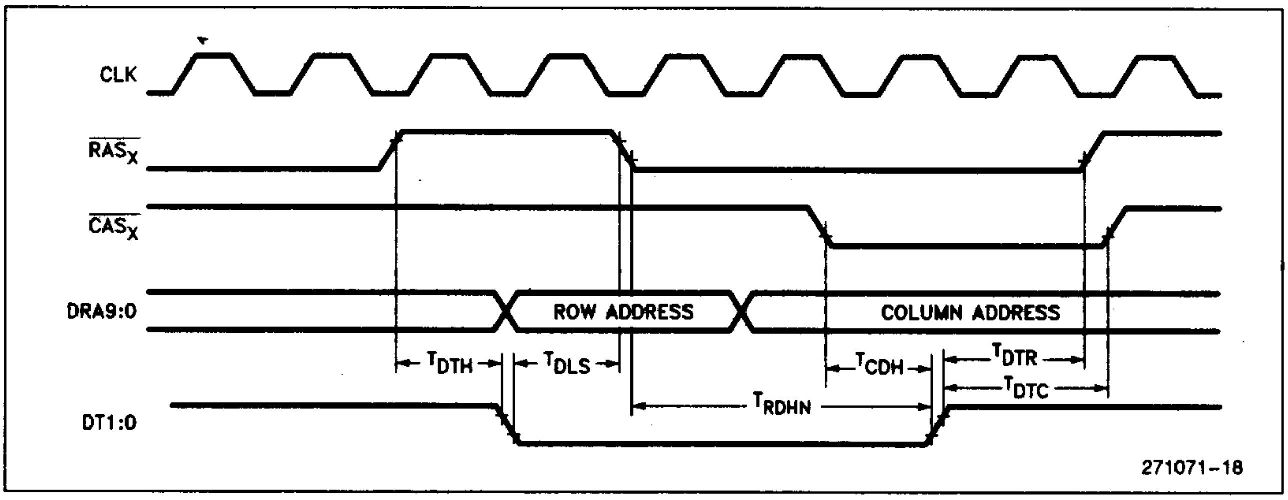


271071-16

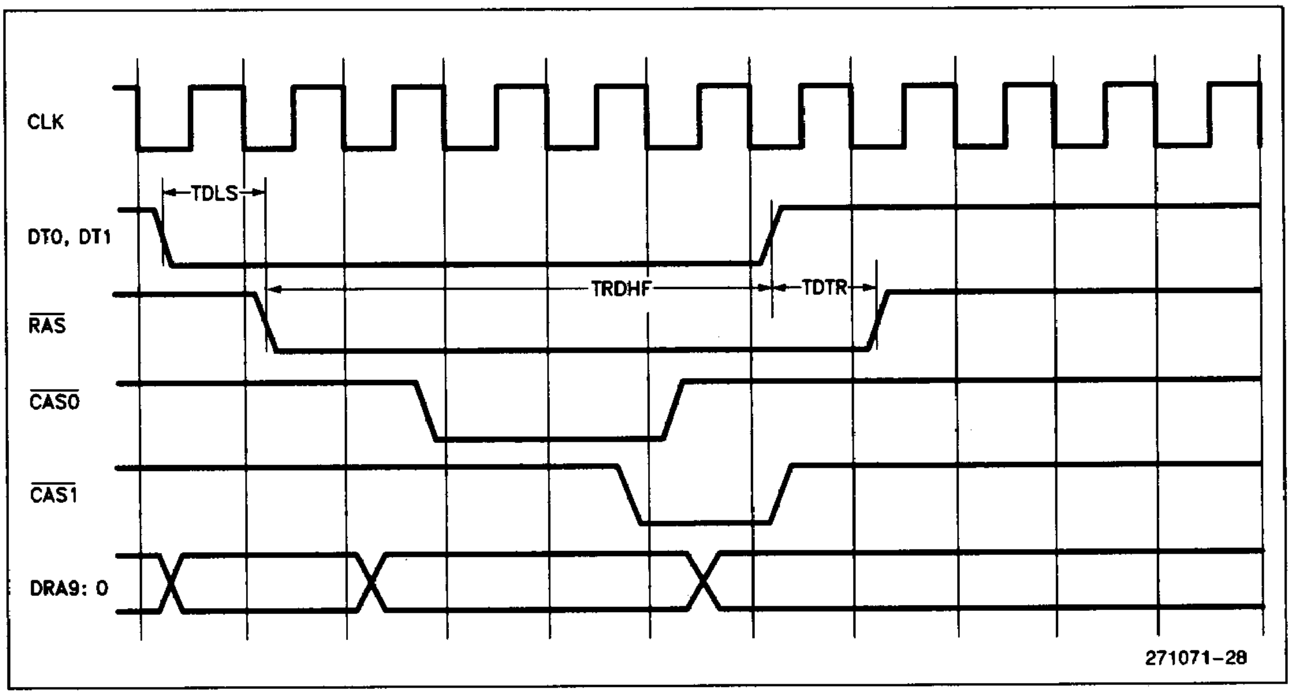
DRAM SIGNALS—INTERLEAVED FAST PAGE MODE WRITE



DRAM SIGNALS—NON-INTERLEAVED PAGE MODE AND FAST PAGE MODE VRAM DATA TRANSFER CYCLE

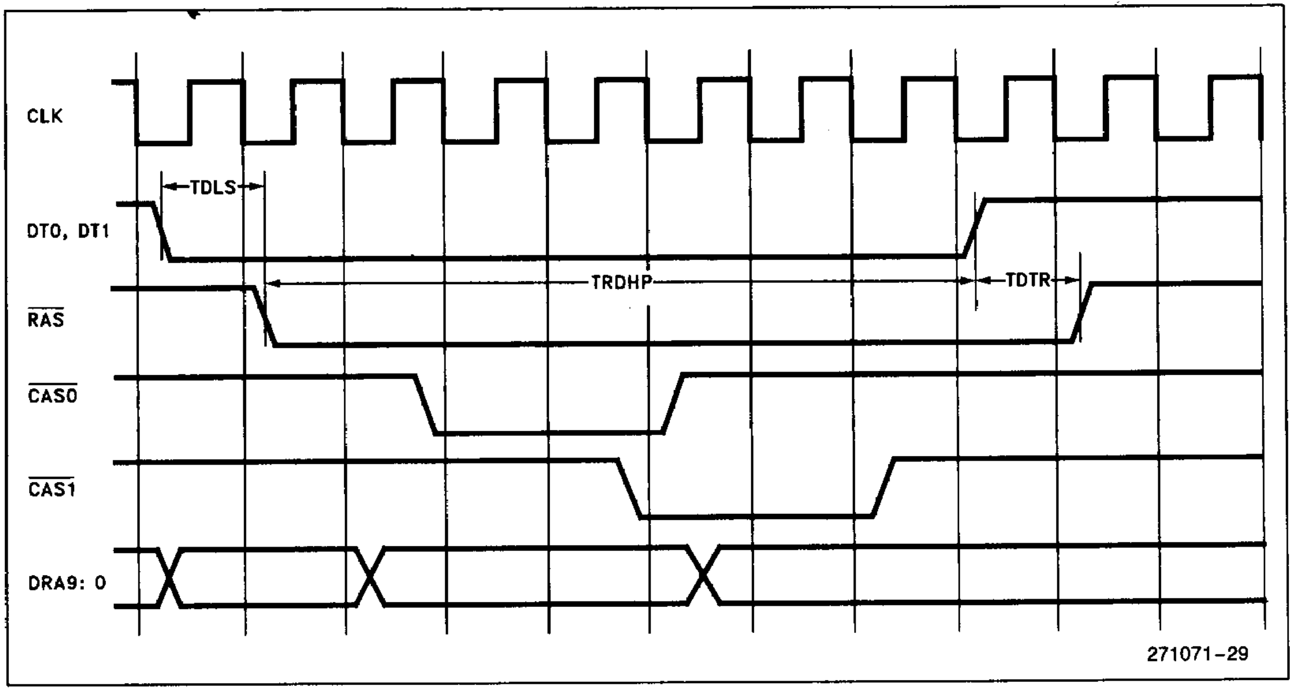


INTERLEAVED FAST PAGE MODE VRAM DATA TRANSFER CYCLE



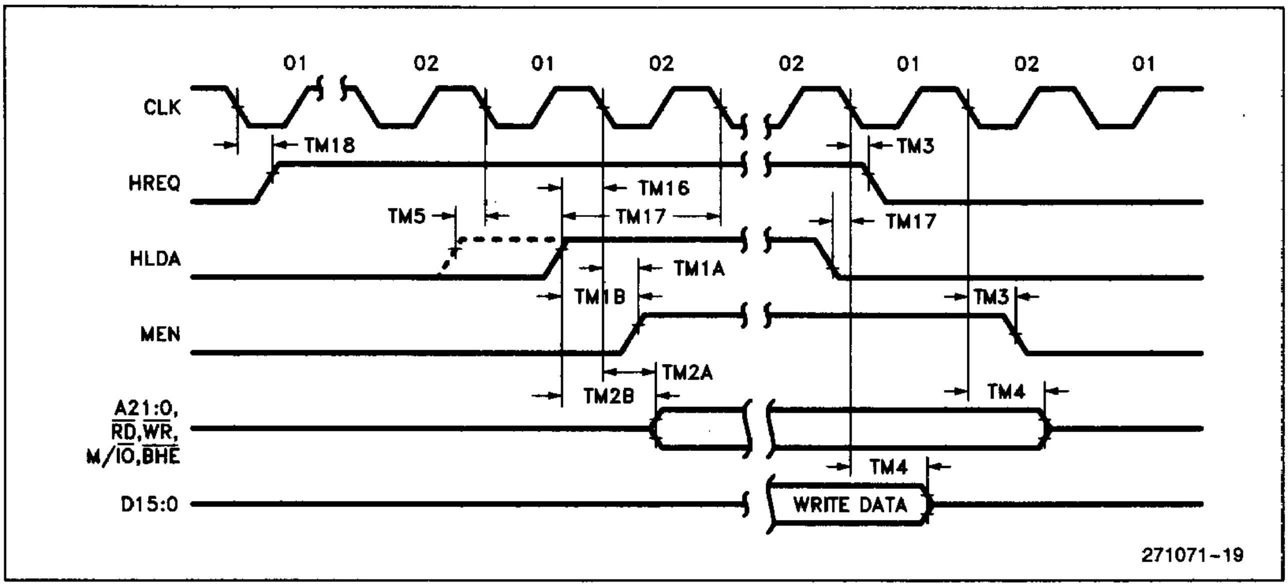
271071-28

INTERLEAVED PAGE MODE VRAM DATA TRANSFER CYCLE

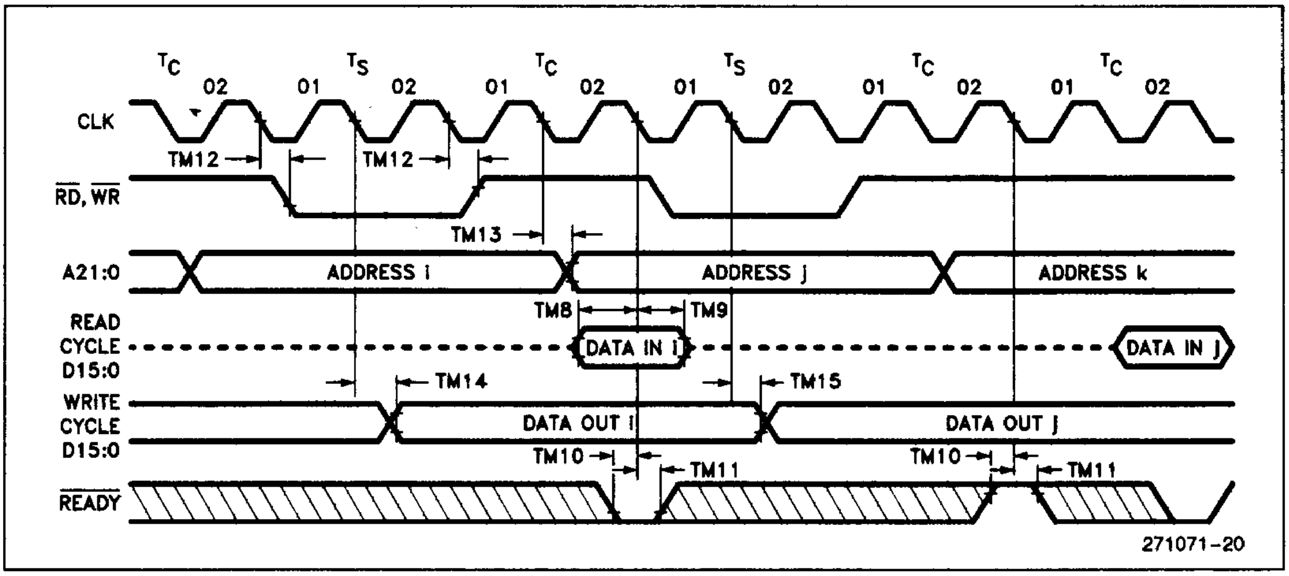


271071-29

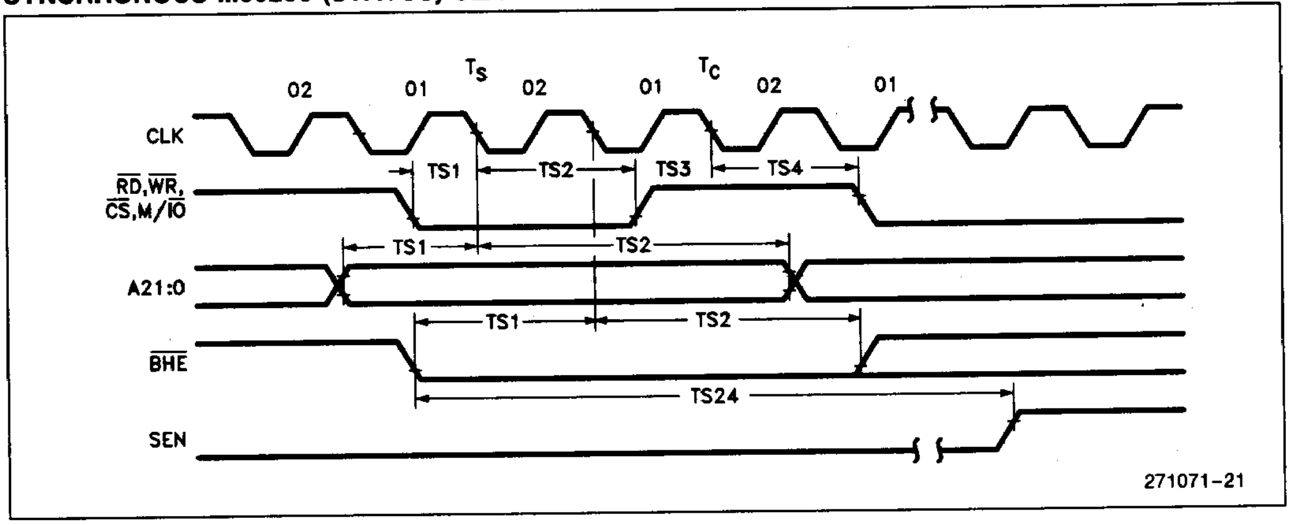
ENTERING AND LEAVING MASTER MODE



MASTER MODE TIMINGS

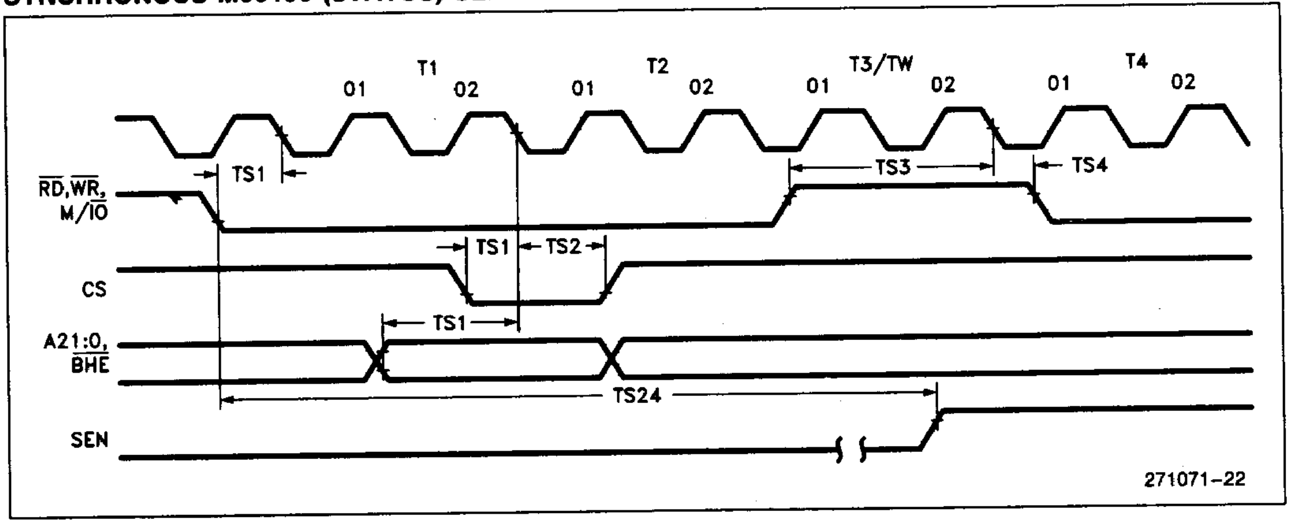


SYNCHRONOUS M80286 (STATUS) SLAVE INTERFACE



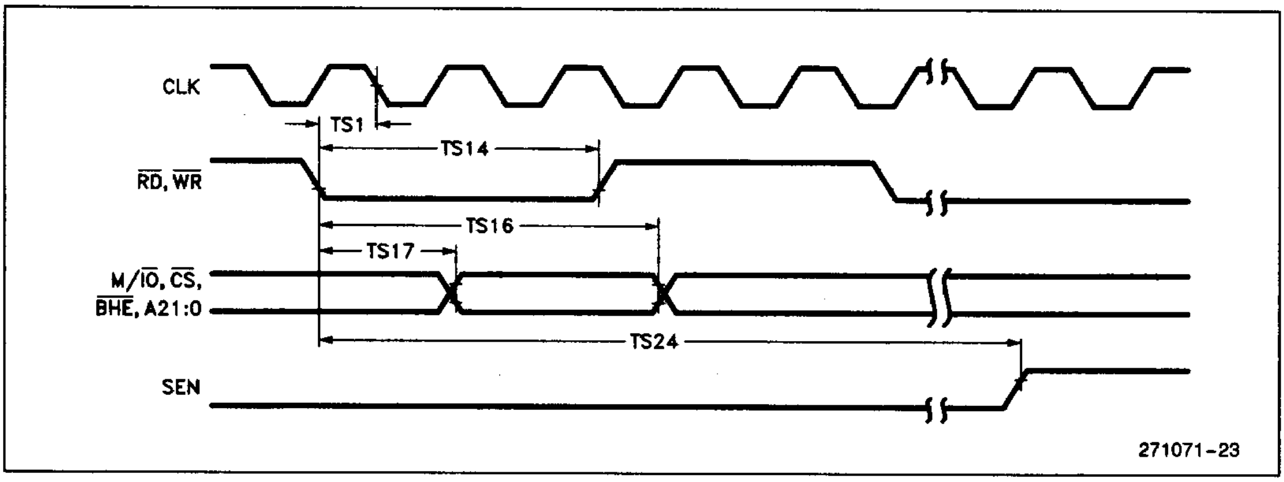
271071-21

SYNCHRONOUS M80186 (STATUS) SLAVE INTERFACE

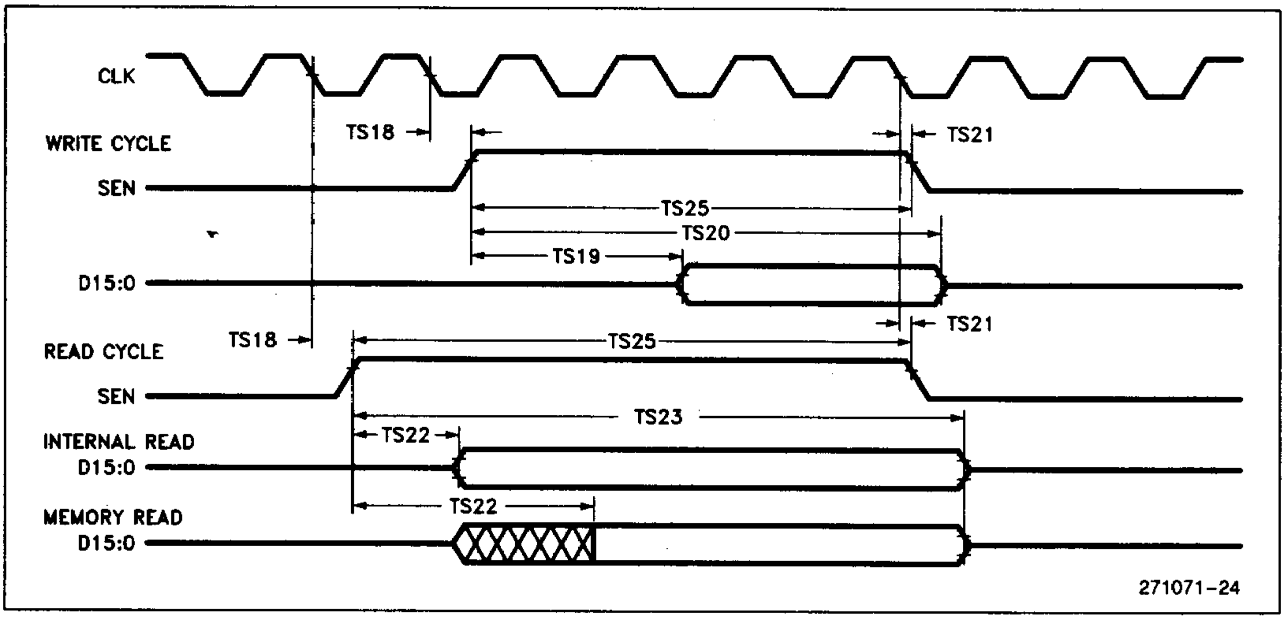


271071-22

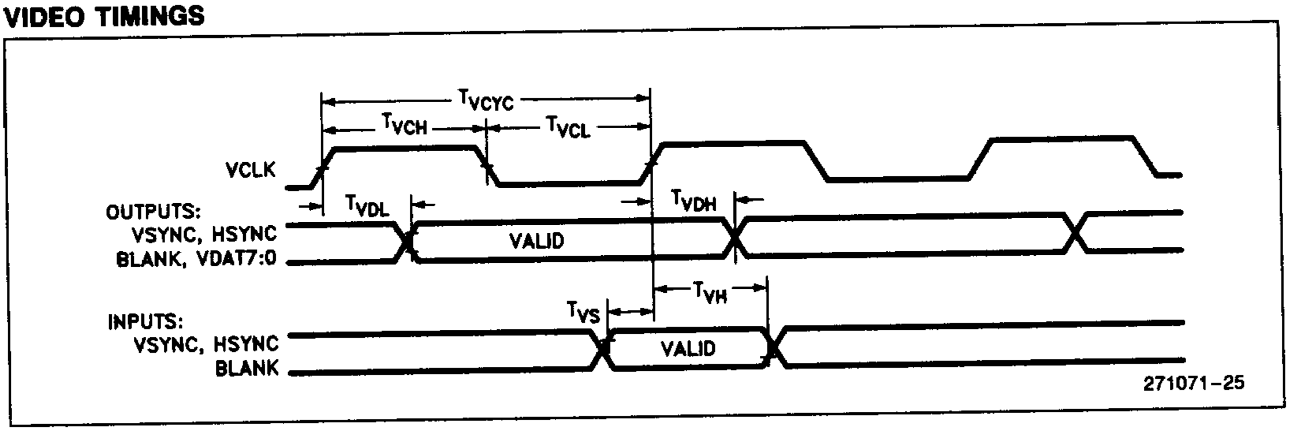
ASYNCHRONOUS SLAVE INTERFACE



SEN/DATA—SLAVE INTERFACE



VIDEO TIMINGS


T_VCYC
T_VCH
T_VCL
VCLK
OUTPUTS:
VSYNC, HSYNC
BLANK, VDAT7:0
T_VDL
T_VDH
VALID
INPUTS:
VSYNC, HSYNC
BLANK
T_VS
T_VH
VALID
271071-25