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PS1140 Termination Module User's Manual
01A000036-03 (Rev A-03)

PS1140 Termination Module User's Manual

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Table 1: Revision History

Rev.	Date	Description
1.0	April 16, 1998	First Created
A-02	May 31, 1998	Released by B. Siim.
A-03	Sept. 4, 1998	Minor revisions by J. Mills



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1. Glossary

The following list will provide some insight into terms used throughout this document:

4 HP	The width of a typical single wide CompactPCI slot. The distance between adjacent 4HP slots is exactly 0.800”.
8 HP	The width of a double wide CompactPCI slot. This type of slot is commonly used for power supplies and CPU modules.
84 HP	This is the typical maximum width of a 21 slot backplane. In actual fact an 84HP backplane supports 21x 4HP slots. The backplane dimensions are not exactly 84x 0.200”. The mechanical drawings should be used for exact dimensions and backplane screw locations.
3U	A half height CompactPCI slot or card.
6U	A full height CompactPCI slot or card.
CPCI	An acronym for the CompactPCI standard.
HP	This terminology refers to a unit of width commonly used within the CompactPCI mechanical specifications. An HP is nominally 0.200” in its common usage.
J1-J5	The CPCI specification uses the terminology J1, J2, J3, J4, or J5 to refer to specific connector locations within a slot. The connectors are numbered from J1 to J5 starting at the bottom of a 6U slot. The connectors are numbered J1 & J2 starting from the bottom of a 3U slot.
P1-P5	Please refer to the description for J1-J5.
ATX	Intel and industry PC manufacturers have introduced a new line of motherboards which uses a new type of power supply connector to provide +5, +3.3V, +12V & -12V to the motherboard. All PS13xx and PS14xx CompactPCI backplane members can be powered from one of these new power supplies. Intel’s web site (www.intel.com) has a downloadable ATX motherboard specification which fully specifies this power supply connector.



2. Background Information

The following documents should be used for reference when designing CompactPCI systems:

- PICMG 2.0 D2.20 CompactPCI Specification.
- PCI Local Bus Specification Rev 2.1
- PCI Bridge Specification Rev 1.0
- IEEE Std. 1101.1-1991
- IEEE Std. 1101.10-1996
- PCI Hardware and Software Architecture & Design 3rd edition. (ISBN 0-929392-32-9)
- ATX Specification Version 2.01, Intel Corporation, February 1997.



3. Termination Module Overview

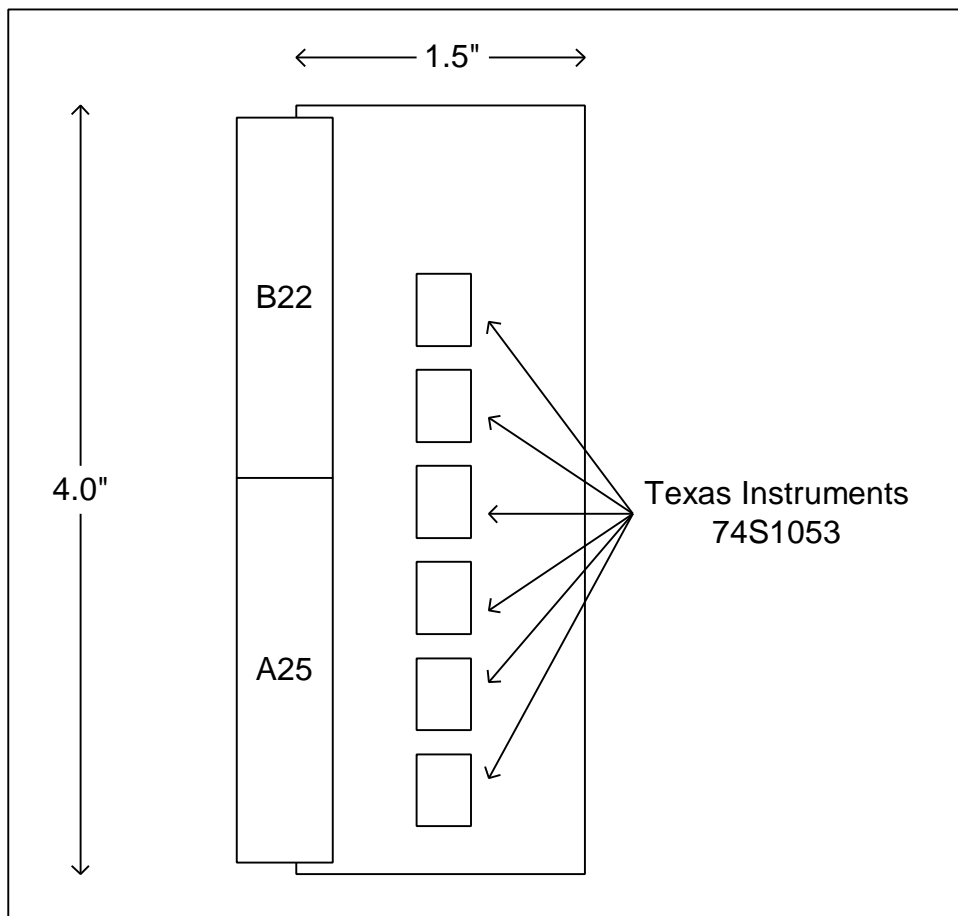
The CompactPCI specification requires that any backplane with 8 physical slots must have its CompactPCI signals terminated with a schottky diode array at the end of the backplane opposite the system slot.

The PS1140 terminates all of the critical PCI signals as required by the CPCI specification. All 32-bit and 64-bit signals are terminated, so the PS1140 can be used on 32-bit or 64-bit backplanes.

All PixStream™ backplanes that have bus segments with 8 physical slots will have appropriate connectors available for the installation of this module. The peripheral slot at the end of the bus farthest from the system slot will have long-tail connectors in the J1 and J2 positions. The PS1140 plugs into these connectors from the rear of the backplane.

Note that this module is only required when there are 8 physical slots on a CPCI bus segment. The requirement for termination is a function of the physical length of the bus, not the number of loads present on the bus.

Figure 1: PS1140 Diode Termination Module



4. Termination Module Details

4.1 Mechanical

The module is a 2 layer PCB approximately 4" tall, 1.5" wide, and 0.063" thick. The CPCI connectors (J1 and J2 only) are keyed such that the module can only be plugged into the rear of a backplane.

4.2 Power

The termination diodes are only connected to +5V and GND. Negligible current (<400 μ A) is drawn when the bus is inactive. There is no decoupling present on the board.

4.3 PCI Bus

The following signals are terminated:

AD[0:63], C/BE[0:7]#, REQ64#, ACK64#, PAR64, SERR#, SBO#, STOP#, DEVSEL#, PERR#, SDONE, PAR, IRDY#, TRDY#, LOCK#, FRAME#, RST#, INTA#, INTB#, INTC#, INTD#

Care should be taken if the PS1140 is used on a 32-bit backplane where J2 is installed. Even if they are not used by the CPCI bus, the terminators will still be connected to the 64-bit signals of J2. If the peripheral board in the slot opposite the termination module attempts to use the terminated pins, it is possible that the terminators could interfere with normal operation.