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Rev.1.0 June 27, 2006

2.7W/CH STEREO CLASS-D AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TMPA2155DS is a stereo class-D audio power amplifier IC. With BTL(Bridge-Tied-Load) configuration, it delivers up to 2.7W/ch(5.4W in all) into a 3 ohm load or 2.3W/ch(4.6W in all) into a 4 ohm load or 1.5W/ch(3W in all) into an 8 ohm load. No external heat-sink is required.

For multiple-input applications, independent gain control and corner frequency can be implemented by summing the input sources through resistor ratio and input capacitor values. Automatic voltage gain control makes the best use of battery.

Analog input signal is converted into digital output which drives directly to the speaker. High power efficiency is achieved due to digital output at the load. The audio information is embedded in PWM(Pulse Width Modulation)

APPLICATIONS

Multimedia application includes Cellular Phones, PDAs, DVD/CD players, TFT LCD TVs/Monitors, 2.1 channel/5.1 channel audio systems, USB audio. It is also ideal for other portable devices like Wireless Radios.

FEATURES

- + 2.5V to 6V Single Supply
- + Up to 2.7W / Ch at 5V, 3 ohms
- Up to 85% Power Efficiency
- Automatic output power control (APC)
- + 2.2mA / Ch Quiescent Current at 5V
- + Less Than 0.2uA / Ch Shutdown Current
- Pop-less Power-Up, Shutdown and Recovery
- Differential 250 KHz PWM Allows Bridge-Tied Load to Doubles Output Power and Eliminates LC Output Filter
- Thermal Shutoff and Automatic Recovery
- Compatible with earphone application
- Output Pin Short-Circuit Protection (Short to Other

Outputs, Short to VCC, Short to Ground)

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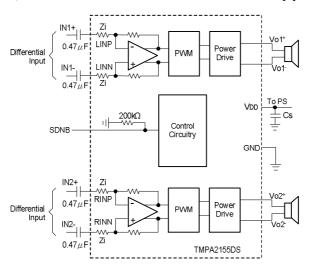
Differential Signal Processing Improves CMRR

Package

for PCB layout.

TSSOP20, QFN24 Available For best performance, please refer to <u>http://www.taimec.com.tw/English/EVM.htm</u> <u>http://www.class-d.com.tw/English/EVM.htm</u>

REFERENCE CIRCUIT (Please refer to TMPA002.APP for application)



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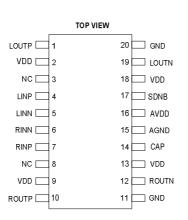
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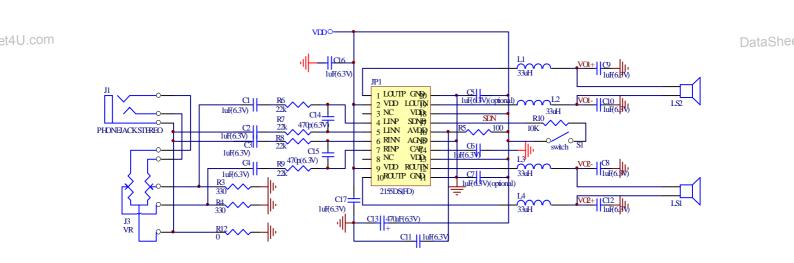
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(Please email <u>david@taimec.com.tw</u> for complete datasheet.)

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Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.



Typical Application

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

	In normal mode	-0.3V to 6V	V
Supply voltage, VDD, AVDD	In shutdown mode	-0.3V to 7V	V
Input voltage, Vi	-0.3V to VDD+0.3V		
Continuous total power dissipation	See package dissipation ratings		
Operating free-air temperature, TA	-20 to 85	°C	
Operating junction temperature, TJ	-20 to 150		
Storage temperature, Tstg	-40 to 150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITONS

		MIN	NOM	МАХ	UNIT
Supply voltage, VDD, AVDD		2.5		6	V
High-level input voltage, Vін	SDNB	2		Vdd	V
Low-level input voltage, V⊫	SDNB	0		0.8	V
Operating free-air temperature, TA		-20		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING	Ta≤25 °C	TA = 70 °C	TA = 85 °C
	FACTOR	POWER RATING	POWER RATING	POWER RATING
TSSOP20	8.73 mW/ °C	1.09W	698mW	567mW

ELECTRICAL CHARACTERISTICS

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T _A =25 °C (unless otherwise noted) DataSheet4U.com							
	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
Vos	Output offset voltage (measured differentially)	VI=0V,Av=2, V _{DD} =AV _{DD} =2.5V to 5.5V		25		mV	
PSRR	Power supply rejection ratio	$V_{DD}=AV_{DD}=2.5V$ to 5.5V		-75	-55	dB	
CMRR	Common mode rejection ratio	$V_{DD}=AV_{DD}=2.5V$ to 5.5V, VIC=1Vpp, RL=8 Ω		-55	-50	dB	
IIH	High-level input current	V _{DD} =AV _{DD} =5.5V, VI=5.8V (SDNB)		30		μA	
IIL	Low-level input current	V _{DD} =AV _{DD} =5.5V, VI=-0.3V (SDNB)			1	μA	
lq	Quiescent current / Ch	$V_{DD}=AV_{DD}=5V$, no load		2.2	3	mA	
IQ (SD)	Shutdown current / Ch	V(SDN)=0.8V, V _{DD} =AV _{DD} =2.5V to 5.5V		0.2	0.5	μA	
rDS(on)	Static output resistance	$V_{DD}=AV_{DD}=5.5V$		790		mΩ	
f(sw)	Switching frequency	$V_{DD}=AV_{DD}=2.5V$ to 5.5V	230	280	330	kHz	
*Av	BTL Gain	$V_{DD}=AV_{DD}=2.5V$ to 5.5V, RL=8 Ω	12	16	20	V V	
Rsdn	Resistance from shutdown to GND	V(SDNB)=5V		200		kΩ	
Zı	Input impedance	RINN,RINP,LINN,LINP		15		kΩ	

*The gain of the amplifier is determined by, for $V_{\text{DD}}{=}V_{\text{DDA}}{=}2.5V$ to 5.5V

 $Gain = \frac{320 kohms}{Ri + 15 kohms} \quad \mbox{where Ri is the external serial resistance at the input pin.}$

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OPERATING CHARACTERISTICS

 $T_A=25 \ ^{\circ}C, RL=8\Omega$ speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYP	MAX	UNIT
		RL=8Ω	V _{DD} =AV _{DD} =5V. THD+N=10%,f=1kHz.	1.5		W
Po Output power / Ch (Limited by thermal condition)		RL=4Ω		2.3		W
	(RL=3Ω		2.7		W
THD+N	Total harmonic distortion plus noise	$V_{DD}=AV_{DD}=5V$, Po=0.85W, RL=8 Ω , f=1kHz		0.55		
		$V_{DD}=AV_{DD}=5V$, Po=1.3W, RL=4 Ω , f=1kHz		0.55		%
		$V_{DD}=AV_{DD}=5V$, PO=1.5W, RL=3 Ω , f=1kHz		0.64		
SNR	Signal-to-noise ratio	V_{DD} =A V_{DD} =5V, Po=1W, RL=8 Ω		95		dB
Crosstalk	Crosstalk between outputs	V _{DD} =AV _{DD} =5V, Po=1W	-68		dB	

TERMINAL FUNCTIONS

TERMINAL			DECODIDE ION	
NAME	PIN NO	I/O	DESCRIPTION	
AGND	15	-	Analog ground DataSheet4U.com	
AVdd	16	-	Analog Power supply	
CAP	14	I	Capacitance for power up delay	
GND	11,20	-	Digital ground	
LINN	5	I	Negative input of left channel	
LINP	4	I	Positive input of left channel	
LOUTN	19	0	egative output of left channel	
LOUTP	1	0	ositive output of left channel	
NC	3,8	-	o Connection	
RINN	6	I	legative input of right channel	
RINP	7	Ι	Positive input of right channel	
ROUTN	12	0	Negative output of right channel	
ROUTP	10	0	Positive output of right channel	
SDNB	17	I	Shutdown terminal (active low logic)	
Vdd	2,9,13,18	-	Digital Power supply	

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TYPICAL CHARACTERISTICS

Note 1. Input coupling $1\mu F$ capacitors are used for all measurements.

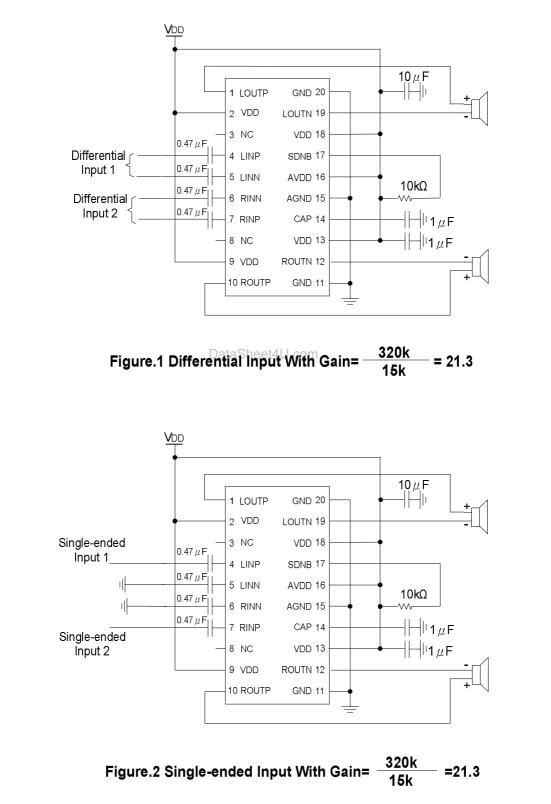
- 2. Differential inputs are applied and BTL outputs are measured.
- 3. Balanced LC filter is used for THD+N measurement and power efficiency measurement.
- 4. Characteristic frequency of the LC filter is set 41KHz unless otherwise specified.

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APPLICATION INFORMATION



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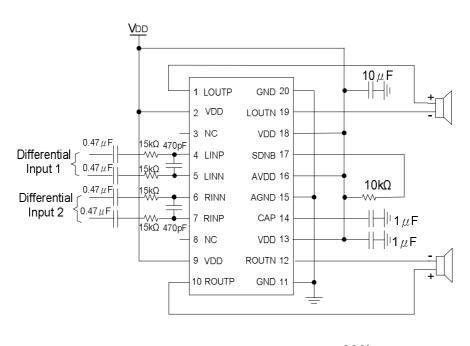
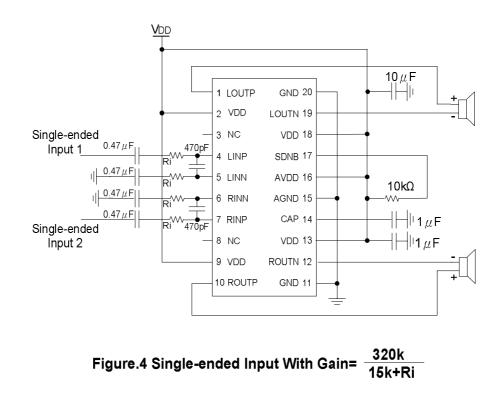


Figure.3 Differential Input With Gain= $\frac{320k}{15k+15k}$ = 10.7 DataSheet4U.com

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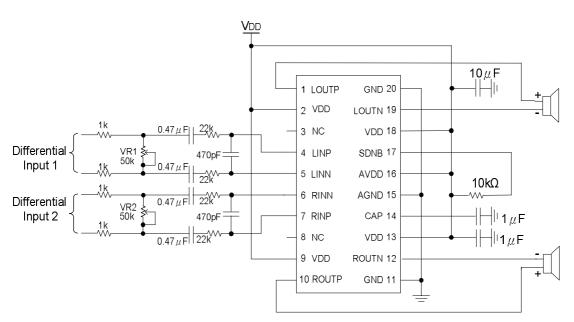


Figure.5 Differential Input With Gain Control

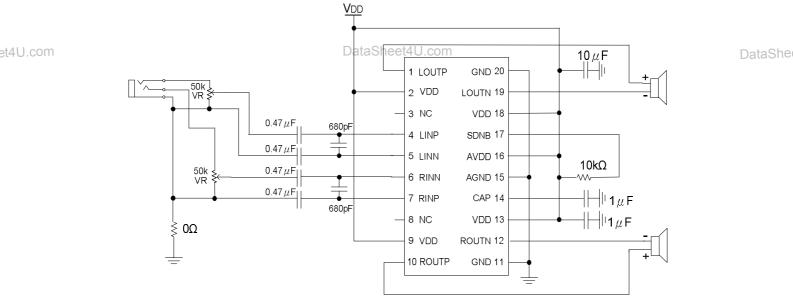


Figure.6 Single-ended Input With Gain Control

I Input Resistors and Gain

The gain of the amplifier is determined by, for VDD=VDDA =2.5V to 5.5V

 $Gain = \frac{320kohms}{Ri+15kohms}$ where Ri is the external serial resistance at the input pin.

Note : Please refer to document 010 APP for more application examples.

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DETAILED DESCRIPTION

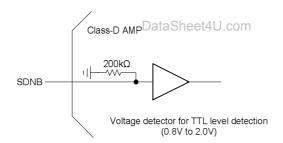
Efficiency

The output transistors of a class D amplifier act as switches. The power loss is mainly due to the turn on resistance of the output transistors when driving current to the load. As the turn on resistance is so small that the power loss is small and the power efficiency is high. With 8 ohm load the power efficiency can be better than 85%.

Shutdown

The shutdown mode reduces power consumption. A LOW at shutdown pin forces the device in shutdown mode and a HIGH forces the device in normal operating mode. Shutdown mode is useful for power saving when not in use. This function is useful when other devices like earphone amplifier on the same PCB are used but class D amplifier is not necessary. Internal circuit for shutdown is shown below.





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Pop-less

A soft start capacitor can be added to the CAP pin. This capacitor introduces delay for the internal circuit to be stable before driving the load. The pop or click noise when power up/down or switching in between shutdown mode can be thus eliminated. The delay time is proportional to the value of the capacitance. It is about 500ms for a capacitor of 1uF at 5v.

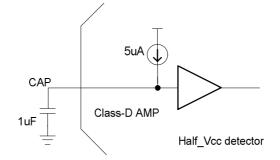
CAP

Cap provides a way of soft startup delay. A 5uA current source and a half_Vcc detector are integrated in the chip. The charged capacitor is externally hooked up. For C=1uF the half_Vcc delay is

 $T = CV / I = (1uF \times 2.5V) / 5uA = 0.5 \text{ seconds}$

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Voltage gain

The voltage gain is defined in the table on page 3. For lower voltage gain one can add external input resistors to input pins. If external resistors are used they should be well matched. Well matched input resistors are also required even for single ended input configuration for low noise.

Automatic output Power Control (APC)

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The voltage gain is self adjusted in the chip over voltage range. This means that, regardless supply voltage change, the output power keeps about the same for a given input level from VDD=5.5v to 2.5v. It allows the best use of the battery.

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Differential input VS single ended input

Differential input offers better noise immunity over single ended input. A differential input amplifier suppresses common noise and amplifies the difference voltage at the inputs. For single ended applications just tie the negative input end of the balanced input structure to ground. If external input resistors are used, the negative input has to be grounded with a series resistor of the same value as the positive input to reduce common noise.

Output filter

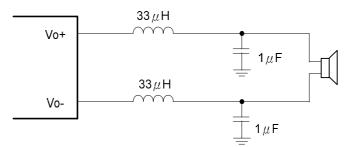
Ferrite bead filter can be used for EMI purpose. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker. EMI is also affected by PCB layout and the placement of the surrounding components.

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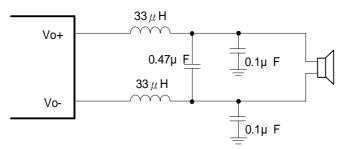
The suggested LC values for different speaker impendence are showed in following figures for reference.







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Typical LC Output Filter (2)

Over temperature protection

A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145° C and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120° C.

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Over current protection

A current detection circuit is built in the device to detect the switching current of the output stages of the device. It disables the device when the current is beyond about 3.5amps. It protects the device when there is an accident short between outputs or between output and power/gnd pins. It also protects the device when an abnormal low impedance is tied to the output. High current beyond the specification may potentially causes electron migration and permanently damage the device. Shutdown or power down is necessary to resolve the protection situation. There is no automatic recovery from over current protection.

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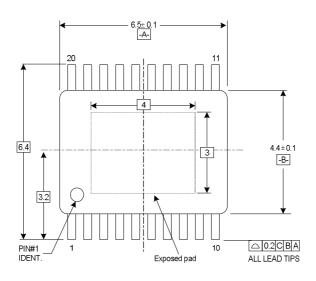
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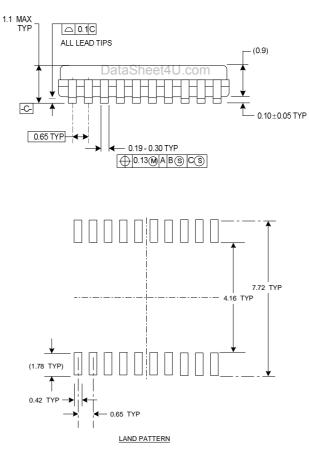
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Physical Dimensions (IN MILLIMETERS)





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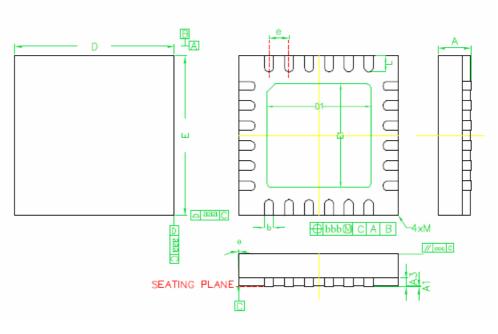
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ANTER ATTACKS OF	DIMENSIONS IN MILLIMETERS				
SYMBOLS	MIN	NOM	MAX		
Α	0.80	0.90	1.00		
A1	0	0.015	0.030		
A3		0.20REF.			
b	0.18	0.23	0.28		
D	3.90	4.00BSC	4.10		
D1	2.50	2.60	2.70		
Е	3.90	4.00°BSC	4.10		
E 1	2.50	2.60	2.70		
e		0.50BSC			
L	0.32	0.40	0.48		
θ	-12		0		
aaa		0.25			
bbb		0.10			
ccc		0.10			
Μ			0.05		
Burr	0	0.030	0.060		

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