National Semiconductor

TP50981/TP50981A, TP50982/TP50982A, TP50985/TP50985A Push Button Pulse Dialer Circuits

General Description

This family of monolithic CMOS circuits provides all logic necessary to convert keyboard inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory capable of storing up to 17 digits allows keyboard entries to be made at rates comparable to those of tone-dialing telephones and provides one-key redial of the last number dialed. The keyboard inputs interface directly to a standard 2-of-7 keypad with positive-common or an inexpensive form A-type keyboard. Two outputs, one for pulsing the telephone line and one to mute the receiver, are provided along with pin selectable Break/Make ratios and an on-chip voltage regulator. The low voltage and low current requirements of these devices allow direct telephone line powered operation.

Features

- TP50981/TP50981A, TP50985/TP50985A for pulsing loop in shunt with speech network
- TP50982/TP50982A for pulsing loop in series with speech network
- 1.7V, 150 μA operation TP50981A, TP50982A and TP50985A
- Single-contact or positive-common key inputs
- Break/Make ratio pin selectable
- On-chip voltage regulator
- On-chip oscillator using 480 kHz ceramic resonator
- Scratchpad (new number storage without dialing) on TP50985/TP50985A
- 10/20 pps option on TP50985/TP50985A

Block Diagram

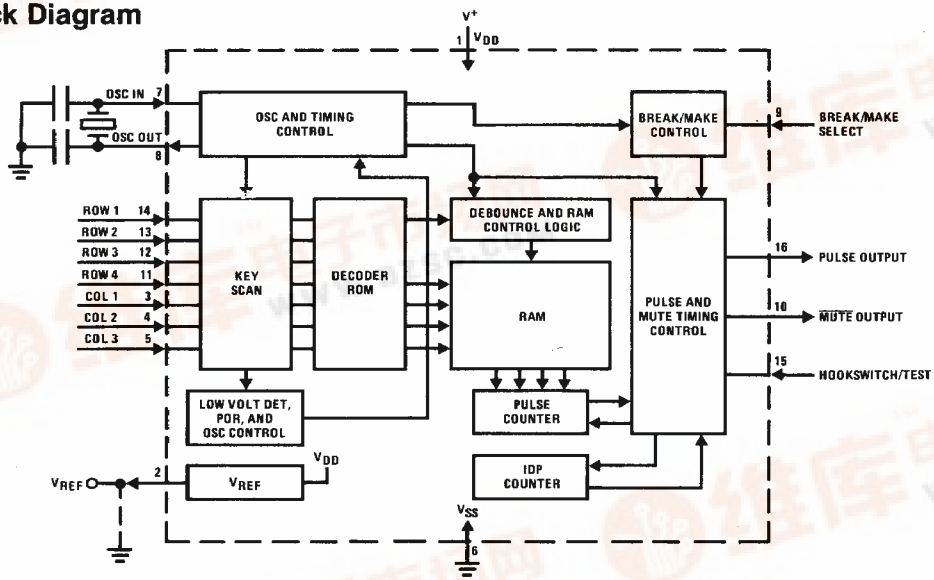
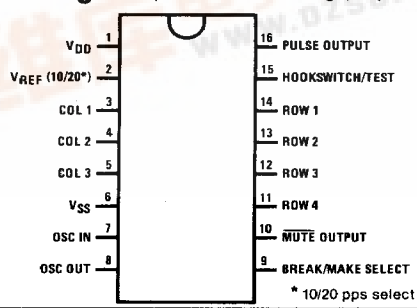


FIGURE 1

Connection Diagram (Dual-In-Line Package, Top View)



Order Number TP50981N, TP50981AN, TP50982N, TP50982AN, TP50985N or TP50985AN
See NS Package N16A

* 10/20 pps select input on TP50985/TP50985A

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}–V_{SS})	6.0V
Voltage on Any Pin	V_{DD} + 0.3V to V_{SS} – 0.3V
Operating Temperature	– 30°C to + 70°C
Storage Temperature	– 55°C to + 150°C
Maximum Power Dissipation (25°C)	500 mW

DC Electrical Characteristics

T_A within operating temperature range, V_{DD} min ≤ V_{DD} ≤ 5.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Min DC Supply Voltage					
TP50981, TP50982, TP50985	Pin 1 Ref. Pin 6	2.5			V
TP50981A, TP50982A, TP50985A		1.7			V
Memory Retention Current	V_{DD} = 1.7V, Notes 1 and 2		0.5	1.0	μA
DC Operating Current	Off-Hook, Valid Key, V_{REF} Tied to V_{SS}		100	150	μA
V_{REF} Sink Current	V_{DD} = 5.0V	1.0			mA
$\overline{MUTE}$ Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	0.5	2.0		mA
PULSE Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	1.0	4.0		mA
$\overline{MUTE}$ and PULSE Leakage	V_{DD} = 5.0V, V_O = 5.0V		0.001	1.0	μA
Keyboard Contact Resistance				1.0	kΩ
Keyboard Capacitance				30	pF
Logic '0' Level Input		V_{SS}		0.2 V_{DD}	V
Logic '1' Level Input		0.8 V_{DD}		V_{DD}	V
Keyboard Pull-Up Resistance			4.0		kΩ
Keyboard Pull-Down Resistance			100		kΩ
HOOKSWITCH Pull-Up Resistance			100		kΩ

Note 1: On-hook mode, V_{REF} tied to V_{SS}, all outputs open.
Note 2: Power-on reset and low-voltage-detect circuits inhibit the redial function if the supply voltage falls below V_{DD} Min.

AC Electrical Characteristics

T_A within operating temperature range, V_{DD} min ≤ V_{DD} ≤ 5.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	Anti-Resonant Mode		480		kHz
Keyboard Debounce Time	OSC IN = 480 kHz	9		11	ms
Oscillator Start-Up Time	V_{DD} = V_{DD} Min		5.0		ms
Pulse Rate			10.0		pps
Break Time	Pin 9 @ V_{DD}		61.0		ms
	Pin 9 @ V_{SS}		67.0		ms
Interdigit Pause			800		ms

Functional Description

The time base for this family of pulse dialers is derived from a 480 kHz ceramic resonator in anti-resonant mode. In the on-hook condition, the oscillator is stopped and all keyboard row and column inputs are forced to V_{DD} which inhibits any key closures from effecting the circuit. After going off-hook the oscillator remains off and the keyboard inputs go to a static sensing mode. Upon sensing a single key closure, the oscillator starts, and the row and column inputs are alternately scanned at a 500 Hz rate. When the circuit senses a valid key closure for the required debounce time, the key is written into memory and outpulsing begins for that key. Further valid keys are entered in sequence, provided that no more than 17 digits remain to be outpulsed. If no further key is entered, following the IDP the oscillator will stop and the key inputs will return to the static sensing mode awaiting further keys or a return to the on-hook condition. By maintaining power to the device while on-hook, the last number dialed (up to 17 digits) is stored in the memory. On going off-hook (HOOKSWITCH goes to V_{SS}) the stored number can be automatically redialed by entering either * or # as the first key (TP50981/TP50981A and TP50982/TP50982A). Entry of any digit as the first key following off-hook clears the redial memory and enters digits in sequence, starting at location 1.

The * key on the TP50985/TP50985A is redefined to provide entry to the Scratchpad feature. This mode allows the outpulsing memory to be overwritten with a new telephone number without that number being outpulsed. Scratchpad mode can be entered directly after going off-hook or during a conversation by keying * followed by the next desired number. The new number can only be outpulsed by returning on-hook, then off-hook followed by the # key, which will redial the last number as normal.

The TP50985/TP50985A also enables the user to select an output pulse rate of either 10 pps by connecting pin 2 to ground or 20 pps by connecting pin 2 to V_{DD}. On this version V_{REF} is connected to V_{SS} internally.

Pin Descriptions

V_{DD} (pin 1): This is the positive supply to the device and is referenced to V_{SS} (pin 6). The voltage on this pin must be limited to less than 6V either externally or by current-limiting the supply to the on-chip voltage regulator. In the last-number-stored mode a minimum of 1 μA of supply current must be available to this pin while on-hook.

V_{REF} (pin 2): In normal applications, this pin is tied to V_{SS} (pin 6) which enables the on-chip voltage regulator circuit. When V_{REF} is tied to V_{SS}, the voltage regulator will provide a current sink from V_{DD} to V_{SS} of a minimum of 1 mA with V_{DD} equal to 5V.

KEYBOARD INPUTS (pins 3, 4, 5, 11, 12, 13, and 14): A valid key entry is defined as either connecting a single row to a single column or connecting V_{DD} simultaneously to a single row and a single column. This allows direct interface to an inexpensive single-contact (form A) keyboard, the standard 2-of-7 keyboard with positive-common, or logic-generated inputs.

In the on-hook condition [HOOKSWITCH/TEST (pin 15) connected to V_{DD}] the keyboard inputs are disabled and pulled high. Upon entering the off-hook condition the keyboard inputs go to a static sensing mode until a key closure is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The key must then remain valid continuously for the specified debounce time before the circuit will accept and decode it and begin outpulsing.

V_{SS} (pin 6): This is the negative supply.

OSCILLATOR IN, OUT (pins 7, 8): The device contains an on-chip oscillator circuit designed to work with a 480 kHz ceramic resonator (anti-resonant mode) and 2 external capacitors, normally 100 pF. A 1 MΩ resistor is included on-chip for good oscillator stability. The circuit may also be driven with an external 480 kHz source on OSCILLATOR IN (pin 7).

BREAK/MAKE SELECT (pin 9): The Break/Make ratio is selected by connecting pin 9 to either V_{DD} or V_{SS}. Table I indicates the available ratios.

TABLE I. BREAK/MAKE SELECT

Input to BREAK/MAKE (pin 9)	PULSE OUTPUT Break	Make
V_{DD}	61%	39%
V_{SS}	67%	33%

$\overline{\text{MUTE}}$ (pin 10): This pin is the output of an open-drain N-channel transistor. It drives a simple interface circuit to mute the receiver during outpulsing. See the timing diagram and application notes for further information concerning this output.

HOOKSWITCH/TEST (pin 15): This input has a 100 kΩ internal pull-up resistor to V_{DD}. Allowing this pin to float, or connecting a V_{DD} level puts the circuit in the on-hook idle mode.

With this pin connected to V_{SS} the circuit is in the off-hook mode and will accept keyboard inputs, and outpulse them at the normal 10 pps rate. When the outpulsing is complete, the oscillator stops and waits for further key inputs. If, however, pin 15 is taken to V_{DD} while the circuit is still outpulsing the remaining digits will be outpulsed at 100 times the normal rate (BREAK/MAKE becomes 50%). This allows for rapid testing of the device and also provides a means for resetting the circuit if power to the device is maintained while on-hook. (Note: Taking the worst-case of 17 zeros remaining to be outpulsed, this operation could take 300 ms to complete. Therefore, to ensure that the circuit has been properly reset, pin 15 should remain at V_{DD} for more than 300 ms before entering a new number.)

PULSE OUTPUT (pin 16): The pulse output consists of an open-drain N-channel transistor. It is intended to drive a transistor interface circuit to pulse the telephone line with the correct Break/Make ratio, IDP timing, and pulse rate. On the TP50981/TP50981A, TP50985/TP50985A this output is normally low and pulses high. On the TP50982/TP50982A the output is normally high and pulses low. See *Figure 2* for further details of the timing differences between the parts.

Timing Diagram

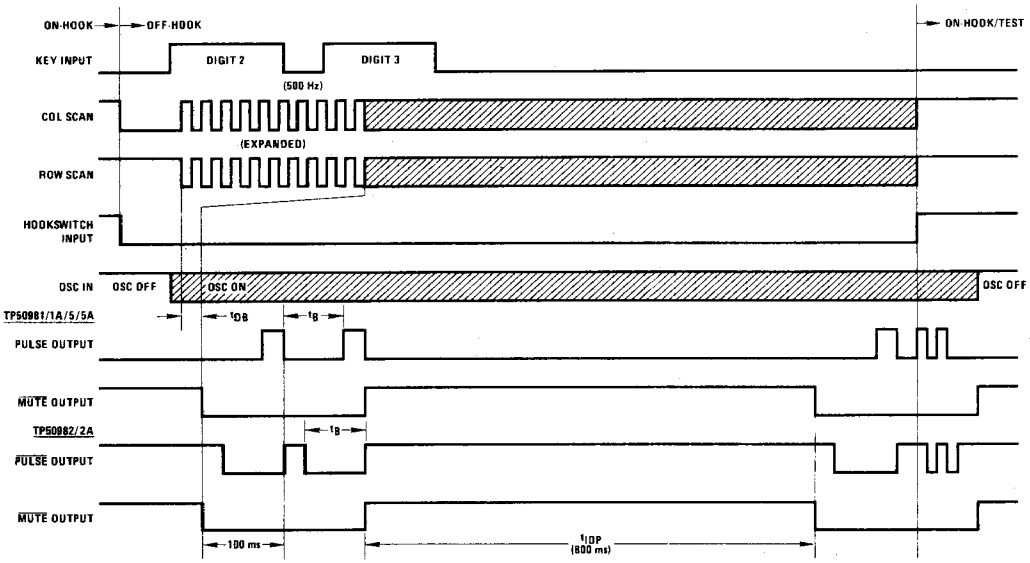


FIGURE 2

Applications Information

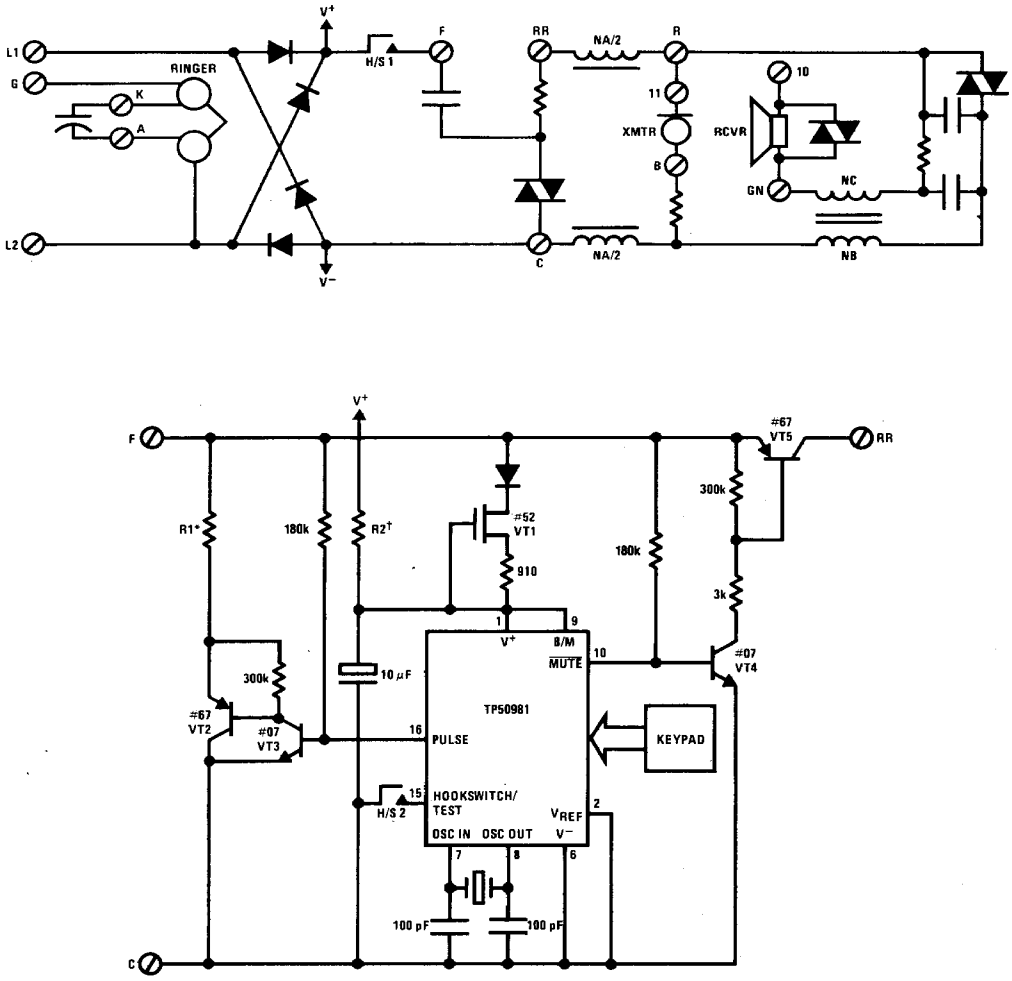
The TP50981/TP50981A, TP50985/TP50985A PULSE output is designed to drive a pulsing loop circuit in shunt with the speech network, as shown in *Figure 3*. During outpulsing the MUTE circuit is turned off to isolate the speech network from the line. VT2 and VT3 conduct during MAKE periods, R1 adjusts telephone pulsing resistance. VT2 and VT3 turn off during BREAK periods, loop current is then the sum of the device supply current, plus R2 and R3 currents. These currents should be designed to meet the system maximum BREAK current specification, where applicable. The on-chip voltage regulator enables the device to be fed from a current-limited supply of 150 μA minimum, as shown in *Figure 3*.

The TP50982/TP50982A PULSE output is designed for a series pulsing loop, as shown in *Figure 4*. In this case the $\overline{\text{MUTE}}$ circuit isolates only the receiver, so that current flows through the speech network while outpulsing MAKE periods. VT3 cuts off this current during BREAK periods.

To take maximum advantage of the low current consumption of the TP50981A, TP50982A, TP50985A in the on-hook, last-number-stored mode, all other current paths must be minimized. These include leakage of the decoupling capacitor C1, and reverse leakage of current through the current source, which could flow to ground via the transistor interface circuits and speech network. If on-hook current is drawn from the telephone line, reverse leakage of the two back-biased diodes in the rectifier bridge must also be considered. Virtually the full station battery voltage may appear across these diodes in the on-hook condition of *Figures 3 and 4*, hence the diodes should be specified for minimum leakage current at 50V reverse bias and maximum operating temperature.

Ceramic resonators for the oscillator circuit can be obtained from various companies including muRata, Toko, Vernitron and Radio Materials Corporation. The anti-resonant frequency, f_a, should be 480 kHz. Note that resonators are often referred to by their resonant frequency, f_r, which is typically 15 kHz–25 kHz lower than f_a. Consult manufacturers' data for specifications and tolerances.

Applications Information (Continued)



*R1 typically 150Ω.

†R2 = 20M for TP50981, TP50985; R2 = 50M for TP50981A, TP50985A.

# indicates National Semiconductor Discrete process number.

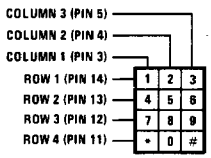
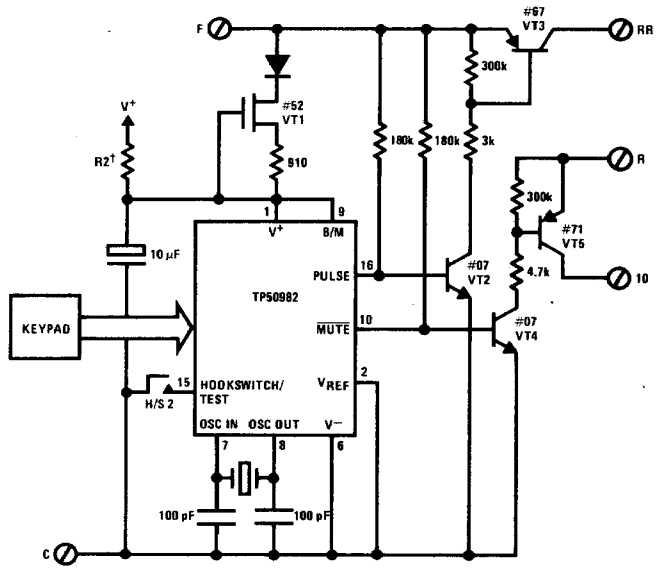


FIGURE 3. TP50981, TP50985 Shunt Dialer Application

Applications Information (Continued)



†R2 = 20M for TP50982, R2 = 50M for TP50982A

FIGURE 4. TP50982 Series Dialer Application