Alcor Micro Corp.

# Data Book

## AU6391

## USB2.0 to ATA/ATAPI Bridge Controller

## Technical Reference Manual

**Product Specification**

**Preliminary Release**

**Revision 0.9**

**Confidential** **Mar 2006**

# Data sheet status

| | |
|---|---|
| Objective specification | This data sheet contains target specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |

# Revision History

| Date | Revision | Description |
|---|---|---|
| Mar 2006 | 0.9 | Preliminary release |

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# 1.0 Introduction

## 1.1 Description

The AU6391 is a single chip USB 2.0 to ATA/ATAPI controller. It is used as the primary controller of an external USB 2.0 hard disk or CD/DVD box.

To maximize the data throughput and achieve the best compatibility, the AU6391 is equipped with Alcor's proprietary automatic speed negotiation (ASN) algorithm. The ASN algorithm allows AU6390 to select optimized operating mode that device can best support from PIO mode 0~4 and Ultra DMA mode 2/4.

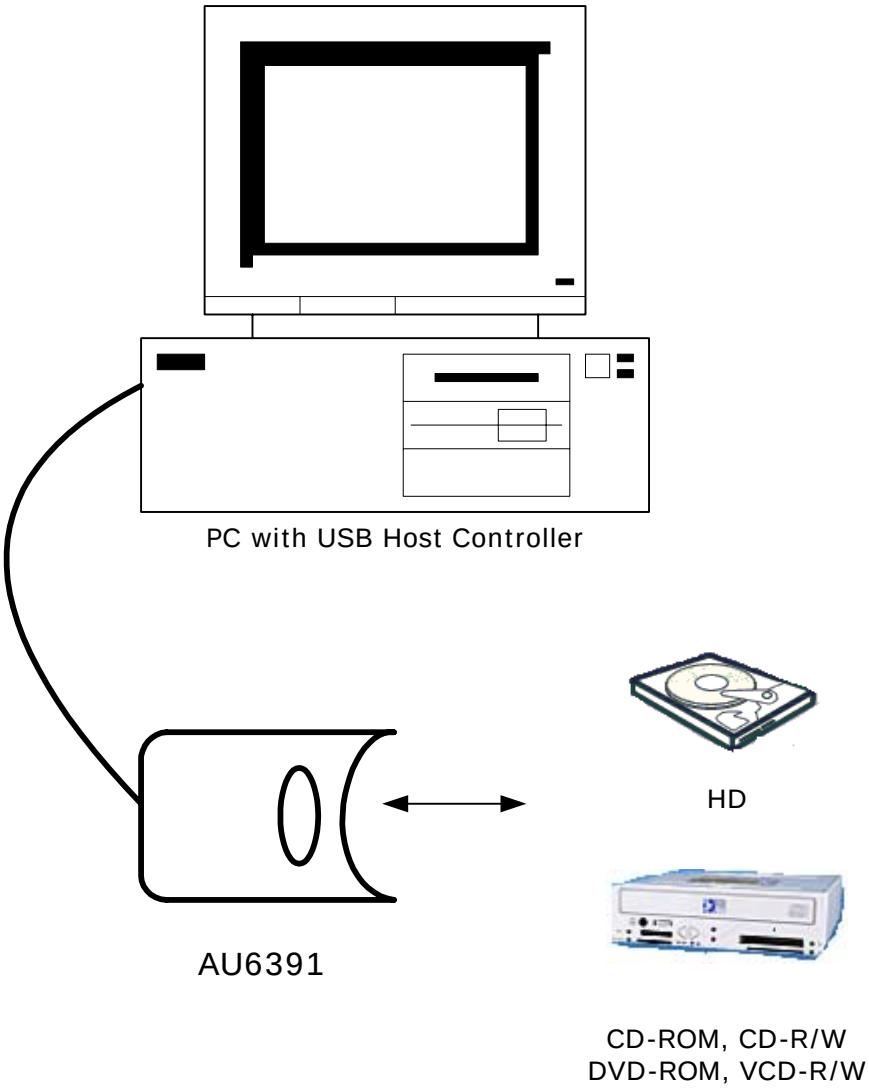
## 1.2 Features

- Supports USB 2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Supports ATA/ATAPI-6 specification Revision 1.0
  - PIO mode 0~4
  - UDMA mode 2/4
- Supports ATA/ATAPI device configured in master or slave mode
- Supports 48-bit addressing for large capacity hard drive
- Hardware DMA engine integrated for performance enhancement
- Work with default driver from Windows ME/2000/XP and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- One LED pin for activities indication
- Self-powered device
- 48pin LQFP package
- Runs at 12MHz clock.

# 2.0 Application Block Diagram

Following is the application diagram of a typical removable USB2.0 ATA/ATAPI device. Users can exchange the digital content between ATA/ATAPI device and PC (Notebook).

## 2.1 Block Diagram



# 3.0 Pin Assignment

The AU6391 is packed in 48pin-LQFP. Below figure shows signal name for each pin and the table in the following page describes each pin in detail.

**Figure 3.1 Pin Assignment Diagram**

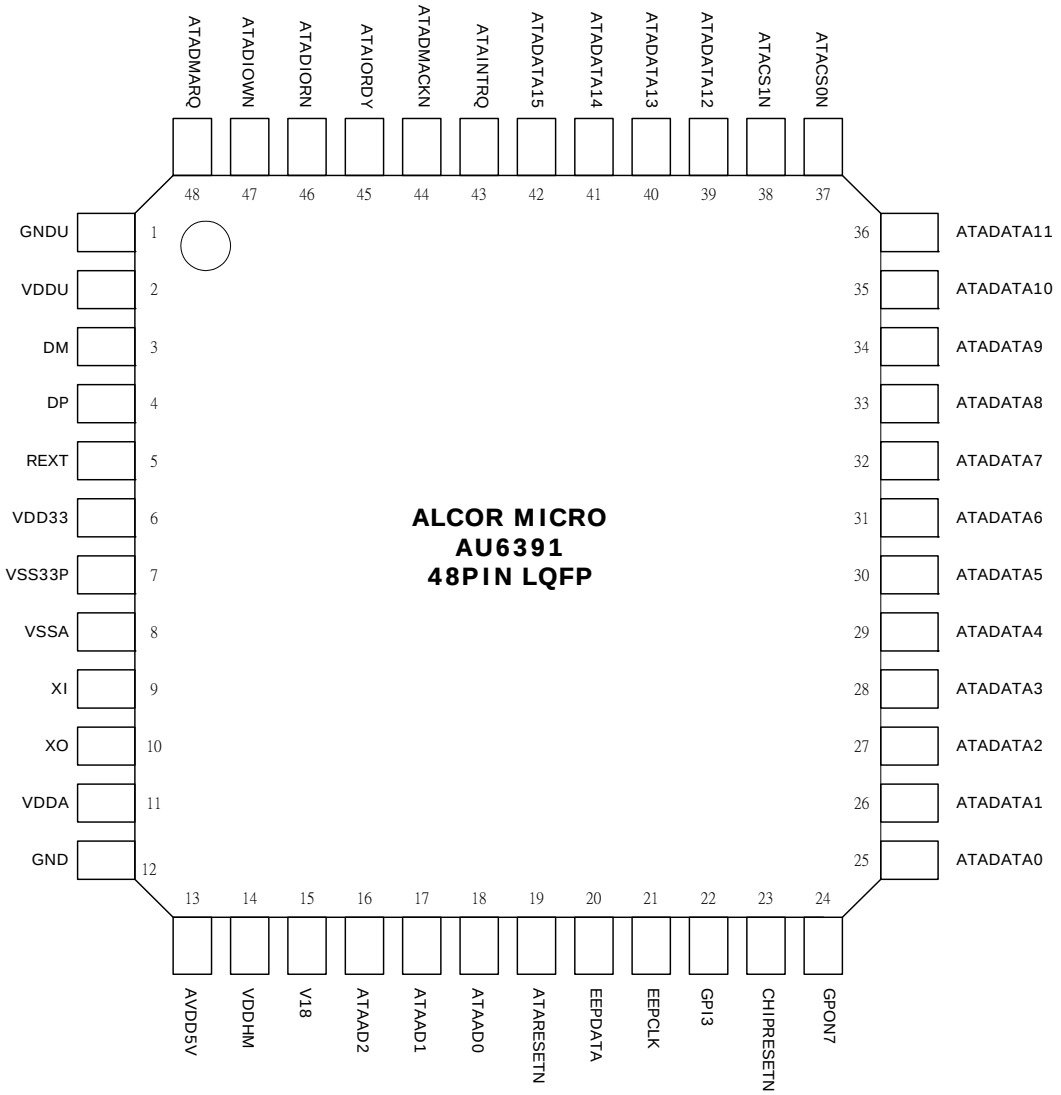


**Table 3.1 Pin Descriptions**

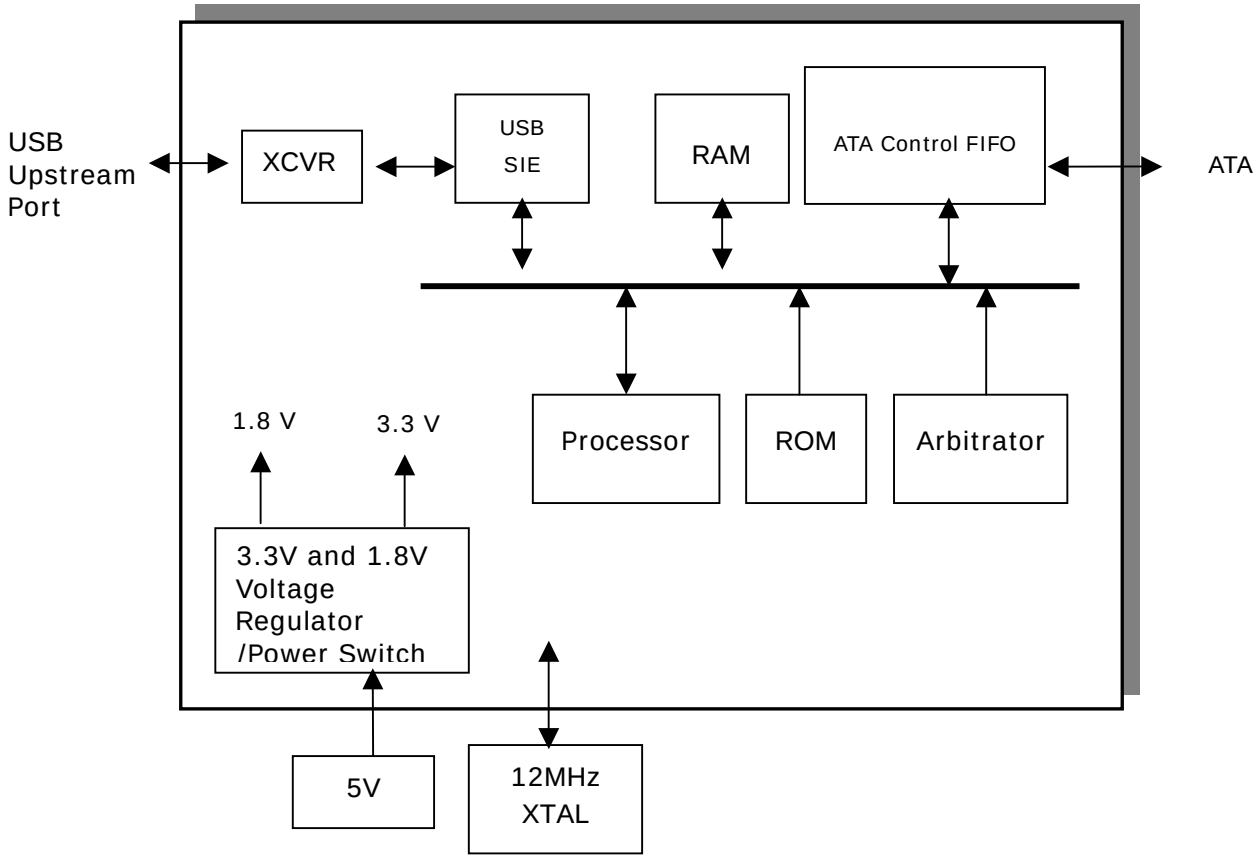
| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GNDU | PWR | UTMI POWER |
| 2 | VDDU | PWR | 1.8V |
| 3 | DM | | USB DM |
| 4 | DP | | USB DP |
| 5 | REXT | I | |
| 6 | VDD33 | PWR | 3.3V |
| 7 | VSS33P | PWR | |
| 8 | VSSA | PWR | |
| 9 | XI | I | 12 MHz crystal input. |
| 10 | XO | O | 12 MHz crystal output. |
| 11 | VDDA | PWR | 1.8V |
| 12 | GND | | Pin to Gnd |
| 13 | AVDD5V | | |
| 14 | VDDHM | PWR | |
| 15 | V18 | PWR | 1.8 V Input |
| 16 | ATAAD2 | O | ATA Address bus |
| 17 | ATAAD1 | O | ATA Address bus |
| 18 | ATAAD0 | O | ATA Address bus |
| 19 | ATARESETN | O | ATA Reset |
| 20 | EEPDATA | B | I2C |
| 21 | EEPCLK | B | I2C |
| 22 | GPI3 | I | General Purpose Input. |
| 23 | CHIPRESETN | I | Reset (low active to reset the whole chip), must be pull up with RC. |
| 24 | GPON7 | O | General Purpose Output. |

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 25 | ATADATA0 | I/O | ATA Data Bus |
| 26 | ATADATA1 | I/O | ATA Data Bus |
| 27 | ATADATA2 | I/O | ATA Data Bus |
| 28 | ATADATA3 | I/O | ATA Data Bus |
| 29 | ATADATA4 | I/O | ATA Data Bus |
| 30 | ATADATA5 | I/O | ATA Data Bus |
| 31 | ATADATA6 | I/O | ATA Data Bus |
| 32 | ATADATA7 | I/O | ATA Data Bus |
| 33 | ATADATA8 | I/O | ATA Data Bus |
| 34 | ATADATA9 | I/O | ATA Data Bus |
| 35 | ATADATA10 | I/O | ATA Data Bus |
| 36 | ATADATA11 | I/O | ATA Data Bus |
| 37 | ATACS0N | O | ATA Chip Select0 |
| 38 | ATACS1N | O | ATA Chip Select1 |
| 39 | ATADATA12 | I/O | ATA Data Bus |
| 40 | ATADATA13 | I/O | ATA Data Bus |
| 41 | ATADATA14 | I/O | ATA Data Bus |
| 42 | ATADATA15 | I/O | ATA Data Bus |
| 43 | ATAINTRQ | I | ATA Interput request |
| 44 | ATADMACKN | O | ATA Control Signal DMACKN |
| 45 | ATAIORDY | I | ATA Control Signal IORDY |
| 46 | ATADIORN | O | ATA Control Signal DIORN |
| 47 | ATADIOWN | O | ATA Control Signal DIOWN |
| 48 | ATADMARQ | I | ATA Control Signal DMARQ |

# 4.0 System Architecture and Reference Design

## 4.1 AU6391 Block Diagram

**Figure 4.1 AU6391 Block Diagram**



# 5.0 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| SYMBOL | PARAMETER | RATING | UNITS |
|---|---|---|---|
| $V_{CC}$ | Power Supply | -0.3 to $V_{CC}$+0.3 | V |
| $V_{IN}$ | Input Voltage | -0.3 to 3.6 | V |
| $V_{OUT}$ | Output Voltage | -0.3 to $V_{CC}$+0.3 | V |
| $T_{STG}$ | Storage Temperature | -40 to 150 | $^{O}$C |

## 5.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | 3.0 | 3.3 | 3.6 | V |
| $V_{DD}$ | Digital Supply | 2.25 | 2.5 | 2.75 | V |
| $V_{IN}$ | Input Voltage | 0 | 3.3 | 5.2 | V |
| $T_{OPR}$ | Operating Temperature | 0 | | 85 | $^{O}$C |

## 5.3 Leakage Current and Capacitance

**Table 5.3 General DC Characteristics**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Input current | no pull-up or pull-down | -10 | ±1 | 10 | μA |
| $I_{OZ}$ | Tri-state leakage current | | -10 | ±1 | 10 | μA |
| $C_{IN}$ | Input capacitance | Pad Limit | | 2.8 | | ρF |
| $C_{OUT}$ | Output capacitance | Pad Limit | | 2.8 | | ρF |
| $C_{BID}$ | Bi-directional buffer capacitance | Pad Limit | | 2.8 | | ρF |

## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

**Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells**

| SYMBOL | PARAMETER | CONDITIONS | Limits | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{CC}$ | Power supply | 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| $V_{il}$ | Input low voltage | LVTTL | | | 0.8 | V |
| $V_{ih}$ | Input high voltage | | 2.0 | | | V |
| $V_{ol}$ | Output low voltage | $\lvert I_{ol} \rvert$ =2~16mA | | | 0.4 | V |
| $V_{oh}$ | Output high voltage | $\lvert I_{oh} \rvert$ =2~16mA | 2.4 | | | V |
| $R_{pu}$ | Input pull-up resistance | PU=high, PD=low | 40 | 75 | 190 | KΩ |
| $R_{pd}$ | Input pull-down resistance | PU=low, PD=high | 40 | 75 | 190 | KΩ |
| $I_{in}$ | Input leakage current | $V_{in}$= $V_{CC}$ or 0 | -10 | ±1 | 10 | μA |
| $I_{oz}$ | Tri-state output leakage current | | -10 | ±1 | 10 | μA |

## 5.5 USB Transceiver Characteristics

**Table 5.5 Electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| AVCC | Analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| VCC | Digital supply voltage | | 2.25 | 2.5 | 2.75 | V |
| $I_{CC}$ | Operating supply current | High speed operating at 480 MHz | | | 73 | mA |
| $I_{CC(susp)}$ | Suspend supply current | In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected | | | 120 | μA |

**Table 5.6 Static characteristic：Digital pin**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input levels | | | | | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | | V |
| Output levels | | | | | | |
| $V_{OL}$ | Low-level output voltage | | | | 0.2 | V |
| $V_{OH}$ | High-level output voltage | | VCC-0.2 | | | V |

**AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃**

**Table 5.7 Static characteristic：Analog I/O pins（DP/DM）**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| USB2.0 Transceiver（HS） | | | | | | |
| Input Levels（differential receiver） | | | | | | |
| $V_{HSDIFF}$ | High speed differential input sensitivity | $\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit | 300 | | | mV |
| $V_{HSCM}$ | High speed data signaling common mode voltage range | | -50 | | 500 | mV |
| $V_{HSSQ}$ | High speed squelch detection threshold | Squelch detected | | | 100 | mV |
| | | No squelch detected | 150 | | | mV |
| $V_{HSDSC}$ | High speed disconnection detection threshold | Disconnection detected | 625 | | | mV |
| | | Disconnection not detected | | | 525 | mV |
| Output Levels | | | | | | |
| $V_{HSOI}$ | High speed idle level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOL}$ | High speed low level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOH}$ | High speed high level output voltage(differential) | | -360 | | 400 | mV |
| $V_{CHIRPJ}$ | Chirp-J output voltage（differential） | | 700 | | 1100 | mV |
| $V_{CHIRPK}$ | Chirp-K output voltage（differential） | | -900 | | -500 | mV |
| Resistance | | | | | | |
| $R_{DRV}$ | Driver output impedance | Equivalent resistance used as internal chip only | 3 | 6 | 9 | Ω |
| | | Overall resistance including external resistor | 40.5 | 45 | 49.5 | |
| Termination | | | | | | |
| $V_{TERM}$ | Termination voltage for pull-up resistor on pin RPU | | 3.0 | | 3.6 | V |
| USB1.1 Transceiver（FS/LS） | | | | | | |
| Input Levels（differential receiver） | | | | | | |
| $V_{DI}$ | Differential input sensitivity | $\lvert V_{I(DP)}-V_{I(DM)} \rvert$ | 0.2 | | | V |
| $V_{CM}$ | Differential common mode voltage | | 0.8 | | 2.5 | V |
| Input Levels（single-ended receivers） | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SE}$ | Single ended receiver threshold | | 0.8 | | 2.0 | V |
| Output levels | | | | | | |
| $V_{OL}$ | Low-level output voltage | | 0 | | 0.3 | V |
| $V_{OH}$ | High-level output voltage | | 2.8 | | 3.6 | V |

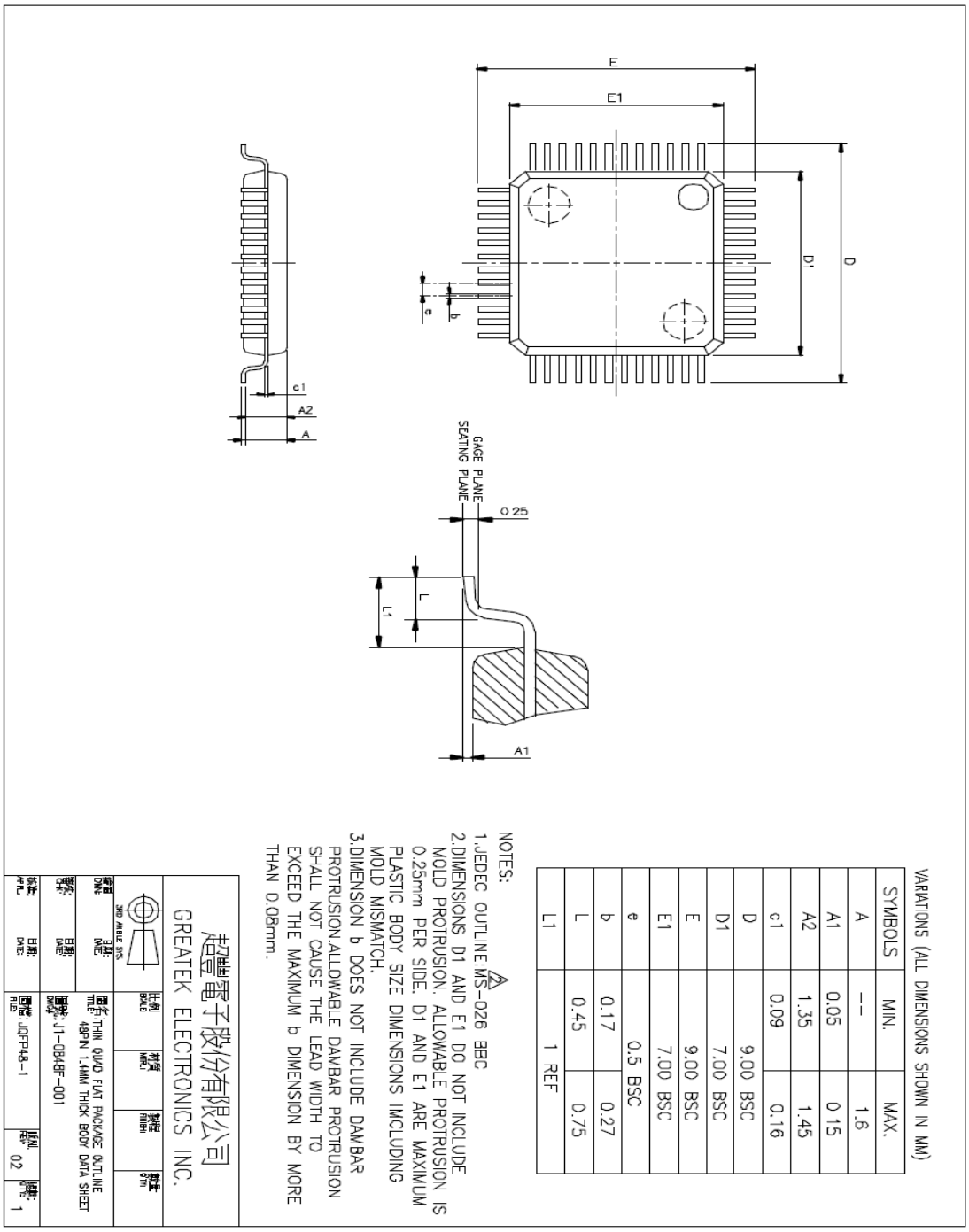
**AVCC=3.0V~3.6V；VCC=2.25V~2.75V；Temp=0℃~115℃**

**Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Driver Characteristics | | | | | | |
| High-Speed Mode | | | | | | |
| $t_{HSR}$ | High-speed differential rise time | | 500 | | | ps |
| $t_{HSF}$ | High-speed differential fall time | | 500 | | | ps |
| Full-Speed Mode | | | | | | |
| $t_{FR}$ | Rise time | CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$； | 4 | | 20 | ns |
| $t_{FF}$ | Fall time | CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$； | 4 | | 20 | ns |
| $t_{FRMA}$ | Differential rise/fall time matching（$t_{FR}$ / $t_{FF}$） | Excluding the first transition from idle mode | 90 | | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V |
| Low-Speed Mode | | | | | | |
| $t_{LR}$ | Rise time | CL=200pF-600pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$； | 75 | | 300 | ns |
| $t_{LF}$ | Fall time | CL=200pF-600pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$； | 75 | | 300 | ns |
| $t_{LRMA}$ | Differential rise/fall time matching（$t_{LR}$ / $t_{LF}$） | Excluding the first transition from idle mode | 80 | | 125 | % |
| $V_{CRS}$ | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V |
| $V_{OH}$ | High-level output voltage | | 2.8 | | 3.6 | V |

# 6.0 Mechanical Information

**Figure 6.1 Mechanical Information Diagram**



# 7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

**SIE** Serial Interface Engine
**ATA** Advanced Technology Attachment
**UTMI** USB Transceiver Macrocell Interface

【MEMO】

**About Alcor Micro, Corp**

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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