查询SC22201供应商 捷多邦，专业PCB打样工厂，24小时

SIERRA SEMICONDUCTOR

SC22101/SC22201
Electrically Erasable, Programmable Memories

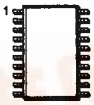
FEATURES

- ☐ CMOS EE Technology
- ☐ Single 5 V supply
- ☐ Reliable CMOS floating gate process
- ☐ 18-pin DIP package
- ☐ Self-timed write operation
- ☐ Multiplexed address and data bus
- ☐ Data polling
- ☐ 10,000 erase/write cycles
- ☐ Minimum 10 years data retention

18-PIN DIP PACKAGE

SC22101CN
SC22201CN

20-PIN SOIC PACKAGE



SC22201CM

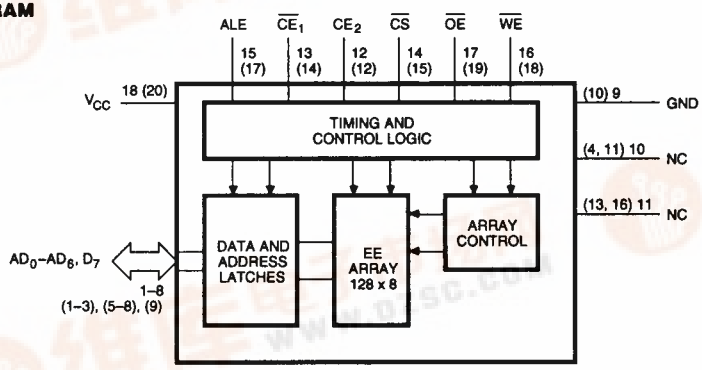
GENERAL DESCRIPTION

The SC22101 and SC22201 are 128 by 8 programmable, non-volatile, parallel access memories built with Sierra's proprietary CMOS floating gate process. Data and address lines are multiplexed, enabling these devices to be packaged in an 18-pin DIP, saving board space. The pin-out is identical to the Intel 8185 static RAM and the 2001 Nonvolatile RAM, allowing the memories to directly interface with Intel and other popular 8-bit and 16-bit microprocessors and microcontrollers.

The write cycle is simplified by a self-timed erase before write circuit on-chip. The end of write cycle can be determined by polling the data pins, or the controller can simply allow a minimum time between a write command and the subsequent command. To prevent undesirable modification of the memory contents during system power up or power down, a lockout circuit ignores write commands while V_{CC} is below the prescribed level of VLKO.

Applications for these memories include storing position data in robotic systems, storing local area network node address and parameter settings in data communications equipment, storing set-up and last position data in industrial control systems and storing PBX switch data in telecommunications equipment.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PIN NUMBERS; NUMBERS IN ( ) ARE SOIC PIN NUMBERS.

找PDF 维库一下 pdf.dzsc.com

PIN DESCRIPTIONS

PIN*	NAME	DESCRIPTION
1–8 (1–3), (5–8), (9)	AD_0–AD_6, D_7	Multiplexed address and data bits. D_7, Pin 8 and Pin (9), is DATA only.
(4)	NC	No connection
9 (10)	GND	Ground, 0 V.
10 (11)	NC	No connection
11 (13)	NC	No connection. No internal connection is made to this pin and it may be left floating.
12 (12)	CE2	Chip Enable 2 (see Table 1)
13 (14)	$\overline{CE1}$	Chip Enable 1 (see Table 1)
14 (15)	$\overline{CS}$	Chip Select (see Table 1)
(16)	NC	No connection
15 (17)	ALE	Address Latch Enable
16 (18)	$\overline{WE}$	Write Enable
17 (19)	$\overline{OE}$	Output Enable
18 (20)	V_{CC}	Positive power supply, 5 V.

* Pin numbers not in ( ) are for 18-pin DIP; those in ( ) are for 20 pin SOIC.

FUNCTIONAL DESCRIPTION

Table 1 shows the different modes of operation as a function of the control signals. Standby powered down mode: Both write and read are inhibited and the device's power consumption is greatly reduced. Standby powered up mode: the device consumes the operating power, but read and write are inhibited. Inhibit mode: the device is write protected to avoid inadvertent modifications while the read and write pins are changing.

Read Operation

Figure 2 shows the timing diagram for READ operation. The address as well as the states of $\overline{CE1}$ and CE2 are latched on the falling edge of ALE. Pins 1 through 7 are used for address bits.

Data appear on pins 1 through 8 after $\overline{OE}$ becomes active (low).

Write Operation

Write operation's timing is shown in Figure 3. Similar to the READ operation, the address and states of $\overline{CE1}$ and CE2 are latched on the falling edge of the ALE. After the address is latched, the $\overline{WE}$ becomes active (low) for the minimum time of TCC and returns to inactive state. This initiates the internally timed write operation. No external erase before write operation is needed and data lines as well as control lines may change after the write operation is initiated.

$\overline{DATA}$ Polling

After the write operation is initiated, its conclusion can be monitored by putting the device in the READ mode and polling the D7 data bit. The data bit will be logical inverse of the bit being written to a location in memory until the write operation is completed. At this time the D7 data bit will be the same as the last D7 data bit written into memory.

Write Lockout

During system power up or power down, an on-chip write lockout circuit prevents spurious WRITES into the memory locations while V_{CC} is lower than the specified lockout voltage VLKO. This frees the system designer from having to design external write protection circuits.

MODE	$\overline{CE1}$	CE2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

Notes: V_{IL} = Logical Low Input V_{IH} = Logical High Input
Hi-Z = High Impedance State X = Don't Care
The $\overline{CE1}$ and CE2 inputs are latched by the falling edge of ALE.

Table 1. Modes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	7 V
Voltage on Any Pin	V_{CC}+0.5 V GND–0.5 V
Storage Temperature Range	–65 to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temperature (Soldering 10 s)	300°C

A.C. TEST CONDITIONS

Output Load	1TTL gate and C_L = 100 pF
Input Rise and Fall Times (10% to 90%)	20 ns
Input Pulse Levels	0.0 V to 3.0 V
Input/Output Timing Reference Level	0.8 V and 2.0 V

OPERATING CONDITIONS (Applies to DC and AC Characteristics)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS

			SC22101			SC22201			
PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4			0.4	V
V_{IH}	High Level Input Voltage		2.0		V_{CC}+0.5	2.0		V_{CC}+0.5	V
V_{IL}	Low Level Input Voltage		–0.5		0.8	–0.5		0.8	V
V_{LKO}	V_{CC} Level for Write Lockout		4.0		4.4	3.8		4.4	V
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$			±10.0			±10.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$			±10.0			±10.0	µA
I_{CC}	Operating Supply Current	TTL Inputs			15.0			15.0	mA
		CMOS Inputs			10.0			10.0	mA
I_{CCPD}	Standby Supply Current	TTL Inputs			5.0			5.0	mA
		CMOS Inputs			100			100	µA
I_{SC}	Short-Circuit Current	1 Output Pin Shorted		40			40		mA
	Endurance		10,000				10,000		

Notes: 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

e derating—Plastic "N" package: –12 mW/°C from 65°C to 85°C.

CAPACITANCE (T_A = 25°C, f = 1 MHz) (Note 3)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	$V_{IN} = 0$ V		5	10	pF
$C_{I/O}$	Input/Output Capacitance	$\overline{OE} = \overline{CE1} = \overline{CS} = V_{IH}$ $CE2 = V_{IL}$			10	pF

Note: 3. These parameters are sampled and not 100% tested.

AC CHARACTERISTICS

		SC22101		SC22201		
PARAMETER*	DESCRIPTION	MIN	MAX	MIN	MAX	UNITS
TAL	Address to Latch Setup Time	50		50		ns
TLA	Address Hold Time After Latch	45		45		ns
TLC	Latch to OE/WE Control	80		80		ns
TOE	Valid Data Out Delay from Read Control		170		170	ns
TLD	ALE to Data Out Valid		300		300	ns
TLL	Latch Enable Width	100		100		ns
TOH	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (whichever changes first)	0		0		ns
TOLZ	$\overline{OE}$ Low to Output Driven	10		10		ns
TRDF	Data Bus Float After Read	0		0	95	ns
TCL	OE/WE Control to Latch Enable	0		0		ns
TCC	OE/WE Control Width	250		250		ns
TDW	Data In to Write Setup Time	150		150		ns
TWD	Data In Hold Time After Write	20		20		ns
TSC	Chip Select Set-Up to OE/WE Control	0		50		ns
TCS	Chip Select Hold Time After OE/WE Control	0		10		ns
TALCE	Chip Enable Set-Up to ALE Falling	30		30		ns
TLACE	Chip Enable Hold Time After ALE Falling	45		45		ns
TWR	Byte Write Cycle Time		20		40	ms
TWH	Data Invalid After $\overline{WE}$ Falling		1		1	ms

*See Figures 2 and 3.

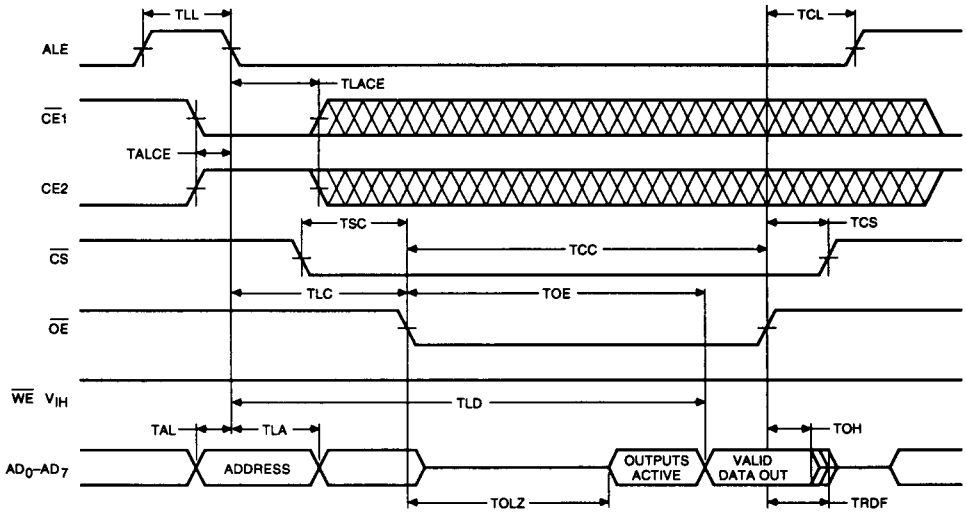


Figure 2. Read Timing

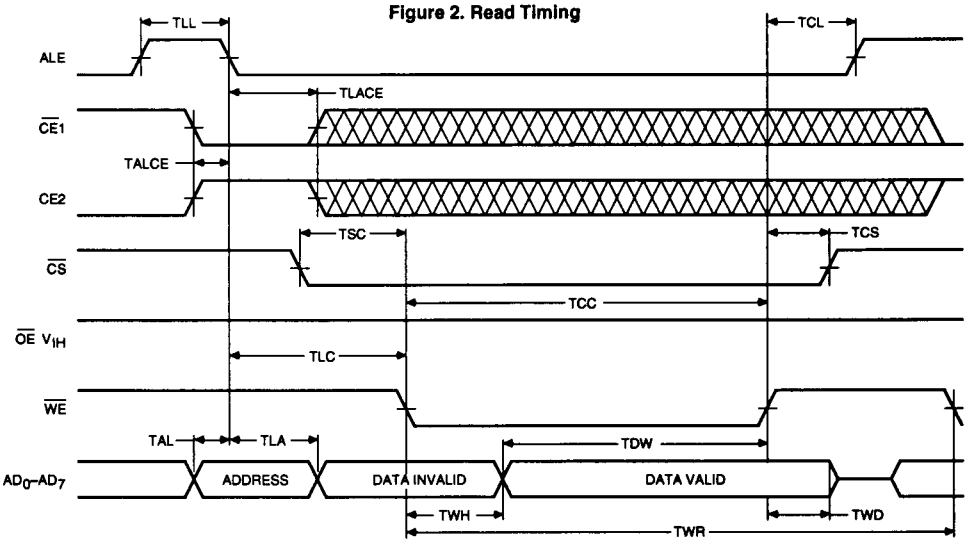
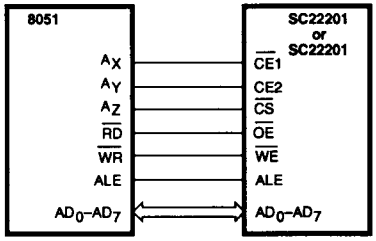


Figure 3. Write Timing



Note: A_X, A_Y, A_Z are any three of the 8051 address pins A_8–A_{15}. By connecting $\overline{CE1}$, CE2, and $\overline{CS}$ to specific address lines, the SC22201, can be mapped to a particular range in memory, without the need for an external memory address decoder.

Figure 4. Using The SC22101 or SC22201 with an 8051 Microcontroller