FEATURES

- High-quality zoom and shrink scaling engine (Compatible with VGA thru SXGA)
- Integrated 8-bit triple-ADC/PLL
- On-screen display controller (OSD)
- Supports single-RGB inputs
- Supports composite sync and SOG separator
- Programmable 10-bit gamma correction
- Integrated Brightness & Contrast control adjustment
- Supports PWM backlit intensity control
- Supports sRGB
- Green PC and low EMI features
- Built-in LVDS transmitter
- Low standby power mode (< 15mA)

■ High-Performance Scaling Engine
- Programmable shrink/zoom capabilities
- High-quality scaling for all VESA and IBM mode to fit screen
- Variable sharpness control

■ Analog RGB Compliant Input Port
- Supports up to SXGA at 75Hz
- Supports Composite Sync and SOG (Sync-on-Green) separator

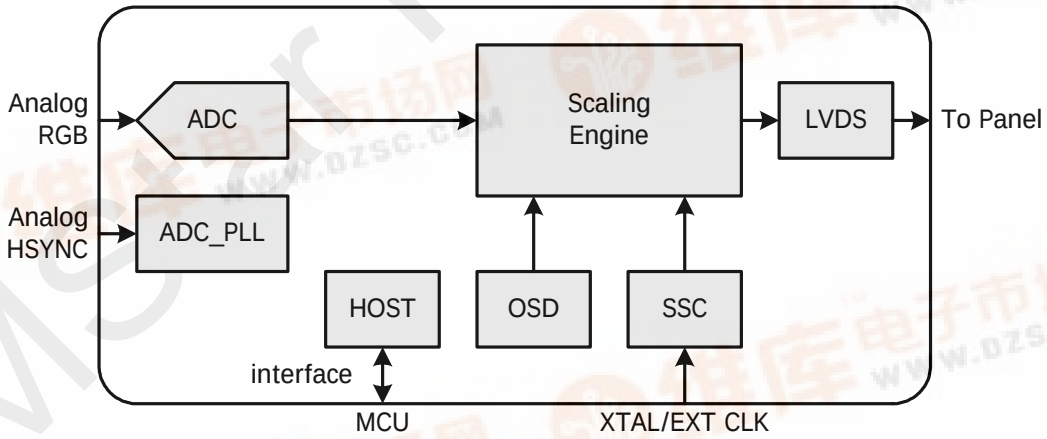
■ Auto-Detection/Tune
- Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE), and input mode (all VESA & IBM modes w/ resolution and polarity) detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Smart screen-fitting

■ On-Screen OSD Controller
- Built-in OSD generator with 256 character font programmable RAM
- Supports for 4/8 multi-color fonts
- Gradient color function
- Supports button function
- Pattern generator for production test
- Support OSD MUX and alpha blending capability

■ LVDS Display Interface
- Supports Dual Link up to 135MHz dot clock for SXGA
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA
- With 6/8 bits options
- Reduced swing for LVDS for low EMI

■ External Connection/Component
- Built-in DDC circuit
- Supports serial (up to 400Kbit/sec) bus type

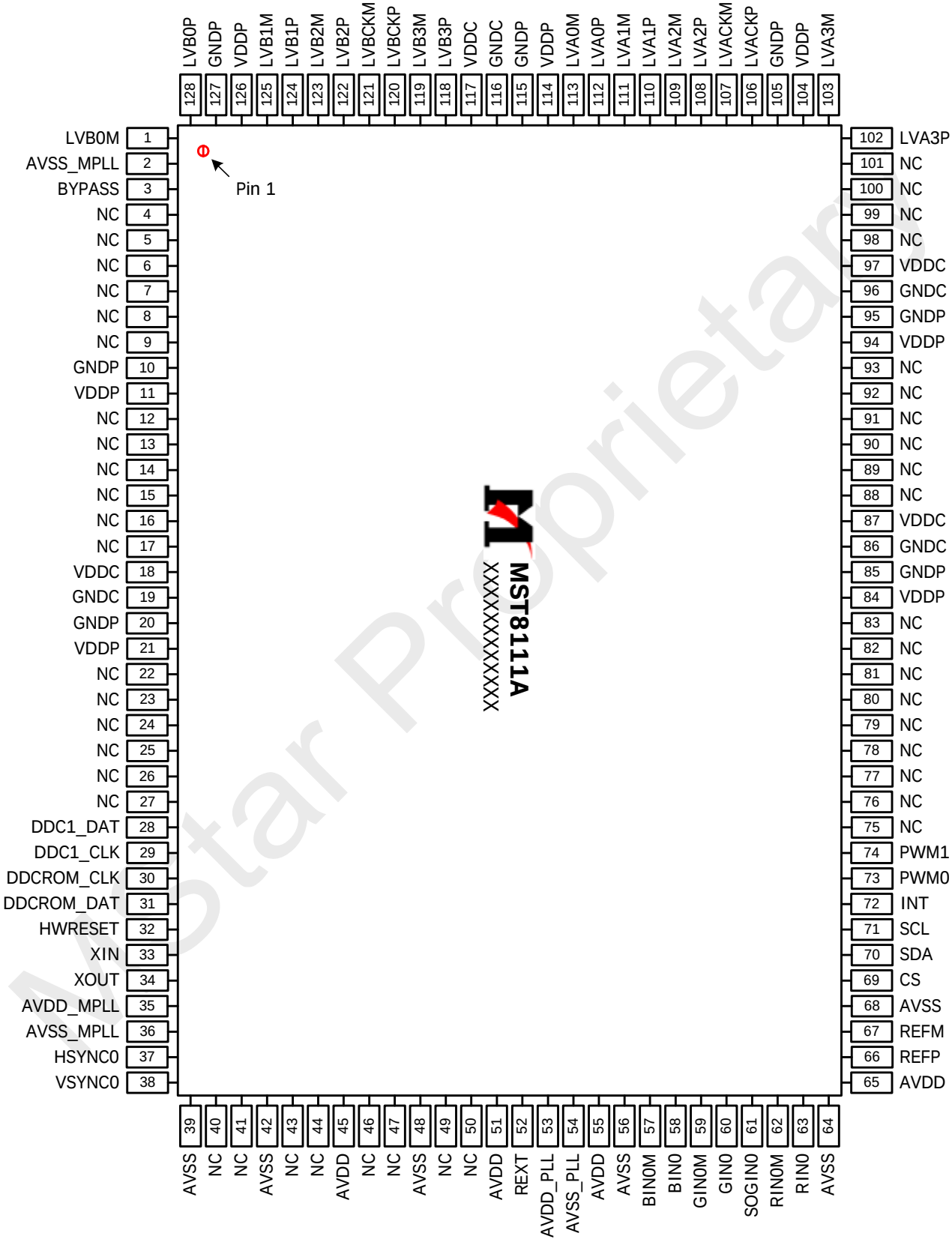
BLOCK DIAGRAM



GENERAL DESCRIPTION

The MST8111A is a high performance, and fully integrated graphics processing IC solution for LCD monitors with resolutions up to SXGA. It is configured with an integrated triple-ADC/PLL, a high quality scaling engine, an on-screen display controller, a built-in output clock generator, and LVDS display interface. To further reduce system costs, the MST8111A also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST8111A)



PIN DESCRIPTION

CPU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware reset; active high	32
CS	Input w/ 5V-tolerant	3 Wire Serial Bus Chip Select; active high	69
SDA	I/O w/ 5V-tolerant	3 Wire Serial Bus Data; 4mA driving strength	70
SCL	Input w/ 5V-tolerant	3 Wire Serial Bus Clock	71
INT	Output	CPU interrupt; 4mA driving strength	72

Analog Interface

Pin Name	Pin Type	Function	Pin
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC input	37
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC input	38
REFP		Internal ADC top de-coupling pin	66
REFM		Internal ADC bottom de-coupling pin	67
RIN0	Analog Input	Analog red input	63
RIN0M	Analog Input	Reference ground for analog red input	62
SOGIN0	Analog Input	Sync-on-green input	61
GIN0	Analog Input	Analog green input	60
GIN0M	Analog Input	Reference ground for analog green input	59
BIN0	Analog Input	Analog blue input	58
BIN0M	Analog Input	Reference ground for analog blue input	57
REXT		External resistor 390 ohm to AVDD	52

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	A-Link Negative LVDS Differential Data Output	113
LVA0P	Output	A-Link Positive LVDS Differential Data Output	112
LVA1M	Output	A-Link Negative LVDS Differential Data Output	111
LVA1P	Output	A-Link Positive LVDS Differential Data Output	110
LVA2M	Output	A-Link Negative LVDS Differential Data Output	109
LVA2P	Output	A-Link Positive LVDS Differential Data Output	108
LVA3M	Output	A-Link Negative LVDS Differential Data Output	103
LVA3P	Output	A-Link Positive LVDS Differential Data Output	102
LVACKM	Output	A-Link Negative LVDS Differential Clock Output	107
LVACKP	Output	A-Link Positive LVDS Differential Clock Output	106
LVB0M	Output	B-Link Negative LVDS Differential Data Output	1
LVB0P	Output	B-Link Positive LVDS Differential Data Output	128
LVB1M	Output	B-Link Negative LVDS Differential Data Output	125
LVB1P	Output	B-Link Positive LVDS Differential Data Output	124
LVB2M	Output	B-Link Negative LVDS Differential Data Output	123
LVB2P	Output	B-Link Positive LVDS Differential Data Output	122
LVB3M	Output	B-Link Negative LVDS Differential Data Output	119
LVB3P	Output	B-Link Positive LVDS Differential Data Output	118
LVBCKM	Output	B-Link Negative LVDS Differential Clock Output	121

Pin Name	Pin Type	Function	Pin
LVBCKP	Output	B-Link Positive LVDS Differential Clock Output	120

GPIO Interface

Pin Name	Pin Type	Function	Pin
GOUT1/PWM1	Output	GOUT1/PWM1; 4mA driving strength	74
GOUT0/PWM0	Output	GOUT0/PWM0; 4mA driving strength	73

Misc. Interface

Pin Name	Pin Type	Function	Pin
BYPASS		For External Bypass Capacitor	3
DDC1_DAT	I/O w/ 5V-tolerant	DDC Data for analog interface; 4mA driving strength	28
DDC1_CLK	Input w/ 5V-Tolerant	DDC Clock for analog interface	29
DDCROM_CLK	Input w/ 5V-Tolerant	DDC ROM Clock	30
DDCROM_DAT	I/O w/ 5V-tolerant	DDC ROM Data; 4mA driving strength	31
XIN	Crystal Oscillator Input	Xin	33
XOUT	Crystal Oscillator Output	Xout	34

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD	3.3V Power	ADC Power	45, 51, 55, 65
AVSS	Ground	ADC Ground	39, 42, 48, 56, 64, 68
AVDD_PLL	3.3V Power	PLL Power	53
AVSS_PLL	Ground	PLL Ground	54
AVDD_MPLL	3.3V Power	MPLL Power	35
AVSS_MPLL	Ground	MPLL Ground	2, 36
VDDP	3.3V Power	Digital Output Power	11, 21, 84, 94, 104, 114, 126
GNDP	Ground	Digital Output Ground	10, 20, 85, 95, 105, 115, 127
VDDC	2.5V Power	Digital Core Power	18, 87, 97, 117
GNDC	Ground	Digital Core Ground	19, 86, 96, 116

No Connects

Pin Name	Pin Type	Function	Pin
NC		No Connect. Leave These Pins Floating.	4-9, 12-17, 22-27, 40, 41, 43, 44, 46, 47, 49, 50, 75-83, 88-93, 98-101

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
Resolution		8		Bits
DC ACCURACY				
Differential Nonlinearity		±0.5	+1.50/-1.0	LSB
Integral Nonlinearity		±1		LSB
No Missing Codes		Guaranteed		
ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			20	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	20		162.5	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
Channel to Channel Matching		0.5%		Full-Scale

Specifications subject to change without notice.

Absolute Maximum Ratings

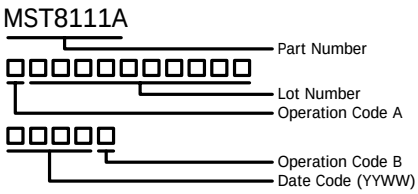
Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		34		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		6.0		°C/W

Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST8111A	0°C to +70°C	PQFP	128

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST8111A comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST8111A_data_sheet_v01	• Initial release	May 2003

MECHANICAL DIMENSIONS