General Purpose 8051 MCU 64K Flash Type with ISP

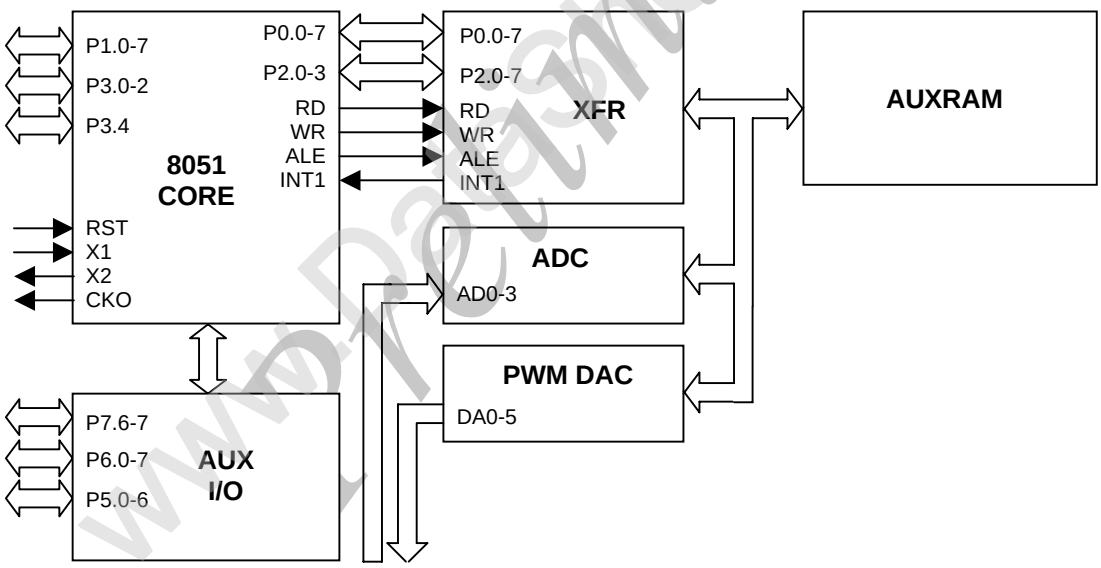
GENERAL DESCRIPTIONS

The CS8954 micro-controller is an 8051 CPU core embedded device especially tailored for consumer and/or general purpose applications. It includes an 8051 CPU core, 768-byte SRAM, 4 channels of 6-bit ADC, 6 channels of PWM DAC, and a 64K-byte internal program Flash-ROM memory in 40-pin PDIP, 44-pin PLCC or PQFP package.

FEATURES

- 8051 core, 12MHz operating frequency with single/double CPU clock option
- 0.35um process
- 3.3V power supply
- 768-byte RAM
- 64K-byte program Flash memory
- Maximum 6 channels of PWM DAC
- Watchdog timer with programmable interval
- Single/double frequency clock output
- Hardware In system programming (ISP) without boot code
- Two external interrupts
- Maximum 4 channels of 6-bit ADC
- Flash-ROM code protection selection
- 40-pin PDIP, 44-pin PLCC or PQFP package

BLOCK DIAGRAM

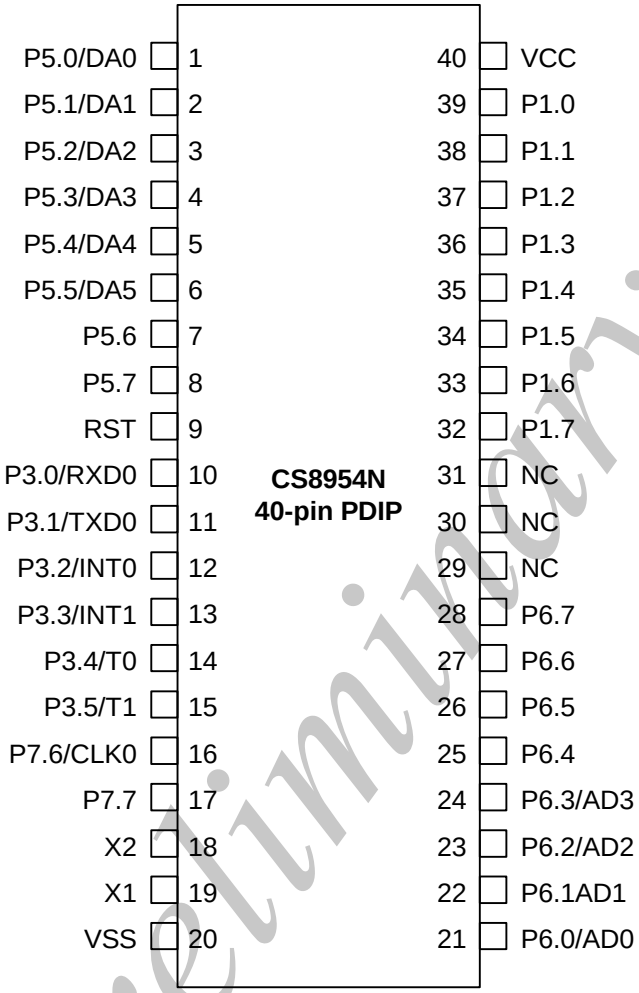


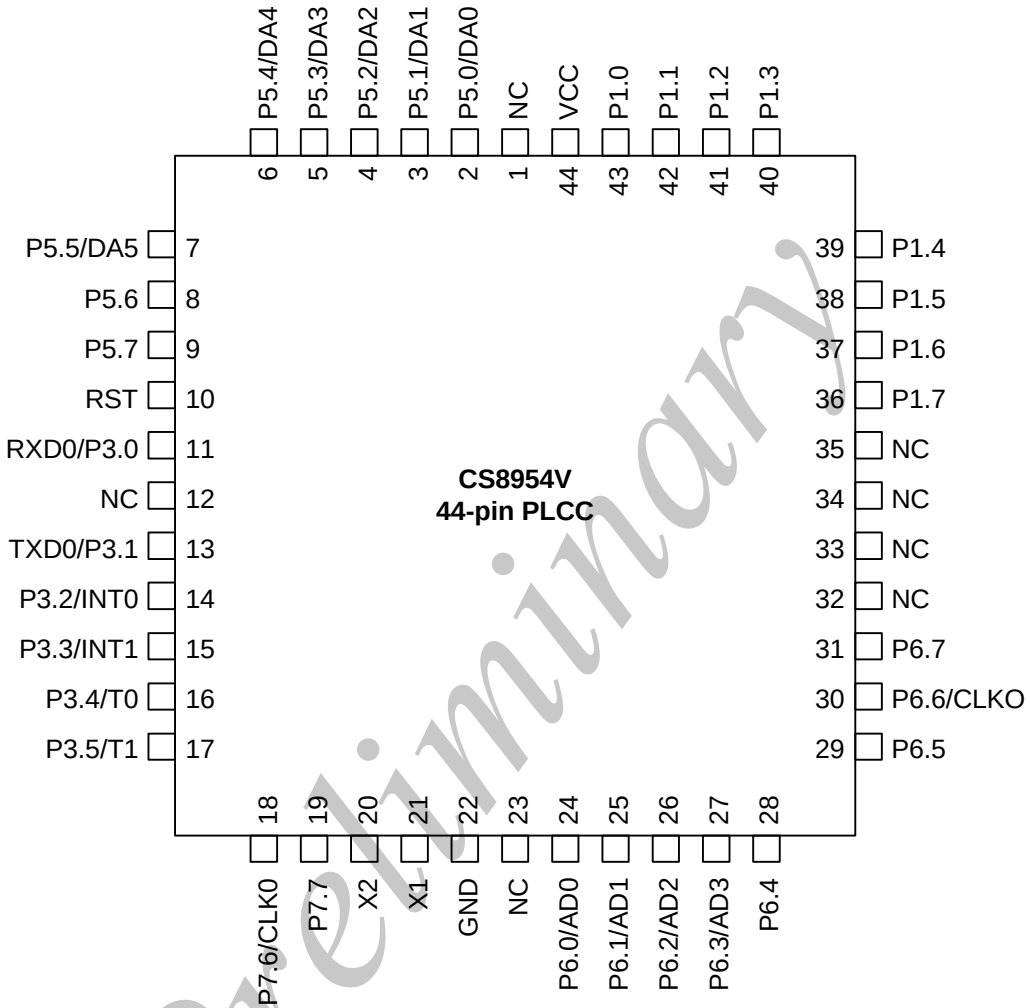
Myson Century, Inc.
Taiwan:
No. 2, Industry East Rd. III,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

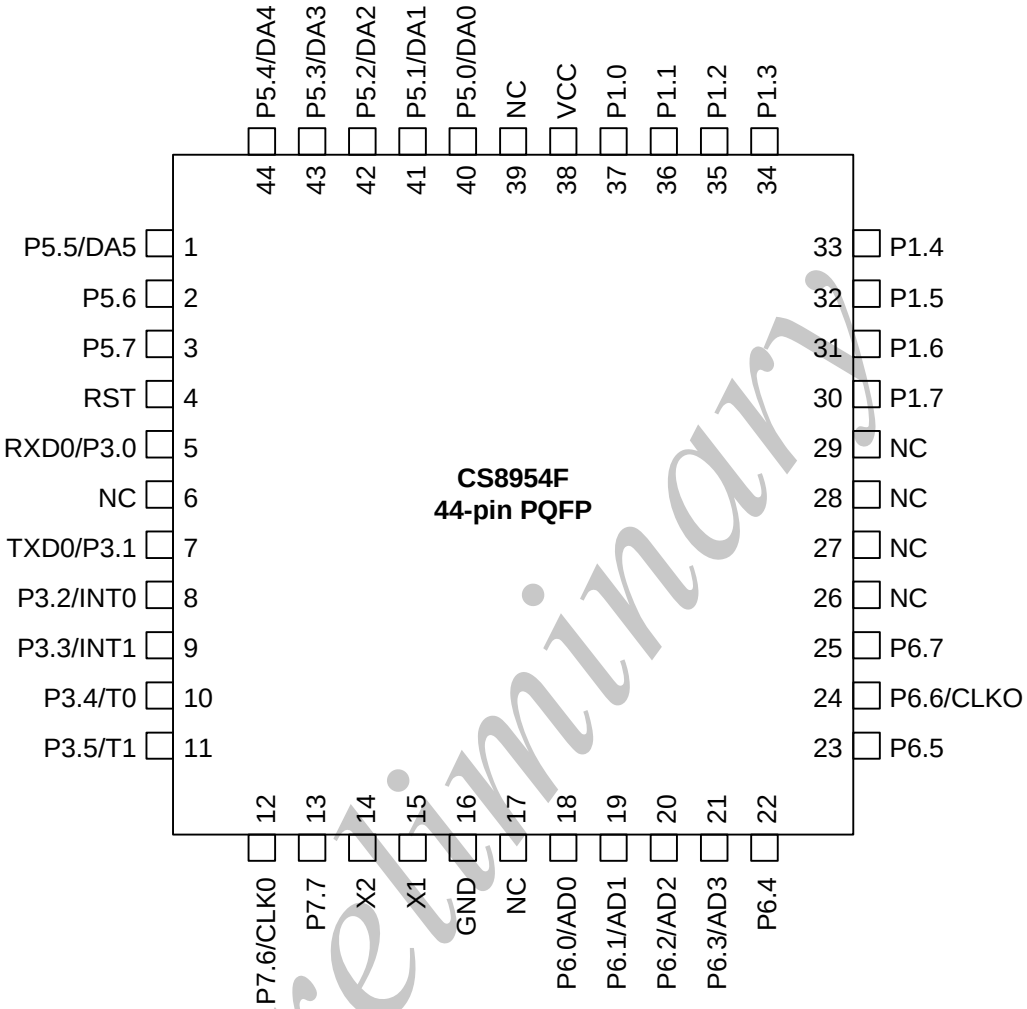
USA:
4020 Moorpark Avenue Suite 115
San Jose, CA, 95117
Tel: 408-243-8388 Fax: 408-243-3188

sales@myson.com.tw
www.myson.com.tw

PIN CONNECTION







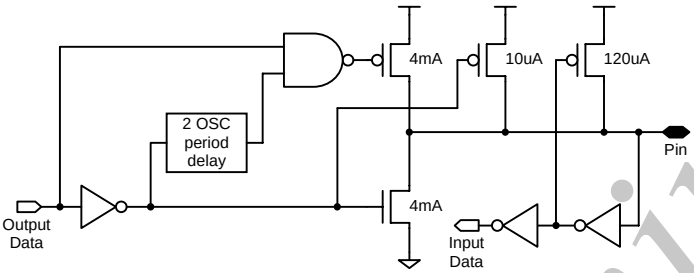
PIN CONFIGURATION

A “CMOS output pin” means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

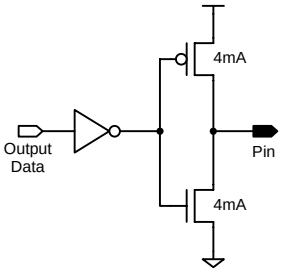
A “open drain pin” means it can sink at least 4mA current. It can be used as input or output function and needs an external pull up resistor.

A “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.

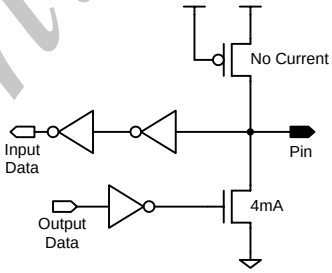
There is an internal-pull down resistance on each CMOS PAD and an internal pull-down resistance on each input PAD. It is recommended to add a pull high resistance on each open drain pin.



8051 Standard Pin



CMOS Output Pin



Open Drain Pin

PIN DESCRIPTION

Name	Pin No.	I/O	Description
NC	1	-	No connection
P5.0/DA0	2	I/O	General purpose I/O (Open drain)
P5.1/DA1	3	I/O	General purpose I/O (Open drain)
P5.2/DA2	4	I/O	General purpose I/O (Open drain)
P5.3/DA3	5	I/O	General purpose I/O (Open drain)
P5.4/DA4	6	I/O	General purpose I/O (Open drain)
P5.5/DA5	7	I/O	General purpose I/O (Open drain)
P5.6	8	I/O	General purpose I/O
P5.7	9	I/O	General purpose I/O
RST	10	I	High Active RESET
P3.0/RXD0	11	I/O	Serial port 0 input
NC	12	-	No connection
P3.1/TXD0	13	I/O	Serial port 0 output
P3.2/INT0	14	I/O	General purpose I/O /External interrupt(Standard 8051)
P3.3/INT1	15	I/O	General purpose I/O /External interrupt(Standard 8051)
P3.4/T0	16	I/O	General purpose I/O (Standard 8051)
P3.5/T1	17	I/O	General purpose I/O (Standard 8051)
P7.6/CLKO	18	I/O	General purpose I/O /Clock out (CMOS)
P7.7	19	I/O	General purpose I/O (CMOS)
X2	20	O	Crystal Out
X1	21	I	Crystal In
VSS	22	-	Ground
NC	23	-	No connection
P6.0/AD0	24	I/O	General purpose I/O (CMOS) /6-bit ADC channel 0 input
P6.1/AD1	25	I/O	General purpose I/O (CMOS) /6-bit ADC channel 1 input
P6.2/AD2	26	I/O	General purpose I/O (CMOS) /6-bit ADC channel 2 input
P6.3/AD3	27	I/O	General purpose I/O (CMOS) /6-bit ADC channel 3 input
P6.4	28	I/O	General purpose I/O (CMOS)
P6.5	29	I/O	General purpose I/O (CMOS)
P6.6	30	I/O	General purpose I/O (CMOS)
P6.7	31	I/O	General purpose I/O (CMOS)
NC	32	-	No connection
NC	23	-	No connection
NC	23	-	No connection
NC	35	I/O	No connection
P1.7	36	I/O	General purpose I/O (Standard 8051)
P1.6	37	I/O	General purpose I/O (Standard 8051)
P1.5	38	I/O	General purpose I/O (Standard 8051)

P1.4	39	I/O	General purpose I/O (Standard 8051)
P1.3	40	I/O	General purpose I/O (Standard 8051)
P1.2	41	I/O	General purpose I/O (Standard 8051)
P1.1	42	I/O	General purpose I/O (Standard 8051)
P1.0	43	I/O	General purpose I/O (Standard 8051)
VCC	44	-	3.3V power

FUNCTIONAL DESCRIPTIONS

8051 CPU Core

The CPU core of CS8954 is compatible with the industry standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers, five interrupt sources and a serial interface. The CPU core fetches its program code from the 64K bytes Flash memory in CS8954. It uses Port0 and Port2 to access the "external special function register" (XFR) and external auxiliary RAM (AUXRAM).

The CPU core can run at single/double rate when FclkE is set. Once one of the bits is set, the CPU runs as if a 24MHz X'tal is applied on CS8954, but the peripherals (DDC, for example) still run at the original frequency.

Note: All registers listed in this document reside in 8051's external RAM area (XFR). For internal RAM memory map, please refer to 8051 spec..

Memory Allocation

i) Internal Special Function Registers (SFR)

The SFR is a group of registers that are the same as standard 8051.

ii) Internal RAM

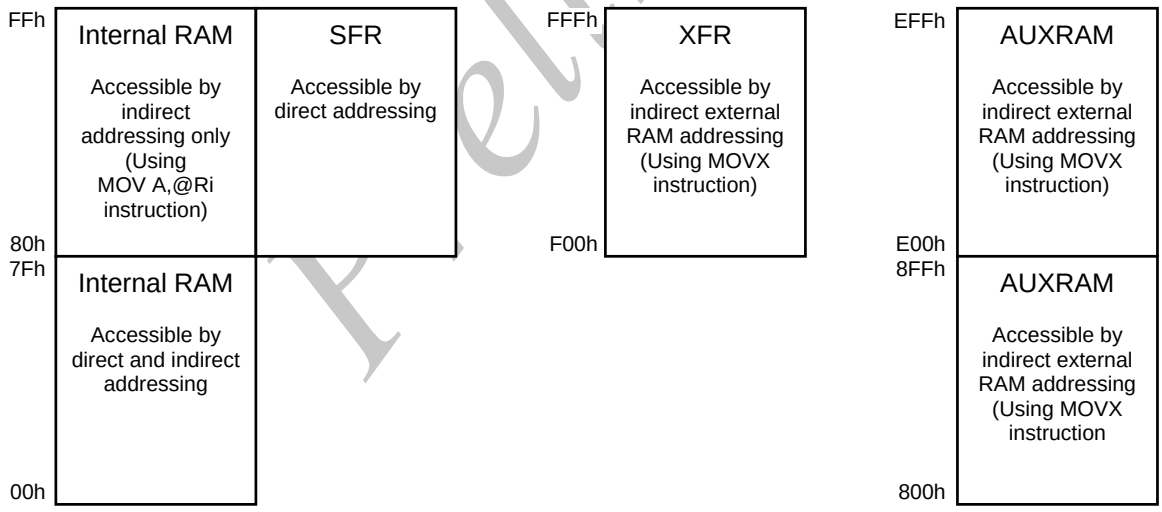
There are total 256 bytes internal RAM in CS8954, the same as standard 8052.

iii) External Special Function Registers (XFR)

The XFR is a group of registers allocated in the 8051 external RAM area F00h – FFFh. These registers are used for special functions. Programs can use "MOVX" instruction to access these registers.

iv) Auxiliary RAM (AUXRAM)

There are total 512 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - 8FFh and E00h - EFFh. Programs can use "MOVX" instruction to access the AUXRAM.



Chip Configuration

The Chip Configuration registers define configuration of the chip and function of the pins.

Reg name	addr	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0
PADMOD	F50h(w)								AD0E
PADMOD	F51h(w)			P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	REV0		REV0					
PADMOD	F53h(w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w)	PWMF	DIV253	FclkE	DCLK				IP77E
PADMOD	F5Eh(w)								
PADMOD	F5Fh(w)	P77oe	P76oe						

PADMOD (w) : Pad mode control registers. (All are "0" in Chip Reset. The registers named as “REV0” are reserved for testing, all of them should be written “0” after reset)

AD0E = 1 → Pin “P6.0/AD0” is AD0.
= 0 → Pin “P6.0/AD0” is P6.0.
P55E = 1 → Pin “DA5/P5.5” is P5.5.
= 0 → Pin “DA5/P5.5” is DA5.
P54E = 1 → Pin “DA4/P5.4” is P5.4.
= 0 → Pin “DA4/P5.4” is DA4.
P53E = 1 → Pin “DA3/P5.3” is P5.3.
= 0 → Pin “DA3/P5.3” is DA3.
P52E = 1 → Pin “DA2/P5.2” is P5.2.
= 0 → Pin “DA2/P5.2” is DA2.
P51E = 1 → Pin “DA1/P5.1” is P5.1.
= 0 → Pin “DA1/P5.1” is DA1.
P50E = 1 → Pin “DA0/P5.0” is P5.0.
= 0 → Pin “DA0/P5.0” is DA0.
Rev0 = 0 → These 2 bit MUST be written to 0 after Chip Reset
P57oe = 1 → P5.7 is output pin.
= 0 → P5.7 is input pin.
P56oe = 1 → P5.6 is output pin.
= 0 → P5.6 is input pin.
P55oe = 1 → P5.5 is output pin.
= 0 → P5.5 is input pin.
P54oe = 1 → P5.4 is output pin.
= 0 → P5.4 is input pin.
P53oe = 1 → P5.3 is output pin.
= 0 → P5.3 is input pin.
P52oe = 1 → P5.2 is output pin.

= 0 → P5.2 is input pin.
P51oe = 1 → P5.1 is output pin.
= 0 → P5.1 is input pin.
P50oe = 1 → P5.0 is output pin.
= 0 → P5.0 is input pin.
P67oe = 1 → P6.7 is output pin.
= 0 → P6.7 is input pin.
P66oe = 1 → P6.6 is output pin.
= 0 → P6.6 is input pin.
P65oe = 1 → P6.5 is output pin.
= 0 → P6.5 is input pin.
P64oe = 1 → P6.4 is output pin.
= 0 → P6.4 is input pin.
P63oe = 1 → P6.3 is output pin.
= 0 → P6.3 is input pin.
P62oe = 1 → P6.2 is output pin.
= 0 → P6.2 is input pin.
P61oe = 1 → P6.1 is output pin.
= 0 → P6.1 is input pin.
P60oe = 1 → P6.0 is output pin.
= 0 → P6.0 is input pin.
COP17 = 1 → Pin “P1.7” is CMOS Output.
= 0 → Pin “P1.7” is 8051 standard I/O.
COP16 = 1 → Pin “P1.6” is CMOS Output.
= 0 → Pin “P1.6” is 8051 standard I/O.
COP15 = 1 → Pin “P1.5” is CMOS Output.
= 0 → Pin “P1.5” is 8051 standard I/O.
COP14 = 1 → Pin “P1.4” is CMOS Output.
= 0 → Pin “P1.4” is 8051 standard I/O.
COP13 = 1 → Pin “P1.3” is CMOS Output.
= 0 → Pin “P1.3” is 8051 standard I/O.
COP12 = 1 → Pin “P1.2” is CMOS Output.
= 0 → Pin “P1.2” is 8051 standard I/O.
COP11 = 1 → Pin “P1.1” is CMOS Output.
= 0 → Pin “P1.1” is 8051 standard I/O.
COP10 = 1 → Pin “P1.0” is CMOS Output.
= 0 → Pin “P1.0” is 8051 standard I/O.
P77oe = 1 → P7.7 is output pin.
= 0 → P7.7 is input pin.
P76oe = 1 → P7.6 is output pin.
= 0 → P7.6 is input pin.
IP77E = 1 → Pin “P7.7 is P7.7 if IP76E = 1 in ICE mode.
= 0 → reserved.

OPTION (w) : Chip option configuration (All are "0" in Chip Reset).

PWMF = 1 → Selects 94KHz PWM frequency.
= 0 → Selects 47KHz PWM frequency.
DIV253 = 1 → PWM pulse width is 253-step resolution.
= 0 → PWM pulse width is 256-step resolution.
FclkE = 1 → CPU is running at double rate
= 0 → CPU is running at normal rate
DCLK = 1 → CKO outputs double frequency system clock.
= 0 → CKO outputs single frequency system clock.

I/O Ports

i) Port1

Port1 is a group of pseudo open drain pins or CMOS output pins. It can be used as general purpose I/O. Behavior of Port1 is the same as standard 8051.

ii) P3.0-2, P3.4

If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Behavior of Port3 is the same as standard 8051.

iii) Port5, Port6 and Port7

Port5, Port6 and Port7 are used as general purpose I/O. S/W needs to set the corresponding P5(n)oe and P6(n)oe to define whether these pins are input or output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT5	F37h(r/w)								P57
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
PORT7	F76h(r/w)								P76
PORT7	F77h(r/w)								P77

PORT5 (r/w) : Port 5 data input/output value.

PORT6 (r/w) : Port 6 data input/output value.

PWM DAC

Each output pulse width of PWM DAC converter is controlled by an 8-bit register in XFR. The frequency of PWM clock is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output pulses low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							

DA0-5 (r/w) : The output pulse width control for DA0-5.

* All of PWM DAC converters are centered with value 80h after power on.

A/D converter

The CS8954 is equipped with 4 VDD range 6-bit A/D converters. The ADC conversion range is from VSS to VDD, S/W can select the current convert channel by setting the SADC3 - SADC0 bit. The refresh rate for the ADC is OSC freq./1536 (128us for 12MHz X'tal).

The ADC compares the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 63). The ADC output value is N when pin voltage is greater than VDD*N/64 and smaller than VDD*(N+1)/64.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)	ADC convert result							
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

WDT (w) : Watchdog Timer control register.

WEN = 1 → Enables Watchdog Timer.
WCLR = 1 → Clears Watchdog Timer.
WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.
= 1 → Overflow interval = 1 x 0.25 sec.
= 2 → Overflow interval = 2 x 0.25 sec.
= 3 → Overflow interval = 3 x 0.25 sec.
= 4 → Overflow interval = 4 x 0.25 sec.
= 5 → Overflow interval = 5 x 0.25 sec.
= 6 → Overflow interval = 6 x 0.25 sec.
= 7 → Overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.

ENADC	= 1	→ Enables ADC.
SADC0	= 1	→ Selects ADC0 pin input.
SADC1	= 1	→ Selects ADC1 pin input.
SADC2	= 1	→ Selects ADC2 pin input.
SADC3	= 1	→ Selects ADC3 pin input.

ADC (r) : ADC convert result.

In System Programming function (ISP)

The Flash memory can be programmed by a specific WRITER in parallel mode, or by IIC Host in serial mode while the system is working. The features of ISP are outlined as below:

1. Single 3.3V power supply for Program/Erase/Verify.
2. Block Erase: 1024 bytes for Program Code, 10mS
3. Whole Flash erase (Blank): 10mS
4. Byte/Word programming Cycle time: 60uS per byte
5. Read access time: 50ns
6. Only one two-pin IIC bus (shared with DDC2) is needed for ISP in user/factory mode.
7. IIC Bus clock rates up to 140KHz.
8. Whole 64K-byte Flash programming within 6 Sec.(It depends on the external IIC speed)
9. CRC check provides 100% coverage for all single/double bit errors.

There are two methods to enter the ISP mode which are described as below:
Method 1). The Valid ISP Slave Address and Compared data are transmitted
Method 2). Write 93h to ISP enable register (ISPEN)

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							

ISPSLV (w) : ISP Slave IIC's address.
bit7-2 : ISP Slave IIC's address to which the ISP block should respond. The default value is 100101.
ISPEN(w) : Write 93h to enable ISP Mode for ISP enable method 2.

Memory Map of XFR

Address F00h to F0Ah are all reserved for testing, user should not change their values or just keep them all 0 after reset.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
REV	F00h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F01h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F02h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F03h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F04h (w)	REV	REV	REV	REV	REV	REV	REV	REV

REV	F06h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F07h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F08h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F09h (w)	REV	REV	REV	REV	REV	REV	REV	REV
REV	F0Ah (w)	REV	REV	REV	REV	REV	REV	REV	REV
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							
ISPCMP1	F0Dh(w)	ISP compared data 1 [7:0]							
ISPCMP2	F0Eh(w)	ISP compared data 2 [7:0]							
ISPCMP3	F0Fh(w)	ISP compared data 3 [7:0]							
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)			ADC convert Result					
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
PADMOD	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	F51h(w)	P57E	P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	Rev0		Rev0					
PADMOD	F53h(w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w)	PWMF	DIV253	FclkE	DCLK				IP77E

PADMOD	F5Eh(w)								
PADMOD	F5Fh(w)	P77oe	P76oe						
PORT7	F76h(r/w)								P76
PORT7	F77h(r/w)								P77
ETCTR	F88h (w)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
	F88h (r)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
ETMOD	F89h (w)								DCEN
	F89h (r)								DCEN
	F8Ah (w)	THET							
	F8Ah (r)	THET							
	F8Bh (w)	TLET							
	F8Bh (r)	TLET							
	F8Ch (w)	RCAPETH							
	F8Ch (r)	RCAPETH							
	F8Dh (w)	TCAPETL							
	F8Dh (r)	TCAPETL							
EINT1PEN	F8Eh (w)	EEINT1	ETE	TSTP1					

ELECTRICAL PARAMETERS

Absolute Maximum Ratings

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +3.6	V
Maximum Input Voltage (HSYNC, VSYNC & open-drain pins)	Vin1	-0.3 to 3.3+0.3	V
Maximum Input Voltage (other pins)	Vin2	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

Allowable Operating Conditions

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD	3.3V applications	3.0	3.6	V
Input "H" Voltage	Vih	3.3V applications	0.6 x VDD	VDD +0.3	V
Input "L" Voltage	Vil	3.3V applications	-0.3	0.3 x VDD	V
Operating Freq.	Fopg		-	15	MHz

DC Characteristics

at: Ta=0 to 70 °C, VDD=3.3V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, open drain pin	Voh1	VDD=3.3V, Ioh=0uA	2.65			V
Output "H" Voltage, 8051 I/O port pin	Voh2	VDD=3.3V, Ioh=-50uA	2.65			V
Output "H" Voltage, CMOS output	Voh3	VDD=3.3V, Ioh=-4mA	2.65			V
Output "L" Voltage	Vol	Iol=5mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=3.3V	150		250	Kohm
Pin Capacitance	Cio				15	pF

AC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=3.3V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		7.5	µS
VS input pulse Width	tVIPW	fXtal=12MHz	3			µS
HSYNC to Hblank output jitter	tHHBJ				5	nS
H+V to Vblank output delay	tVVBD	fXtal=12MHz		8		uS
VS pulse width in H+V signal	tVCPW	FXtal=12MHz	20			µS

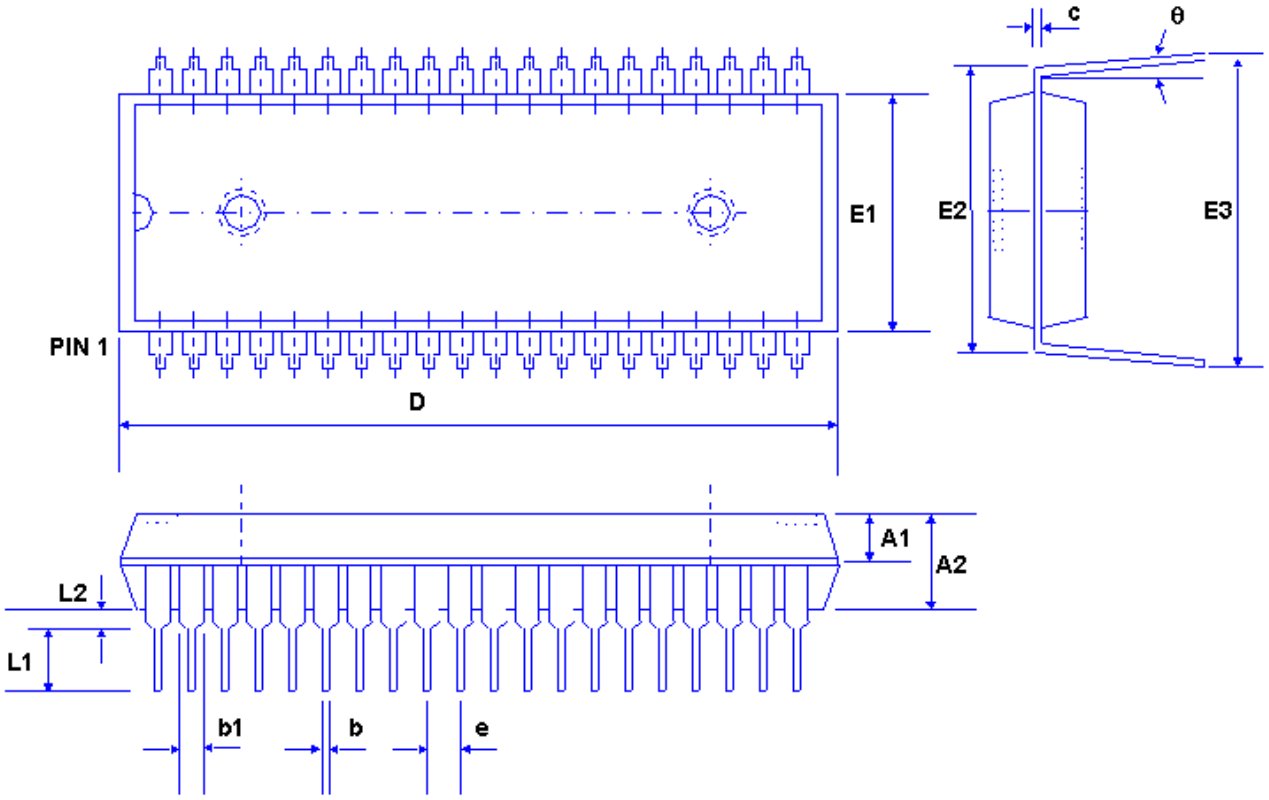
Test Mode Condition

In normal application, users should avoid the CS8954 entering its test mode or writer mode, outlined as follows: adding pull-up resistor to HSCL1/HSDA1/HSCL2/HSDA2 pins is recommended.

Test Mode: RESET's falling edge & P3.0=0 & P3.1=0 & P5.6 = 0

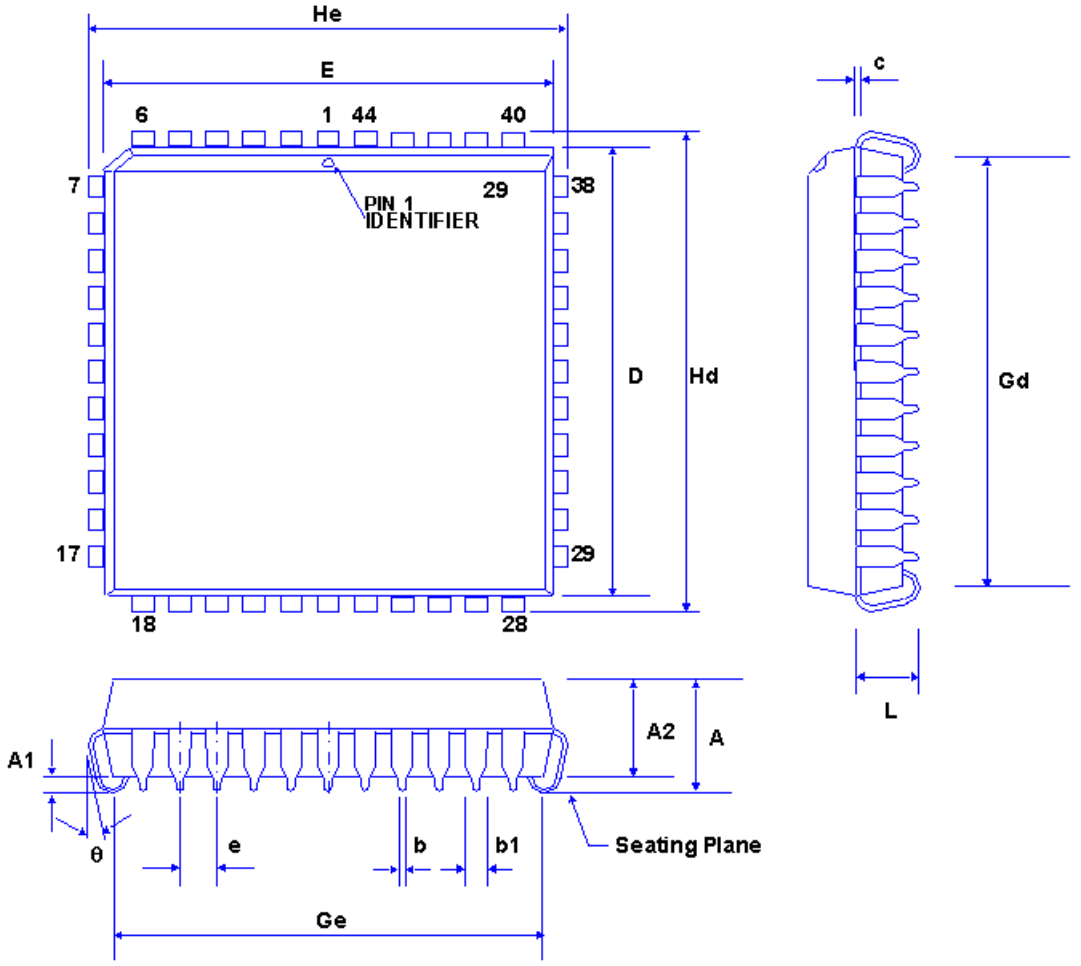
PACKAGE DIMENSION

40-pin PDIP



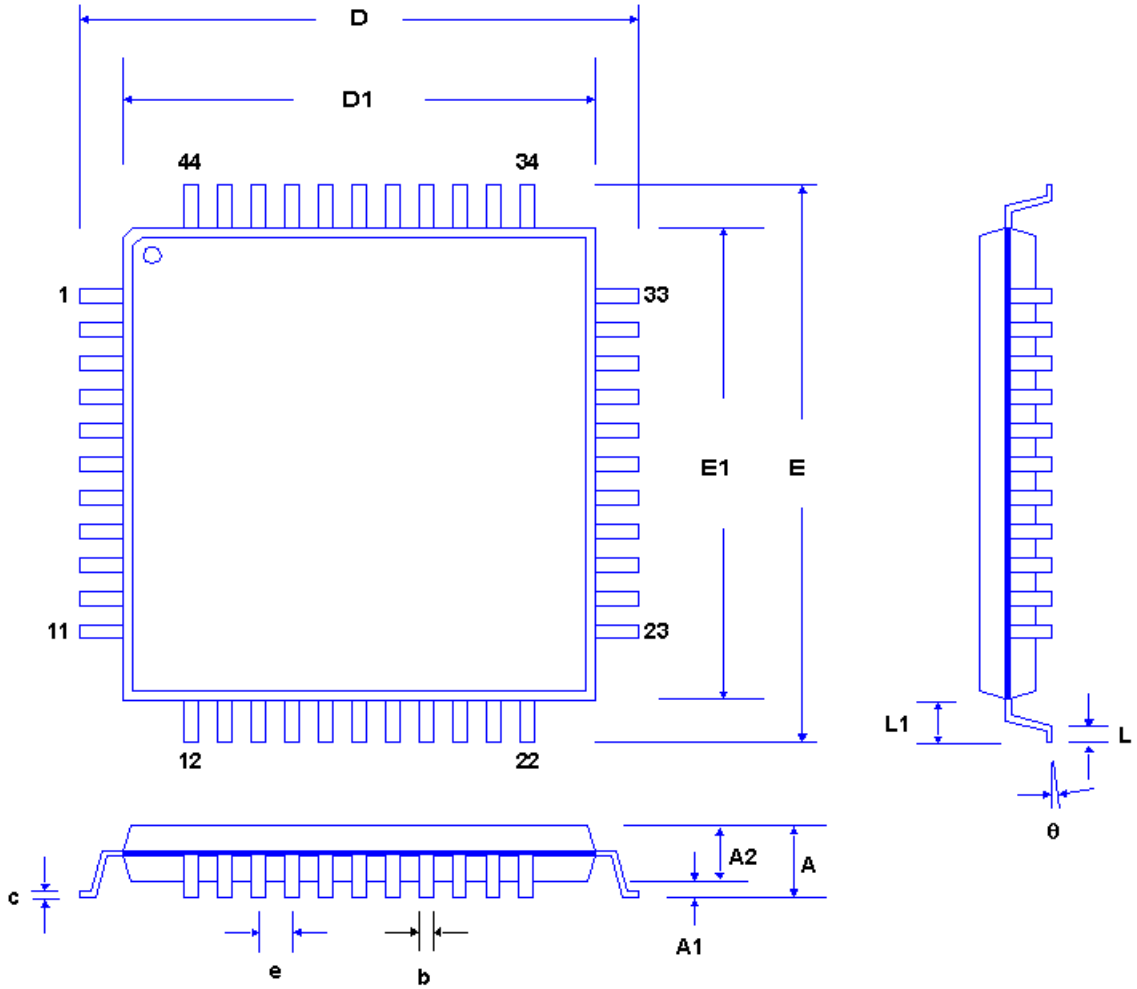
Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A1	1.65	1.78	1.91	0.065	0.070	0.075
A2	3.81	3.94	4.06	0.150	0.155	0.160
b	0.41	0.46	0.56	0.016	0.018	0.022
b1	1.22	1.27	1.37	0.048	0.050	0.054
c	0.20	0.25	0.36	0.008	0.010	0.014
D	-	52.18	52.58	-	2.055	2.070
E1	13.59	13.72	13.84	0.535	0.540	0.545
E2	14.99	15.24	15.49	0.590	0.600	0.610
E3	16.00	16.51	17.02	0.630	0.650	0.670
e	2.29	2.54	2.79	0.090	0.100	0.110
L1	3.05	3.30	3.56	0.120	0.130	0.140
L2	0.254	-	-	0.010	-	-
ɗ	0º	7.5º	15º	0º	7.5º	15º

44-pin PLCC



Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	4.70	-	-	0.185
A1	0.51	-	-	0.020	-	-
A2	3.70	3.80	3.90	0.145	0.150	0.155
b	0.41	0.46	0.56	0.016	0.018	0.022
b1	0.65	0.70	0.80	0.026	0.028	0.032
c	0.18	0.25	0.33	0.007	0.010	0.013
D	16.46	16.60	16.71	0.648	0.653	0.658
E	16.46	16.60	16.71	0.648	0.653	0.658
e	1.27 (Typ)			0.050 (Typ)		
Gd	15.00	15.50	16.00	0.590	0.610	0.630
Ge	15.00	15.50	16.00	0.590	0.610	0.630
Hd	17.30	17.50	17.80	0.680	0.690	0.700
He	17.30	17.50	17.80	0.680	0.690	0.700
L	2.29	2.54	2.80	0.090	0.100	0.110
ɗ	0º	-	10º	0º	-	10º

44-pin PQFP



Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	2.70	-	-	0.105
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	1.90	2.00	2.20	0.075	0.079	0.087
b	0.3 (Typ)			0.012 (Typ)		
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.00	13.20	13.40	0.510	0.520	0.530
D1	9.90	10.00	10.10	0.390	0.040	0.041
E	13.00	13.20	13.40	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.040	0.041
e	0.80 (Typ)			0.030 (Typ)		
L	0.73	0.88	0.93	0.029	0.035	0.037
L1	-	1.60	-	-	0.063	-
ɗ	0º	-	7º	0º	-	7º

Ordering Information

Standard Configurations:

Prefix	Part Type	Package Type
CS	8954N 8954V 8954F	N: PDIP V: PLCC F: PQFP