1 GSPS 14-Bit, 3.3V CMOS Direct Digital Synthesizer

Preliminary Technical Data — AD9910

FEATURES

- 1GSPS internal clock speed (up to 400MHz analog out)
- Integrated 1GSPS 14-bit DAC
- 32-bit tuning word
- Phase noise ≤ –123 dBc/Hz @ 1 kHz offset (400Mhz carrier)
- Excellent dynamic performance >80 dB narrowband SFDR
- Serial I/O control
- Automatic linear and nonlinear frequency sweeping capability
- 8 frequency/phase offset profiles
- 1.8V & 3.3 V power supply
- Software and hardware controlled power-down
- 100-lead TQFP/EP package
- Integrated 1024 word × 32-bit RAM
- PLL REFCLK multiplier
- Parallel Datapath Interface
- Internal oscillator, can be driven by a single crystal
- Phase modulation capability
- Amplitude modulation capability
- Multichip synchronization

APPLICATIONS

- Agile LO frequency synthesis
- Programmable clock generator
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar Modulator
- Fast Frequency Hopping

FUNCTIONAL BLOCK DIAGRAM

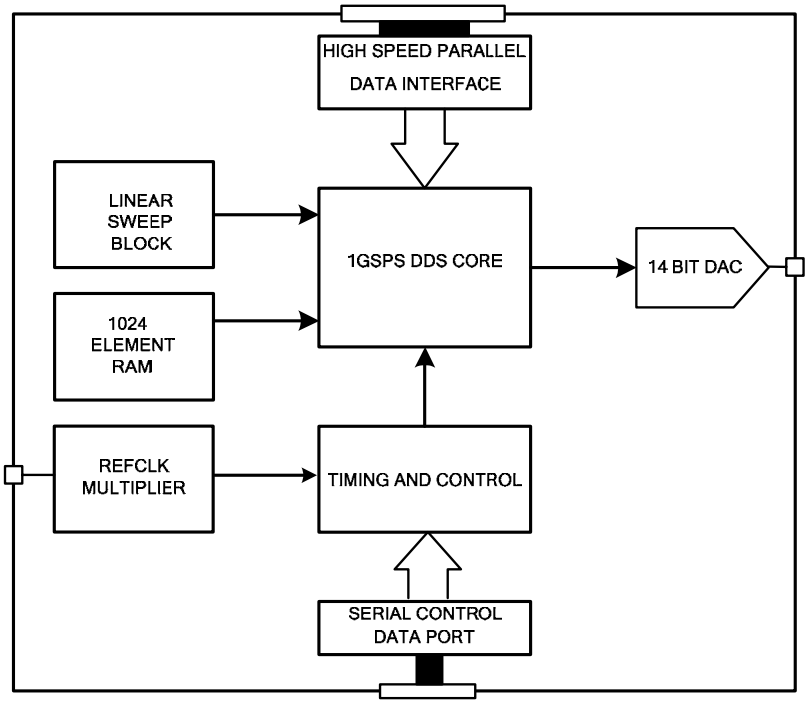

Figure 1. AD9910 Functional Block Diagram

Rev. PrD

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REVISION HISTORY

Revision PrA: Initial Preliminary for PSD1

Revision PrB: Update for Initial Silicon

GENERAL DESCRIPTION

The AD9910 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS. The AD9910 employs an advanced, proprietary DDS technology that provides a significant reduction in power consumption without sacrificing performance. The DDS/DAC combination forms a digitally programmable, high frequency, analog output synthesizer capable of generating a frequency-agile sinusoidal waveform at frequencies up to 400 MHz. The user has access to the three signal control parameters used to control the DDS: frequency, phase and amplitude. The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1GSPS sample rate, the tuning resolution is ~0.23Hz. The DDS also enables fast phase and amplitude switching capability.

The AD9910 is controlled by programming its internal control registers via a serial I/O port. The AD9910 includes an integrated static RAM to support various combinations of frequency, phase and/or amplitude modulation. The AD9910 also supports a user defined, digitally controlled, linear sweep mode of operation. In this mode frequency, phase or amplitude can be varied linearly over time. For more advanced modulation functions, a high speed parallel data input port is included to enable direct frequency, phase, amplitude, or polar modulation.

The AD9910 is specified to operate over the extended industrial temperature range (see Absolute Max Ratings table).

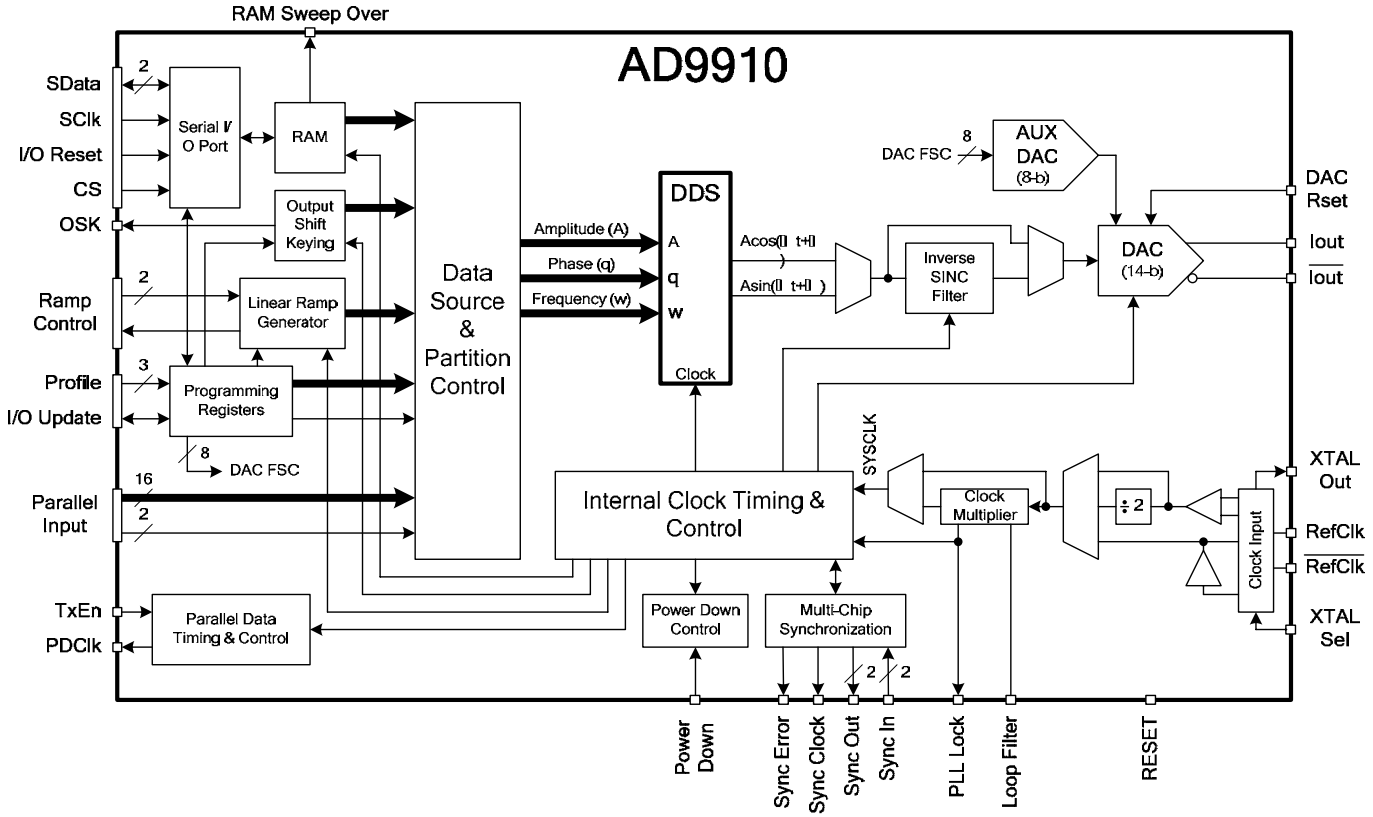


Figure 2: AD9910 detailed block diagram

AD9910—ELECTRICAL SPECIFICATIONS

Table 1. Unless otherwise noted, AVDD, DVDD = DVDD_I/O = 3.3 V ± 5%, R_{SET} = 3.92 kΩ, External Reference Clock Frequency = 25 MHz with REFCLK Multiplier Enabled at 40×.

Parameter	Min	Typ	Max	Unit
REF CLOCK INPUT CHARACTERISTICS				
Frequency Range				
REFCLK Multiplier Disabled	1		1000	MHz
REFCLK Multiplier Enabled at 4×	TBD		250	MHz
REFCLK Multiplier Enabled at 64×	TBD		15.625	MHz
Input Capacitance		3		pF
Input Impedance		1.5		kΩ
Duty Cycle		50		%
Duty Cycle with REFCLK Multiplier Enabled	35		65	%
REFCLK Input Power[1]	–15	0	+3	dBm
DAC OUTPUT CHARACTERISTICS				
Full Scale Output Current		20	30	mA
Gain Error	-0.5		+0.5	%FS
Output Offset			0.6	µA
Differential Nonlinearity		1		LSB
Integral Nonlinearity		2		LSB
Output Capacitance		5		pF
Residual Phase Noise @ 1 kHz Offset, 40 MHz A_{OUT}				
REFCLK Multiplier Enabled @ 64×		TBD		dBc/Hz
REFCLK Multiplier Enabled @ 4×		TBD		dBc/Hz
REFCLK Multiplier Disabled		–132		dBc/Hz
Voltage Compliance Range	2.5			V
Wideband SFDR				
1 MHz to 80 MHz Analog Out		80		dBc
80 MHz to 160 MHz Analog Out		66		dBc
160 MHz to 240 MHz Analog Out		63		dBc
240 MHz to 320 MHz Analog Out		58		dBc
320 MHz to 400 MHz Analog Out		55		dBc
Narrow Band SFDR				
80 MHz Analog Out (±1 MHz)		87		dBc
80 MHz Analog Out (±250 kHz)		89		dBc
80 MHz Analog Out (±50 kHz)		91		dBc
80 MHz Analog Out (±10 kHz)		93		dBc
240 MHz Analog Out (±1 MHz)		85		dBc
240 MHz Analog Out (±250 kHz)		87		dBc
240 MHz Analog Out (±50 kHz)		89		dBc
240 MHz Analog Out (±10 kHz)		91		dBc
320 MHz Analog Out (±1 MHz)		83		dBc
320 MHz Analog Out (±250 kHz)		85		dBc
320 MHz Analog Out (±50 kHz)		87		dBc
320 MHz Analog Out (±10 kHz)		89		dBc
400 MHz Analog Out (±1 MHz)		81		dBc
400 MHz Analog Out (±250 kHz)		83		dBc
400 MHz Analog Out (±50 kHz)		85		dBc
400 MHz Analog Out (±10 kHz)		87		dBc
TIMING CHARACTERISTICS				

Parameter	Min	Typ	Max	Unit
Serial Control Bus				
Maximum Frequency		25		Mbps
Minimum Clock Pulse Width Low		7		ns
Minimum Clock Pulse Width High		8		ns
Maximum Clock Rise/Fall Time		2		ns
Minimum Data Setup Time		3		ns
Minimum Data Hold Time		0		ns
Maximum Data Valid Time		25		ns
Wake-Up Time[2]		1		ms
Minimum Reset Pulse Width High		5		SYSCLK Cycles[3]
I/O UPDATE, PS0, PS1 to SYNCCLK Setup Time		4		ns
I/O UPDATE, PS0, PS1 to SYNCCLK Hold Time		1		ns
Parallel Data Bus				
Maximum Frequency		250		Mword/sec
Data setup time (to PDCLK)		TBD		nsec
Data hold time (to PDCLK)		TBD		nsec
Latency				
I/O UPDATE to Frequency Change Prop Delay		TBD		SYSCLK Cycles
I/O UPDATE to Phase Offset Change Prop Delay		TBD		SYSCLK Cycles
I/O UPDATE to Amplitude Change Prop Delay		TBD		SYSCLK Cycles
CMOS LOGIC INPUTS				
Logic 1 Voltage @ DVDD_I/O (Pin 43) = 3.3 V	2.2			V
Logic 0 Voltage @ DVDD_I/O (Pin 43) = 3.3 V			0.8	V
Logic 1 Current		3	12	µA
Logic 0 Current			12	µA
Input Capacitance		2		pF
CMOS LOGIC OUTPUTS (1 mA Load)				
Logic 1 Voltage	2.8			V
Logic 0 Voltage			0.4	V
POWER CONSUMPTION				
Single Tone Mode		700	TBD	mW
With RAM or Linear Sweep Enabled		800	TBD	mW
Rapid Power-Down Mode		500	TBD	mW
Full-Sleep Mode		50	TBD	mW
SYNCHRONIZATION FUNCTION[4]				
Maximum SYNC Clock Rate	TBD	250		MHz
SYNC_CLK Alignment Resolution[5]		±1		SYSCLK Cycles

[1] To achieve the best possible phase noise, the largest amplitude clock possible should be used. Reducing the clock input amplitude will reduce the phase noise performance of the device.

[2] Wake-up time refers to the recovery from analog power-down modes (see section on Power-Down Modes of Operation). The longest time required is for the reference clock multiplier PLL to relock to the reference. The wake-up time assumes there is no capacitor on DAC_BP and that the recommended PLL loop filter values are used.

[3] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external reference clock frequency.

[4] SYNC_CLK = ¼ SYSCLK rate. For SYNC_CLK rates ≥ 50 MHz, the high speed sync enable bit, CFR2<11>, should be set.

[5] This parameter indicates that the digital synchronization feature cannot overcome phase delays (timing skew) between system clock rising edges. If the system clock edges are aligned, the synchronization function should not increase the skew between the two edges.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Maximum Junction Temperature	150°C
AVDD(1.8V), DVDD(1.8V) supplies	2 V
AVDD(3.3V), DVDD_I/O(3.3V) supplies	4V
Digital Input Voltage)	–0.7 V to +4V
Digital Output Current	5 mA
Storage Temperature	–65°C to +150°C
Operating Temperature	–40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	38°C/W
θ_{JC}	15°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

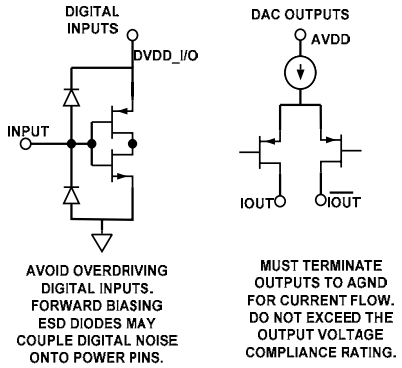
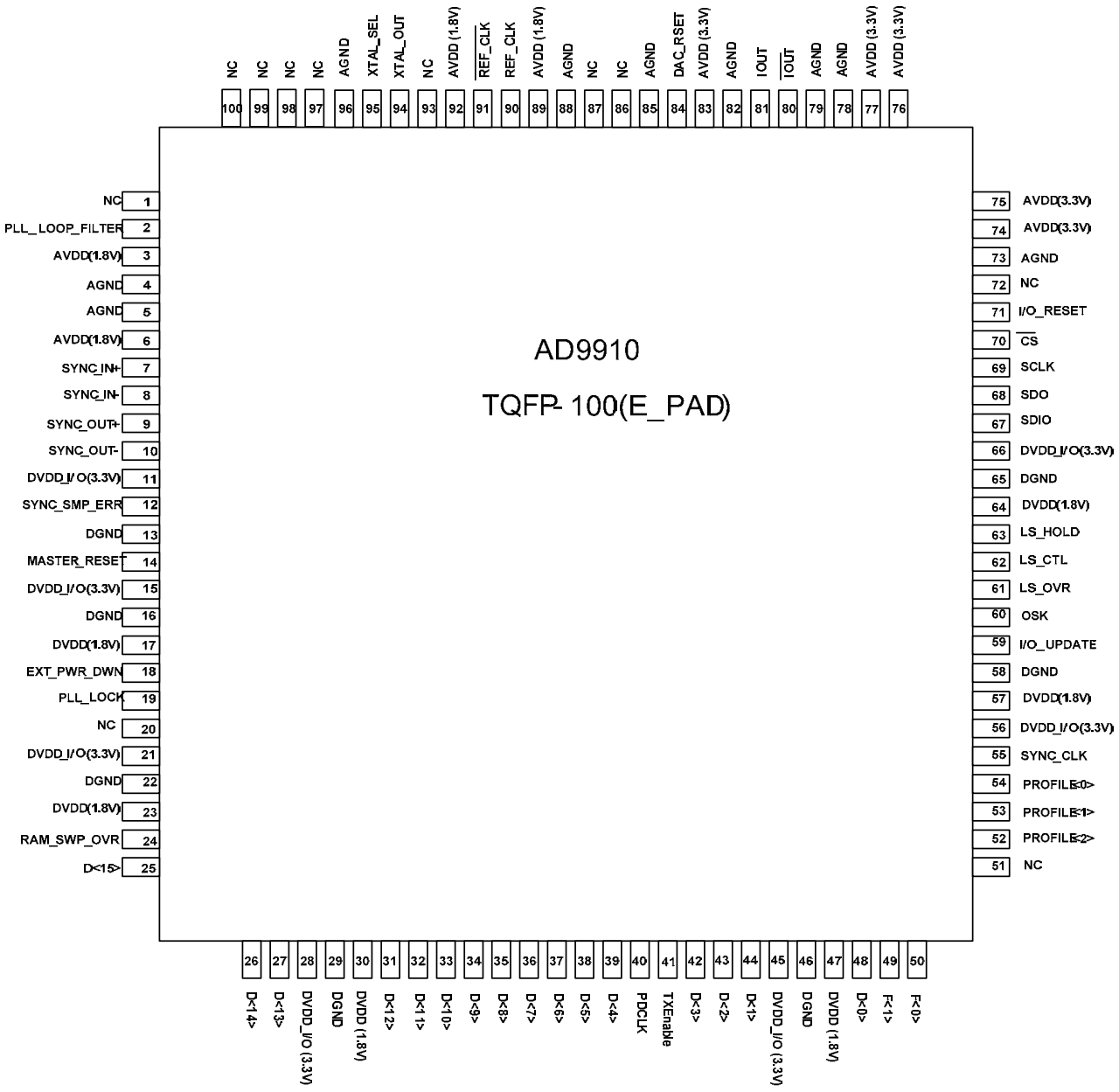


Figure 3. Equivalent Input and Output Circuits

DEVICE PIN DIAGRAM



PIN DESCRIPTION & NOMENCLATURE

Pin #	Mnemonic	I/O	Description
1, 20, 72, 86, 87, 93, 97-100	NC		Not Connected. Allow device pin to float.
2	LOOP FILTER	I	PLL loop filter compensation pin. Attach a .01uF and a 243 ohm resistor from this pin to AVDD to provide optimal PLL performance.
3, 6, 89, 92,	AVDD(1.8V)	I	Analog Core VDD: 1.8V Analog Supply
74-77, 83	AVDD (3.3V)	I	Analog DAC VDD: 3.3V Analog Supply.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD: 1.8V Digital Supply.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD: 3.3V Digital Supply.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 58, 65	DGND	I	Digital Ground.
17, 23, 30, 47, 57, 64	DVDD	I	Digital Core VDD: 1.8V Digital Supply
7	SYNC_I+	I	Digital input (rising edge active). Synchronization signal from external master to synchronize internal sub-clocks.
8	SYNC_I-	I	Digital input (rising edge active). Synchronization signal from external master to synchronize internal sub-clocks.
9	SYNC_O+	O	Digitaloutput (rising edge active). Synchronization signal from internal device sub-clocks to synchronize external slave devices.
10	SYNC_O-	O	Digitaloutput (rising edge active). Synchronization signal from internal device sub-clocks to synchronize external slave devices.
12	SYNC_SMP_ERR	O	Digital output (active high). Sync sample error: A high on this pin indicates that the AD9910 did not receive a valid sync signal on SYNC_I+/SYNC_I-.
14	MASTER_ RESET	I	Digital Input (active high). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	Digital input (active high). External Power Down: A high level on this pin initates the currently programmed power down mode. Please see the Power Down Modes section of this document for further details. If unused, tie to ground.
19	PLL_LOCK	O	Digital output (active high). PLL_Lock: A high indicates the clock multiplier PLL has acquired lock to the reference clock input.
24	RAM_SWP_OVER	O	Digital output (active high). RAM Sweep Over: A high indicates the current RAM sweep profile has completed.
25-27, 31-39, 42-44, 48	D<15:0>	I	Parallel input bus (active high).
49, 50	F<1:0>	I	Digital input to determine modulation format.
40	PDCLK	O	Digital output (clock) Parallel Data Clock provides a timing signal for aligning data at the parallel inputs.
41	TxENABLE	I	Digital input (active high). Transmit enable: In burst mode communications, a high on this pin indicates new data for transmission. In continuous mode, this pin should be kept high.
51	NC		No connection, but must be tied to DGND.
52-54	PROFILE <2:0>	I	Digital inputs (active high). Profile select pins: used to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins will transfer the current contents of all I/O buffers to the corresponding registers. State changes should be setup to the IO_SYNC_CLK pin.
55	IO_SYNC_CLK	O	Digital output (clock). Output clock divided by four. Many of the digital inputs on the chip, such as I/O_UPDATE and PROFILE<2:0> need to be setup to the rising edge of this signal
59	I/O_UPDATE	I	Digital input (active high). Input/Output update: A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Digital input (active high). Output shaped keying: When the OSK features (manual or

			automatic), this device controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero, a high sweeps the amplitude up to the amplitude scale factor.
61	LS_OVER	0	Digital output (active high). Linear Sweep Over: Upon completion of a linear frequency sweep, this flag will toggle high.
62	LSCTL	I	Digital input (active high). Linear Sweep Control: controls the direction of linear sweep operation. A high will sweep the frequency from initial frequency to terminal frequency, a low will sweep from the terminal frequency to the initial frequency.
63	LSHOLD	I	Digital input (active high). Linear Sweep Hold: this pin will stall a linear sweep operation prior to reaching the final frequency (initial or terminal) during a rising or falling linear sweep.
67	SDIO	I/O	Digital input/output (active high). Serial data input/output: this pin can be either uni-directional or bidirectional (default), depending on configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional, it is an input only.
68	SDO	O	Digital output (active high). Serial Data output: this pinis only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	O	Digital clock (rising edge on write, falling edge on read). Serial data clock: this pin provides the serial data clock for the control data path. Write operations to the AD9910 use the rising edge. Readback operations from the AD9910 use the falling edge.
70	$\overline{CS}$	I	Ditial input (active low) Chip Select: This pin allows the AD9910 to operate on a common serial bus for the control data path. Bringing this pin low enables the AD9910 to detect serial clock rising/falling edges. Bringing this pin high will cause the AD9910 to ignore input on the serial data pins.
71	I/O_RESET	I	Digital input (active high) I/O Reset: Rather than resetting the entire device during a failed communication cycle, when brought high this pin will reset the state machine of the serial port controller and clear any I/O buffers that have been written since the last I/O Update. When unused, tie this pin to ground to avoid accidental resets.
80	$\overline{IOUT}$	O	Analog output (current mode): Open source DAC complementary output source. Connect through 50Ω to AGND.
81	IOUT	O	Analog output (current mode): Open source DAC output source. Connect through 50Ω to AGND.
84	DAC_RSET	O	Analog reference pin: programs the DAC output full scale reference current. Attach a 10KΩ resistor to AGND.
90	CLK	I	Analog input(active high): Reference CLK input. Can be driven by either an external oscillator or a simple crystal when the internal oscillator is engaged.
91	$\overline{CLK}$	I	Analog input(active high): Reference CLK input
94	XTAL_OUT	O	Analog output (active high). Crystal Output: Provides the output of the internal oscillator's response to a crystal.
95	XTAL_SEL	O	Analog input (active high). Crystal select: A high on this pin (AVDD) enables the internal oscillator for clocking the part with a crystal.

MODES OF OPERATION

The AD9910 has four modes of operation.

1) Single-tone mode
2) RAM modulation mode
3) Linear ramp modulation mode
4) Parallel data port modulation mode

The modes relate to the data source used to supply the DDS with its signal control parameters: frequency, phase, and amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is handled automatically based on the mode and/or specific control bits.

In single-tone mode, data is routed to the DDS directly from the programming registers. In RAM modulation mode, data is routed to the DDS directly from the contents of the RAM. In linear ramp modulation mode, data is routed to the DDS from a digital ramp generator. In parallel data port modulation mode, data is routed to the DDS directly from the parallel data port.

NOTE: The various modulation modes generally operate on only one of the DDS signal control parameters (two in the case of the polar modulation format). The static (i.e., unmodulated) DDS signal control parameters are stored in their appropriate programming registers and automatically routed to the DDS based on the selected mode.

A separate output shift keying (OSK) function is also available. This function employs a separate digital linear ramp generator that only affects the DDS's amplitude parameter. As such, the OSK function can not be used when one of the modulation modes is operating on the DDS's amplitude parameter.

SINGLE-TONE MODE

In single-tone mode (Figure 4), the three DDS signal control parameters are supplied directly from the programming registers. The device can be programmed to operate with or without profiles. A profile is an independent register that contains the three DDS signal control parameters. There are eight available Profile Registers.

When programmed to operate with parameter profiles, each profile can be accessed independently. A particular profile is made selected via the three external Profile Select Pins. A change in the state of the Profile Select Pins along with the next rising edge of *Sync Clock* updates the DDS with the parameters specified by the selected profile.

NOTE: When the OSK function is enabled, its amplitude data overrides the amplitude parameter stored in the Profile Registers.

When programmed to operate without profiles the three DDS signal control parameters reside in separate registers. Frequency is controlled via the FTW register. Phase offset is controlled via the POW register. Amplitude is controlled via the amplitude scale factor that resides in the ASF register.

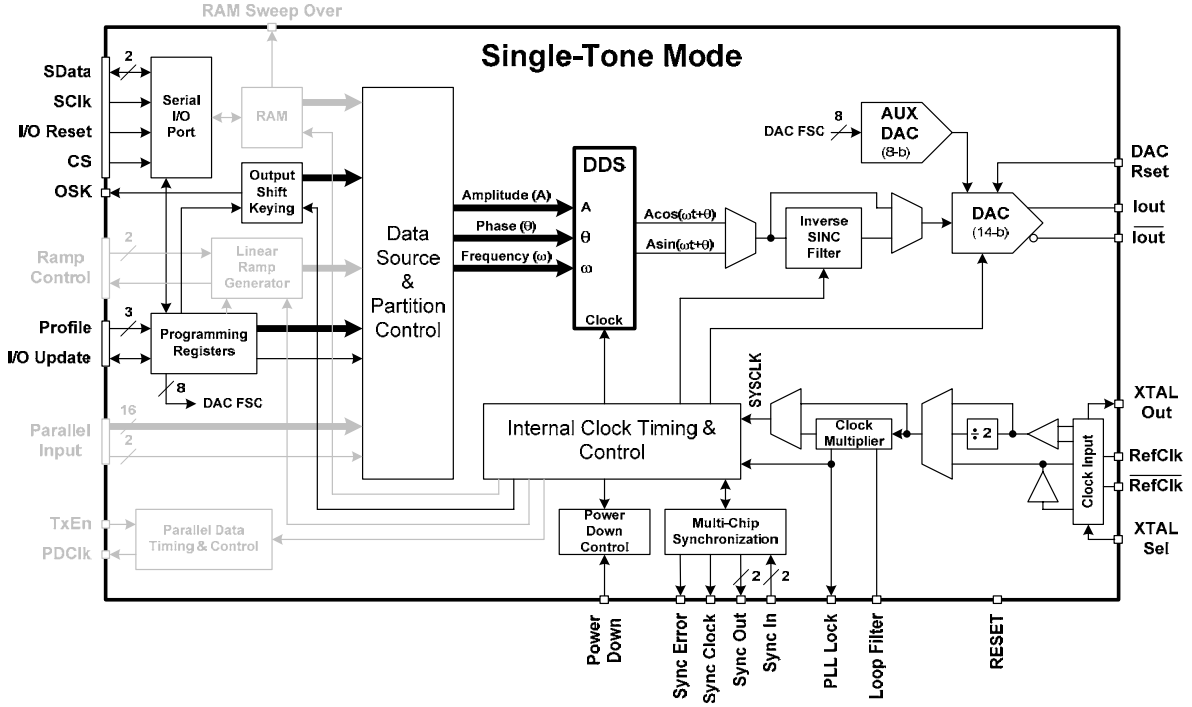


Figure 4: Single-tone mode

RAM MODULATION MODE

In RAM modulation mode (Figure 5) the modulated DDS signal control parameter(s) are supplied directly from RAM. The RAM contains 1024 32-bit words. It provides a very flexible method for generating arbitrary, time-dependent data patterns. The rate at which words are extracted from the RAM is controlled by a programmable timer. Thus, each word can be thought of as a 32-bit sample, which successive samples delivered at a sample rate determined by the programmable timer.

The destination of the samples is also under program control. That is, the sample can be routed to any of the three DDS control parameters; frequency, phase, and amplitude. The ability to generate a time-dependent amplitude, phase, or frequency signal enables modulation of any one of the parameters controlling the DDS carrier signal. In addition, a polar modulation format is also available, in which each RAM sample is partitioned into a magnitude and phase component: 16 bits phase allocated to phase and 14 bits allocated to magnitude.

NOTE: When the OSK function is enabled, its amplitude data overrides any RAM data that is destined for the DDS amplitude control parameter.

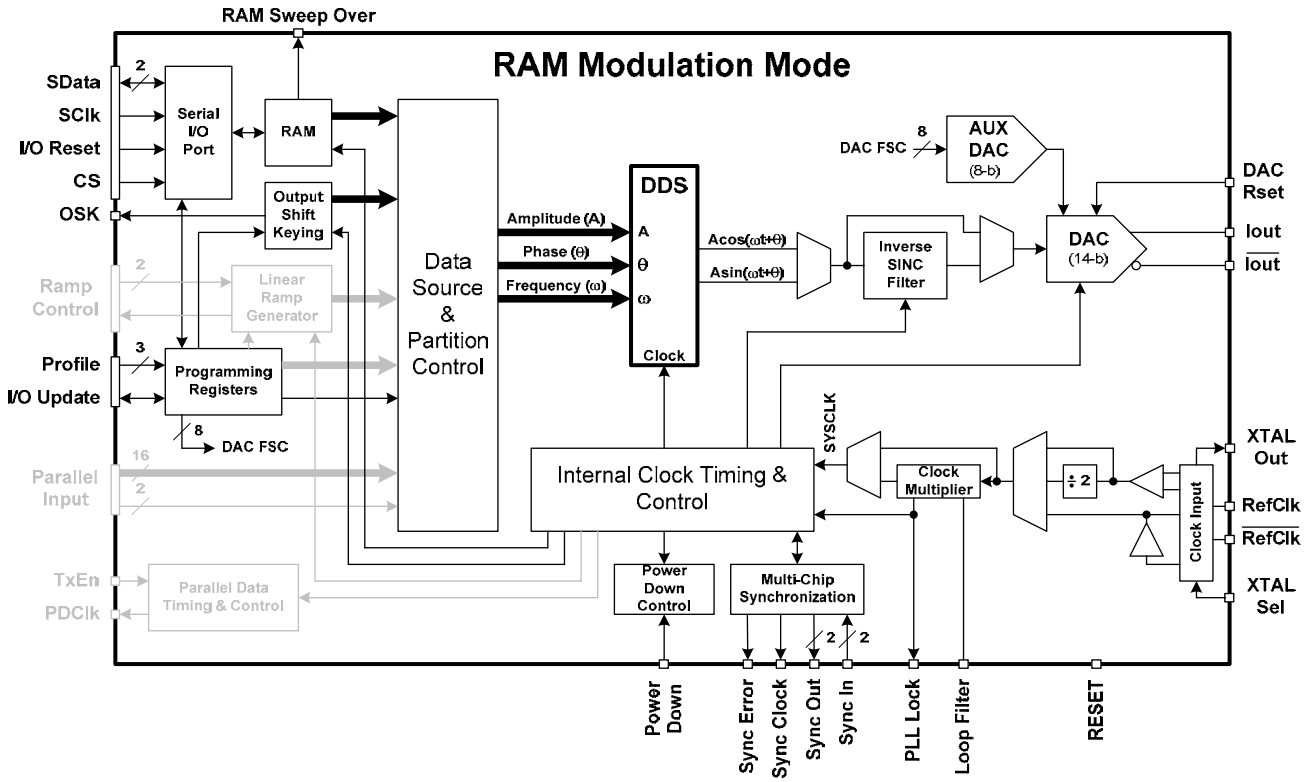


Figure 5: RAM modulation mode

LINEAR RAMP MODULATION MODE

In linear ramp modulation mode (Figure 6), the modulated DDS signal control parameter is supplied directly from Linear Ramp Generator. The ramp generation parameters are controlled via the serial I/O port.

The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp. The upper and lower boundaries of the ramp, the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp are all programmable.

The ramp is digitally generated with 32-bit output resolution. The 32-bit output of the Linear Ramp Generator can be programmed to represent frequency, phase, or amplitude. When programmed to represent frequency all 32 bits are used. However, when programmed to represent phase or amplitude, only the 16 MSBs or 14 MSB, respectively, are used.

The ramp direction (rising/falling) is controlled externally by the LSCTL pin. An additional pin (LSHOLD) allows the user to freeze the ramp generator at its present state.

NOTE: When the OSK function is enabled, its amplitude data overrides any Linear Ramp data that is destined for the DDS amplitude control parameter.

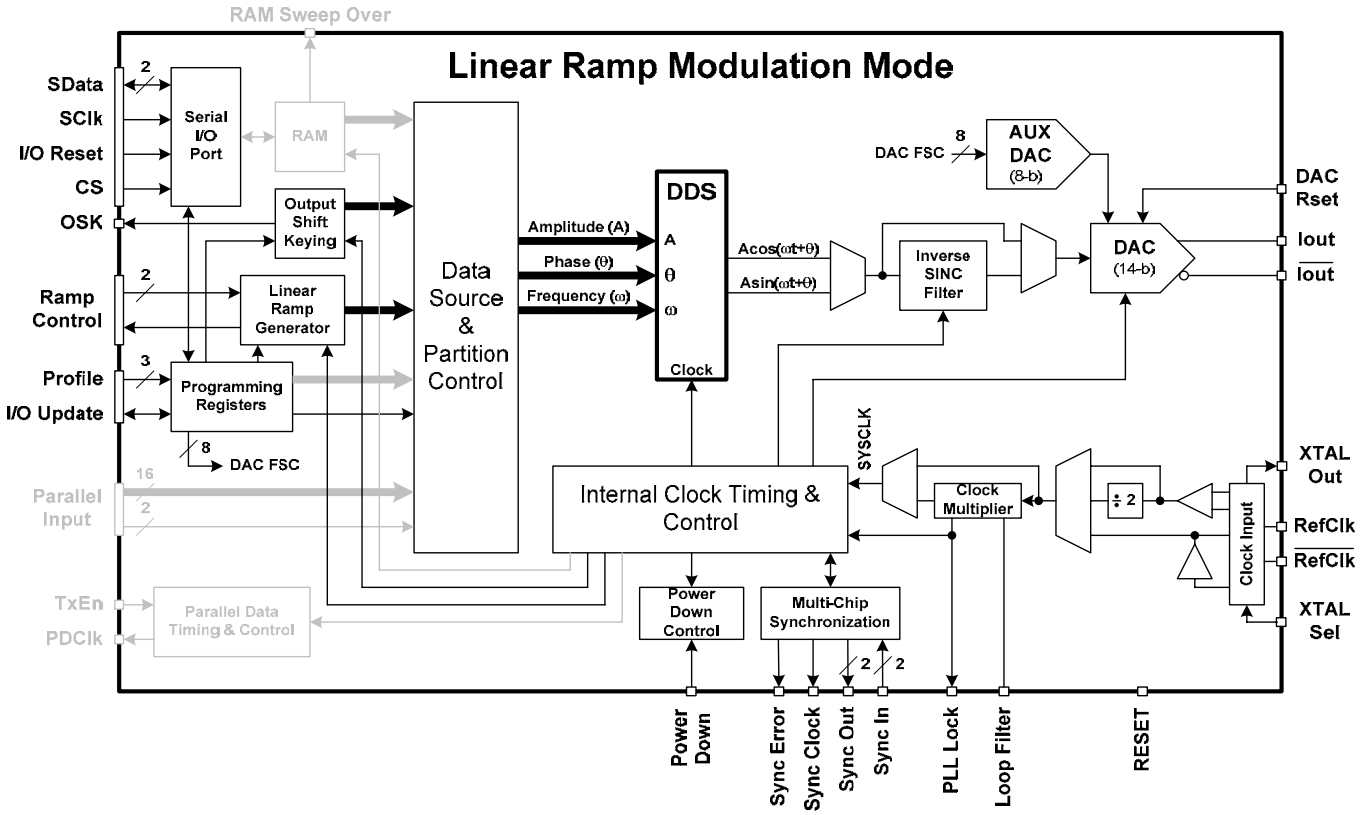


Figure 6: Linear ramp modulation mode

PARALLEL DATA PORT MODULATION MODE

In parallel data port modulation mode (Figure 7) the modulated DDS signal control parameter(s) are supplied directly from the 18-bit parallel data port.

Table 2 defines the relationship between the destination bits, the partitioning of the 16-bit data word and the destination of the data (in terms of the DDS signal control parameters).

NOTE: When the OSK function is enabled, its amplitude data overrides any parallel port data that is destined for the DDS amplitude control parameter.

The sample rate of the parallel data port is ¼ of the DAC sample rate. The AD9910 generates the PDCLK signal, which is a clock signal that runs at ¼ of the DAC sample rate and serves as a data clock. Each rising edge of PDCLK is used to latch the 18 bits of user-supplied data into the data port.

The AD9910 also accepts a user generated TxEn signal that acts as a gate for the user supplied data. When TxEn is logic 0 the device ignores the data supplied to the port. However, internally, the 16-bit data words are either forced to logic zeros or held at their last state when TxEn transitions from a logic 1 to a logic 0. The treatment of the 16-bit data words when TxEn is logic 0 is controlled by a bit in the programming registers. The destination bits, on the other hand, always retain their last state when TxEn transitions to a logic 0.

The data port is partitioned into two sections. The 16 MSBs make up a 16-bit data word and the 2 LSBs make up a 2-bit destination word. The destination word defines how the 16-bit data word is applied to the DDS signal control parameters.

When the destination bits indicate that the data word is destined as a DDS frequency parameter, there is an additional consideration. Recall that the DDS frequency parameter is a 32-bit word. However, the data word is only 16 bits, which means that the 16-bit data word must somehow be properly aligned with the 32-bit frequency parameter. This is accomplished by means of 4-bit *FM Gain* word in the programming registers. The FM Gain word allows the user to apply a weighting factor to the 16-bit data word.

The default value of the FM Gain word is 0. In the default state, the data word and the DDS frequency parameter are LSB aligned. Each increment in the value of the FM Gain word shifts the 16-bit data word to the left relative to the DDS fre-

quency parameter, thereby increasing its affect on the DDS frequency by a factor of 2. The FM Gain word effectively controls the maximum frequency range spanned by the data word.

Table 2: Parallel port destination bits

Destination Bits <1:0>	Data Word Partitioning <17:2>	DDS Signal Control Parameter	Remarks
00	<17:4>	14-bit amplitude parameter (unsigned integer)	Amplitude scales from 0 to $1-2^{-14}$. <3:0> are ignored.
01	<17:2>	16-bit phase parameter (unsigned integer)	Phase offset ranges from 0 to $2\pi(1-2^{-16})$ radians.
10	<17:2>	32-bit frequency parameter (unsigned integer)	The alignment of 16-bit data word with the 32-bit frequency parameter is controlled by a 4-bit FM Gain word in the programming registers.
11	<17:10> <9:2>	8 bits amplitude (unsigned integer) 8 bits phase (unsigned integer)	The MSB of the data word amplitude aligns with the MSB of the DDS's 14-bit amplitude parameter. The 6 LSBs of the DDS's amplitude parameter are assigned from bits <5:0> of the ASF register. The resulting 14-bit word scales the amplitude from 0 to $1-2^{-14}$. The MSB of the data word phase aligns with the MSB of the DDS's 16-bit phase parameter. The 8 LSBs of the DDS's phase parameter are assigned from bits <7:0> of the POW register. The resulting 16-bit word offsets the phase from 0 to $2\pi(1-2^{-16})$ radians.

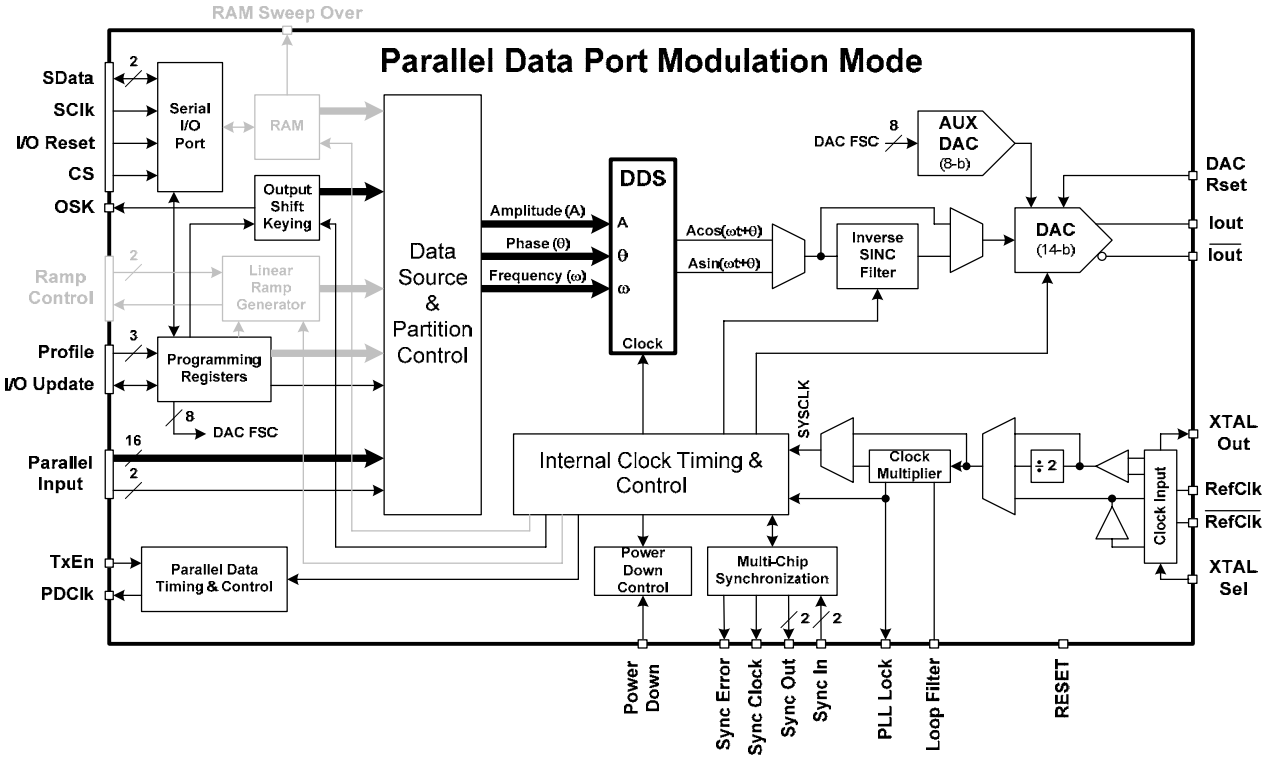


Figure 7: Parallel data port modulation mode