Product Bulletin

TMS320TCI6488 DSP Platform

The TMS320TCI6488 (TCI6488) device is a very high-performance DSP designed specifically for WCDMA wireless infrastructure baseband applications. With a high level of functional integration and a high channel density supported on a single device, the TCI6488 DSP offers a modular and scalable design with a small footprint. The TCI6488 DSP is therefore an ideal solution for pico, micro and macro BTS and enables an SOC baseband solution for WCDMA Tx and Rx applications. OEMs can accelerate their channel card development with the use of the TCI6488 DSP, since it offers a software-programmable solution and allows for the reuse of existing C64x™ and C64x+™ DSP code.

Key Benefits

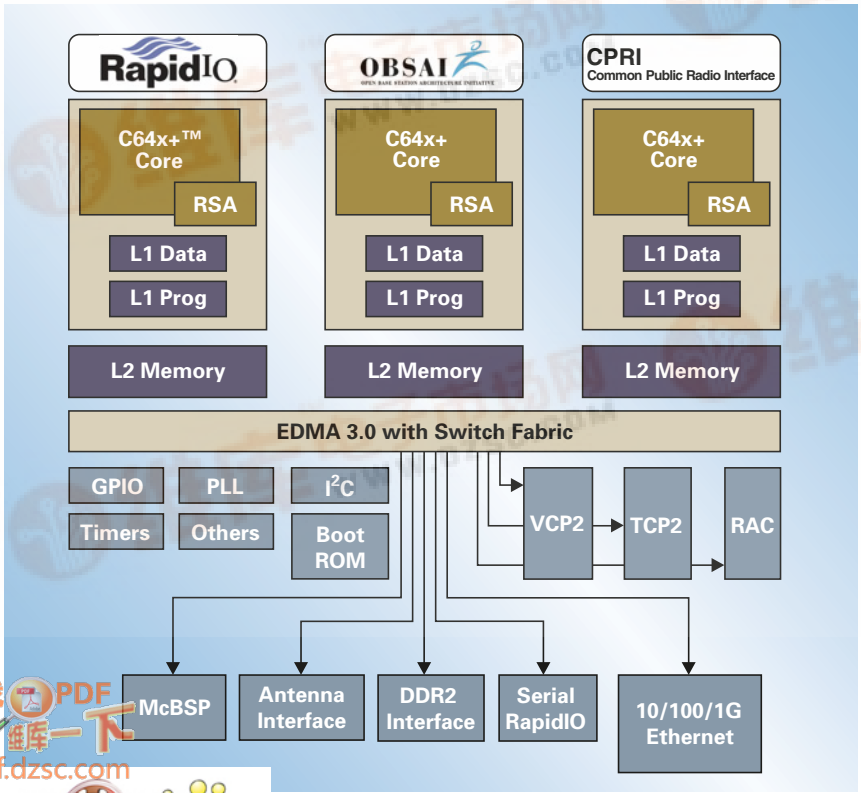
- WCDMA SOC platform
  - SOC baseband solution for WCDMA Tx and Rx processing
  - Built-in receiver accelerator coprocessor (RAC) performs Rx chip-rate processing
- Scalable platform
  - Modular design is ideal for pico, micro and macro BTS
- Quick time to market
  - Software-programmable solutions with the reuse of existing software leads to a shorter development cycle
- Cost optimization
  - Functional integration leads to lower system cost and eliminates the need for accelerator ASICs

TCI6488 DSP Architecture

The TCI6488 high-performance DSP has three independent DSP subsystems. At the heart of each subsystem is a 1.0-GHz C64x+ DSP core. For flexibility, the 3 Mbytes of L2 SRAM/cache can be configured in multiple ways, such as 1/1/1 Mbytes or 1.5/1/0.5 Mbytes, among the three DSP cores. To support wireless applications, the DSP contains a number of specialized coprocessors:

- Viterbi-decoder coprocessor 2 (VCP2)
- Turbo-decoder coprocessor 2 (TCP2)
- Receiver accelerator coprocessor (RAC)

Figure 1. TCI6488 DSP Block Diagram



The RAC subsystem is a receiver chip-rate accelerator based on a generic correlator coprocessor (GCCP). It supports UMTS operations, assists in transferring received antenna data to the receive core and performs receive functions targeted at WCDMA Macro BTS. Another important feature of the TCI6488 is its support of standard interfaces such as serial RapidIO (SRIO), Gigabit Ethernet, DDR2 and McBSP. The TCI6488 also supports the OBSAI and CPRI antenna interfaces, with up to six configurable links at a maximum rate of 3.072 Gbps (OBSAI) and 2.4576 Gbps (CPRI).

Key Features

- 3.0 GHz of total raw DSP processing power
- A total of 3 Mbytes of total on-chip L2 SRAM/cache
- Standard C64x+™ DSP core
  - Enables reuse of existing DSP software
- Dedicated RAC coprocessor
  - Performs chip-rate Rx functions: Preamble detect, path search and finger despread
- Industry-leading 65-nm silicon technology
  - Enables a high level of functional integration on a single device
  - Enables a high-channel-density solution
- Software-programmable resources
  - Enables the reuse of MIPS and memory resources on the DSP for various types of functionality
- Standard interfaces
  - SGMII Gigabit Ethernet, DDR2, two serial RapidIO (SRIO) links, McBSP, I²C, GPIO
- Debug interface
  - EMU/trace
- Antenna interfaces
  - OBSAI and CPRI standards-compliant antenna interface

The EDMA 3.0 switch-fabric engine supports high-bandwidth, low-latency internal communications. The EDMA manages communications between peripherals, memories, accelerators and DSP cores.

Interfaces

TCI6488 supports standard antenna, network, device and interdevice communication interfaces as well as a high-speed interface to communicate with external memory:

Antenna Interface

Six configurable (full-duplex) links in either OBSAI or CPRI modes that can support a variety of data rates. Supports OBSAI/CPRI daisy chaining between DSPs.

- OBSAI—614.4-Mbps, 1.2288-Gbps, 2.4576-Gbps link rates supported
- CPRI—768-Mbps, 1.536-Gbps, 3.072-Gbps link rates supported

Network Interface

- 10/100/1000 Ethernet (SGMII)

Interdevice Communication

- SRIO—Two 1x lanes at a rate of 1.25, 2.5 or 3.125 Gbps each
- SRIO daisy chain capability between TCI6488 DSPs
  - Multiple TCI6488 DSPs on a card can be interconnected via an SRIO daisy chain
  - Hardware packet-forwarding mechanism supports passing data through the daisy chain to a specific TCI6488 DSP
- McBSP—Two McBSP links, each at 100 Mbps
  - McBSP can be used for multichannel clocked serial communications
- I²C—One I²C link at 400 kbps
  - I²C can be used for communication links between integrated circuits or for peripheral devices on an embedded system

Memory Interface

- DDR2-400 to DDR2-667 support

TCI6488 DSP Applications

The TCI6488 DSP offers a very high-density SOC baseband solution that is easily scalable for pico, micro and macro BTS applications for the WCDMA standard.

General Characteristics

- Supports pico to macro via the TCI6488 scalable architecture
- Supports various radio topologies including:
  - TD-SCDMA, WiMAX, cdma2000 and UMTS Tx
  - ASIC-plus-DSP implementations for UMTS
- Code compatible with C64x and C64x+ platforms

UMTS (NOM) Macro BTS Tx and Rx

- 48 users per device (voice)
- 32 users per device (64 kbps)
- 8 users per device (384 kbps)

UMTA (High Performance) Rx Only Macro BTS

- 64 users per device (voice)
- 48 users per device (64 kbps)

UMTS Pico BTS Solution Tx and Rx

- 96 users per device (voice)
- 64 users per device (64 kbps)

UMTS HSUPA (E-DCH)

- Up to 10 Mbps UL HSUPA raw

UMTS Macro BTS—HSDPA DL (3 Sectors)

- 48 users per device (64 kbps UL with Mac-HS and no Tx chip rate)

RAC

The RAC subsystem shown in Figure 2 is a chip-rate accelerator that is used in the receiver side of the BTS. It is based on a GCCP that supports UMTS-specific operations. The RAC assists in transferring received antenna data to the receive core and performs receive functions targeted for WCDMA Macro BTS applications.

The RAC subsystem consists of two GCCP accelerators that are used for finger despread (FD), path search (PS), preamble detection (PD) and stream power estimation (SPE). In addition, the RAC has a back-end interface (BEI) for management of RAC configuration and data output. There is a front-end interface (FEI) to receive antenna data for processing and to provide access to MMRs and memories in the RAC subsystem. The RAC has three ports that are connected to the DMA crossbar—two master connections to BEI and one slave to FEI.

Transmit Chip-Rate Accelerator Using RSA

Transmit chip-rate processing is implemented by DSP subsystem and its associated RSA extensions. The DSP core generates both OVSF and PN codes and provides the multiplied result of these two codes as input to the RSA. The modulated user symbols are also provided as input to the RSA. The RSA applies the code values to the modulated symbols to achieve spreading and scrambling. It is also capable of carrying out the stream aggregation functionality.

SmartReflex™ Technology

The increased processing demands of today's advanced wireless networks have also increased power consumption. To solve this problem, Texas Instruments (TI) has implemented a new power- and performance-management technology called SmartReflex™ in the TCI6488 DSP. This technology closely monitors circuit speed and dynamically adjusts voltages to meet exact performance requirements. As a result, minimum power is used for each operating frequency, thereby reducing the amount of heat produced by the device. This provides the flexibility to add multiple TCI6488 devices on a single card while still meeting the designer's power budget.

Advanced 65-nm Platform

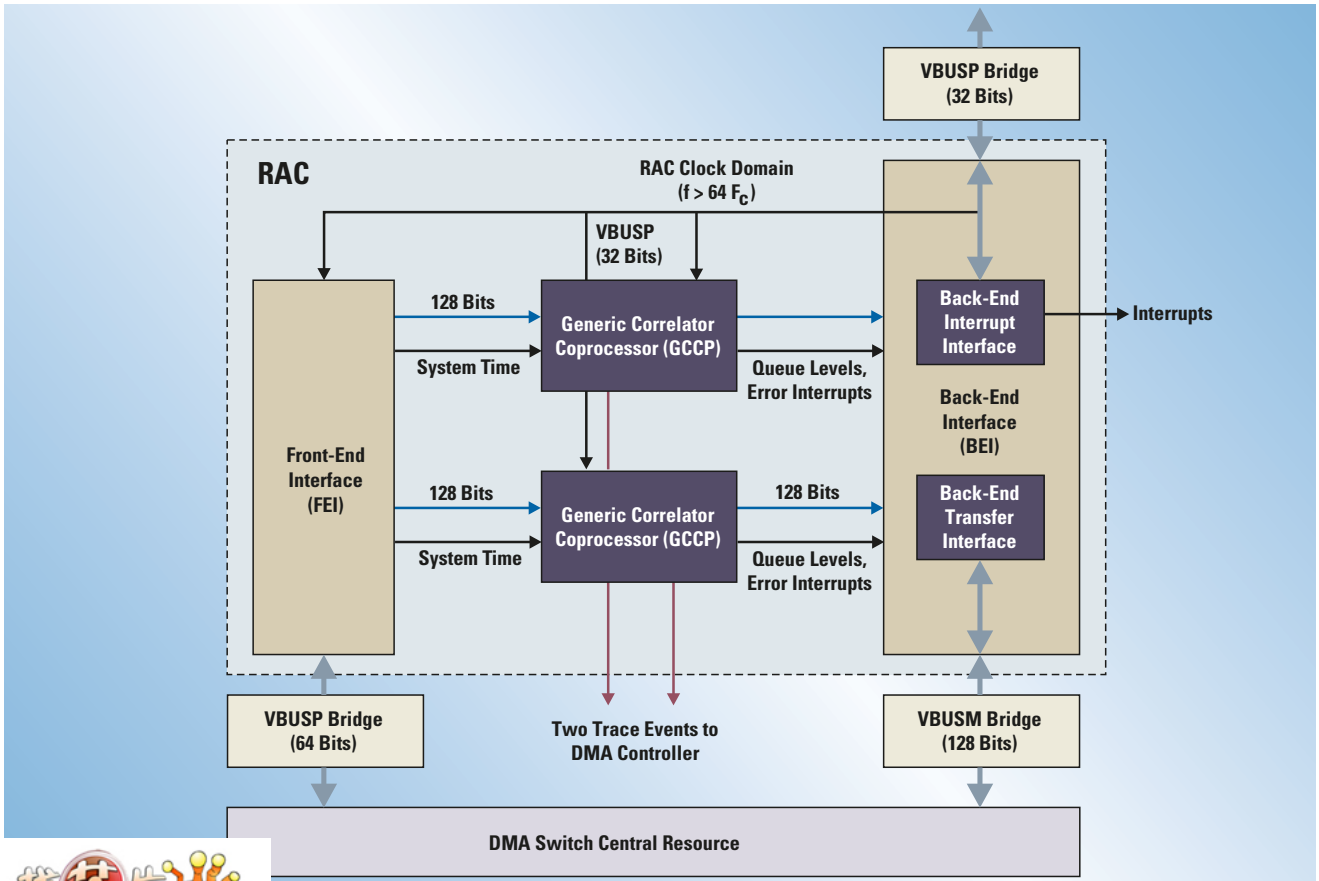
The TCI6488 is built on the latest cutting-edge technology, the new 65-nm process node. This process technology doubles the transistor density of the previous 90-nm process, shrinking equivalent designs and boosting transistor performance. This allows the TCI6488 to perform at a level that is an order of magnitude higher than the previous process node at a fraction of the power consumption.

For More Information

To learn more about the TMS320TCI6488 DSP—or other wireless solutions from TI—visit

www.ti.com/wi

Figure 2. Receiver Chip-Rate Processing Using RAC



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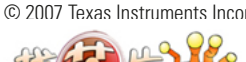

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