S3524A

AMERICAN MICROSYSTEMS, INC.

2600Hz Digital Frequency Detector

August 1996

Features

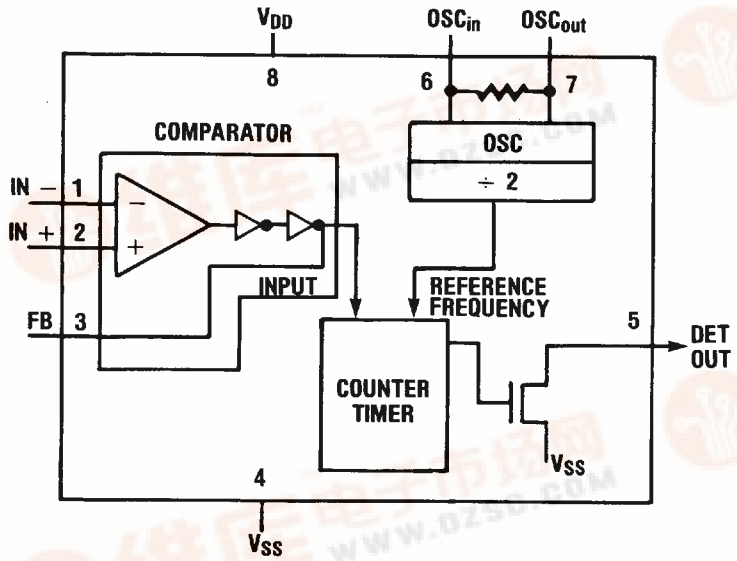
- 2600Hz Center Frequency With 70Hz Bandwidth.
- Small 8-Pin Minidip Package
- Operation From a Low Cost 3.58MHz TV Color-burst Crystal or External Clock
- Input Comparator for Squaring and Sensitivity Adjustment
- Low Power CMOS Technology

Description

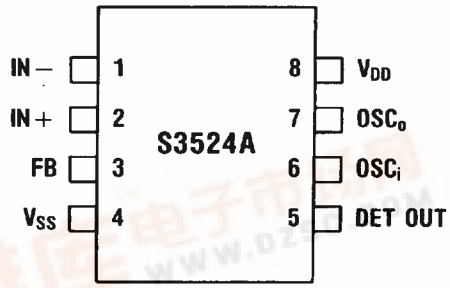
The S3524 is a digital Frequency Detector used to accurately determine if an incoming tone is within a set of predefined limit frequencies. It checks every period of the incoming signal, giving a true output for each period falling within the desired bandwidth.

The S3524A, using a 3.58 MHz clock, will detect a 2600Hz frequency within 70Hz bandwidth. It is primarily designed to follow the S3526B 2600Hz bandpass filter as shown in Figure 4.

Block Diagram



Pin Configuration



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Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS})	± 15V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Analog Input	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to GND)	4.75	5	5.25	V
V_{SS}	Negative Supply (Ref. to GND)	−4.75	−5	−5.25	V
PD	Power Dissipation			100	mW
V_{IN}	Input Signal Level	43			mV (RMS)
R_0	Load Resistance	6			k Ω

Pin Description

Name	Number	Description
V_{DD}	8	Positive Power Supply. Typically +5V.
V_{SS}	4	Negative Power Supply. Typically −5V.
IN−	1	Input comparator for setting sensitivity and squaring of analog signals. Signal sensitivity is controlled by selecting external resistors.
IN+	2	
FB	3	
DET OUT	5	The detector output. Open drain type output for ease of interface. DET OUT will be high after one full cycle of valid signal is detected, and will remain high until an out of frequency cycle is detected.
OSC IN	6	Oscillator terminals for 3.58MHz reference crystal or clock. Uses standard TV crystal or a rail-to-rail CMOS clock may be used.
OSC OUT	7	

Operation and Applications Information

Figure 1.

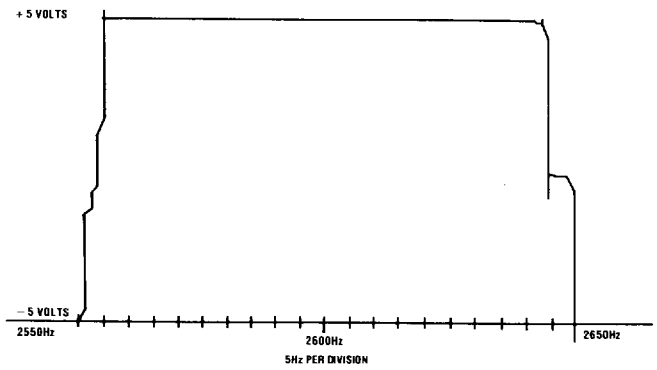

Figure 2. Representative Circuit

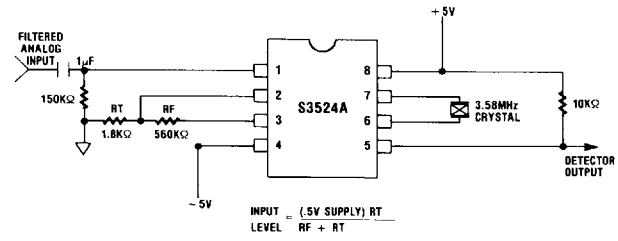

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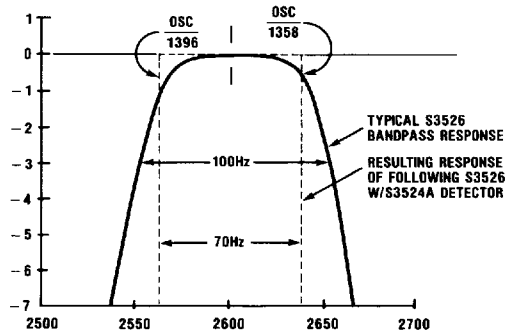
Figure 3. Effective Response of S3526 Bandpass Filter Followed by S3524A Digital Detector



IN SINGLE SUPPLY SITUATION THE GROUND FOR THE SENSITIVITY ADJUSTMENT WOULD BE 1/2 (V_{DD}-V_{SS}) AS DETERMINED BY A REGULATOR OR RESISTIVE VOLTAGE DIVIDER. OFFSET COMPENSATION WOULD BE DONE BY VARYING THE HALF VOLTAGE POINT SLIGHTLY IF DESIRED.

Figure 5. A Typical Detection Bandwidth 2600 for Application Circuit in Figure 4 at 10V

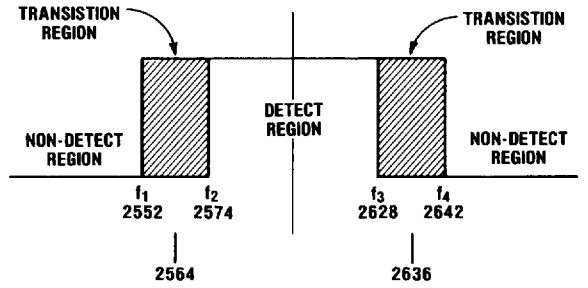


Figure 4. Circuit Example Showing S3526B and S3524A Combined to Provide Narrow Detection Bandwidth