TECHNICAL MANUAL

LSI53C895
PCI to Ultra2 SCSI I/O Processor with LVD Link™ Universal Transceivers

Version 3.2

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This document describes the LSI Logic LSI53C895 PCI to Ultra2 SCSI I/O Processor with LVD Link Universal Transceivers and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This book is the primary reference and technical manual for the LSI53C895 PCI to Ultra2 SCSI I/O Processor with LVD Link™ Universal Transceivers. It contains a complete functional description for the product and includes complete physical and electrical specifications.

This technical manual assumes the user is familiar with the current and proposed standards for SCSI and PCI. For additional background information on these topics, please refer to the list of reference materials provided below.

Audience

This document was prepared for system designers and programmers who are using this device to design an Ultra2 SCSI port for PCI-based personal computers, workstations, servers, or embedded applications.

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction** contains the general description about the LSI53C895.
- Chapter 2, **Functional Description** contains details about the three functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS processor.
- Chapter 3, **PCI Functional Description** contains the PCI bus commands and functions supported.
- Chapter 4, **Signal Descriptions** contains information about the signal definitions using tables and illustrations.

- Chapter 5, **Registers** contains descriptions of the PCI registers and the LSI53C895 operating registers.
- Chapter 6, **SCSI SCRIPTS Instruction Set** contains detailed information about utilizing SCSI SCRIPTS mode.
- Chapter 7, **Electrical Characteristics** contains information pertaining to DC and AC Characteristics for the LSI53C895.
- Appendix A, **Register Summary** contains a quick reference to the registers used for the LSI53C895.
- Appendix B, **External Memory Interface Diagram Examples** contains four diagram examples pertaining to the interface of the external memory.
- Appendix C, **Circuit Board Layout Issues** provides details concerning signals and other considerations specific to the LSI53C895.

Related Publications

For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1994 (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253 *(SCSI-3 Parallel Interface)*

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

LSI Logic World Wide Web Home Page
www.lsilogic.com

SCSI SCRIPTS™ Processors Programming Guide, Version 2.2,
Order number S14044.A

PCI Special Interest Group
PCI Local Bus Specification, Revision 2.1
2575 N.E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
1.0	7/96	Initial release.
2.0	1/97	Added serial EEPROM interface; changed operation of parallel EPROM interface; added information on Ultra2 SCSI termination; added LVD electrical specifications and Ultra2 SCSI timings; added PCI configuration registers for Subsystem ID and Subsystem Vendor ID; pinout/pin numbering corrections.
3.0	9/98	Merged addendum; merged SEN892 (DIFFSENS) in Chapter 2; Chapter 3 - added 292-BGA figure/tables and updated MAD[3:1] signals;Chapter 7 - substituted source and sink values, and changed other values. Merged SEN893 and SEN898 into Appendix D.
3.1	12/99	LSI Logic formats applied. Changes to Chapter 4 regarding PBGA from 292 to 272. Updated Chapter 6, SCSI SCRIPTS with current information.
3.2	12/00	All product names changed from SYM to LSI.

Contents

Figures

Tables

Chapter 1
Introduction

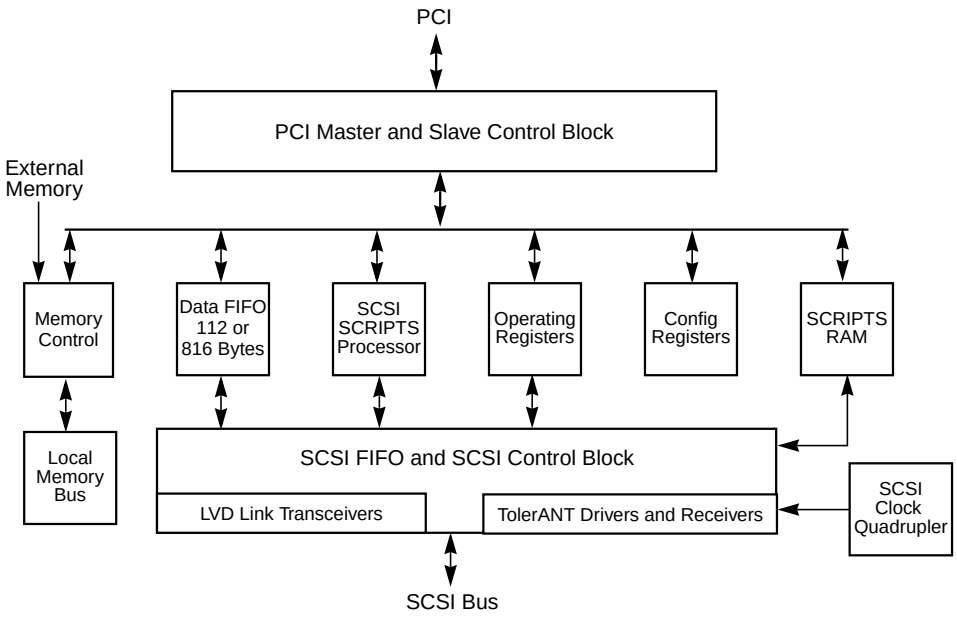
This chapter provides a general overview on the LSI53C895 PCI to Ultra2 SCSI I/O Processor and other members of the LSI53C8XX family of PCI to SCSI I/O Processors. This chapter contains these topics:

1.1 General Description

The LSI53C895 brings Ultra2 SCSI performance to host adapter, workstation, and general computer designs, making it easy to add a high-performance SCSI bus to any PCI system. It supports Ultra2 SCSI transfer rates and allows you to increase SCSI connectivity and cable length with Low Voltage Differential (LVD) signaling for SCSI.

The LSI53C895 has a local memory bus for local storage of the device BIOS ROM in flash memory or standard EEPROMs. The LSI53C895 supports big and little endian byte addressing to accommodate a variety of data configurations. The LSI53C895 supports programming of local flash memory for updates to BIOS or SCRIPTS™ programs. The chip is packaged in a 208-pin quad flat pack or a 272-ball Ball Grid Array (BGA). System diagrams showing the connections of the LSI53C895 with an external ROM or flash memory are pictured in Appendix C. A block diagram of the LSI53C895 is pictured in Figure 1.1 on page 1-2.

Figure 1.1 LSI53C895 Chip Block Diagram



LSI Logic LVD Link™ technology is the LSI Logic implementation of LVD. LVD Link transceivers allow the LSI53C895 to perform Single-Ended (SE) and LVD transfers, and support external High Voltage Differential (HVD) transceivers. The LSI53C895 integrates a high performance SCSI core, a PCI bus master DMA core, and the LSI Logic SCSI SCRIPTS processor to meet the flexibility requirements of SCSI-3 and Ultra2 SCSI standards. It is designed to implement multithreaded I/O algorithms with a minimum of processor intervention, solving the protocol overhead problems of previous intelligent and nonintelligent adapter designs.

1.1.1 New Features in the LSI53C895

The LSI53C895 is functionally similar to the LSI53C875 PCI to SCSI I/O processor, with added support for Ultra2 SCSI. Some software enhancements, and use of LVD, enable the LSI53C895 to transfer data at Ultra2 SCSI transfer rates. Most of the feature enhancements in the LSI53C895 are included to enable the chip to take advantage of Ultra2 SCSI transfer rates.

- Optional 816-byte DMA FIFO supports large block transfers at Ultra2 SCSI speeds. The default FIFO size is 112 bytes.

- Thirty-one levels of SCSI Synchronous Offset increases the pace of synchronous transfers to match Ultra2 SCSI transfer speeds.
- On-chip LVD Link transceivers allow increased connectivity, longer cable length, and improved performance. They also automatically sense the type of device connected to the SCSI bus and switch as needed to SE, LVD, or HVD mode (if the chip is connected to external transceivers).
- On-chip SCSI clock quadrupler can achieve 160 MHz frequency with an external 40 MHz oscillator.
- Supports Subsystem ID and Subsystem Vendor ID registers in PCI configuration space.
- Support for serial EEPROM interface.

1.2 Benefits of LVD Link

The LSI53C895 supports LVD for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than supported by SE SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of HVD SCSI without the added cost of external differential transceivers. Ultra2 SCSI with LVD allows a longer SCSI cable and more devices on the bus, using the same cables defined in the SCSI-3 Parallel Interface standard for Ultra SCSI. LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing SE devices, the LSI53C895 features universal LVD Link transceivers that can switch between LVD and SE SCSI modes. The LVD Link technology also supports high power differential signaling in legacy systems when external transceivers are connected to the LSI53C895. This allows the LSI53C895 to be used in both legacy and Ultra2 SCSI applications.

1.3 Benefits of Ultra2 SCSI

Ultra2 SCSI is an extension of the SPI-2 draft standard that allows faster synchronous SCSI transfer rates and defines a new physical layer, LVD SCSI. LVD SCSI provides an incremental evolution from SCSI-2 and Ultra SCSI. When enabled, Ultra2 SCSI performs 40 megatransfers per second, which results in approximately double the synchronous transfer rates of Ultra SCSI. The LSI53C895 can perform 16 bit, Ultra2 SCSI synchronous transfers as fast as 80 Mbytes/s. This advantage is most noticeable in heavily loaded systems or large-block size applications such as video on-demand and image processing.

One advantage of Ultra2 SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments. The primary software changes enable the chip to perform synchronous negotiations for Ultra2 SCSI rates, and to enable the clock quadrupler. Ultra2 SCSI uses the same connectors as Ultra SCSI, but can operate with longer cables and more devices on the bus. Chapter 2 contains more information on migrating from an Ultra SCSI design to support Ultra2 SCSI.

1.4 TolerANT® Technology

The LSI53C895 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation drives the SCSI Request, Acknowledge, Data, and Parity signals active HIGH rather than allowing them to be passively pulled up by terminators. Active negation is enabled by setting bit 7 in the SCSI Test Three (STEST3) register.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT input signal filtering is a built in feature of the LSI53C895 and all LSI Logic Fast SCSI, Ultra SCSI, and Ultra2 SCSI

devices. On the LSI53C895, the user can select a filtering period of 30 or 60 ns, with bit 1 in the SCSI Test Two (STEST2) register.

The benefits of TolerANT technology include increased immunity to noise when the signal is going HIGH, better performance due to balanced duty cycles, and improved fast SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power up or power down, so other devices on the bus are also protected from data corruption. When it is used with the LVD Link transceivers, TolerANT technology provides excellent signal quality and data reliability in real world cabling environments. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.5 LSI53C895 Benefits Summary

This section provides an overview of the LSI53C895 benefits and features. It includes these topics:

- SCSI Performance
- PCI Performance
- Integration
- Ease of Use
- Flexibility
- Reliability
- Testability

1.5.1 SCSI Performance

To improve SCSI performance, the LSI53C895:

- Has integrated LVD Link universal transceivers which:
  - Support SE, LVD, and HVD signals (with external transceivers)
  - Allow greater device connectivity and longer cable length
  - LVD Link transceivers save the cost of external differential transceivers
  - Support a long-term performance migration path

- Bursts up to 512 bytes across the PCI bus through its 816 byte FIFO
- Performs wide Ultra2 SCSI synchronous transfers as fast as 80 Mbytes/s
- Includes an on-chip SCSI clock quadrupler that allows the chip to achieve Ultra2 SCSI transfer rates with a 40 MHz clock
- Includes 4 Kbytes internal RAM for SCRIPTS instruction storage
- Has 31 levels of SCSI synchronous offset
- Supports variable block size and scatter/gather data transfers.
- Performs sustained memory-to-memory DMA transfers faster than 47 Mbytes/s (@ 33 MHz)
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces Interrupt Service Routine (ISR) overhead through a unique interrupt status reporting method
- Includes Load and Store SCRIPTS instructions to increase performance of data transfers to and from chip registers
- Supports target disconnect and later reconnect with no interrupt to the system processor
- Supports multithreaded I/O algorithms in SCSI SCRIPTS with fast I/O context switching
- Supports expanded register Move instructions for additional arithmetic capability

1.5.2 PCI Performance

To improve PCI performance, the LSI53C895:

- Complies with PCI 2.1 specification
- Supports 32-bit 33 MHz PCI interface
- Bursts 2, 4, 8, 16, 32, 64, or 128 Dwords across the PCI bus
- Supports 32-bit word data bursts with variable burst lengths
- Prefetches up to 8 Dwords of SCRIPTS instructions
- Bursts SCRIPTS op code fetches across the PCI bus

- Performs zero wait-state bus master data bursts faster than 110 Mbytes/s (@ 33 MHz)
- Supports PCI Cache Line Size register
- Supports PCI Write and Invalidate, Read Line, and Read Multiple commands

1.5.3 Integration

The LSI53C895 contains these integration features:

- Integrated LVD transceivers
- Full 32-bit PCI DMA bus master
- Memory to Memory Move instructions to allow use as a third-party PCI bus DMA controller
- High performance SCSI core
- Integrated SCRIPTS processor

1.5.4 Ease of Use

The LSI53C895 provides ease of use by having:

- Up to one megabyte of add-in memory support for BIOS and SCRIPTS storage
- Direct PCI to SCSI connection
- Reduced SCSI development effort
- Compiler-compatible with existing LSI53C7XX and LSI53C8XX family SCRIPTS
- Direct connection to PCI, and SCSI SE and differential buses
- Development tools and sample SCSI SCRIPTS available
- Maskable and pollable interrupts
- Wide SCSI, A or P cable, and up to 16 devices supported
- Three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 25.6 seconds
- Software for PC-based operating system support
- Support for relative jumps
- SCSI selected as ID bits for responding with multiple IDs

1.5.5 Flexibility

The LSI53C895 contains these flexibility features:

- Universal LVD transceivers that are backward compatible with SE or high power differential devices
- High level programming interface (SCSI SCRIPTS)
- Programs local memory bus flash memory
- Big/Little endian support
- Selectable 112 or 816 byte DMA FIFO for backward compatibility
- Tailored SCSI sequences execute from main system RAM or internal SCRIPTS RAM
- Flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Support for changes in the logical I/O interface definition
- Low level access to all registers and all SCSI bus signals
- Fetch, Master, and Memory Access control pins
- Separate SCSI and system clocks
- SCSI clock quadrupler bits enable Ultra2 SCSI transfer rates with a 40 MHz SCSI clock
- Selectable IRQ pin disable bit
- Ability to route system clock to SCSI clock

1.5.6 Reliability

The LSI53C895 contains these reliability features:

- 2 kV ESD protection on SCSI signals
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed through protection (minimum leakage current through SCSI pads)
- More than 25% of pins are power and ground

- Power and ground isolation of I/O pads and internal chip logic
- TolerANT technology provides:
  - Active negation of SCSI data, parity, request, and acknowledge signals for improved fast SCSI transfer rates
  - Input signal filtering on SCSI receivers improves data integrity, even in noisy cabling environments

1.5.7 Testability

The LSI53C895 contains these testability features:

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Support for single-step mode operation
- Test mode (AND tree) to check pin continuity to the board

Chapter 2
Functional Description

This chapter provides information about three functional blocks for the LSI53C895 processor: SCSI core, DMA core, and SCRIPTS processor. Other topics include specific interfaces, modes, and various options. Chapter 2 contains these sections:

Note that LSI Logic supplies software that supports the LSI53C895 and the entire LSI Logic product line of SCSI processors and controllers.

2.1 SCSI Core

The SCSI core supports an 8-bit or 16-bit data bus. It supports Ultra2 SCSI synchronous transfer rates up to 80 Mbytes/s on a 16-bit, LVD SCSI bus. The SCSI core can be programmed with SCSI SCRIPTS, making it easy to “fine tune” the system for specific mass storage devices or SCSI-3 requirements.

The SCSI core offers low-level register access or a high-level control interface. Like first generation SCSI devices, the LSI53C895 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus is useful for error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core could perform a self-selection and operate as both an initiator and a target.

The integrated SCRIPTS processor controls the LSI53C895 SCSI core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory or local memory. These commands instruct the SCSI core to transfer information, change bus phases and, in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

2.2 DMA Core

The DMA core is a bus master DMA device that attaches directly to the industry standard PCI Bus. The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

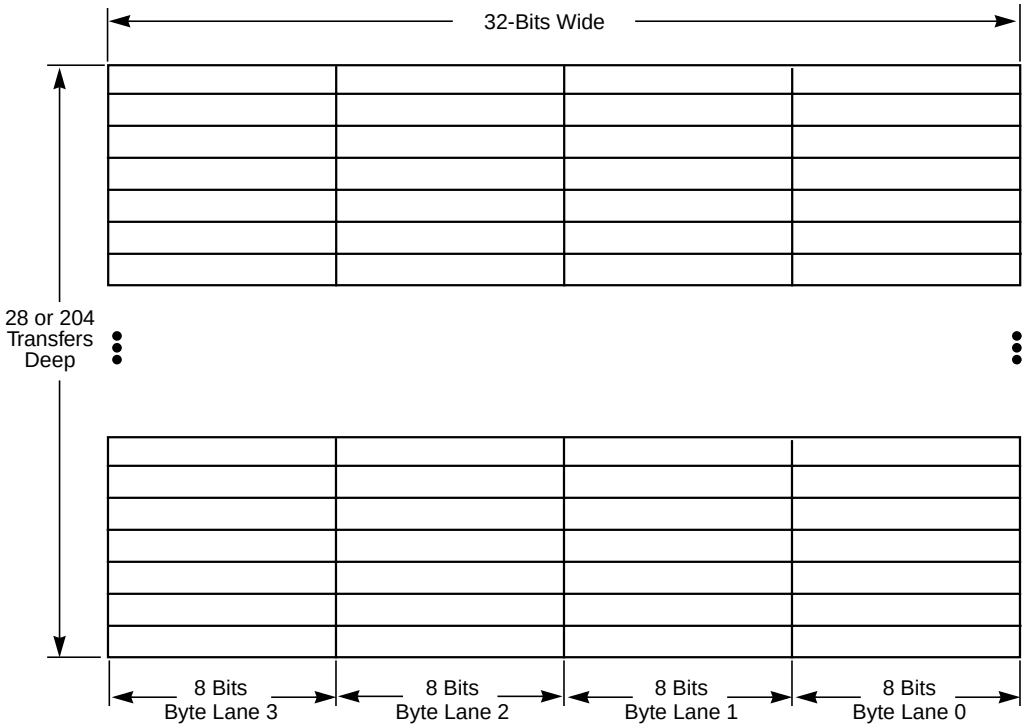
The LSI53C895 supports 32-bit memory and automatically supports misaligned DMA transfers. A 112 or 816 byte FIFO allows the LSI53C895 to support 2, 4, 8, 16, 32, 64, or 128 Dword bursts across the PCI bus interface.

2.2.1 DMA FIFO

The DMA FIFO is 4-bytes wide and 28 or 204 transfers deep. The DMA FIFO is illustrated in Figure 2.1. To assure compatibility with older products in the LSI53C8XX family, the user may set the DMA FIFO size to 112 bytes by clearing the DMA FIFO Size bit, bit 5 in the Chip Test Five (CTEST5) register.

The 816-byte FIFO size is related to the LSI53C895 FIFO architecture. It does not reflect any specific system design parameters or expectations.

Figure 2.1 DMA FIFO Sections



2.2.1.1 Data Paths

The data path through the LSI53C895 is dependent on whether data is being moved into or out of the chip. It also depends on whether SCSI data is being transferred asynchronously or synchronously.

Figure 2.2 shows how data is moved to/from the SCSI bus in each of the different modes. To determine if any bytes remain in the data path when the chip halts an operation, follow the detailed instructions in the next sections.

Asynchronous SCSI Send – Follow these steps for asynchronous SCSI send operations:

Step 1. To calculate DMA FIFO size:

If the DMA FIFO size is set to 112 bytes, look at the DMA FIFO (DFIFO) and DMA Byte Counter (DBC) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F for a byte count between zero and 112.

If the DMA FIFO size is set to 816 bytes (using bit 5 of the Chip Test Five (CTEST5) register), subtract the 10 least significant bits of the DMA Byte Counter (DBC) register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits [1:0] in the Chip Test Five (CTEST5) register and bits [7:0] of the DMA FIFO (DFIFO) register. AND the result with 0x3FF for a byte count between zero and 816.

Step 2. To determine if any bytes are left in the SCSI Output Data Latch (SODL) register, read bit 5 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers.

If bit 5 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SCSI Output Data Latch (SODL) register is full, respectively. Checking this bit also reveals bytes left in the SCSI Output Data Latch (SODL) register from a Chained Move operation with an odd byte count.

Synchronous SCSI Send – Follow these steps for synchronous SCSI send:

Step 1. To calculate DMA FIFO size:

If the DMA FIFO size is set to 112 bytes, look at the DMA FIFO (DFIFO) and DMA Byte Counter (DBC) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation,

subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F for a byte count between zero and 112.

If the DMA FIFO size is set to 816 bytes (using bit 5 of the Chip Test Five (CTEST5) register), subtract the 10 least significant bits of the DMA Byte Counter (DBC) register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits [1:0] in the Chip Test Five (CTEST5) register and bits [7:0] of the DMA FIFO (DFIFO) register. AND the result with 0x3FF for a byte count between zero and 816.

Step 2. To determine if any bytes are left in the SCSI Output Data Latch (SODL) register, read bit 5 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers.

If bit 5 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SCSI Output Data Latch (SODL) register is full, respectively. Checking this bit also reveals bytes left in the SCSI Output Data Latch (SODL) register from a Chained Move operation with an odd byte count.

Step 3. To determine if any bytes are left in the SODR register (a hidden buffer register which is not accessible), read bit 6 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) registers.

If bit 6 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte in the SODR register is full.

Asynchronous SCSI Receive – Follow these steps for asynchronous SCSI receive:

Step 1. To calculate DMA FIFO size:

If the DMA FIFO size is set to 112 bytes, look at the DMA FIFO (DFIFO) and DMA Byte Counter (DBC) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F for a byte count between zero and 112.

If the DMA FIFO size is set to 816 bytes (using bit 5 of the Chip Test Five (CTEST5) register), subtract the 10 least significant bits of the DMA Byte Counter (DBC) register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits [1:0] in the Chip Test Five (CTEST5) register and bits [7:0] of the DMA FIFO (DFIFO) register. AND the result with 0x3FF for a byte count between zero and 816.

Step 2. To determine if any bytes are left in the SCSI Input Data Latch (SIDL) register, read bit 7 in the SCSI Status Zero (SSTAT0) and SCSI Status Two (SSTAT2) register. If bit 7 is set in the SCSI Status Zero (SSTAT0) or SCSI Status Two (SSTAT2), then the least significant byte or the most significant byte is full.

Step 3. To determine whether a byte is left in the SCSI Wide Residue (SWIDE) register, read the Wide SCSI Receive bit (SCSI Control Two (SCNTL2), bit 0) Synchronous SCSI Receive.

This applies toward any wide transfers that have been performed using the Chained Move instruction.

Follow these steps for synchronous SCSI receive:

Step 1. To calculate DMA FIFO size:

If the DMA FIFO size is set to 112 bytes, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register. AND the result with 0x7F for a byte count between zero and 112.

If the DMA FIFO size is set to 816 bytes (using bit 5 of the Chip Test Five (CTEST5) register), subtract the 10 least significant bits of the DMA Byte Counter (DBC) register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits [1:0] in the Chip Test Five (CTEST5) register and bits [7:0] of the DMA FIFO (DFIFO) register. AND the result with 0x3FF for a byte count between zero and 816.

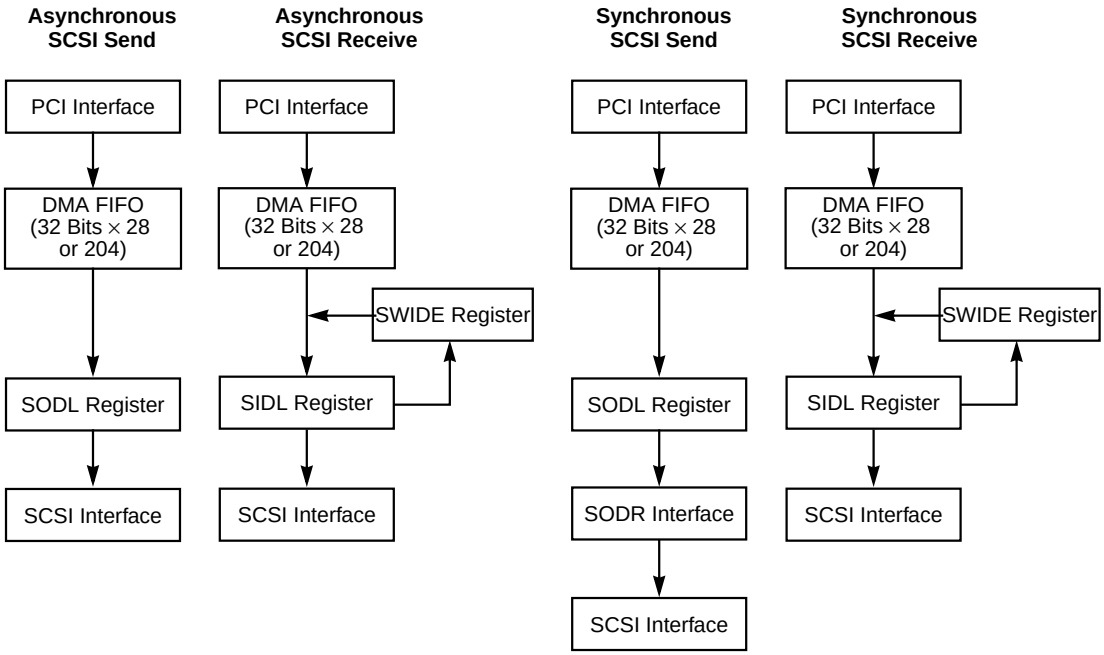
Step 2. Read bits [7:4] of the SCSI Status One (SSTAT1) register and bit 4 of the SCSI Status Two (SSTAT2) register, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Step 3. To determine whether a byte is left in the SCSI Wide Residue (SWIDE) register, read the Wide SCSI Receive bit (SCSI

Control Two (SCNTL2), bit 0) LSI53C895 Host Interface Data Paths.

This applies toward any wide transfers that have been performed using the Chained Move instruction.

Figure 2.2 LSI53C895 Host Interface SCSI Datapath



2.3 SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI commands to be fetched from host memory or internal SCRIPTS RAM. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores and are executed from 32-bit system RAM or internal SCRIPTS RAM. The SCRIPTS processor executes complex SCSI bus sequences independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. Algorithms may be designed to tune SCSI bus performance to adjust to new bus device types (such as scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2

or SCSI-3 logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are hardware independent, so they can be used interchangeably on any host or CPU system bus.

2.3.1 Internal SCRIPTS RAM

The LSI53C895 has 4 Kbytes (1024 x 32 bits) of internal, general purpose RAM. The RAM is designed for SCRIPTS program storage, but is not limited to this type of information. When the chip fetches SCRIPTS instructions or Table Indirect information from the internal RAM, these fetches remain internal to the chip and do not use the PCI bus. Other types of access to the RAM by the LSI53C895 use the PCI bus as if they were external accesses. The MAD5 pin enables the 4 Kbytes internal RAM, when it is connected to V_{DD} through a 4.7 KΩ resistor. To disable the internal RAM, connect a 4.7 KΩ resistor between the MAD5 pin and V_{SS}.

The PCI system BIOS can relocate the RAM anywhere in a 32-bit address space. The RAM Base Address register in PCI configuration space contains the base address of the internal RAM. This register is similar to the ROM Base Address register in PCI configuration space. To simplify loading of SCRIPTS instructions, the base address of the RAM appears in the Scratch Register B (SCRATCHB) register when bit 3 of the Chip Test Two (CTEST2) register is set. The RAM is byte-accessible from the PCI bus and is visible to any bus-mastering device on the bus. External accesses to the RAM (that is, by the CPU) follow the same timing sequence as a standard slave register access, except that the target wait-states required drops from 5 to 3.

A complete set of development tools is available for writing custom drivers with SCSI SCRIPTS. For more information on the SCSI SCRIPTS instructions supported by the LSI53C895, see Chapter 6, “SCSI SCRIPTS Instruction Set.”

2.4 Prefetching SCRIPTS Instructions

To enable the prefetch logic, set the Prefetch Enable bit in the DMA Control (DCNTL) register. After doing so, the prefetch logic in the LSI53C895 fetches 8 Dwords of instructions. The prefetch logic automatically determines the maximum burst size that it can perform,

based on the burst length as determined by the values in the DMA Mode (DMODE) register. If the burst size is less than four Dwords, the LSI53C895 performs normal instruction fetches. While the LSI53C895 is prefetching SCRIPTS instructions, the PCI Cache Line Size register value does not have any effect and the Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate commands are not used.

The LSI53C895 may flush the contents of the prefetch buffer under certain conditions, listed below, to ensure that the chip always operates from the most current version of the software. When one of these conditions apply, the contents of the prefetch buffer are flushed automatically.

1. On every Memory Move instruction.

   The Memory Move instruction is often used to place modified code directly into memory. To make sure that the chip executes all recent modifications, the prefetch buffer flushes its contents and loads the modified code every time an instruction is issued. To avoid inadvertently flushing the prefetch buffer contents, use the No Flush option for all Memory Move operations that do not modify code within the next 8 Dwords. For more information on this instruction, refer to Chapter 6.

2. On every Store instruction.

   The Store instruction may also be used to place modified code directly into memory. To avoid inadvertently flushing the prefetch buffer contents, use the No Flush option for all Store operations that do not modify code within the next 8 Dwords.

3. On every write to the DSP.

4. On all Transfer Control instructions.

   When the transfer conditions are met, the prefetch buffer is flushed. This is necessary because the next instruction to be executed is not the sequential next instruction in the prefetch buffer.

5. Prefetch Flush bit (DMA Control (DCNTL), bit 6) is set.

   The buffer flushes whenever this bit is set. The bit is self-clearing.

2.4.1 Op Code Fetch Burst Capability

Setting the Burst Op Code Fetch Enable bit in the DMA Mode (DMODE) register (0x38) causes the LSI53C895 to burst in the first two Dwords of all instruction fetches. If the instruction is a Memory to Memory move, the third Dword is accessed in a separate ownership. If the instruction is an indirect type, the additional Dword is accessed in a subsequent bus ownership. If the instruction is a table indirect block move, the LSI53C895 uses two accesses to obtain the four Dwords required, in two bursts of two Dwords each.

Note: This feature only works if prefetching is disabled.

2.5 Designing an Ultra2 SCSI System

Since Ultra2 SCSI is based on existing SCSI standards, it can use existing driver programs as long as the software is able to negotiate for Ultra2 SCSI synchronous transfer rates. Additional software modifications may be needed to take advantage of the new features in the LSI53C895.

In the area of hardware, LVD SCSI is required to achieve Ultra2 SCSI transfer rates and to support the longer cable and additional devices on the bus. All devices on the bus must have LVD SCSI to guarantee Ultra2 SCSI transfer rates. Chapter 7, “Electrical Characteristics,” contains Ultra2 SCSI timing information. In addition to the guidelines in the draft standard, make the following software and hardware adjustments to accommodate Ultra2 SCSI transfers:

Step 1. Set the Ultra Enable bit, bit 7 in the SCSI Contr0l Three (SCNTL3) register, to enable Ultra2 SCSI transfers.

Step 2. Set the TolerANT Enable bit, bit 7 in the SCSI Test Three (STEST3) register, whenever the Ultra Enable bit is set.

Step 3. Do not extend the SREQ/SACK filtering period with SCSI Test Two (STEST2), bit 1. When the Ultra Enable bit is set, the filtering period is fixed at 8 ns for Ultra2 SCSI or 15 ns for Ultra SCSI, regardless of the value of the SREQ/SACK Filtering bit.

Step 4. Use the SCSI clock quadrupler.

2.5.1 Using the SCSI Clock Quadrupler

The LSI53C895 can quadruple the frequency of a 40 MHz SCSI clock, allowing the system to perform Ultra2 SCSI transfers. This option is user-selectable with bit settings in the SCSI Test One (STEST1), SCSI Test Three (STEST3), and SCSI Contr0l Three (SCNTL3) registers. At power-on or reset, the quadrupler is disabled and powered down. Follow these steps to use the clock quadrupler:

Step 1. Set the SCLK Quadrupler Enable bit (SCSI Test One (STEST1), bit 3).

Step 2. Poll bit 5 of the SCSI Test 4 (STEST4) register. The LSI53C895 sets this bit as soon as it locks in the 160 MHz frequency. The frequency lockup takes approximately 100 microseconds.

Step 3. Halt the SCSI clock by setting the Halt SCSI Clock bit (SCSI Test Three (STEST3), bit 5).

Step 4. Set the clock conversion factor using the SCF (bits [6:4]) and CCF (bits [2:0]) fields in the SCSI Contr0l Three (SCNTL3) register.

Step 5. Set the SCLK Quadrupler Select bit (SCSI Test One (STEST1), bit 2).

Step 6. Clear the Halt SCSI Clock bit (SCSI Test Three (STEST3), bit 5).

2.6 LSI53C895 Interfaces

This section contains information about:

- Parallel ROM Interfaces
- Serial EEPROM Interfaces
- SCSI Bus Interfaces

2.6.1 Parallel ROM Interface

The LSI53C895 supports up to one megabyte of external memory in binary increments from 16 Kbytes, to allow the use of expansion ROM for add-in PCI cards. The device also supports flash ROM updates through the add-in interface and the GPIO4 pin (used to control V_{PP}

which is the power supply for programming external memory). This interface is designed for low-speed operations such as downloading instruction code from ROM; it is not intended for dynamic activities such as executing instructions.

System requirements include the LSI53C895, two or three external 8-bit address holding registers (HCT273 or HCT374), and the appropriate memory device. The 4.7 KΩ resistors on the Memory Address/Data (MAD) bus require use of HC or HCT external components. If in-system flash ROM updates are required, a 7406 inverter (high voltage open collector inverter), an MTD4P05, and several passive components are also needed. The memory size and speed is determined by pull-up/pull-down configuration on the 8-bit bidirectional memory bus at power up. The LSI53C895 senses this bus shortly after the release of the Reset signal and configures the ROM Base Address register and the memory cycle state machines for the appropriate conditions.

The LSI53C895 supports a variety of sizes and speeds of expansion ROM, using pull-up and pull-down resistors on the MAD[3:0]) pins. Pins MAD[3:1] allow the user to define how much external memory is available to the LSI53C895. Table 2.1 shows the memory space associated with the possible values of MAD[3:1]. The MAD[3:1] pins are fully defined in Chapter 4, "Signal Descriptions." Appendix C, "Circuit Board Layout Issues," shows an example set of interface drawings.

Table 2.1 External Memory Support

MAD[3:1]	Available Memory Space
0b000	16 Kbytes
0b001	32 Kbytes
0b010	64 Kbytes
0b011	128 Kbytes
0b100	256 Kbytes
0b101	512 Kbytes
0b110	1024 Kbytes
0b111	No external memory present

To use one of the configurations mentioned above in a host adapter board design, put 4.7 KΩ pull-up and pull-down resistors on the appropriate MAD pins, corresponding to the available memory space. For example, to connect to a 32 Kbytes external ROM, use pull-downs on MAD(3) and MAD(2) and a pull-up on MAD(1).

Note: The LSI53C875 contains internal pull-ups on the MAD bus. The LSI53C895 requires external resistors to pull up the MAD bus to V_{DD}.

The LSI53C895 allows the system to determine the size of the available external memory using the Expansion ROM Base Address register in the PCI configuration space. For more information on how this works, refer to the PCI specification or the Expansion ROM Base Address register description in Chapter 5, "Registers."

MAD(0) is the slow ROM pin. When pulled down, it enables two extra clock cycles of data access time, which allows use of slower memory devices.

The external memory interface also supports updates to flash memory. The 12-volt power supply for flash memory, V_{PP}, is enabled and disabled with the GPIO4 pin and the GPIO4 control bit. For more information on the GPIO4 pin, refer to Chapter 4, "Signal Descriptions."

2.6.2 Serial EEPROM Interface

The LSI53C895 implements an interface that allows attachment of a serial EEPROM device to the GPIO0 and GPIO1 pins. Four different modes of operation are possible; each one relates to different values for the serial EEPROM interface, the Subsystem ID register, and the Subsystem Vendor ID register. The modes are programmable through the MAD6 and MAD7 pins, which are sampled at power-up or hard reset.

2.6.2.1 Mode A: 4.7 KΩ Pull-ups on MAD6 and MAD7

In this mode, GPIO0 is the Serial Data Signal (SDA) and GPIO1 is the Serial Clock Signal (SCL). Certain data in the serial EEPROM is automatically loaded into chip registers at power-up or hard reset.

The format of the serial EEPROM data is defined in Table 2.2. If the EEPROM is not present, or the checksum fails, the Subsystem ID and Subsystem Vendor ID registers read back all zeros. At power-up or hard reset, only five bytes are loaded into the chip from locations 0x00 through 0x04.

Table 2.2 Mode A Serial EEPROM Data Format

Byte	Description
0x00	Subsystem Vendor ID, LSB. This byte is loaded into the least significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
0x01	Subsystem Vendor ID, MSB. This byte is loaded into the most significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
0x02	Subsystem ID, LSB. This byte is loaded into the least significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
0x03	Subsystem ID, MSB. This byte is loaded into the most significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
0x04	Checksum. This 8-bit checksum is formed by adding, bytewise, each byte contained in locations 0x00–0x03 to the seed value 0x55, and then taking the 2's complement of the result.
0x05–0xFF	Reserved.
0x100–EOM	Contains user data.

2.6.2.2 Mode B: 4.7 KΩ Pull-down on MAD6, and 4.7 KΩ Pull-up on MAD7

In this mode, GPIO0 and GPIO1 are each defined as either the SDA or the SCL, since both pins are controlled through software.

No data is automatically loaded into chip registers at power-up or hard reset. The Subsystem ID register and Subsystem Vendor ID registers are read/write, in violation of the PCI specification, with a default value of all zeros.

2.6.2.3 Mode C: 4.7 KΩ Pull-downs on MAD6 and MAD7

In this mode, GPIO1 is the SDA and GPIO0 is the SCL. Certain data in the serial EEPROM is automatically loaded into chip registers at power-up or hard reset.

The format of the serial EEPROM data is defined in Table 2.3. If the EEPROM is not present, or the checksum fails, the Subsystem ID and Subsystem Vendor ID registers read back all zeros. At power-up or hard

reset, only five bytes are loaded into the chip from locations 0xFB through 0xFF.

Table 2.3 Mode C Serial EEPROM Data Format

Byte	Description
0x00–0xFA	Contains user data.
0xFB	Subsystem Vendor ID, LSB. This byte is loaded into the least significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
0xFC	Subsystem Vendor ID, MSB. This byte is loaded into the most significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
0xFD	Subsystem ID, LSB. This byte is loaded into the least significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
0xFE	Subsystem ID, MSB. This byte is loaded into the most significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
0xFF	Checksum. This 8-bit checksum is formed by adding, bytewise, each byte contained in locations 0xFB–0xFE to the seed value 0x55, and then taking the 2's complement of the result.
0x100–EOM	Contains user data.

2.6.2.4 Mode D: 4.7 KΩ Pull-up on MAD6, and 4.7 KΩ Pull-down on MAD7

This is a reserved mode and should not be used.

2.6.3 SCSI Bus Interface

The LSI53C895 performs SE and LVD transfers, and supports traditional (high power) differential operation when the chip is connected to external high power differential transceivers.

To support LVD SCSI, all SCSI data and control signals have a positive and a negative signal line, as in HVD. In SE and HVD operation, the negative signals perform the SCSI data and control function. In HVD mode, the positive signals provide directional control and in SE mode they are virtual ground drivers. TolerANT technology provides signal

filtering at the inputs of SREQ/ and SACK/ to increase immunity to signal reflections.

2.6.3.1 LVD Link Technology

To support greater device connectivity and a longer SCSI cable, the LSI53C895 features LVD Link technology, which is the LSI Logic implementation of LVD SCSI. LVD Link transceivers provide the inherent reliability of differential SCSI and a long-term migration path of faster SCSI transfer rates.

LVD Link technology is based on current drive; its low output current reduces the power needed to drive the SCSI bus, so that the I/O drivers can be integrated directly onto the chip. This reduces the cost and complexity compared to traditional (high power) differential designs. LVD Link lowers the amplitude of noise reflections and allows higher transmission frequencies.

The LSI Logic LVD Link transceivers operate in LVD and SE modes. They allow the chip to detect a HVD signal when the chip is connected to external HVD transceivers. The LSI53C895 automatically detects which type of signal is connected, based on voltage detected by the DIFFSENS pin. Bits 7 and 6 of the SCSI Test 4 (STEST4) register contain the encoded value for the type of signal that is detected (LVD, SE, or HVD). Refer to the SCSI Test 4 (STEST4) register description for encoding and other bit information.

2.6.3.2 HVD Mode

To maintain backward compatibility with legacy systems, the LSI53C895 can operate in HVD Mode (when the chip is connected to external differential transceivers). In HVD mode, the SD+ [15:0], SDP+ [1:0], REQ+, ACK+, RST+, BSY+, and SEL+ signals control the direction of external differential pair transceivers. The LSI53C895 is placed in differential mode by setting the DIF bit, bit 5 of the STEST2 register (0x4E). Setting this bit 3-states the BSY–, SEL–, and RST– pads so they can be used as pure input pins. In addition to the standard SCSI lines, the LSI53C895 uses these signals during HVD operation as shown in Table 2.4:

Table 2.4 HVD Operation

Signal	Function
BSY+, SEL+, RST+	Active HIGH signals used to enable the differential drivers as outputs for SCSI signals BSY–, SEL–, and RST–, respectively
SD+[15:0], SDP+[1:0]	Active HIGH signals used to control direction of the differential drivers for SCSI data and parity lines, respectively
ACK+	Active HIGH signal used to control direction of the differential driver for initiator group signals ATN– and ACK–
REQ+	Active HIGH signal used to control direction of the differential drivers for target group signals MSG–, C/D–, I/O–, and REQ/–
DIFFSENS	Input to the LSI53C895 used to detect the voltage level of a SCSI signal to determine whether it is a SE, LVD, or HVD signal. The result is displayed in SCSI Test 4 (STEST4), bits [7:6].

In the differential wiring diagram example shown in Figure 2.7, the LSI53C895 is connected to the TI SN75976A2 differential transceiver for Ultra SCSI operation. The recommended value of the pull-up resistor on the REQ–, ACK–, MSG–, C/D–, I/O–, ATN–, SD[7:0]–, and SDP0– lines is 680 Ω when the Active Negation portion of LSI Logic TolerANT technology is not enabled. When TolerANT is enabled, the recommended resistor value on the REQ–, ACK–, SD[7:0]–, and SDP0– signals is 1.5 KΩ. The electrical characteristics of these pins change when TolerANT is enabled, permitting a higher resistor value.

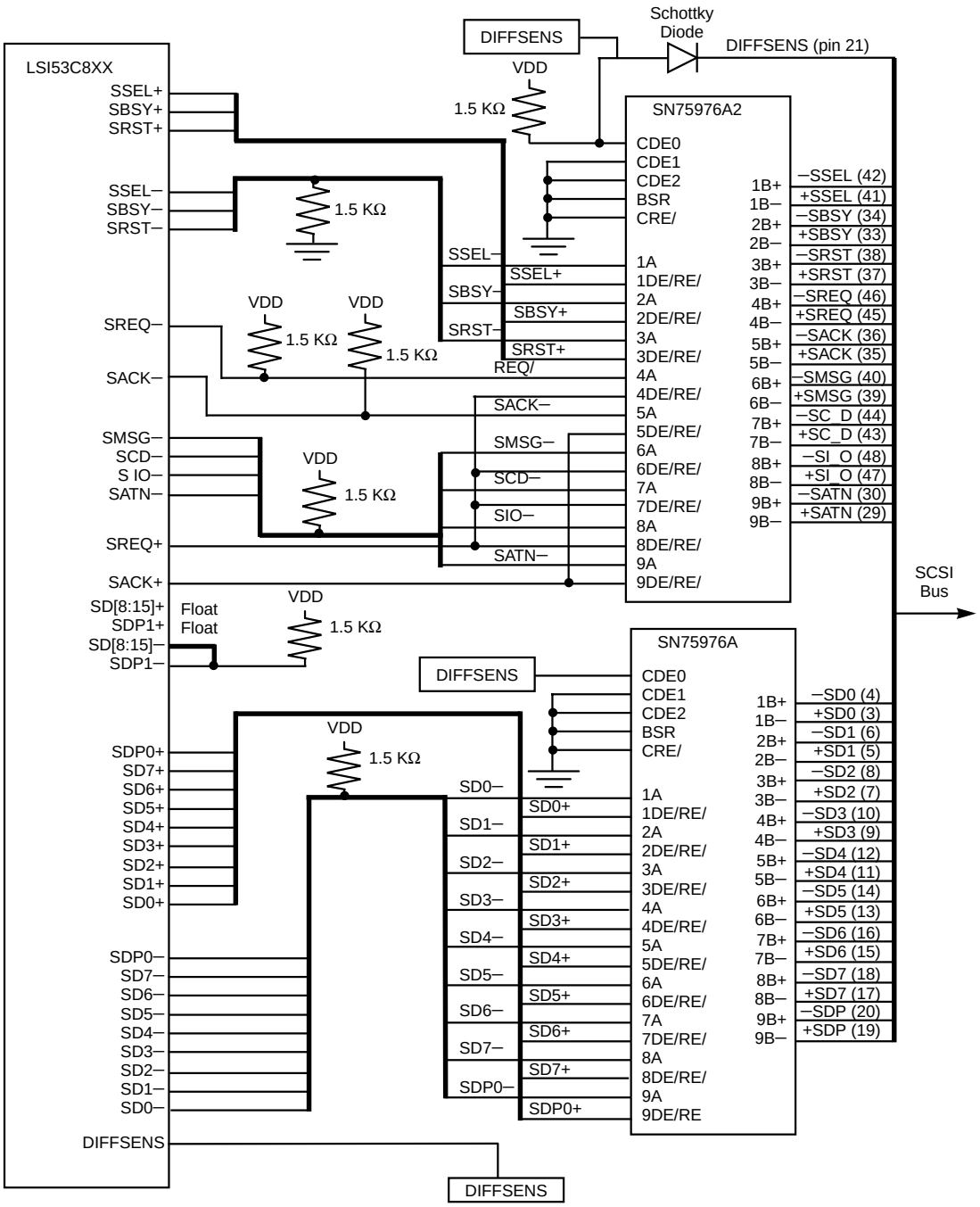
To interface the LSI53C895 to the SN75976A2, connect the positive pins in the SCSI LVD pair of the LSI53C895 directly to the transceiver enables (nDE/RE/). These signals control the direction of the channels on the SN75976A2.

The SCSI bidirectional control and data pins (SD[7:0]– SDP0–, REQ–, ACK–, MSG–, I_O–, C_D–, and ATN–) of the LSI53C895 connect to the bidirectional data pins (nA) of the SN75976A2 with a pull-up resistor. The pull-up value should be no lower than the transceiver I_{OL} can tolerate, but not so high as to cause RC timing problems. The three remaining pins, SEL–, BSY–, and RST–, are connected to the SN75976A2 with a

pull-down resistor. The pull-down resistors are required when the pins (nA) of the SN75976A2 are configured as inputs. When the data pins are inputs, the resistors provide a bias voltage to both the LSI53C895 pins (SEL–, BSY–, and RST–) and the SN75976A2 data pins. Because the SEL–, BSY–, and RST– pins on the LSI53C895 are inputs only, this configuration allows for the SEL–, BSY–, and RST– SCSI signals to be asserted on the SCSI bus. The differential pairs on the SCSI bus are reversed when connected to the SN75976A2, due to the active low nature of the SCSI bus.

8-Bit/16-Bit SCSI and the HVD Interface – In an 8-bit SCSI bus, the SD[15:8] pins on the LSI53C895 should be pulled up with a 1.5 KΩ resistor or terminated like the rest of the SCSI bus lines. This is very important, as errors may occur during reselection if these lines are left floating.

Figure 2.3 8-Bit HVD Wiring Diagram for Ultra2 SCSI



2.7 LSI53C895 Modes

This section provides information about:

- PCI Cache Mode
- Big and Little Endian Modes
- Loopback Mode

2.7.1 PCI Cache Mode

The LSI53C895 supports the PCI specification for an 8-bit Cache Line Size register located in PCI configuration space. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. In conjunction with the Cache Line Size register, the PCI commands Read Line, Read Multiple, and Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands. For more information on PCI cache mode operations, refer to Chapter 3, “PCI Functional Description.”

2.7.2 Big and Little Endian Modes

The LSI53C895 supports both big and little endian byte ordering through pin selection. In big endian mode, the first byte of an aligned SCSI to PCI transfer is routed to lane three and successive transfers are routed to descending lanes. This mode of operation also applies to data transfers over the add-in ROM interface. The byte of data accessed at memory location 0x0000 is routed to lane three, and the data at location 0x0003 is routed to byte lane 0. In little endian mode, the first byte of an aligned SCSI to PCI transfer is routed to lane zero and successive transfers are routed to ascending lanes. This mode of operation also applies to the add-in ROM interface. The byte of data accessed at memory location 0x0000 is routed to lane zero, and the data at memory location 0x0003 is routed to byte lane 3.

The BIG_LIT pin gives the LSI53C895 the flexibility of operating with either big or little endian byte orientation. Internally, in either mode, the actual byte lanes of the DMA FIFO and registers are not modified. The LSI53C895 supports slave accesses in big or little endian mode.

When a Dword is accessed, no repositioning of the individual bytes is necessary since Dwords are addressed by the address of the least significant byte. SCRIPTS always uses Dwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When less than a Dword is accessed, individual bytes must be repositioned. Internally, the LSI53C895 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lanes. The registers always appear on the same byte lane, but the address of the register is repositioned.

Big and little endian mode selection has the most effect on individual byte access. Internally, the LSI53C895 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane. The registers always appear on the same byte lane, but the address of the register is repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address ‘n’. No byte ordering exists in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc. The only difference is that in a little endian system, address 0 is on byte lane 0, and in big endian mode address 0 is on byte lane 3.

Correct SCRIPTS are generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instruction with the byte ordering that the SCRIPTS processor expects.

Software drivers for the LSI53C895 should access registers by their logical name (that is, SCNTL0) rather than by their address. The logical name should be equated to the register big endian address in big endian mode (SCNTL0 = 0x03), and its little endian address in little endian mode (SCNTL0 = 0x00). In this way, no change occurs to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed.

Addressing of registers from within a SCRIPTS instruction is independent of bus mode. Internally, the LSI53C895 always operates in little endian mode.

2.7.3 Loopback Mode

The LSI53C895 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip communicate with itself. When the Loopback Enable bit is set in the SCSI Test One (STEST1) register, the LSI53C895 allows control of all SCSI signals, whether the LSI53C895 is operating in initiator or target mode. For more information on this mode of operation, refer to the *SCSI SCRIPTS Processors Programming Guide*.

2.8 Parity Options

The LSI53C895 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. Table 2.5 defines the bits that are involved in parity control and observation. Table 2.6 describes the parity control function of the Enable Parity Checking and Assert SCSI Even Parity bits in the SCSI Control Zero (SCNTL0) register. Table 2.7 describes the options available when a parity error occurs.

Table 2.5 Bits Used for Parity Control and Generation

BIt Name	Location	Description
Assert SATN/ on Parity Errors	SCSI Control Zero (SCNTL0), Bit 1	Causes the LSI53C895 to automatically assert SATN/ when it detects a parity error while operating as an initiator.
Enable Parity Checking	SCSI Control Zero (SCNTL0), Bit 3	Enables the LSI53C895 to check for parity errors. The LSI53C895 checks for odd parity.
Assert Even SCSI Parity	SCSI Control One (SCNTL1), Bit 2	Determines the SCSI parity sense generated by the LSI53C895 to the SCSI bus.
Disable Halt on SATN/ or a Parity Error (Target Mode Only)	SCSI Control One (SCNTL1), Bit 5	Causes the LSI53C895 not to halt operations when a parity error is detected in target mode.
Enable Parity Error Interrupt	SCSI Interrupt Enable Zero (SIEN0), Bit 0	Determines whether the LSI53C895 generates an interrupt when it detects a SCSI parity error.
Parity Error	SCSI Interrupt Status Zero (SIST0), Bit 0	This status bit is set whenever the LSI53C895 has detected a parity error on the SCSI bus.

Table 2.5 Bits Used for Parity Control and Generation (Cont.)

BIt Name	Location	Description
Status of SCSI Parity Signal	SCSI Status Zero (SSTAT0), Bit 0	This status bit represents the active HIGH current state of the SCSI SDP0 parity signal.
SCSI SDP1 Signal	SCSI Status Two (SSTAT2), Bit 0	This bit represents the active HIGH current state of the SCSI SDP1 parity signal.
Latched SCSI Parity	SCSI Status Two (SSTAT2), Bit 3 SCSI Status One (SSTAT1), Bit 3	These bits reflect the SCSI odd parity signal corresponding to the data latched into the SCSI Input Data Latch (SIDL) register.
Master Parity Error Enable	Chip Test Four (CTEST4), Bit 3	Enables parity checking during master data phases.
Master Data Parity Error	DMA Status (DSTAT), Bit 6	Set when the LSI53C895 as a master detects that a target device has signaled a parity error during a data phase.
Master Data Parity Error Interrupt Enable	DMA Interrupt Enable (DIEN), Bit 6	By clearing this bit, a Master Data Parity Error does not cause IRQ/ to be asserted, but the status bit is set in the DMA Status (DSTAT) register.
Enable Parity Error Response	Command, Bit 6	Parity checking and parity error reporting are enabled on the PCI bus.

Table 2.6 SCSI Parity Control

EPC[1]	AESP[1]	Description
0	0	Does not check for parity errors. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
0	1	Does not check for parity errors. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.
1[2]	0	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
1	1	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.

1. Key:
   EPC = Enable Parity Checking (bit 3 SCSI Control Zero (SCNTL0)).
   ASEP = Assert SCSI Even Parity (bit 2 SCSI Control One (SCNTL1)).
2. This table only applies when the Enable Parity Checking bit is set.

Table 2.7 SCSI Parity Errors and Interrupts

DHP[1]	PAR	Description
0	0	Halts when a parity error occurs in target or initiator mode and does *not* generate an interrupt.
0	1	Halts when a parity error occurs in target mode and generates an interrupt in target or initiator mode.
1	0	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is not generated.
1	1	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is generated.

1. Key: DHP = Disable Halt on SATN/ or Parity Error (bit 5 SCSI Control One (SCNTL1)).
PAR = Parity Error (bit 0 SCSI Interrupt Enable Zero (SIEN0)).

2.8.1 SCSI Termination

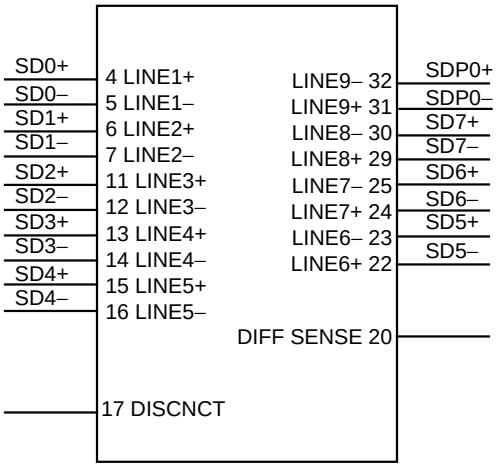
The terminator networks provide the biasing needed to pull signals to an inactive voltage level. They also match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of the SCSI chain, and only at the ends. No system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they can be removed, or there should be a means of disabling them with software.

SE cables can use a 220 Ω pull-up to the terminator power supply (Term-Power) line and a 330 Ω pull-down to ground. Due to the high-performance nature of the LSI53C895, Regulated (or Active) termination is recommended. Figure 2.4 shows a Unitrode active terminator. For additional information, refer to the SCSI-2 Specification. TolerANT active negation can be used with either termination network.

For information on terminators that support LVD, refer to the SPI-2 draft standard.

Note: When using the LSI53C895 in a design with an 8-bit SCSI bus, all 16 data lines still must be terminated or pulled HIGH.

Figure 2.4 Regulated Termination for Ultra2 SCSI



- DIFF SENSE connects to the SCSI bus DIFFsense line to detect what type of devices (SE, LVD, or HVD) are connected to the SCSI bus.
- DSCNCT shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.
- Use additional UCC6350 terminators to connect signals and additional wide SCSI data bytes as needed.

2.8.2 System Engineering Note

In the LSI53C895, transmission mode detection for SE, HVD, and LVD is implemented by using the DIFFSENS line. Table 2.8 shows the corresponding voltages and what mode they indicate.

Table 2.8 Transmission Mode

Mode	SE	LVD	HVD
Voltage	–0.35 to +0.5	0.7 to 1.9	2.4 to 5.5

The SCSI Parallel Interface 2 Specification Revision 1.1 (SPI-2) has timing specific mode requirements that state a bus mode change must be sensed for at least a continuous 100 ms to be valid. The signal drivers should remain in a high impedance state at power-up until the device is capable of full logical operation for at least 100 ms. The bus mode detected by the DIFFSENS line has remained stable for at least another 100 ms after that. In order to achieve the sufficient 100 ms delay required by the standard, follow these steps when a mode change is detected.

At power-up:

Step 1. Set bit 3 in SCSI Test Two (STEST2) (register 0x4E), to place the SCSI drivers in a high impedance state.

Step 2. Enable the SCSI Bus Mode Change (SBMC) interrupt by setting bit 4 in SCSI Interrupt Enable One (SIEN1) (register 0x41).

Step 3. If a SCSI bus mode change is detected, then SCSI Interrupt Status One (SIST1) (register 0x43), bit 4 indicates a SBMC interrupt.

Step 4. Clear the interrupt by reading SCSI Interrupt Status Zero (SIST0) (register 0x42) and SCSI Interrupt Status One (SIST1).

Step 5. Wait 100 ms.

Step 6. Check that no more SBMC interrupts have occurred.

If not, the DIFFSENS line has not changed voltage levels and the bus mode is stable so then proceed to:

a. Read bits [7:6] in SCSI Test 4 (STEST4) (register 0x52).

b. Write these two bits to SCSI Test Zero (STEST0) (register 0x4C), bits [5:4]. This forces the SCSI bus mode to the correct operating mode.

Note: If an SBMC interrupt occurs between steps 4 and 6, handle the interrupt and return to step 3.

Bits [5:4] in SCSI Test Zero (STEST0) are normally used as part of the SSAID and are read only. These bits may be written as part of a special test mode that forces the SCSI bus mode to one of three operating modes: SE, LVD, or HVD. The bit encoding is the same that is shown in the Table 5.11 under SCSI Test 4 (STEST4) for bits [7:6].

Step 7. Clear bit 3 in SCSI Test Two (STEST2) to remove the SCI drivers from the high impedance state.

During normal operation:

Step 1. Enable the SCSI Bus Mode Change (SBMC) interrupt. Bit 4 in SCSI Interrupt Enable One (SIEN1) should be set.

Step 2. If a SCSI bus mode change is detected, SCSI Interrupt Status One (SIST1), bit 4 indicates a SCSI Bus Mode Change (SBMC) interrupt.

Step 3. Clear the interrupt by reading SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1).

Step 4. Wait 100 ms.

Step 5. Check that no more SBMC interrupts have occurred.

If not, the DIFFSENS line has not changed voltage levels and the bus mode is stable so then proceed to:

a. Read bits [7:6] in SCSI Test 4 (STEST4).

b. Write two bits 5 and 4 to SCSI Test Zero (STEST0)).

Note: Bits [5:4] in SCSI Test Zero (STEST0) are normally used as part of the SSAID and are read only. These bits may be written as part of a special test mode that forces the SCSI bus mode to one of three operating modes: SE, LVD, or HVD. The bit encoding is the same that is shown in the Table 5.11 under SCSI Test 4 (STEST4) for bits [7:6]. This forces the SCSI bus to the correct operating mode.

If a SBMC interrupt did occur between steps 3 and 5, handle the interrupt and return to step 3.

The SBMC interrupt can cause a problem in systems that use multiple software drivers where the drivers pass control to one another after a chip reset. This problem occurs when the LSI53C895 is connected to a SE SCSI bus because the SBMC interrupt is generated after each reset. In particular, this problem occurs with NetWare when control is passed between the NetWare and DOS drivers. After a soft reset, the LSI53C895 defaults to LVD mode. If SE devices are on the bus and pull the DIFFSENS line low, a SBMC interrupt is generated and requires a response from the driver.

One solution is to use a soft abort by writing a one to bit 7 in the Interrupt Status (ISTAT) register instead of a soft reset to stop current SCSI transactions. This would halt current transactions without altering chip

settings such as the clock quadrupler and the clock divider setup. The pending transactions would then start over.

2.8.3 (Re)Select During (Re)Selection

In multithreaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select a target and is reselected by another. The Select SCRIPTS instruction has an alternate address to which the SCRIPTS jump when this situation occurs. An analogous situation occurs for target devices being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a Set Initiator instruction or the target SCRIPTS should start with a Set Target instruction. The Selection and Reselection Enable bits (SCSI Chip ID (SCID) bits 5 and 6, respectively) should both be asserted so that the LSI53C895 may respond as an initiator or as a target. If only selection is enabled, the LSI53C895 cannot be reselected as an initiator. There are also status and interrupt bits in the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Enable Zero (SIEN0) registers that indicate whether the LSI53C895 has been selected (bit 5) and reselected (bit 4).

2.9 Synchronous Operation

The LSI53C895 can transfer synchronous SCSI data in both initiator and target modes. The SCSI Transfer (SXFER) register controls both the synchronous offset and the transfer period. It can be loaded by the CPU before SCRIPTS execution begins, from within SCRIPTS by using a Table Indirect I/O instruction, or with a Read-Modify-Write instruction.

The LSI53C895 can receive data from the SCSI bus at a synchronous transfer period as short as 25 ns, regardless of the transfer period used to send data. The LSI53C895 can receive data at one-fourth of the divided SCLK frequency. Depending on the SCLK frequency, the negotiated transfer period, and the synchronous clock divider, the LSI53C895 can send synchronous data at intervals as short as 25 ns for Ultra2 SCSI, 50 ns for Ultra SCSI, 100 ns for fast SCSI, and 200 ns for SCSI-1.

2.9.1 Determining the Data Transfer Rate

Synchronous data transfer rates are controlled by bits in two different registers of the LSI53C895. A brief description of the bits is provided below. Figure 2.5 illustrates the clock division factors used in each register, and the role of the register bits in determining the transfer rate.

2.9.1.1 SCSI Control Three (SCNTL3) Register, Bits [6:4] (SCF[2:0])

The SCF[2:0] bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider controls the rate at which data can be received. This rate must not exceed 160 MHz. The receive rate of synchronous SCSI data is one-fourth of the SCF divider output. For example, if SCLK is 160 MHz and the SCF value is set to divide by one, then the maximum rate at which data can be received is 40 MHz (160/(1*4) = 40).

2.9.1.2 SCSI Control Three (SCNTL3) Register, Bits [2:0] (CCF[2:0])

The CCF[2:0] bits select the factor by which the frequency of SCLK is divided before being presented to the asynchronous SCSI core logic. This divider must be set according to the input clock frequency in the Figure 2.5.

2.9.1.3 SCSI Transfer (SXFER) Register, Bits [7:5] (TP[2:0])

The TP[2:0] divider bits determine the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode. This value further divides the output from the SCF divider.

2.9.2 Ultra2 SCSI Synchronous Data Transfers

Ultra2 SCSI is an extension of current Ultra SCSI synchronous transfer specifications. It allows negotiation of synchronous transfer periods as short as 25 ns, which is half the 50 ns period allowed under Ultra SCSI. This allows a maximum transfer rate of 80 Mbytes/s on a 16-bit, LVD SCSI bus. The LSI53C895 has a SCSI clock quadrupler that must be enabled for the chip to perform Ultra2 SCSI transfers with a 40 MHz oscillator. In addition, the following bit values affect the chip's ability to support Ultra2 SCSI synchronous transfer rates:

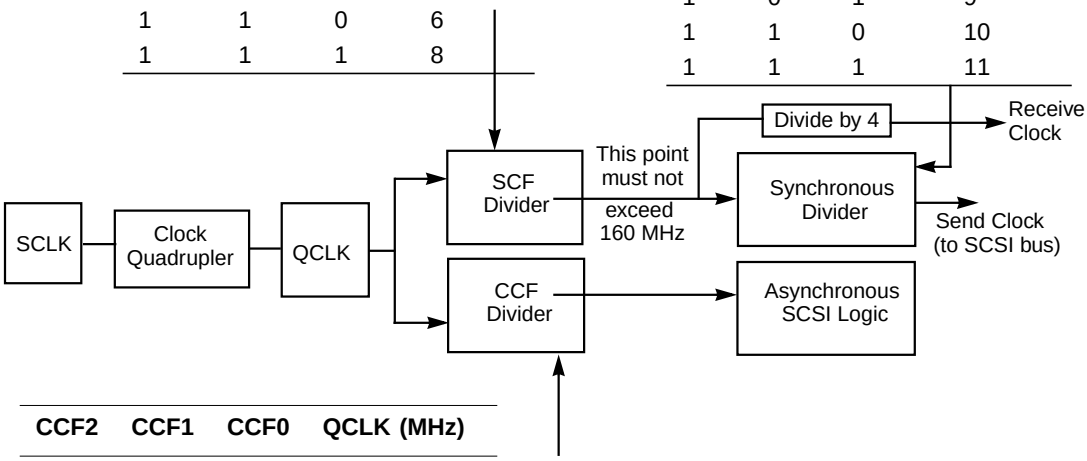
- Clock Conversion Factor bits, SCSI Contr0l Three (SCNTL3) register bits [2:0] and Synchronous Clock Conversion Factor bits, SCSI Contr0l Three (SCNTL3) register bits [6:4]. These fields support a value of 0b111, which allows the 160 MHz SCLK frequency to be divided down by 8 for the asynchronous logic.
- Ultra2 SCSI Enable bit, SCSI Contr0l Three (SCNTL3) register, bit 7. Setting this bit enables Ultra2 SCSI synchronous transfers in systems that use the internal SCSI clock quadrupler.
- TolerANT Enable bit, SCSI Test Three (STEST3) register, bit 7. Active negation must be enabled for the LSI53C895 to perform Ultra2 SCSI transfers.

  Note: The clock quadrupler requires a 40 MHz external clock. LSI Logic software assumes that the LSI53C895 is connected to a 40 MHz external clock, which is quadrupled to achieve Ultra2 SCSI transfer rates.

Figure 2.5 Determining the Synchronous Transfer Rate

SCF2	SCF1	SCF0	SCF Divisor
0	0	1	1
0	1	0	1.5
0	1	1	2
1	0	0	3
0	0	0	3
1	0	1	4
1	1	0	6
1	1	1	8

TP2	TP1	TP0	XFERP Divisor
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11



CCF2	CCF1	CCF0	QCLK (MHz)
0	0	0	50.1–66.00
0	0	1	16.67–25.00
0	1	0	25.01–37.50
0	1	1	37.51–50.00
1	0	0	50.01–66.00
1	0	1	75.01–80.00
1	1	0	120
1	1	1	160

Example:

QCLK (Quadrupled SCSI Clock) = 160 MHz, SCF = 1(/1), XFERP = 0(/4),
CCF = 7 (/8)
Synchronous send rate = (QCLK/SCF)/XFERP = (160/1)/4 = 40 Mbytes/s
Synchronous receive rate = (QCLK/SCF)/4 = (160/1)/4 = 40 Mbytes/s

2.10 Interrupt Handling

The SCRIPTS processor in the LSI53C895 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the LSI53C895.

2.10.1 Polling and Hardware Interrupts

The external microprocessor is informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used for other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the LSI53C895 asserts the Interrupt Request (IRQ/) line that interrupts the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware interrupts for long waits, and use polling for short waits.

2.10.2 Registers

The registers in the LSI53C895 that are used for detecting or defining interrupts are:

- Interrupt Status (ISTAT)
- SCSI Interrupt Status Zero (SIST0)
- SCSI Interrupt Status One (SIST1)
- DMA Status (DSTAT)
- SCSI Interrupt Enable Zero (SIEN0)
- SCSI Interrupt Enable One (SIEN1)
- DMA Control (DCNTL)
- DMA Interrupt Enable (DIEN)

2.10.2.1 ISTAT

Interrupt Status (ISTAT) is the only register that can be accessed as a slave during SCRIPTS operation; therefore, the Interrupt Status (ISTAT) register is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin has been asserted in association with a hardware interrupt. The Interrupt on the Fly (INTF) bit should be the first interrupt serviced. It must be written to one to be cleared. This interrupt must be cleared before servicing any other interrupts. If the SIP bit in the Interrupt Status (ISTAT) register is set, then a SCSI-type interrupt has occurred and the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers should be read. If the DIP bit in the Interrupt Status (ISTAT) register is set, then a DMA-type interrupt has occurred and the DMA Status (DSTAT) register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

2.10.2.2 SIST0 and SIST1

SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers contain the SCSI-type interrupt bits. Reading these registers determines which condition or conditions caused the SCSI-type interrupt, and clears that SCSI interrupt condition.

If the LSI53C895 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the LSI53C895 attempts to send the contents of the DMA FIFO to memory before generating the interrupt.

If the LSI53C895 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. If this situation occurs, the DMA FIFO Empty (DFE) bit in DMA Status (DSTAT) should be checked.

If this bit is cleared, set the Clear DMA FIFO (CLF) and Clear SCSI FIFO (CSF) bits before continuing. The CLF bit is bit 2 in Chip Test Three (CTEST3). The CSF bit is bit 1 in SCSI Test Three (STEST3).

2.10.2.3 DSTAT

The DMA Status (DSTAT) register contains the DMA-type interrupt bits. Reading this register determines which condition or conditions caused the DMA-type interrupt, and clears that DMA interrupt condition. Bit 7,

DFE bit in DMA Status (DSTAT) is purely a status bit; it does *not* generate an interrupt under any circumstances and is not cleared when read. DMA interrupts flushes neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the DMA Status (DSTAT) register should be checked after any DMA interrupt.

If the DFE bit is cleared, then the FIFOs must be cleared by setting the Clear DMA FIFO (CLF) and Clear SCSI FIFO (CSF) bits. Setting the Flush DMA FIFO (FLF) bit flushes the FIFO.

2.10.2.4 SIEN0 and SIEN1

The SCSI Interrupt Enable Zero (SIEN0) and SCSI Interrupt Enable One (SIEN1) registers are the interrupt enable registers for the SCSI interrupts in SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1).

2.10.2.5 DIEN

The DMA Interrupt Enable (DIEN) register is the interrupt enable register for DMA interrupts in DMA Status (DSTAT).

2.10.2.6 DCNTL

When bit 1 in the DMA Control (DCNTL) register is set, the IRQ/ pin is not asserted when an interrupt condition occurs. The interrupt is not lost or ignored, but merely masked at the pin. Clearing this bit when an interrupt is pending immediately asserts the IRQ/ pin. As with any register other than Interrupt Status (ISTAT), this register can only be accessed by a SCRIPTS instruction during SCRIPTS execution.

2.10.3 Fatal vs. Nonfatal Interrupts

A fatal interrupt, as the name implies, always stops SCRIPTS from running. All nonfatal interrupts become fatal when they are enabled by setting the appropriate interrupt enable bit. Interrupt masking is discussed later in Section 2.10.4, “Masking,” page 2-35. All DMA interrupts (indicated by the DIP bit in Interrupt Status (ISTAT) and one or more bits in DMA Status (DSTAT) being set) are fatal.

Some SCSI interrupts are nonfatal. These are indicated by the SIP bit in the Interrupt Status (ISTAT) and one or more bits in SCSI Interrupt Status

Zero (SIST0) or SCSI Interrupt Status One (SIST1) being set. When the LSI53C895 is operating in Initiator mode, only the Function Complete (CMP), Selected (SEL), Reselected (RSL), General Purpose Timer Expired (GEN), and Handshake to Handshake Timer Expired (HTH) interrupts are nonfatal. When operating in Target mode CMP, SEL, RSL, Target mode: SATN/ active (M/A), GEN, and HTH are nonfatal. Refer to the description for the Disable Halt on a Parity Error or SATN/ active (Target Mode Only) (DHP) bit in the SCSI Control One (SCNTL1) register. This information describes how to configure the chip behavior when the SATN/ interrupt is enabled during Target mode operation. The Interrupt on the Fly interrupt is also nonfatal, since SCRIPTS can continue when it occurs.

Nonfatal interrupts prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. SCRIPTS do not stop when:

- Arbitration is complete (CMP set).
- The LSI53C895 has been selected or reselected (SEL or RSL set).
- The initiator has asserted ATN (target mode: SATN/ active).
- The General Purpose or Handshake-to-Handshake timers expire.

These interrupts are not needed for events that occur during high-level SCRIPTS operations.

2.10.4 Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the SCSI Interrupt Enable Zero (SIEN0) and SCSI Interrupt Enable One (SIEN1) (for SCSI interrupts) registers or DMA Interrupt Enable (DIEN) (for DMA interrupts) register. How the chip responds to masked interrupts depends on whether:

- Polling or hardware interrupts are being used.
- The interrupt is fatal or nonfatal.
- The chip is operating in Initiator or Target mode.

If a nonfatal interrupt is masked and that condition occurs, SCRIPTS do not stop, the appropriate bit in the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) is still set, the SIP bit in the Interrupt

Status (ISTAT) is not set, and the IRQ/ pin is not asserted. See the subsection entitled “Fatal vs. Nonfatal Interrupts,” for a list of the nonfatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS still stop, the appropriate bit in the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), or SCSI Interrupt Status One (SIST1) register is set, and the SIP or DIP bits in the Interrupt Status (ISTAT) is set, but the IRQ/ pin is not asserted.

When the chip is initialized, enable all fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, the SCRIPTS halt and the system does not detect it unless it times out and checks the Interrupt Status (ISTAT) after a certain period of inactivity.

If Interrupt Status (ISTAT) is being polled instead of using hardware interrupts, then masking a fatal interrupt makes no difference since the SIP and DIP bits in the Interrupt Status (ISTAT) inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted does not deassert IRQ/.

2.10.5 Stacked Interrupts

The LSI53C895 stacks interrupts if they occur one after the other. If the SIP or DIP bits in the Interrupt Status (ISTAT) register are set (first level), then at least one pending interrupt already exists, and any future interrupts are stacked in extra registers behind the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts set additional bits in the extra registers behind SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT). When the first level of interrupts are cleared, all the interrupts that came in afterward move into the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT). After the first interrupt is cleared by reading the appropriate register, these three events occur:

1. The IRQ/ pin is deasserted for a minimum of three CLKs.

2. The stacked interrupt(s) move into the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), or DMA Status (DSTAT).
3. The IRQ/ pin is asserted once again.

Since a masked nonfatal interrupt does not set the SIP or DIP bits, interrupt stacking does not occur. A masked, nonfatal interrupt still posts the interrupt in SCSI Interrupt Status Zero (SIST0), but does not assert the IRQ/ pin. Since no interrupt is generated, future interrupts move right into the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked nonfatal interrupt is still set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but are not stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts do not attempt to flush the FIFOs before generating the interrupt. It is important to set either the Clear DMA FIFO (CLF) and Clear SCSI FIFO (CSF) bits if a DMA interrupt occurs and the DMA FIFO Empty (DFE) bit is not set. This is because any future SCSI interrupts are not posted until the DMA FIFO is clear of data. These *locked out* SCSI interrupts are posted as soon as the DMA FIFO is empty.

2.10.6 Halting in an Orderly Fashion

When an interrupt occurs, the LSI53C895 attempts to halt in an orderly fashion as explained below.

- If the interrupt occurs in the middle of an instruction fetch, the fetch is completed, except in the case of a Bus Fault. Execution does not begin, but the DSP points to the next instruction since it is updated when the current instruction is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the LSI53C895 attempts to flush the DMA FIFO to memory before halting. Under any other circumstances, only the current cycle

is completed before halting, so the DFE bit in DMA Status (DSTAT) should be checked to see if any data remains in the DMA FIFO.

- SCSI SREQ/SACK handshakes that have begun are completed before halting.
- The LSI53C895 attempts to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions and once instruction execution begins, it continues to completion before halting.
- If the instruction is a JUMP/CALL WHEN/IF <phase>, the DMA SCRIPTS Pointer (DSP) is updated to the transfer address before halting.
- All other instructions may halt before completion.

2.10.7 Sample Interrupt Service Routine

A sample of an interrupt service routine for the LSI53C895 is shown below. This routine can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if using hardware interrupts.

1. Read Interrupt Status (ISTAT).
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) indicate which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).
4. If only the DIP bit is set, read DMA Status (DSTAT) to clear the interrupt condition and get the DMA interrupt status. The bits in the DMA Status (DSTAT) indicate which DMA interrupt(s) occurred and determine what action is required to service the interrupt(s).
5. If both the SIP and DIP bits are set, read SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) registers to clear interrupts, insert a 12 CLK delay between the consecutive reads to ensure that the interrupts clear properly.

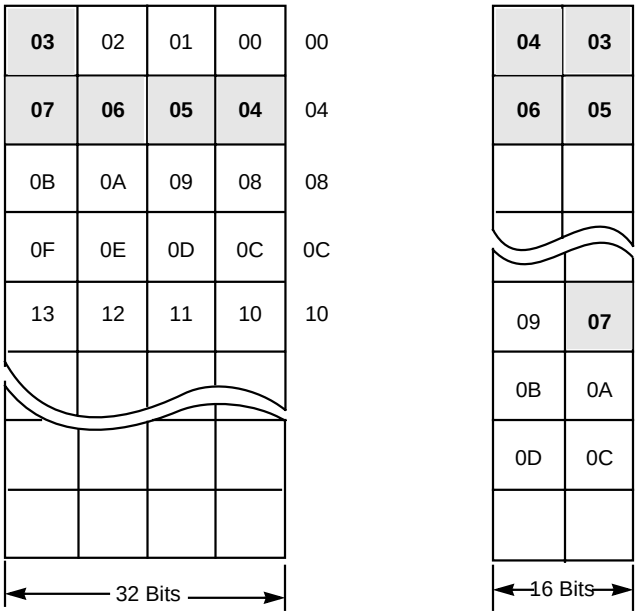
Both the SCSI and DMA interrupt conditions should be handled before leaving the interrupt service routine. It is recommended that the DMA interrupt be serviced before the SCSI interrupt because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.

6. When using polled interrupts, go back to step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin is asserted again if there are any stacked interrupts. This re-enters the system into the interrupt service routine.

2.11 Chained Block Moves

Since the LSI53C895 has the capability to transfer 16-bit wide SCSI data, a unique situation occurs when dealing with odd bytes. The Chained Move (CHMOV) SCRIPTS instruction along with the Wide SCSI Send (WSS) and Wide SCSI Receive (WSR) bits in the SCSI Control Two (SCNTL2) register facilitate these situations. Figure 2.6 illustrates the Chained Block Move instruction.

Figure 2.6 Block Move and Chained Block Move Instructions



Notes:

CHMOV 5, 3 when DATA_OUT: Moves five bytes from address 03 in the host memory to the SCSI bus (bytes 03, 04, 05, and 06 are moved and byte 07 remains in the low-order byte of the SCSI Output Data Latch register and is married with the first byte of the following MOVE instruction).

MOVE 5, 9 when DATA_OUT: Moves five bytes from address 09 in the host memory to the SCSI bus.

2.11.1 Wide SCSI Send Bit (WSS)

The WSS bit is set whenever the SCSI core is sending data (Data Out for initiator or Data In for target), and the core detects a partial transfer at the end of a chained Block Move SCRIPTS instruction. Note that this flag is not set if a normal Block Move instruction is used. Under this condition, the SCSI core does not send the low-order byte of the last partial memory transfer across the SCSI bus. Instead, the low-order byte is temporarily stored in the lower byte of the SCSI Output Data Latch (SODL) register and the WSS flag is set. The hardware uses the WSS flag to determine what behavior must occur at the start of the next data send transfer. When the WSS flag is set at the start of the next transfer,

the first byte (the high-order byte) of the next data send transfer is married with the stored low-order byte in the SCSI Output Data Latch (SODL) register; and the two bytes are sent out across the bus, regardless of the type of Block Move instruction (normal or chained). The flag is automatically cleared when the married word is sent. The flag is alternately cleared through SCRIPTS or by the microprocessor. Additionally, the microprocessor or SCRIPTS can use this bit for error detection and recovery purposes.

2.11.2 Wide SCSI Receive Bit (WSR)

The WSR bit is set whenever the SCSI core is receiving data (Data In for initiator or Data Out for target), and the core detects a partial transfer at the end of a block move or chained block move SCRIPTS instruction. When WSR is set, the high-order byte of the last SCSI bus transfer is not transferred to memory. Instead, the byte is temporarily stored in the SCSI Wide Residue (SWIDE) register. The hardware uses the WSR bit to determine what behavior must occur at the start of the next data receive transfer. The bit is automatically cleared at the start of the next data receive transfer. The microprocessor or SCRIPTS can alternatively clear this bit. Additionally, the microprocessor or SCRIPTS can use this bit for error detection and recovery purposes.

2.11.3 SCSI Wide Residue (SWIDE) Register

This register stores data for partial byte data transfers. For receive data, the SCSI Wide Residue (SWIDE) register holds the high-order byte of a partial SCSI transfer which has not yet been transferred to memory. This stored data may be a residue byte (and therefore ignored) or it may be valid data that is transferred to memory at the beginning of the next Block Move instruction.

2.11.4 SCSI Output Data Latch (SODL) Register

For send data, the low-order byte of the SCSI Output Data Latch (SODL) register holds the low-order byte of a partial memory transfer which has not yet been transferred across the SCSI bus. This stored data is usually married with the first byte of the next data send transfer, and both bytes are sent across the SCSI bus at the start of the next data send block move command.

2.11.5 Chained Block Move SCRIPTS Instruction

A chained Block Move SCRIPTS instruction transfers consecutive data send or data receive blocks. Using the chained block move instruction facilitates partial receive transfers and allows correct partial send behavior without additional op code overhead. Behavior of the chained Block Move instruction varies slightly for sending and receiving data.

For receive data (Data In for initiator or Data Out for target), a chained Block Move instruction indicates that if a partial transfer occurred at the end of the instruction, the WSR flag is set. The high-order byte of the last SCSI transfer is stored in the SCSI Wide Residue (SWIDE) register rather than transferred to memory. The contents of the SCSI Wide Residue (SWIDE) register should be the first byte transferred to memory at the start of the chained block move data stream. Since the byte count always represents data transfers to/from memory (as opposed to the SCSI bus), the byte transferred out of the SCSI Wide Residue (SWIDE) register is one of the bytes in the byte count.

If the WSR bit is cleared when a receive data chained Block Move instruction is executed, the data transfer occurs similar to that of the regular block move instruction. Whether the WSR bit is set or clear, when a normal block move instruction is executed, the contents of the SCSI Wide Residue (SWIDE) register is ignored and the transfer takes place normally. For “N” consecutive wide data receive Block Move instructions, the 2nd through the Nth Block Move instructions should be chained block moves.

For send data (Data Out for initiator or Data In for target), a chained Block Move instruction indicates that if a partial transfer terminates the chained block move instruction, the last low-order byte (the partial memory transfer) should be stored in the lower byte of the SCSI Output Data Latch (SODL) register and not sent across the SCSI bus. Without the chained block move instruction, the last low-order byte would be sent across the SCSI bus. The starting byte count represents data bytes transferred from memory but not to the SCSI bus when a partial transfer exists. For example, if the instruction is an Initiator chained Block Move Data Out of five bytes (and WSS is not previously set), five bytes are transferred out of memory to the SCSI core, four bytes are transferred from the SCSI core across the SCSI bus, and one byte is temporarily stored in the lower byte of the SCSI Output Data Latch (SODL) register waiting to be married with the first byte of the next block move instruction.

Regardless of whether a chained Block Move or normal Block Move instruction is used, if the WSS bit is set at the start of a data send command, the first byte of the data send command is assumed to be the high-order byte and is married with the low-order byte stored in the lower byte of the SODL register before the two bytes are sent across the SCSI bus. For “N” consecutive wide data send Block Move commands, the first through the (Nth – 1) Block Move instructions should be Chained Block Moves.

Chapter 3
PCI Functional Description

This chapter describes the PCI functional description for the LSI53C895 chip and includes these topics:

3.1 PCI Addressing

There are three types of PCI-defined address spaces:

1. Configuration space
2. Memory space
3. I/O space

Configuration space is a contiguous 256 x 8-bit set of addresses dedicated to each “slot” or “stub” on the bus. Decoding C_BE/[3:0] determines if a PCI cycle is intended to access configuration register space. The IDSEL bus signal is a “chip select” that allows access to the configuration register space only. A configuration read/write cycle without IDSEL is ignored. The eight lower order addresses are used to select a specific 8-bit register. AD[10:8] are decoded as well, but they must be zero or the LSI53C895 does not respond. According to the PCI specification, AD[10:8] are to be used for multifunction devices. The host processor uses the PCI configuration space to initialize the LSI53C895.

The lower 128 bytes of the LSI53C895 configuration space holds system parameters while the upper 128 bytes map into the LSI53C895 operating

registers. For all PCI cycles except configuration cycles, the LSI53C895 registers are located on the 256-byte block boundary defined by the base address assigned through the configured register. The LSI53C895 operating registers are available in both the upper and lower 128-byte portions of the 256-byte space selected.

At initialization time, each PCI device is assigned a base address (in the case of the LSI53C895, the upper 24 bits of the address are selected) for memory accesses and I/O accesses. On every access, the LSI53C895 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the LSI53C895 and the low order eight bits define the register to be accessed. A decode of C_BE/ [3:0] determines which registers and what type of access is to be performed.

PCI defines memory space as a contiguous 32-bit memory address that is shared by all system resources, including the LSI53C895. Base Address One (Memory) determines which 256-byte memory area this device occupies.

PCI defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the LSI53C895. Base Address Register Zero (I/O) determines which 256-byte I/O area this device occupies.

3.2 PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE/[3:0] lines during the address phase. PCI bus command encoding and types appear in Table 3.1.

The I/O Read command reads data from an agent mapped in I/O address space. All 32 address bits are decoded.

The I/O Write command writes data to an agent when mapped in I/O address space. All 32 address bits are decoded.

The Memory Read, Memory Read Multiple, and Memory Read Line commands read data from an agent mapped in memory address space. All 32 address bits are decoded.

The Memory Write and Memory Write and Invalidate commands write data to an agent when mapped in memory address space. All 32 address bits are decoded.

Table 3.1 PCI Bus Commands Supported

C_BE[3:0]	Command Type	Supported as Master	Supported as Slave
0b0000	Special Interrupt Acknowledge	No	No
0b0001	Special Cycle	No	No
0b0010	I/O Read Cycle	Yes	Yes
0b0011	I/O Write Cycle	Yes	Yes
0b0100	Reserved	n/a	n/a
0b0101	Reserved	n/a	n/a
0b0110	Memory Read	Yes	Yes
0b0111	Memory Write	Yes	Yes
0b1000	Reserved	n/a	n/a
0b1001	Reserved	n/a	n/a
0b1010	Configuration Read	No	Yes
0b1011	Configuration Write	No	Yes
0b1100	Memory Read Multiple	Yes[1]	No (defaults to 0b0110)
0b1101	Dual Address Cycle	No	No
0b1110	Memory Read Line	Yes[2]	No (defaults to 0b0110)
0b1111	Memory Write and Invalidate	Yes[3]	No (defaults to 0b0111)

1. This operation is selectable by bit 2 in the DMA Mode (DMODE) operating register
2. This operation is selectable by bit 3 in the DMA Mode (DMODE) operating register.
3. This operation is selectable by bit 0 in the Chip Test Three (CTEST3) operating register.

3.3 PCI Cache Mode

The LSI53C895 supports the PCI specification for an 8-bit Cache Line Size register located in PCI configuration space. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. In conjunction with the Cache Line Size register, the PCI commands Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands.

3.3.1 Support for PCI Cache Line Size Register

The LSI53C895 supports the PCI specification for an 8-bit Cache Line Size register in PCI configuration space. It can sense and react to nonaligned addresses corresponding to cache line boundaries.

3.3.2 Selection of Cache Line Size

The cache logic selects a cache line size based on the values for the burst size in the DMA Mode (DMODE) register, bit 2 in the Chip Test Five (CTEST5) register, and the PCI Cache Line Size register.

Note: The LSI53C895 does not automatically use the value in the PCI Cache Line Size register as the cache line size value. The chip scales the value of the Cache Line Size register down to the nearest binary burst size allowed by the chip (2, 4, 8, 16, 32, 64, or 128), compares this value to the burst size defined by the values of the DMA Mode (DMODE) register and bit 2 of the Chip Test Five (CTEST5) register, then selects the smallest as the value for the cache line size. The LSI53C895 uses this value for all burst data transfers.

3.3.3 Alignment

The LSI53C895 uses the calculated line size value to monitor the current address for alignment to the cache line size. When it is not aligned, the chip attempts to align to the cache boundary by using a “smart aligning” scheme. This means that it attempts to use the largest burst size possible that is less than the cache line size, to reach the cache

boundary quickly with no overflow. This process is a stepping mechanism that steps up to the highest possible burst size based on the current address.

The stepping process begins at a 4-Dword boundary. The LSI53C895 first tries to align to a 4-Dword boundary (0x0000, 0x0010, etc.) by using single Dword transfers (no bursting). Once this boundary has been reached the chip evaluates the current alignment to various burst sizes allowed, and selects the largest possible as the next burst size, while not exceeding the cache line size. The chip then issues this burst, and re-evaluates the alignment to various burst sizes, again selecting the largest possible while not exceeding the cache line size, as the next burst size. This stepping process continues until the chip reaches the cache line size boundary or runs out of data. Once a cache line boundary is reached, the chip uses the cache line size as the burst size from then on, except in the case of multiples (explained below). The alignment process is finished at this point.

Example: Cache Line Size - 16, Current Address = 0x01 – The chip is not aligned to a 4-Dword cache boundary (the stepping threshold), so it issues four single-Dword transfers (the first is a 3-byte transfer). At address 0x10, the chip is aligned to a 4-Dword boundary, but not aligned to any higher burst size boundaries that are less than the cache line size. So, the LSI53C895 issues a burst of 4. At this point, the address is 0x20, and the chip evaluates that it is aligned not only to a 4-Dword boundary, but also to an 8-Dword boundary. It selects the highest, 8, and bursts 8 Dwords. At this point, the address is 0x40, which is a cache line size boundary. Alignment stops, and the burst size from then on is switched to 16.

3.3.4 Memory Move Misalignment

The LSI53C895 does not operate in a cache alignment mode when a Memory Move instruction type is issued and the read and write addresses are different distances from the nearest cache line boundary. For example, if the read address is 0x21F, the write address is 0x42F, and the cache line size is eight (8), the addresses are byte aligned, but they are not the same distance from the nearest cache boundary. The read address is 1 byte from the cache boundary 0x220 and the write address is 17 bytes from the cache boundary 0x440. In this situation, the chip does not align to cache boundaries and operates as an LSI53C825.

3.3.5 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except that it additionally guarantees a minimum transfer of one complete cache line; that is, the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register at address 0x0C in PCI configuration space. The LSI53C895 enables Memory Write and Invalidate cycles when bit 0 in the Chip Test Three (CTEST3) register (WRIE) and bit 4 in the PCI Command register are set. This causes Memory Write and Invalidate commands to be issued when the following conditions are met:

1. The CLSE bit, WRIE bit, and PCI configuration Command register, bit 4 must be set.
2. The Cache Line Size register must contain a legal burst size (2, 4, 8, 16, 32, 64, or 128) value AND that value must be less than or equal to the DMA Mode (DMODE) burst size.
3. The chip must have enough bytes in the DMA FIFO to complete at least one full cache line burst.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the LSI53C895 issues a Memory Write and Invalidate command instead of a Memory Write command during all PCI write cycles.

3.3.5.1 Multiple Cache Line Transfers

The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The chip issues a burst transfer as soon as it reaches a cache line boundary. The size of the transfer is not automatically the cache line size, but rather a multiple of the cache line size as allowed for in the Revision 2.1 of the PCI specification. The logic selects the largest multiple of the cache line size based on the amount of data to transfer, with the maximum allowable burst size being that determined from the DMA Mode (DMODE) burst size bits and Chip Test Five (CTEST5), bit 2. If multiple cache line size transfers are not desired, the DMA Mode (DMODE) burst size can be set to exactly the cache line size and the chip only issues single cache line transfers.

After each data transfer, the chip re-evaluates the burst size based on the amount of remaining data to transfer and again selects the highest possible multiple of the cache line size, no larger than the DMA Mode (DMODE) burst size. The most likely scenario of this scheme is that the chip selects the DMA Mode (DMODE) burst size after alignment, and issues bursts of this size. The burst size, in effect, throttles down toward the end of a long Memory Move or Block Move transfer until only the cache line size burst size is left. The chip finishes the transfer with this burst size.

3.3.5.2 Latency

In accordance with the PCI specification, the chip's latency timer is ignored when issuing a Memory Write and Invalidate command such that when a latency time-out has occurred, the LSI53C895 continues to transfer up until a cache line boundary is reached. At that point, the chip relinquishes the bus and finishes the transfer at a later time using another bus ownership. If the chip is transferring multiple cache lines it continues to transfer until the next cache boundary is reached.

3.3.5.3 PCI Target Retry

During a Write and Invalidate transfer, if the target device issues a retry (STOP with no TRDY, indicating that no data was transferred), the LSI53C895 relinquishes the bus and immediately tries to finish the transfer on another bus ownership. The chip issues another Memory Write and Invalidate command on the next ownership in accordance with the PCI specification.

3.3.5.4 PCI Target Disconnect

During a Write and Invalidate transfer, if the target device issues a disconnect the LSI53C895 relinquishes the bus and immediately tries to finish the transfer on another bus ownership. The chip does not issue another Write and Invalidate command on the next ownership unless the address is aligned.

3.3.5.5 Memory Read Line Command

This command is identical to the Memory Read command, except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data

transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary rather than a single memory cycle. The Read Line Mode function that exists in the previous LSI53C8XX chips has been modified in the LSI53C895 to reflect the PCI Cache Line Size register specifications. The functionality of the Enable Read Line bit (bit 3 in DMA Mode (DMODE)) has been modified to more resemble the Write and Invalidate mode in terms of conditions that must be met before a Memory Read Line command is issued. However, the Read Line option operates exactly like the previous LSI53C8XX chips when cache mode has been disabled by a CLSE bit reset or when certain conditions exist in the chip (explained below).

The Read Line mode is enabled by setting bit 3 in the DMA Mode (DMODE) register. If cache mode is disabled, Read Line commands are issued on every read data transfer, except op code fetches, as in previous LSI53C8XX chips.

If cache mode has been enabled, a Read Line command is issued on all read cycles, except op code fetches, when the following conditions have been met:

1. The CLSE and Enable Read Line bits must be set.
2. The Cache Line Size register must contain a legal burst size value (2, 4, 8, 16, 32, 64, or 128) AND that value must be less than or equal to the DMA Mode (DMODE) burst size.
3. The number of bytes to be transferred at the time a cache boundary has been reached must be equal to or greater than the DMA Mode (DMODE) burst size.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip issues a Memory Read Line command instead of a Memory Read during all PCI read cycles. Otherwise, it issues a normal Memory Read command.

3.3.6 Memory Read Multiple Command

This command is identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The LSI53C895 supports PCI Read Multiple functionality and issues Memory Read Multiple commands on

the PCI bus when the Read Multiple Mode is enabled. This mode is enabled by setting bit 2 of the DMA Mode (DMODE) register (ERMP). If cache mode has been enabled, a Memory Read Multiple command is issued on all read cycles, except op code fetches, when the following conditions have been met:

1. The CLSE and ERMP bits must be set.
2. The Cache Line Size register must contain a legal burst size value (2, 4, 8, 16, 32, 64, or 128) and that value must be less than or equal to the DMA Mode (DMODE) burst size.
3. The number of bytes to be transferred at the time a cache boundary has been reached must be at least twice the full cache line size.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip issues a Memory Read Multiple command instead of a Memory Read during all PCI read cycles.

3.3.6.1 Burst Size Selection

The Memory Read Multiple command reads in multiple cache lines of data in a single bus ownership. The number of cache lines to be read is a multiple of the cache line size as allowed in the PCI Local Bus Specification, Revision 2.1 standard. The logic selects the largest multiple of the cache line size based on the amount of data to transfer, with the maximum allowable burst size being determined from the DMA Mode (DMODE) burst size bits and Chip Test Five (CTEST5), bit 2.

3.3.6.2 Read Multiple with Read Line Enabled

When both the Read Multiple and Read Line modes have been enabled, the Memory Read Line command is not issued if the above conditions are met. Instead, a Memory Read Multiple command is issued, even though the conditions for Read Line have been met.

If the Read Multiple mode is enabled and the Read Line mode has been disabled, Memory Read Multiple commands are still issued if the Read Multiple conditions are met.

3.3.6.3 Unsupported PCI Commands

The LSI53C895 does not respond to reserved commands, special cycle, dual address cycle, or interrupt acknowledge commands as a slave. It never generates these commands as a master.

3.4 Configuration Registers

The Configuration registers are accessible only by the system BIOS during PCI configuration cycles, and are not available to the user at any time. No other cycles, including SCRIPTS operations, can access these registers. The lower 128 bytes hold configuration data while the upper 128 bytes hold the LSI53C895 operating registers, which are described in Chapter 5, “Registers.” These registers can be accessed by SCRIPTS or the host processor.

Note: The configuration register descriptions provide general information only to indicate which PCI configuration addresses are supported in the LSI53C895. Refer to the PCI Local Bus Specification, Revision 2.1 for more detailed information.

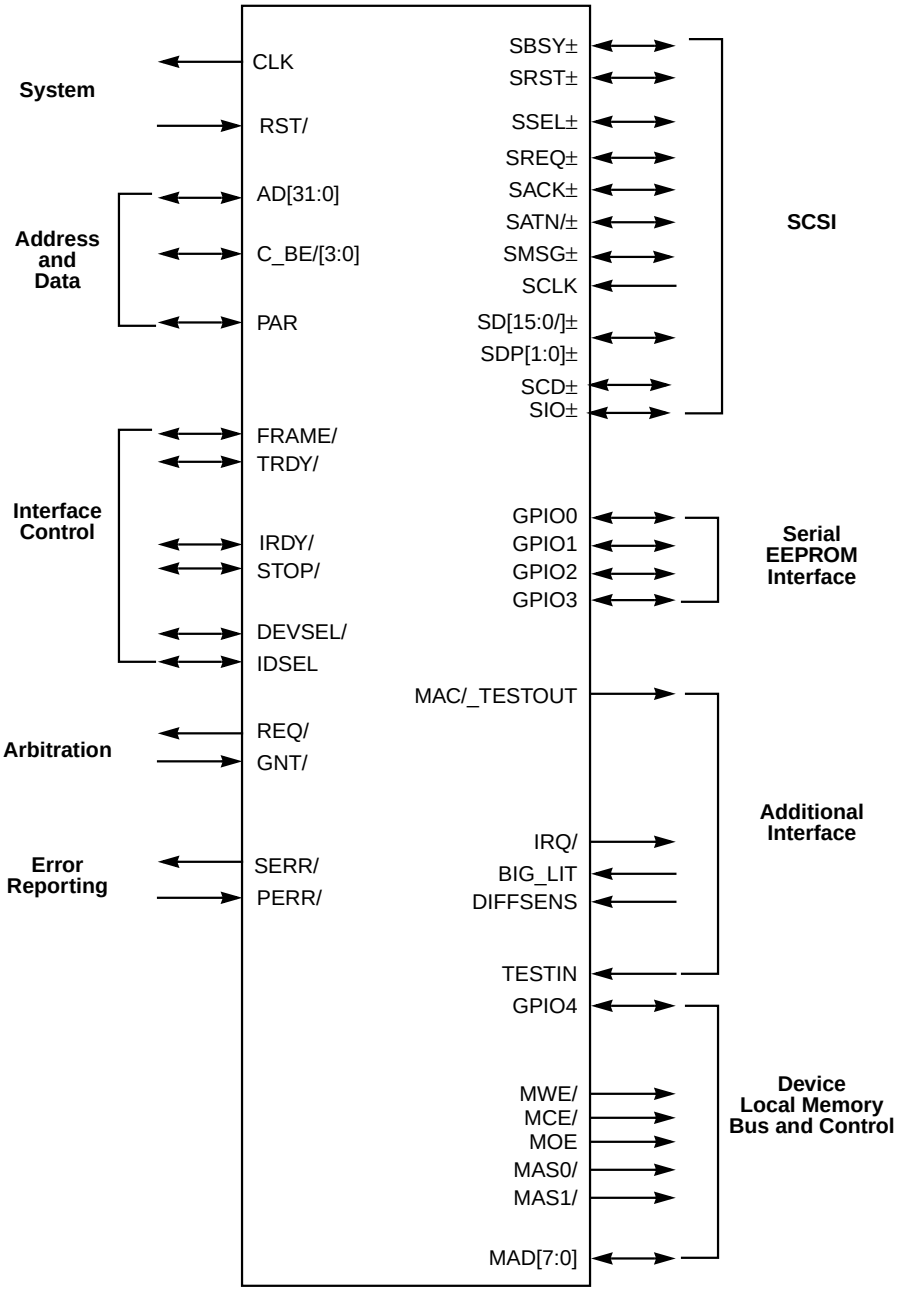
Chapter 4
Signal Descriptions

This chapter presents the LSI53C895 pin configurations and signal definitions by using tables and illustrations. Figure 4.1 is the functional signal grouping for the LSI53C895. The pin definitions are in Table 4.1 through Table 4.12. These definitions are organized into the following functional groups: System, Address/Data, Interface Control, Arbitration, Error Reporting, SCSI, and Optional Interface.

This chapter includes these main topics:

A slash (/) at the end of the signal name indicates that the active state occurs when the signal is at a LOW voltage. When the slash is absent, the signal is active at a HIGH voltage.

Figure 4.1 LSI53C895 Functional Signal Grouping



There are four signal type definitions:

1. I — Input, a standard input-only signal
2. O — Totem Pole Output, a standard output driver
3. T/S — 3-state, a bidirectional, 3-state input/output pin
4. S/T/S — Sustained 3-state, an active LOW 3-state signal owned and driven by one and only one agent at a time

4.1 Voltage Capabilities and Limitations

The LSI53C895 uses 5 V biasing pins to allow the device to handle up to 5 V input voltage to the PCI and external memory interface pins. When the LSI53C895 is used in a 5 V PCI system, the biasing pins (V5BIAS(P)) must be supplied with 5 V. When they are used in a 3 V only PCI environment, these biasing pins must be supplied with 3.3 V. The external memory pins (GPIO pins and MAD[7:0]) also use 5 Volt tolerant I/O pads. They also have a 5 V biasing pin (V5BIAS(M)). These pins should be supplied with 5 V when using 5 V memory devices, and with 3.3 V when using 3.3 V memory devices. The SCLK input is also a 5 V tolerant input pin.

The chip cannot operate normally if the 5 V biasing pins are grounded or disconnected. In addition, the PCI biasing pins should not be shorted to the memory bias pin if mixed voltage environments (such as 5 V PCI with 3 V memories) are possible. All other V_{DD} supplies to the LSI53C895 must be set for 3.3 V operation. In addition, the chip only drives 3.3 V on any of the pins when they operate as outputs.

4.2 Internal Pull-ups on LSI53C895 Pins

Several pins on the LSI53C895 use internal pull-ups. Table 4.1 describes the conditions under which these pull-ups are enabled or disabled.

Table 4.1 LSI53C895 Internal Pull-ups

Pin Name	Pull-up Current	Conditions for Pull-up
PCI pins except IRQ, CLK and RST	25 µA	Pull-ups enabled when AND-tree mode is enabled by driving TESTIN LOW
IRQ	25 µA	Pull-up enabled when AND-tree mode is enabled by driving TESTIN LOW or when the IRQ mode bit (bit 3 of DCNTL (0x3B)) is cleared[1]
RST, CLK	N/A	No pull-up
MAD [7:0]	N/A	No pull-ups
MAS/[1:0], MCE/, MOE/, MWE/	25 µA	Pull-up enabled when AND-tree mode is enabled by driving TESTIN LOW or if the ZMODE bit (bit7 of Chip Test Four (CTEST4) (0x21)) is set
GPIO[4:0]	N/A	No pull-ups
SCSI pads and SCLK	N/A	No pull-ups
RBIAS+, RBIAS–	N/A	No pull-ups
DIFFSENS	N/A	No pull-up, analog input protect pin
BIG_LIT/	25 µA	Pull-up enabled when AND-tree mode is enabled by driving TESTIN LOW
MAC/_TESTOUT	N/A	No pull-up, output only
TEST pin 82	25 µA	Pull-up all the time
TEST pin 177	25 µA	Pull-up all the time
TESTIN	25 µA	Pull-up all the time
TEST pins 180, 181, 182, 183	25 µA	Pull-up enabled when AND-tree mode is enabled by driving TESTIN LOW or if a hidden bit (bit7 of SCSI Test Zero (STEST0) (0x4C)) is cleared (default = cleared)

1. When bit 3 of DMA Control (DCNTL) is set, the pad becomes a totem pole output pad and drives both HIGH and LOW.

4.3 Pin Descriptions

Table 4.2 lists the Power and Ground Signals group.

Table 4.2 LSI53C895 Power and Ground Signals

Name[1]	Pin No. Ball No.	Description
V_{DD-PCI}[2]	2, 13, 23, 26, 36, 46, 60, 197 (Pins)	Power supplies to the PCI I/O pins
V_{SS-PCI}[2]	8, 18, 31, 41, 56, 193, 200 (Pins)	Power supplies to the PCI I/O pins
$V_{DD-SCSI}$[2]	86, 96, 115, 125, 134, 144, 164, 174 (Pins)	Power supplies to the SCSI bus I/O pins
$V_{SS-SCSI}$[2]	91, 110, 120, 128, 131, 139, 151, 169 (Pins)	Power supplies to the SCSI bus I/O pins
V_{DD-IO}[2]	73, 81, 184	Power supplies to the external memory interface
V_{SS-IO}[2]	78, 179	Power supplies to the external memory interface
$V_{DD-CORE}$	64, 190 P17, R19, P2, P1	Power supplies to the internal logic core
$V_{SS-CORE}$	68, 187 N18, P20, N1, M3	Power supplies to the internal logic core
V_{DD-A}	85 H19	Power pins used by analog circuitry **Note**: The V_{DD-A} pin is sensitive to noise above 90 mV at frequencies above 140 MHz. Refer to ** for information on filtering schemes to protect this pin and the phase locked loop from high frequency noise.
V_{SS-A}	83 J18	Power pins used by analog circuitry
V5BIAS (PCI)	4, 49 W18, Y4	5 Volt biasing pins for PCI signals. These pins must be supplied with 5 V in a 5 V PCI environment, or 3.3 V when used in a 3 V only PCI environment.
V5BIAS (MEM)	62 T20	5 Volt biasing pin for external memory interface signals. When using 5 V memory devices, this pin should be supplied with 5 V. When using 3.3 V memory devices, it should be supplied with 3.3 V.

Table 4.2 LSI53C895 Power and Ground Signals (Cont.)

Name[1]	Pin No. Ball No.	Description
V_{DD}	F4, K4, R4, D6, U6, D11, U10, D15, U15, F17, L17, R17	Power supplies
V_{SS}	A1, D4, H4, N4, U4, D8, U8, J9[3], K9[3], L9[3], M9[3], J10[3], K10[3], L10[3], M10[3], J11[3], K11[3], L11[3], M11[3], J12[3], K12[3], L12[3], M12[3], D13, U13, D17, H17, N17, U17	Power pins

1. All V_{DD} pins must be supplied 3.3 V. The LSI53C895 output signals drive 3.3 V.
2. In the BGA option, $V_{DD-SCSI}$, V_{DD-PCI} and V_{DD-IO} are connected together and $V_{SS-SCSI}$, V_{SS-PCI}, and V_{SS-IO} are connected together at package.
3. Optional ground pins.

Note: If you apply separate power supplies to the V_{DD-IO} and $V_{DD-CORE}$ pins in a chip testing environment, either power up the pins simultaneously or power up $V_{DD-CORE}$ before V_{DD-IO}. The V_{DD-IO} pins must always power down before $V_{DD-CORE}$.

Table 4.3 lists the System Signals group.

Table 4.3 System Signals

Name	Pin No. Ball No.	Type	Description
CLK	195 T1	I	Clock provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. This clock can optionally be used as the SCSI core clock; however, the LSI53C895 is not able to achieve Fast SCSI-2 (or faster) transfer rates.
RST/	194 R2	I	Reset forces the PCI sequencer of each device to a known state. All T/S and S/T/S signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST/ is active to properly reset the device.

Table 4.4 lists the Address and Data Signals group.

Table 4.4 Address and Data Signals

Name	Pin No. Ball No.	Type	Description
AD[31:0]	199, 201–204, 3, 5, 6, 10–12, 14–17, 19, 33–35, 37–40, 42, 44, 45, 47, 48, 50, 51, 57, 58 U2, V1, V2, W1, V3, Y3, V5, W5, W6, Y6, V7, W7, Y7, V8, W8, Y8, V12, Y13, W13, V13, Y14, W14, Y15, W15, Y17, W17, V17, Y19, V18, Y18, V20	T/S	Physical long word address and data are multiplexed on the same PCI pins. During the first clock of a transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports both read and write bursts. AD[7:0] define the least significant byte, and AD[31:24] define the most significant byte.
C_BE[3:0]/	7, 20, 32, 43 Y5, U9, W12, Y16	T/S	Bus commands and byte enables are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE[3:0]/ define the bus command. During the data phase, C_BE[3:0]/ are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE0/ applies to byte 0, and C_BE3/ applies to byte 3.
PAR	30 Y12	T/S	Parity is the even parity bit that protects the AD[31:0] and C_BE[3:0]/ lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

Table 4.5 lists the Interface Control Signals group.

Table 4.5 Interface Control Pins

Name	Pin No. Ball No.	Type	Description
FRAME/	21 V9	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate a bus transaction is beginning. While FRAME/ is asserted, data transfers continue. When FRAME/ is deasserted, the transaction is in the final data phase or the bus is idle.
TRDY/	24 W10	S/T/S	Target Ready indicates the selected device's ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
IRDY/	22 W9	S/T/S	Initiator Ready indicates the bus master's ability to complete the current data phase of the transaction. This signal is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD[31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	27 W11	S/T/S	Stop indicates that the selected target is requesting the master to stop the current transaction.
DEVSEL/	25 Y10	S/T/S	Device Select indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	9 V6	I	Initialization Device Select is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.

Table 4.6 lists the Arbitration Signals group.

Table 4.6 Arbitration Signals

Name	Pin No. Ball No.	Type	Description
REQ/	198 U1	O	Request indicates to the arbiter that this agent desires use of the PCI bus. This is a point to point signal. Every master has its own REQ/.
GNT/	196 T2	I	Grant indicates to the agent that access to the PCI bus has been granted. This is a point to point signal. Every master has its own GNT/.

Table 4.7 lists the Error Reporting Signals group.

Table 4.7 Error Reporting Signals

Name	Pin No. Ball No.	Type	Description
PERR/	28 V11	S/T/S	Parity Error may be pulsed active by an agent that detects a data parity error. PERR/ can be used by any agent to signal data corruptions.
SERR/	29 U11	O	This open drain output pin reports address parity errors. On detection of a PERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system is unable to continue operation once error processing is complete.

Table 4.8 lists the SCSI Signals, LVD Link Mode group.

Table 4.8 SCSI Signals, LVD Link Mode

Name	Pin No. Ball No.	Type	Description
SCLK	80 J20	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied LOW. For Ultra2 SCSI operation, this pin must be connected to an external 40 MHz oscillator, used with the internal clock quadrupler.
SD–[15:0], SDP–[1:0]	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132 F2, G2, H2, J3, G20, F20, E20, D20, A9, A8, A7, B6, B5, B4, B3, C1, E1, B10	I/O	Negative half of LVD Link signal pair for SCSI data lines. SCSI Data includes the following data lines and parity signals: SD[15:0]/(16-bit SCSI data bus), and SDP[1:0]/(SCSI data parity bits).
SD+[15:0], SDP+[1:0]	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133 F1, G1, H1, J2, G19, F19, E19, D19, B9, B8, B7, A5, A4, A3, B2, D1, F3, C10	I/O	Positive half of LVD Link signal pair for SCSI data lines.
SCTRL–	111, 97, 116, 99, 121, 123, 126, 118, 113 C17, C20, B16, D18, B14, B13, B12, B15, A18	I/O	Negative half of LVD Link signal pair for SCSI Control, which includes the following signals: SCD– SCSI phase line, command/data SIO– SCSI phase line, input/output SMSG– SCSI phase line, message SREQ– Data handshake signal from target device SACK– Data handshake signal from initiator device SBSY– SCSI bus arbitration signal, busy SATN– SCSI Attention, the initiator is requesting a message out phase SRST– SCSI bus reset SSEL– SCSI bus arbitration signal, select device

Table 4.8 SCSI Signals, LVD Link Mode (Cont.)

Name	Pin No. Ball No.	Type	Description
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114 D16, E17, A16, C19, A14, A13, A12, A15, A17	I/O	Positive half of LVD Link signal pair for SCSI Control, which includes the following signals: SCD+ SCSI phase line, command/data SIO+ SCSI phase line, input/output SMSG+ SCSI phase line, message SREQ+ Data handshake signal from target device SACK+ Data handshake signal from initiator device SBSY+ SCSI bus arbitration signal, busy SATN+ SCSI Attention, the initiator is requesting a message out phase SRST+ SCSI bus reset SSEL+ SCSI bus arbitration signal, select device
RBIAS+, RBIAS–	130, 129 A10, A11	I	Used to connect an external resistor to generate the bias current used by LVD Link pads.
DIFFSENS	84 H20	I	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a SE, LVD, or HVD device. The result is displayed in SCSI Test 4 (STEST4) bits[7:6]. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs are 3-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. **Note**: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4.9 lists the SCSI Signals, SE mode group.

Table 4.9 SCSI Pins, SE Mode

Name	Pin No. Ball No.	Type	Description
SCLK	80 J20	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied LOW.
SD–[15:0], SDP–[1:0]	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132 F2, G2, H2, J3, G20, F20, E20, D20, A9, A8, A7, B6, B5, B4, B3, C1, E1, B10	I/O	SCSI Data includes the following data lines and parity signals: SD[15:0]/(16-bit SCSI data bus), and SDP[1:0]/(SCSI data parity bits).
SD+[15:0], SDP+[1:0]	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133 F1, G1, H1, J2, G19, F19, E19, D19, B9, B8, B7, A5, A4, A3, B2, D1, F3, C10	O	These signals drive 0 Volts.
SCTRL–	111, 97, 116, 99, 121, 123, 126, 118, 113 C17, C20, B16, D18, B14, B13, B12, B15, A18	I/O	SCSI Control, includes the following signals: SCD– SCSI phase line, command/data SIO– SCSI phase line, input/output SMSG– SCSI phase line, message SREQ– Data handshake signal from target device SACK– Data handshake signal from initiator device SBSY– SCSI bus arbitration signal, busy SATN– SCSI Attention, the initiator is requesting a message out phase SRST– SCSI bus reset SSEL– SCSI bus arbitration signal, select device

Table 4.9 SCSI Pins, SE Mode (Cont.)

Name	Pin No. Ball No.	Type	Description
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114 D16, E17, A16, C19, A14, A13, A12, A15, A17	O	These pins drive 0 Volts.
DIFFSENS	84 H20	I	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a SE, LVD, or HVD device. The result is displayed in SCSI Test 4 (STEST4) bits [7:6]. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs are 3-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. **Note**: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4.10 lists the SCSI Signals, High Voltage Differential Mode group.

Table 4.10 SCSI Signals, High Voltage Differential Mode

Name	Pin No. Ball No.	Type	Description
SCLK	80 J20	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied LOW.
SD–[15:0] SDP–[1:0]	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132 F2, G2, H2, J3, G20, F20, E20, D20, A9, A8, A7, B6, B5, B4, B3, C1, E1, B10	I/O	SCSI data lines. SCSI Data includes the following data lines and parity signals: SD[15:0]/(16-bit SCSI data bus), and SDP[1:0]/ (SCSI data parity bits).

Table 4.10 SCSI Signals, High Voltage Differential Mode (Cont.)

Name	Pin No. Ball No.	Type	Description
SD+[15:0] SDP+[1:0]	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133 F1, G1, H1, J2, G19, F19, E19, D19, B9, B8, B7, A5, A4, A3, B2, D1, F3, C10	O	Driver direction control for SCSI data lines.
SCTRL–	111, 97, 116, 99, 121, 123, 126, 118, 113 C17, C20, B16, D18, B14, B13, B12, B15, A18	I/O	SCSI Control includes these signals: SCD– SCSI phase line, command/data SIO– SCSI phase line, input/output SMSG– SCSI phase line, message SREQ– Data handshake signal from target device SACK– Data handshake signal from initiator device SBSY– SCSI bus arbitration signal, busy SATN– SCSI Attention, the initiator is requesting a message out phase SRST– SCSI bus reset SSEL– SCSI bus arbitration signal, select device
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114 D16, E17, A16, C19, A14, A13, A12, A15, A17	O	Driver direction control for the external transceivers, which includes the following signals: SREQ+ Data handshake signal from target device SACK+ Data handshake signal from initiator device SBSY+ SCSI bus arbitration signal, busy SRST+ SCSI bus reset SSEL+ SCSI bus arbitration signal, select device **Note**: For HVD operation, SCD+, SIO+, SMSG+, and SATN+ are not used.
DIFFSENS	84 H20	1	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a SE, LVD, or HVD device. The result is displayed in SCSI Test 4 (STEST4), bits [7:6]. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs are 3-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. **Note**: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4.11 lists the Additional Signals group.

Table 4.11 Additional Signals

Name	Pin No. Ball No.	Type	Description
TESTIN	178 K2	I	Test In. When this pin is driven LOW, the LSI53C895 connects all inputs and outputs to an “AND tree.” All SCSI control signals and data lines are connected to the “AND tree.” The output of the “AND tree” is connected to the TESTOUT pin. This allows manufacturers to verify chip connectivity and determine exactly which pins are not properly attached. When the TESTIN pin is driven LOW, internal pull-ups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals are 3-stated, and the MAC/_TESTOUT pin is enabled. Connectivity can be tested by driving one of the LSI53C895 pins LOW. The MAC/_TESTOUT pin should respond by also driving LOW.
GPIO0_ FETCH/	61 T19	I/O	General Purpose I/O pin. Optionally, when driven LOW, this pin indicates that the next bus request is for an op code fetch. This pin powers up as a general purpose input. This pin has two specific purposes in the LSI Logic software. The software uses it to toggle SCSI device LEDs, turning on the LED whenever the LSI53C895 is on the SCSI bus. The software drives this pin LOW to turn on the LED, or drives it HIGH to turn off the LED. This signal can also be used as data I/O for serial EEPROM access. In this case, it is used with the GPIO1 pin, which serves as a clock.
GPIO1_ MASTER/	63 R18	I/O	General Purpose I/O pin. Optionally, when driven LOW, this pin indicates that the LSI53C895 is bus master. This pin powers up as a general purpose input. LSI Logic software supports use of this signal in serial EEPROM applications, when enabled, in combination with the GPIO0 pin. When this signal is used as a clock for serial EEPROM access, the GPIO0 pin serves as data.
GPIO[4:2]	67–65 P19 P18 R20	I/O	General Purpose I/O pins. GPIO4 powers up as an output. LSI Logic software also supports use of this signal as the enable line for V_{PP} the 12 Volt power supply to the external flash memory interface. GPIO[3:2] power up as inputs.
MAC/_ TESTOUT	79 K19	T/S	Memory Access Control. This pin can be programmed to indicate local or system memory accesses (non-PCI applications). It is also used to test the connectivity of the LSI53C895 signals using “AND tree” scheme. The MAC/_TESTOUT pin is only driven as the Test Out function when the TESTIN/ pin is driven LOW.

Table 4.11 Additional Signals (Cont.)

IRQ/	59 U20	O	Interrupt. This signal, when asserted LOW, indicates that an interrupting condition has occurred and that service is required from the host CPU. The output drive of this pin is programmed as either open drain with an internal weak pull-up or, optionally, as a totem pole driver. Refer to the description of the DMA Control (DCNTL) register, bit 3, for additional information.
BIG_LIT/	192 P3	I	Big_Little endian select. When this pin is driven LOW, the LSI53C895 routes the first byte of an aligned SCSI to PCI transfer to byte lane zero of the PCI bus and subsequent bytes received are routed to ascending lanes. An aligned PCI to SCSI transfer routes PCI byte lane zero onto the SCSI bus first, and transfers ascending byte lanes in order. When this pin is driven HIGH, the LSI53C895 routes the first byte of an aligned SCSI to PCI transfer to byte lane three of the PCI bus and subsequent bytes received are routed to descending lanes. An aligned PCI to SCSI transfer routes PCI byte lane three onto the SCSI bus first and transfer descending byte lanes in order. This mode of operation also applies to the external memory interface. When this pin is driven in Little Endian mode and the chip is performing a read from external memory, the byte of data accessed at location 0x00000 is routed to PCI byte lane zero and the data accessed at location 0x00003 is routed to PCI byte lane three. When the chip is performing a write to flash memory, PCI byte lane zero is routed to location 0x00000 and ascending byte lanes are routed to subsequent memory locations. When this pin is driven in Big Endian mode and the chip is performing a read from external memory, the byte of data accessed at location 0x00000 is routed to PCI byte lane three and the data accessed at location 0x00003 is routed to byte lane zero. When the chip is performing a write to flash memory, PCI byte lane three is routed to location 0x00000 and descending byte lanes are routed to subsequent memory locations.
Test Pins	82, 177, 180, 181, 182, 183 J1, J19, K1, L1, L2, L3	I/O	LSI Logic uses Test Pins for diagnostic testing. These pins should not be used in actual system design; they must be left floating or pulled HIGH.

Table 4.12 lists the External Memory Interface Signals group.

Table 4.12 External Memory Interface Signals

Name	Pin No. Ball No.	Type	Description
MAS0/	186 M2	O	Memory Address Strobe 0. This pin latches in the least significant address byte of an external EEPROM or flash memory. Since the LSI53C895 moves addresses eight bits at a time, this pin connects to the clock of an external bank of flip-flops that assemble up to a 20-bit address for the external memory.
MAS/1	185 M1	O	Memory Address Strobe 1. This pin latches in the address byte corresponding to address bits [15:8] of an external EEPROM or flash memory. Since the LSI53C895 moves addresses eight bits at a time, this pin connects to the clock of an external bank of flip-flops that assemble up to a 20-bit address for the external memory.
MAD[7:0]	See individual pin descriptions		The MAD[7:0] pins form the memory address/data bus. This bus is used in conjunction with the memory address strobe pins and external address latches to assemble up to a 20-bit address for an external EEPROM or flash memory. This bus puts out the most significant byte first and finishes with the least significant byte. It also writes data to a flash memory or read data into the chip from external EEPROM or flash memory. The eight signals on the MAD bus have specific functions. Refer to the individual pin descriptions below.
MAD[7:6]	69–70 N19, N20	I/O	MAD[7:6] enable different power-up options related to the external serial EEPROM interface. These options are programmed by connecting a 4.7 KΩ resistor between the appropriate MAD pin and V_{SS}. For more information, refer to the Serial EEPROM Interface section in Chapter 2 and the Subsystem ID/Subsystem Vendor ID register descriptions in Chapter 5. 00 Vendor specific information is automatically downloaded from the serial EEPROM through GPIO0 (clock) and GPIO1 (data) and loaded into PCI configuration registers 0x2C–0x2F 01 Reserved 10 No download is performed, however, the PCI configuration registers 0x2C–0x2F are now writable 11 Vendor-specific information is automatically downloaded from the EEPROM through GPIO0 (data) and GPIO1 (clock) and loaded into PCI configuration registers 0x2C–0x2F

Table 4.12 External Memory Interface Signals (Cont.)

MAD5	71 M18	I/O	The MAD5 pin enables/disables the 4 Kbytes of internal RAM on the LSI53C895. Pull this pin HIGH to enable the SCRIPTS RAM (default), and pull it LOW (with a 4 KΩ resistor) to disable the SCRIPTS RAM.
MAD4	72 M19	I/O	The MAD4 pin is reserved and should be pulled up. It may be used by LSI Logic in future devices.
MAD[3:1]	74–76 M20, L19, L20,	I/O	The MAD[3:1] pins set the size of the external parallel ROM device attached to the LSI53C895. Encoding for these pins is listed below (0 indicates a pull-down resistor is attached, 1 indicates a pull-up resistor is attached). 000 16 Kbytes 001 32 Kbytes 010 64 Kbytes 011 128 Kbytes 100 256 Kbytes 101 512 Kbytes 110 1024 Kbytes 111 No external memory present
MAD0	77 K20	I/O	MAD0 is the slow ROM pin. When pulled down, it enables two extra clock cycles of data access time. This accommodates a 200 ns memory device on the MAD bus. When the pin is HIGH, a 150 ns or faster memory device must be used.
MWE/	188 N2	O	Memory Write Enable. This pin writes the enable signal to an external flash memory.
MOE/	189 N3	O	Memory Output Enable. This pin is used as an output enable signal to an external EEPROM or flash memory during read operations.
MCE/	191, R1	O	Memory Chip Enable. This pin is used as a chip enable signal to an external EEPROM or flash memory device.

Chapter 5
Registers

This chapter contains descriptions of the PCI registers and the LSI53C895 operating registers. The terms “set” and “assert” refer to bits that are programmed to a binary one. Similarly, the terms “deassert,” “clear,” and “reset” refer to bits that are programmed to a binary zero. Reserved bit functions may be changed at any time. These bits should never be set by the user. Unless otherwise indicated, all bits in registers are active high, which means the feature is enabled by setting the bit. The bottom row of every register diagram shows the default register values that are enabled after the chip is powered on or reset.

This chapter includes these topics:

5.1 PCI Configuration Registers

Table 5.1 shows the PCI configuration registers implemented by the LSI53C895. Addresses 0x40 through 0x7F are not defined.

All PCI-compliant devices, such as the LSI53C895, must support the Vendor ID, Device ID, Command, and Status registers. Support of other PCI-compliant registers is optional. In the LSI53C895, registers that are not supported are not writable and return all zeroes when read. Only those registers and bits that are currently supported by the LSI53C895 are described in this chapter. For more detailed information on PCI registers, please see the PCI Local Bus Specification, Revision 2.1.

Table 5.1 PCI Configuration Register Map

31	16	15	0	
Device ID		Vendor ID		0x00
Status		Command		0x04
Class Code			Revision ID (Rev ID)	0x08
Not Supported	Header Type	Latency Timer	Cache Line Size	0x0C
Base Address Zero (I/O)[1]				0x10
Base Address One (Memory)[2]				0x14
RAM Base Address[3]				0x18
Not Supported				0x1C
Not Supported				0x20
Not Supported				0x24
Reserved				0x28
Subsystem ID		Subsystem Vendor ID		0x2C
Expansion ROM Base Address[4]				0x30
Reserved				0x34
Reserved				0x38
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x3C[5]

1. I/O Base is supported.
2. Memory Base is supported.
3. This register powers up enabled and can be disabled by pull-down resistors on the MAD5 pin.
4. If expansion memory is enabled through pull-down resistors on the MAD[7:0] bus.
5. Addresses 0x40 to 0x7F are not defined. All unsupported registers are not writable and return all zeros when read. Reserved registers also return zeros when read.

Register: 0x00–0x01
Vendor ID
Read Only

15															0
VID[15:0]															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

VID[15:0] **Vendor ID** **[15:0]**
This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Register: 0x02–0x03
Device ID
Read Only

15															0
DID[15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

DID[15:0] **Device ID** **[15:0]**
This 16-bit register identifies the particular device. The LSI53C895 Device ID is 0x000C.

Register: 0x04–0x05
Command
Read/Write

15							9	8	7	6	5	4	3	2	1	0
R								SE	R	EPER	R	WIE	R	EBM	EMS	EIS
x	x	x	x	x	x	x		0	x	0	x	0	x	0	0	0

The SCSI Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the LSI53C895 is logically disconnected from the PCI bus for all accesses except configuration accesses.

R	**Reserved**	**[15:9]**
SE	**SERR/ Enable** This bit enables the SERR/ driver. SERR/ is disabled when this bit is cleared. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.	**8**
R	**Reserved**	**7**
EPER	**Enable Parity Error Response** This bit allows the LSI53C895 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled and disabled with this bit. The LSI53C895 always generates parity for the PCI bus.	**6**
R	**Reserved**	**5**
WIE	**Write and Invalidate Enable** This bit allows the LSI53C895 to generate write and invalidate commands on the PCI bus. The WIE bit in the DMA Control (DCNTL) register must also be set for the device to generate Memory Write and Invalidate commands.	**4**
R	**Reserved**	**3**
EBM	**Enable Bus Mastering** This bit controls the ability of the LSI53C895 to act as a master on the PCI bus. A value of zero disables this device from generating PCI bus master accesses. A value of one allows the LSI53C895 to behave as a bus master. The device must be a bus master in order to fetch SCRIPTS instructions and transfer data.	**2**
EMS	**Enable Memory Space** This bit controls the ability of the LSI53C895 to respond to memory space accesses. A value of zero (0) disables the device response. A value of one (1) allows the LSI53C895 to respond to memory space accesses at the address range specified by the Base Address One (Memory) and RAM Base Address registers in the PCI configuration space.	**1**

EIS **Enable I/O Space** **0**
This bit controls the LSI53C895 response to I/O space accesses. A value of zero disables the device response. A value of one allows the LSI53C895 to respond to I/O space accesses at the address range specified by the Base Address Register Zero (I/O) register in the PCI configuration space.

Register: 0x06–0x07

Status
Read/Write

15	14	13	12	11	10	9	8	7		5	4	3			0
DPE	SSE	RMA	RTA	R	DT[1:0]		DPP	R			NC	R			
0	0	0	0	x	0	0	0	x	x	x	1	x	x	x	x

Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is cleared whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 0x8000 to the register.

DPE **Detected Parity Error (from Slave)** **15**
This bit is set by the LSI53C895 whenever it detects a data parity error, even if data parity error handling is disabled.

SSE **Signaled System Error** **14**
This bit is set whenever the device asserts the SERR/ signal.

RMA **Received Master Abort (from Master)** **13**
A master device should set this bit whenever its transaction (except for Special Cycle) is terminated with Master Abort.

RTA **Received Target Abort (from Master)** **12**
A master device should set this bit whenever its transaction is terminated by target abort.

R **Reserved** **11**

DT[10:9] **DEVSEL/ Timing** **[10:9]**
These bits encode the timing of DEVSEL/. These are encoded as:

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved.

These bits are read-only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C895 supports a value of 0b01.

DPR **Data Parity Error Reported** **8**
This bit is set when the following conditions are met:

- The bus agent asserted PERR/ itself or observed PERR/ asserted;
- The agent setting this bit acted as the bus master for the operation in which the error occurred and;
- The Parity Error Response bit in the Command register is set.

R **Reserved** **[7:0]**

Register: 0x08
Revision ID (Rev ID)
Read Only

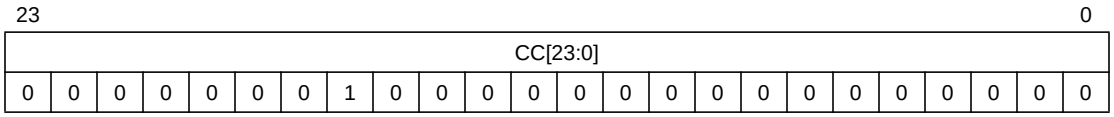
7							0
RID[7:0]							
0	0	0	0	x	x	x	x

RID[7:0] **Revision ID** **[7:0]**
This register specifies a device specific revision identifier. The upper nibble is always set to 0x0000. The lower nibble reflects the current revision level of the device. It should have the same value as the Chip Revision Level bits in the Chip Test Three (CTEST3) register.

Register: 0x09–0x0B

Class Code

Read Only



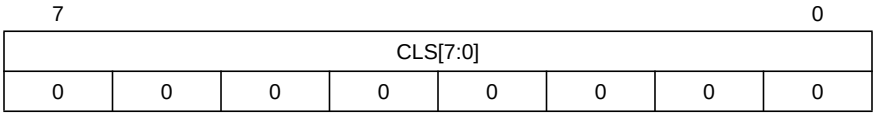
CC[23:0] **Class Code** **[23:0]**

This 24-bit register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 0x010000, which identifies a SCSI controller.

Register: 0x0C

Cache Line Size

Read/Write



CLS[7:0] **Cache Line Size** **[7:0]**

This register specifies the system cache line size in units of 32-bit words. Cache mode is enabled and disabled by the Cache Line Size Enable (CLSE) bit, bit 7 in the DMA Control (DCNTL) register. Setting this bit causes the LSI53C895 to align to cache line boundaries before allowing any bursting, except during memory moves in which the read and write addresses are not aligned to a burst size boundary. For more information on this register, see Section 3.3.1, “Support for PCI Cache Line Size Register.”

Register: 0x0D
Latency Timer
Read/Write

7							0
LT[7:0]							
0	0	0	0	0	0	0	0

LT[7:0] **Latency Timer** **[7:0]**
The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The SCSI functions of the LSI53C895 support this timer. All eight bits are writable, allowing latency values of 0–255 PCI clocks. Use the following equation to calculate an optimum latency value for the SCSI functions of the LSI53C895.

Latency = 2 + (Burst Size * (typical wait states + 1))

Values greater than optimum are also acceptable.

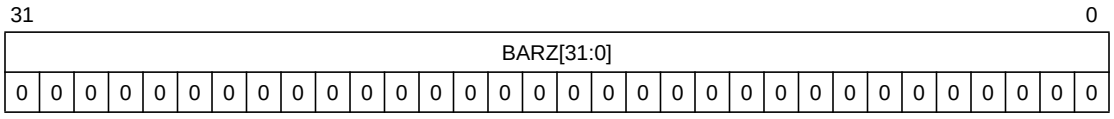
Register: 0x0E
Header Type
Read Only

7							0
HT[7:0]							
0	0	0	0	0	0	0	0

HT[7:0] **Header Type** **[7:0]**
This 8-bit register identifies the layout of bytes 0x10 through 0x3F in the configuration space and also whether or not the device contains multiple functions. The value of this register is 0x00.

Register: 0x10–0x13

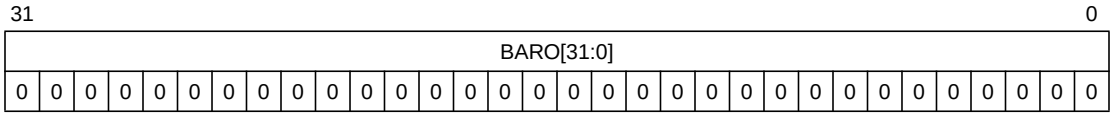
Base Address Register Zero (I/O)
Read/Write



BARZ[31:0] **Base Address Register Zero - I/O** **[31:0]**
This 32-bit base address register maps the operating register set into I/O space. Bit 1 is reserved and returns a zero on all reads, and the other bits are used to map the device into I/O space. For detailed information on the operation of this register, refer to the PCI Local Bus Specification, Revision 2.1.

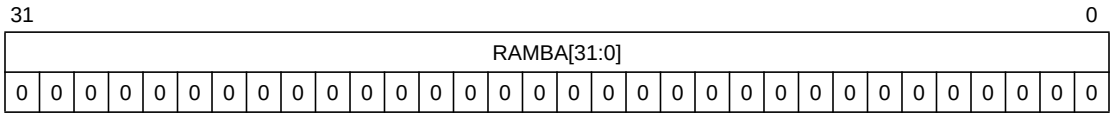
Register: 0x14–0x17

Base Address One (Memory)
Read/Write



BARO[31:0] **Base Address One - Memory** **[31:0]**
This 32-bit base address register maps the operating register set into memory space. Bit 0 is hardwired to zero. For detailed information on the operation of this register, refer to the PCI Local Bus Specification, Revision 2.1.

Register: 0x18–0x1B
RAM Base Address
Read/Write



RAMBA[31:0] **RAM Base Address** **[31:0]**
This 32-bit base address register holds the memory base address of the 4 Kbytes internal RAM. The user can read this register through the Scratch Register B (SCRATCHB) register in the operating register set when bit 3 of the Chip Test Two (CTEST2) register is set.

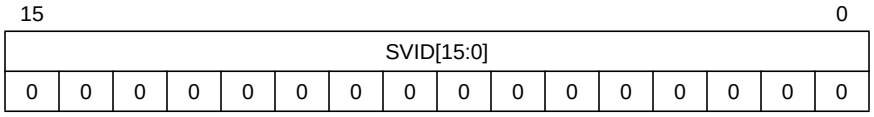
Register: 0x1C–0x1F
Not Supported

Register: 0x20–0x23
Not Supported

Register: 0x24–0x27
Not Supported

Register: 0x28–0x31
Reserved

Register: 0x2C–0x2D
Subsystem Vendor ID
Read Only



SVID[15:0] **Subsystem Vendor ID** **[15:0]**
This 16-bit register uniquely identifies the vendor manufacturing the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from other vendor cards, even if the cards have the same PCI

controller installed on them (and therefore the same Vendor ID and Device ID).

If the external serial EEPROM interface is enabled, this register is automatically loaded at power-up from the external serial EEPROM and contains the value downloaded from the serial EEPROM or a value of 0x0000 if the download fails. All of the bits in this register are cleared if serial EEPROM access is not enabled.

The 16-bit value that should be stored in the external serial EEPROM for this register is the vendor PCI Vendor ID and must be obtained from the PCI Special Interest Group (SIG). Refer to Section 2.6.2, "Serial EEPROM Interface," for more information on downloading a value for this register.

Register: 0x2E–0x2F

Subsystem ID
Read Only

15															0
SID[15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SID[15:0] **Subsystem ID** **[15:0]**

This 16-bit register uniquely identifies the add-in board or subsystem where the LSI53C895 resides. It provides a mechanism for an add-in card vendor to distinguish between its cards that use the same PCI controller installed on them (and therefore the same Vendor ID and Device ID).

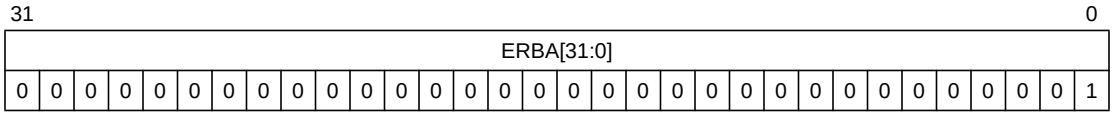
If the external serial EEPROM interface is enabled, this register is automatically loaded at power-up from the external serial EEPROM and contains the value downloaded from the serial EEPROM or a value of 0x0000 if the download fails. All of the bits in this register are cleared if the serial EEPROM access is not enabled. Refer to Section 2.6.2, "Serial EEPROM Interface," for additional information on downloading a value for this register.

In some operating system implementations, bit 15 of this register indicates whether the LSI53C895 is being

controlled by LSI Logic software or by a different device driver. A value of 0 indicates that the LSI Logic software controls the chip, and a value of 1 indicates another driver.

Register: 0x30–0x33

Expansion ROM Base Address
Read/Write



ERBA[31:0] **Expansion ROM Base Address** **[31:0]**

This four-byte register handles the base address and size information for the expansion ROM. It functions exactly like the Base Address Register Zero (I/O) and Base Address One (Memory) registers, except that the encoding of the bits is different. The upper 21 bits correspond to the upper 21 bits of the expansion ROM base address.

The Expansion ROM Enable bit, bit 0, is the only bit defined in this register. This bit controls whether or not the device accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled, and a device is used with or without an expansion ROM depending on the system configuration. To access the external memory interface, also set the Memory Space bit in the Command register.

The host system detects the size of the external memory by first writing the Expansion ROM Base Address register with all ones and then reading back the register. The SCSI functions of the LSI53C895 respond with zeros in all don't care locations. The ones in the remaining bits represent the binary version of the external memory size. For example, to indicate an external memory size of 32 Kbytes, this register, when written with ones and read back, returns ones in the upper 17 bits.

Register: 0x34–0x3B
Reserved

Register: 0x3C
Interrupt Line
Read/Write

7							0
IL[7:0]							
0	0	0	0	0	0	0	0

IL[7:0] **Interrupt Line** **[7:0]**
This register communicates interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value in this register tells which input of the system interrupt controller(s) the device interrupt pin is connected to. Values in this register are specified by system architecture.

Register: 0x3D
Interrupt Pin
Read Only

7							0
IP[7:0]							
0	0	0	0	0	0	0	1

IP[7:0] **Interrupt Pin** **[7:0]**
This register specifies the interrupt pin that the device uses. Its value is set to 0x01 for the INTA/ signal.

Register: 0x3E

Min_Gnt
Read Only

7							0
MG[7:0]							
0	0	0	1	0	0	0	1

MG[7:0] **Min_Gnt** **[7:0]**
This register specifies the desired settings for latency timer values. Min_Gnt specifies how long a burst period the device needs. The value specified in these registers is in units of 0.25 microseconds. The LSI53C895 sets this register to 0x11.

Register: 0x3F

Max_Lat
Read Only

7							0
ML[7:0]							
0	1	0	0	0	0	0	0

ML[7:0] **Max_Lat** **[7:0]**
This register specifies the desired settings for latency timer values. Max_Lat specifies how often the device needs to gain access to the PCI bus. The value specified in these registers is in units of 0.25 microseconds. The LSI53C895 SCSI function sets this register to 0x40.

5.2 SCSI Registers

Table 5.2, the register map, lists registers by operating address.

Note: The only register that the host CPU can access while the LSI53C895 is executing SCRIPTS is the Interrupt Status (ISTAT) register. Attempts to access other registers interferes with the operation of the chip. However, all operating registers are accessible with SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

Note: The LSI53C895 cannot fetch SCRIPTS instructions from the operating register space. Instructions must be fetched from system memory or the internal SCRIPTS RAM.

Table 5.2 SCSI Register Map

SCNTL3	SCNTL2	SCNTL1	SCNTL0	0x00
GPREG	SDID	SXFER	SCID	0x04
SBCL	SSID	SOCL	SFBR	0x08
SSTAT2	SSTAT1	SSTAT0	DSTAT	0x0C
DSA				0x10
RESERVED			ISTAT	0x14
CTEST3	CTEST2	CTEST1	RESERVED	0x18
TEMP				0x1C
CTEST6	CTEST5	CTEST4	DFIFO	0x20
DCMD		DBC		0x24
DNAD				0x28
DSP				0x2C
DSPS				0x30
SCRATCHA				0x34
DCNTL	SBR	DIEN	DMODE	0x38
ADDER				0x3C
SIST1	SIST0	SIEN1	SIEN0	0x40
GPCNTL	MACNTL	SWIDE	SLPAR	0x44
RPID1	RPID0	STIME1	STIME0	0x48
STEST3	STEST2	STEST1	STEST0	0x4C
RESERVED	STEST4	SIDL		0x50
RESERVED		SODL		0x54
RESERVED		SBDL		0x58
SCRATCHB				0x5C
SCRATCHC				0x60
SCRATCHD				0x64
SCRATCHE				0x68
SCRATCHF				0x6C
SCRATCHG				0x70
SCRATCHH				0x74
SCRATCHI				0x78
SCRATCHJ				0x7F

Register: 0x00
SCSI Control Zero (SCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ARB1[1:0]		START	WATN	EPC	R	AAP	TRG
1	1	0	0	0	x	0	0

ARB1[1:0] Arbitration Mode Bits 1 and 0 [7:6]

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection/reselection

Simple Arbitration

1. The LSI53C895 waits for a bus free condition to occur.
2. It asserts SBSY/ and its SCSI ID (contained in the SCSI Chip ID (SCID) register) onto the SCSI bus. If the SSEL/ signal is asserted by another SCSI device, the LSI53C895 deasserts SBSY/, deasserts its ID and sets the Lost Arbitration bit (bit 3) in the SCSI Status Zero (SSTAT0) register.
3. After an arbitration delay, the CPU should read the SCSI Bus Data Lines (SBDL) register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the LSI53C895 has won arbitration.
4. Once the LSI53C895 has won arbitration, SSEL/ must be asserted by using the SCSI Output Control Latch (SOCL) for a bus clear plus a bus settle delay (1.2 µs) before a low-level selection can be performed.

Full Arbitration, Selection/Reselection

1. The LSI53C895 waits for a bus free condition.
2. It asserts SBSY/ and its SCSI ID (the highest priority ID stored in the SCSI Chip ID (SCID) register) onto the SCSI bus.
3. If the SSEL/ signal is asserted by another SCSI device or if the LSI53C895 detects a higher priority ID, the LSI53C895 deasserts SBSY, deasserts its ID, and waits until the next bus free state to try arbitration again.
4. The LSI53C895 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SCSI Status Zero (SSTAT0) register, bit 2.
5. The LSI53C895 performs selection by asserting the following onto the SCSI bus: SSEL/, the target ID (stored in the SCSI Destination ID (SDID) register), and the LSI53C895 ID (stored in the SCSI Chip ID (SCID) register).
6. After a selection is complete, the Function Complete bit is set in the SCSI Interrupt Status Zero (SIST0) register, bit 6.
7. If a selection timeout occurs, the Selection Timeout bit is set in the SCSI Interrupt Status One (SIST1) register, bit 2.

START **Start Sequence** **5**

When this bit is set, the LSI53C895 starts the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low-level mode. During SCSI SCRIPTS operations, the SCRIPTS processor controls this bit. An arbitration sequence should not be started if the connected (CON) bit in the SCSI Control One (SCNTL1) register, bit 4, indicates that the LSI53C895 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCSI Control One (SCNTL1) register should be checked to verify that the LSI53C895 did not connect to the SCSI bus.

WATN	**Select with SATN/ on a Start Sequence** When this bit is set and the LSI53C895 is in initiator mode, the SATN/ signal is asserted during LSI53C895 selection of a SCSI target device. This is to inform the target that the LSI53C895 has a message to send. If a selection timeout occurs while attempting to select a target device, SATN/ is deasserted at the same time SSEL/ is deasserted. When this bit is cleared, the SATN/ signal is not asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low-level mode.	**4**
EPC	**Enable Parity Checking** When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. Parity is also checked as data goes from the SCSI FIFO to the DMA FIFO. If a parity error is detected, bit 0 of the SCSI Interrupt Status Zero (SIST0) register is set and an interrupt may be generated. If the LSI53C895 is operating in initiator mode and a parity error is detected, SATN/ can optionally be asserted, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.	**3**
R	**Reserved**	**2**
AAP	**Assert SATN/ on Parity Error** When this bit is set, the LSI53C895 automatically asserts the SATN/ signal upon detection of a parity error. SATN/ is only asserted in initiator mode. The SATN/ signal is asserted before deasserting SACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the LSI53C895 to assert SATN/ in this manner. A parity error is detected on data received from the SCSI bus. If the Assert SATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, SATN/ is not automatically asserted on the SCSI bus when a parity error is received.	**1**

TRG **Target Mode** **0**

This bit determines the default operating mode of the LSI53C895. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET TARGET or CLEAR TARGET). When this bit is set, the chip is a target device by default. When this bit is cleared, the LSI53C895 is an initiator device by default.

Caution: Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator modes.

Register: 0x01

SCSI Control One (SCNTL1)

Read/Write

7	6	5	4	3	2	1	0
EXC	ADB	DHP	CON	RST	AESP	IARB	SST
0	0	0	0	0	0	0	0

EXC **Extra Clock Cycle of Data Setup** **7**

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design margin, though it affects the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time. Setting this bit only affects SCSI send operations.

ADB **Assert SCSI Data Bus** **6**

When this bit is set, the LSI53C895 drives the contents of the SCSI Output Data Latch (SODL) onto the SCSI data bus. When the LSI53C895 is an initiator, the SCSI I/O signal must be inactive to assert the SCSI Output Data Latch (SODL) contents onto the SCSI bus. When the LSI53C895 is a target, the SCSI I/O signal must be active for the SCSI Output Data Latch (SODL) contents to be asserted onto the SCSI bus. The contents of the SCSI Output Data Latch (SODL) register can be asserted at any time, even before the LSI53C895 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low-level mode.

DHP **Disable Halt on Parity Error or ATN (Target Only)** **5**

The DHP bit is only defined for target mode. When this bit is cleared, the LSI53C895 halts the SCSI data transfer when a parity error is detected or when the SATN/ signal is asserted. If SATN/ or a parity error is received in the middle of a data transfer, the LSI53C895 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the LSI53C895 transfers data until there are no outstanding synchronous offsets. If the LSI53C895 is receiving data, any data residing in the DMA FIFO is sent to memory before halting.

When this bit is set, the LSI53C895 does not halt the SCSI transfer when SATN/ or a parity error is received.

CON **Connected** **4**

This bit is automatically set any time the LSI53C895 is connected to the SCSI bus as an initiator or as a target. It is set after the LSI53C895 successfully completes arbitration or when it has responded to a bus initiated selection or reselection. This bit is also set after the chip wins simple arbitration when operating in low-level mode. When this bit is cleared, the LSI53C895 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

RST **Assert SCSI RST/ Signal** **3**

Setting this bit asserts the SRST/ signal. The SRST/ output remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop.

AESP **Assert Even SCSI Parity (force bad parity)** **2**

When this bit is set, the LSI53C895 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the LSI53C895. If parity checking is enabled, then the LSI53C895 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

IARB **Immediate Arbitration** **1**

Setting this bit causes the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multithreaded applications. The ARB[1:0] bits in SCSI Control Zero (SCNTL0) should be set for full arbitration and selection before setting this bit.

Arbitration is retried until won. At that point, the LSI53C895 holds SBSY and SSEL asserted, and waits for a select or reselect sequence to be requested. The Immediate Arbitration bit is reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition clears IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCSI Control Two (SCNTL2), bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the Interrupt Status (ISTAT) register should be set. Then one of two things will eventually happen:

- The Won Arbitration bit (SCSI Status Zero (SSTAT0), bit 2) is set. In this case, the Immediate Arbitration bit needs to be reset. This completes the abort sequence and disconnects the LSI53C895 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low-level selection may be performed instead.
- The abort completes because the LSI53C895 loses arbitration. This can be detected by the Immediate Arbitration bit being cleared. The Lost Arbitration bit (SCSI Status Zero (SSTAT0), bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

SST **Start SCSI Transfer** **0**

This bit is automatically set during SCRIPTS execution and should not be used. It causes the SCSI core to begin a SCSI transfer and includes SREQ/SACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O

bit in the SCSI Output Control Latch (SOCL) register. This bit is self-clearing. It should not be set for low-level operation.

Caution: Writing to this register while not connected may cause the loss of a selection/reselection by clearing the Connected bit.

Register: 0x02

SCSI Control Two (SCNTL2)
Read/Write

7	6	5	4	3	2	1	0
SDU	CHM	SLPMD	SLPHBEN	WSS	VUE0	VUE1	WSR
0	0	0	0	0	0	0	0

SDU **SCSI Disconnect Unexpected** **7**

This bit is valid in initiator mode only. When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error is generated (see the Unexpected Disconnect bit in the SCSI Interrupt Status Zero (SIST0) register, bit 2). During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write (MOVE 0x00 TO SCSI Control Two (SCNTL2)) before the SCSI core expects a disconnect to occur. This occurs normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting SACK/ after receiving a Disconnect command or Command Complete message.

CHM **Chained Mode** **6**

This bit determines whether or not the SCSI core is programmed for chained SCSI mode. This bit is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode primarily transfers consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte

boundary, the LSI53C895 stores the last byte in the SCSI Wide Residue (SWIDE) register during a receive operation, or in the SCSI Output Data Latch (SODL) register during a send operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

SLPMD **SLPAR Mode Bit** **5**

If this bit is clear, the SCSI Longitudinal Parity (SLPAR) register functions like the LSI53C825. If this bit is set, the SCSI Longitudinal Parity (SLPAR) register reflects the high or low byte of the SLPAR word, depending on the state of SCSI Control Two (SCNTL2), bit 4. It also allows a seed value to be written to the SCSI Longitudinal Parity (SLPAR) register.

SLPHBEN **SLPAR High Byte Enable** **4**

If this bit is clear, the low byte of the SLPAR word is accessible through the SCSI Longitudinal Parity (SLPAR) register. If this bit is set, the high byte of the SLPAR word is present in the SCSI Longitudinal Parity (SLPAR) register.

WSS **Wide SCSI Send** **3**

When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit clears the WSS flag. This clearing function is self-clearing.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of “chain” data in the SCSI Output Data Latch (SODL) register. This data becomes the first low-order byte sent when *married* with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation clears this bit. Also, performing any non-wide transfer clears this bit.

VUE0 **Vendor Unique Enhancements bit 0** **2**

This bit is a read only value indicating whether the group code field in the SCSI instruction is standard or vendor unique. If reset, the bit indicates standard group codes. If set, the bit indicates vendor unique group codes. The value in this bit is reloaded at the beginning of all asynchronous target receives. The default for this bit is reset.

VUE1 **Vendor Unique Enhancements bit 1** **1**

This bit disables the automatic byte count reload during Block Move instructions in the command phase. If this bit is reset, the device reloads the Block Move byte count when the first byte received is one of the standard group codes. If this bit is set, the device does not reload the Block Move byte count, regardless of the group code.

WSR **Wide SCSI Receive** **0**

When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Setting this bit clears the WSR flag. This clearing function is self-clearing.

The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or nonchained block move command, and temporarily stores the high-order byte in the SCSI Wide Residue (SWIDE) register rather than passing the byte out the DMA channel. The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SWIDE may be “residue” data, valid data for a subsequent data transfer, or overrun data. The byte may be read as normal data by starting a data receive transfer.

Performing a SCSI send operation clears this bit. Also, performing any nonwide transfer clears this bit.

Register: 0x03

SCSI Contr0l Three (SCNTL3)

Read/Write

7	6		4	3	2	1	0
ULTRA	SCF[2:0]			EWS	CCF[2:0]		
0	0	0	0	0	0	0	0

ULTRA **Ultra Enable** **7**

Setting this bit enables Ultra SCSI or Ultra2 SCSI synchronous transfer rates. The default value of this bit is 0. This bit should remain cleared if the LSI53C895 is not operating in Ultra SCSI mode or faster.

Set this bit to achieve Ultra SCSI transfer rates in legacy systems that use an 80 MHz clock.

When this bit is set, the signal filtering period for SREQ/ and SACK/ automatically changes to 8 ns for Ultra2 SCSI or 15 ns for Ultra SCSI, regardless of the value of the Extend REQ/ACK Filtering bit in the SCSI Test Two (STEST2) register.

SCF[2:0] **Synchronous Clock Conversion Factor [6:4]**
These bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The bits are encoded as per Table 5.3. For synchronous receive, the output of this divider is always divided by 4 and that value determines the transfer rate. For example, if SCLK is 160 MHz, and the SCF value is set to divide by one, then the maximum synchronous receive rate is 40 MHz ((160/1)/4 = 40).

For synchronous send, the output of this divider gets divided by the transfer period (XFERP) bits in the SCSI Transfer (SXFER) register, and that value determines the transfer rate. For valid combinations of the SCF and XFERP, see Table 5.5 and Table 5.6.

Table 5.3 Synchronous Clock Conversion Factor

SCF2	SCF1	SCF0	Factor Frequency
0	0	0	SCLK/3
0	0	1	SCLK/1
0	1	0	SCLK/1.5
0	1	1	SCLK/2
1	0	0	SCLK/3
1	0	1	SCLK/4
1	1	0	SCLK/6
1	1	1	SCLK/8

For additional information on how the synchronous transfer rate is determined, refer to Chapter 2, “Functional Description.”

EWS **Enable Wide SCSI 3**
When this bit is cleared, all information transfer phases are assumed to be eight bits, and transmitted on SD[7:0]/, SDP0/. When this bit is asserted, data transfers

are done 16 bits at a time, with the least significant byte on SD[7:0]/, SDP/ and the most significant byte on SD[15:8]/, SDP1/. Command, Status, and Message phases are not affected by this bit.

Clearing this bit also clears the Wide SCSI Receive bit in the SCSI Control Two (SCNTL2) register, which indicates the presence of a valid data byte in the SCSI Wide Residue (SWIDE) register.

CCF[2:0] **Clock Conversion Factor** **[2:0]**

These bits select the frequency of the SCLK for asynchronous SCSI operations. The bits are encoded as per Table 5.4.

Table 5.4 Asynchronous Clock Conversion Factor

CCF2	CCF1	CCF0	SCSI Clock (MHz)
0	0	0	50.01–75
0	0	1	16.67–25
0	1	0	25.01–37.5
0	1	1	37.51–50
1	0	0	50.01–75
1	0	1	75.01–80.00
1	1	0	120 (not normally used)
1	1	1	160 (with clock quadrupler and 40 MHz clock)

For additional information on how the synchronous transfer rate is determined, refer to Chapter 2, “Functional Description.”

Register: 0x04
SCSI Chip ID (SCID)
Read/Write

7	6	5	4	3			0
R	RRE	SRE	R	ENC[3:0]			
x	0	0	x	0	0	0	0

R **Reserved** **7**

RRE **Enable Response to Reselection** **6**
When this bit is set, the LSI53C895 is enabled to respond to bus-initiated reselection at the chip ID in the Response ID Zero (RESPID0) and Response ID One (RESPID1) registers. Note that the LSI53C895 does not automatically reconfigure itself to initiator mode as a result of being reselected.

SRE **Enable Response to Selection** **5**
When this bit is set, the LSI53C895 is able to respond to bus-initiated selection at the chip ID in the Response ID Zero (RESPID0) and Response ID One (RESPID1) registers. Note that the LSI53C895 does not automatically reconfigure itself to target mode as a result of being selected.

R **Reserved** **4**

ENC **Encoded Chip SCSI ID** **[3:0]**
These bits store the LSI53C895 encoded SCSI ID. This is the ID that the chip asserts when arbitrating for the SCSI bus. The IDs that the LSI53C895 responds to when being selected or reselected are configured in the Response ID Zero (RESPID0) and Response ID One (RESPID1) registers. The priority of the 16 possible IDs, in descending order is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

Register: 0x05
SCSI Transfer (SXFER)
Read/Write

7			5	4				0
TP[2:0]				MO[4:0]				
0	0	0		0	0	0	0	0

When using Table Indirect I/O commands, bits [7:0] of this register are loaded from the I/O data structure.

For additional information on how the synchronous transfer rate is determined, refer to Chapter 2, "Functional Description."

TP[2:0] **SCSI Synchronous Transfer Period [7:5]**
These bits determine the SCSI synchronous transfer period (XFERP) used by the LSI53C895 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

For Ultra SCSI transfers, the ideal transfer period is 4, and 5 is acceptable. Setting the transfer period to a value greater than 5 is not recommended.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

Use this formula to calculate the synchronous send and receive rates. Table 5.5 and Table 5.6 show examples of possible bit combinations.

Formula:

Synchronous Send Rate = (SCLK/SCF) / XFERP

Synchronous Receive Rate = (SCLK/SCF) / 4

Key:

SCLK = SCSI Clock

CF = Synchronous Clock Conversion Factor, SCNTL3 bits [6:4]

XFERP = Transfer period, SCSI Transfer (SXFER) register bits [7:5]

Table 5.5 Examples of Synchronous Transfer Periods and Rates for SCSI-1

SCLK (MHz)	SCF (SCNTL3 Bits [6:4])	XFERP (SXFER Bits [7:5])	Sync Send Rate (Mbytes/s)	Sync Send Period (ns)	Sync Receive Rate (Mbytes/s)	Synch Receive Period (ns)
80	÷ 4	4	5	200	5	200
80	÷ 4	5	4	250	5	200
66.67	÷ 3	4	5.55	180	5.55	180
66.67	÷ 3	5	4.44	225	5.55	180
50	÷ 2	4	6.25	160	6.25	160
50	÷ 2	5	5	200	6.25	160
40	÷ 2	4	5	200	5	200
37.50	÷ 1.5	4	6.25	160	6.25	160
33.33	÷ 1.5	4	5.55	180	5.55	180
25	÷ 1	4	6.25	160	6.25	160
20	÷ 1	4	5	200	5	200
16.67	÷ 1	4	4.17	240	4.17	240

Table 5.6 Example Synchronous Transfer Periods and Rates for Fast SCSI, Ultra SCSI, and Ultra2 SCSI

SCLK (MHz)	SCF (SCNTL3 Bits [6:4])	XFERP (SXFER Bits [7:5])	Sync Send Rate (Mbytes/s)	Sync Send Period (ns)	Sync Receive Rate (Mbytes/s)	Synch Receive Period (ns)
160	÷ 1	4	40	25	40	25
80	÷ 1	4	20	50	20	50
80	÷ 2	4	10	100	10	100
66.67	÷ 1.5	4	11.11	90	11.11	90
66.67	÷ 1	5	8.88	112.5	11.11	90
50	÷ 1	4	12.5	80	12.5	80
50	÷ 1	5	10	100	12.5	80
40	÷ 1	4	10	100	10	100
37.50	÷ 1	4	9.375	106.67	9.375	106.67
33.33	÷ 1	4	8.33	120	8.33	120
25	÷ 1	4	6.25	160	6.25	160
20	÷ 1	4	5	200	5	200
16.67	÷ 1	4	4.17	240	4.17	240

MO[4:0] **Max SCSI Synchronous Offset** **[4:0]**

These bits describe the maximum SCSI synchronous offset used by the LSI53C895 when transferring synchronous SCSI data in either initiator or target mode. Table 5.7 describes the possible combinations and their relationship to the synchronous data offset used by the LSI53C895. These bits determine the LSI53C895 method of transfer for Data In and Data Out phases only; all other information transfers occur asynchronously.

Table 5.7 Maximum Synchronous Offset

MO4	MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0	0-Asynchronous
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Register: 0x06
SCSI Destination ID (SDID)
Read/Write

7			4	3			0
R				ENC[3:0]			
x	x	x	x	0	0	0	0

R **Reserved** **[7:4]**

ENC **Encoded SCSI Destination ID** **[3:0]**
Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases. When executing SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The user defines the SCSI ID in a SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the 16 possible IDs, in descending order, is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	0	9	8

Register: 0x07
General Purpose (GPREG)
Read/Write

7			5	4			0
R				GPIO[4:0]			
x	x	x	0	x	x	x	x

R **Reserved** **[7:5]**

GPIO[4:0] **General Purpose** **[4:0]**
These bits can be programmed through the General Purpose Pin Control (GPCNTL) register to become inputs, outputs or to perform special functions. As an output, these pins can enable or disable external terminators. These signals can also be programmed as live inputs and sensed through a SCRIPTS Register to Register Move Instruction. GPIO[3:0] default as inputs and GPIO4 defaults as an output pin.

GPIO4 can be used to enable or disable V_{PP}, the 12 V power supply to the external flash memory. This bit powers up with the power to the external memory disabled.

LSI Logic software uses the GPIO0 pin to toggle SCSI device LEDs, turning on the LED whenever the LSI53C895 is on the SCSI bus. This software drives the pin low to turn on the LED or drives it high to turn off the LED.

LSI Logic software uses the GPIO[1:0] pins to support serial EEPROM access. When serial EEPROM access is enabled, GPIO1 is used as a clock and GPIO0 is used as data.

Register: 0x08

SCSI First Byte Received (SFBR)
Read/Write

7							0
1B[7:0]							
0	0	0	0	0	0	0	0

This register contains the first byte received in any asynchronous information transfer phase. For example, when the LSI53C895 is operating in initiator mode, this register contains the first byte received in the Message In, Status, and Data In phases.

When a Block Move instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable through the CPU, and therefore not by a Memory Move. The Load instruction may not be used to write to this register. However, it can be loaded by using SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate LSI53C895 register (such as the SCRATCH register), and then to the SFBR.

This register also contains the state of the lower eight bits of the SCSI data bus during the selection phase if the COM bit in the DMA Control (DCNTL) register is clear.

Register: 0x09

SCSI Output Control Latch (SOCL)
Read /Write

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
0	0	0	0	0	0	0	0

REQ	**Assert SCSI REQ/ Signal**	**7**
ACK	**Assert SCSI ACK/ Signal**	**6**
BSY	**Assert SCSI BSY/ Signal**	**5**
SEL	**Assert SCSI SEL/ Signal**	**4**
ATN	**Assert SCSI ATN/ Signal**	**3**
MSG	**Assert SCSI MSG/ Signal**	**2**
C/D	**Assert SCSI C_D/ Signal**	**1**
I/O	**Assert SCSI I_O/ Signal**	**0**

This register is used primarily for diagnostic testing or programmed I/O operation. The SCRIPTS processor controls this register when executing SCSI SCRIPTS. SOCL should only be used when transferring data through programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the LSI53C895 starts executing normal SCSI SCRIPTS.

Register: 0x0A

SCSI Selector ID (SSID)

Read Only

7	6		4	3			0
VAL	R			ENID[3:0]			
0	x	x	x	0	0	0	0

VAL **SCSI Valid** **7**

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

R **Reserved** **[6:4]**

ENID **Encoded SCSI Destination ID** **[3:0]**

Reading the SCSI Selector ID (SSID) register immediately after the LSI53C895 has been selected or reselected returns the binary-encoded SCSI ID of the device that performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register: 0x0B

SCSI Bus Control Lines (SBCL)

Read Only

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
x	x	x	x	x	x	x	x

REQ	**SREQ/ Status**	**7**
ACK	**SACK/ Status**	**6**
BSY	**SBSY/ Status**	**5**
SEL	**SSEL/ Status**	**4**
ATN	**SATN/ Status**	**3**
MSG	**SMSG/ Status**	**2**
C/D	**SC_D/ Status**	**1**
I/O	**SI_O/ Status**	**0**

When read, this register returns the SCSI control line status. A bit is set when the corresponding SCSI control line is asserted. These bits are not latched. They are a true representation of what is on the SCSI bus at the time the register is read. The resulting read data is synchronized before being presented to the PCI bus to prevent parity errors from being passed to the system. This register can be used for diagnostics testing or operation in low-level mode.

Register: 0x0C
DMA Status (DSTAT)
Read Only

7	6	5	4	3	2	1	0
DFE	MDPE	BF	ABRT	SSI	SIR	R	IID
1	0	0	0	0	0	x	0

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the LSI53C895 stacks interrupts). The DIP bit in the Interrupt Status (ISTAT) register is also cleared. DMA interrupt conditions may be individually masked through the DMA Interrupt Enable (DIEN) register.

When performing consecutive 8-bit reads of the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), and SCSI Interrupt Status One (SIST1) registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure that the interrupts clear properly. Refer to Chapter 2, “Functional Description,” for more information on interrupts.

DFE **DMA FIFO Empty** **7**
This status bit is set when the DMA FIFO is empty. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and does not cause an interrupt.

MDPE **Master Data Parity Error** **6**
This bit is set when the LSI53C895 as a master detects a data parity error, or a target device signals a parity error during a data phase. The Master Parity Error Enable bit (bit 3 of Chip Test Four (CTEST4)) completely disables this MDPE, bit 6.

BF **Bus Fault** **5**
This bit is set when a PCI bus fault condition is detected. A PCI bus fault can only occur when the LSI53C895 is bus master, and is defined as a cycle that ends with a Bad address or Target Abort Condition.

ABRT **Aborted** **4**
This bit is set when an abort condition occurs. An abort condition occurs when a software abort command is

issued by setting bit 7 of the Interrupt Status (ISTAT) register.

SSI **Single-Step Interrupt** **3**
If the Single-Step Mode bit in the DMA Control (DCNTL) register is set, this bit is set and an interrupt generated after successful execution of each SCRIPTS instruction.

SIR **SCRIPTS Interrupt Instruction Received** **2**
This status bit is set whenever an Interrupt instruction is evaluated as true.

R **Reserved** **1**

IID **Illegal Instruction Detected** **0**
This status bit is set any time an illegal or Reserved instruction op code is detected, whether the LSI53C895 is operating in single-step mode or automatically executing SCSI SCRIPTS. Any of the following conditions during instruction execution also sets this bit:

- The LSI53C895 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.
- A Block Move instruction is executed with 0x000000 loaded into the DMA Byte Counter (DBC) register, indicating that zero bytes are to be moved.
- During a Transfer Control instruction, the Compare Data (bit 18) and Compare Phase (bit 17) bits are set in the DMA Byte Counter (DBC) register while the LSI53C895 is in target mode.
- During a Transfer Control instruction, the Carry Test bit (bit 21) is set and either the Compare Data (bit 18) or Compare Phase (bit 17) bit is set.
- A Transfer Control instruction is executed with the Reserved bit 22 set.
- A Transfer Control instruction is executed with the Wait for Valid phase bit (bit 16) set while the chip is in target mode.
- A Load/Store instruction is issued with the memory address mapped to the operating registers of the chip, not including ROM or RAM.

- A Load/Store instruction is issued when the register address is not aligned with the memory address.
- A Load/Store instruction is issued with bit 5 in the DMA Command (DCMD) register clear or bits 3 or 2 set.
- A Load/Store instruction is issued when the count value in the DMA Byte Counter (DBC) register is not set at 1 to 4.
- A Load/Store instruction attempts to cross a Dword boundary.
- A Memory Move instruction is executed with one of the Reserved bits in the DMA Command (DCMD) register set.
- A Memory Move instruction is executed with the source and destination addresses not byte-aligned.

Register: 0x0D

SCSI Status Zero (SSTAT0)

Read Only

7	6	5	4	3	2	1	0
ILF	ORF	OLF	AIP	LOA	WOA	RST	SDP0/
0	0	0	0	0	0	0	0

ILF **SIDL Least Significant Byte Full** **7**

This bit is set when the least significant byte in the SCSI Input Data Latch (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch (SIDL) register before being sent to the DMA FIFO and then to the host bus. The SCSI Input Data Latch (SIDL) register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

ORF **SODR Least Significant Byte Full** **6**

This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be

read or written by the user. Use this bit to determine how many bytes reside in the chip when an error occurs.

OLF **SODL Least Significant Byte Full** **5**
This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SCSI Output Data Latch (SODL) register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. Use this bit to determine how many bytes reside in the chip when an error occurs.

AIP **Arbitration in Progress** **4**
Arbitration in Progress (AIP = 1) indicates that the LSI53C895 has detected a Bus Free condition, asserted SBSY, and asserted its SCSI ID onto the SCSI bus.

LOA **Lost Arbitration** **3**
When set, LOA indicates that the LSI53C895 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

WOA **Won Arbitration** **2**
When set, WOA indicates that the LSI53C895 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCSI Control Zero (SCNTL0) register must be full arbitration and selection for this bit to be set.

RST/ **SCSI RST/ Signal** **1**
This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the Interrupt Status (ISTAT) register. This bit is not latched and may be changing when read.

SDP0/ **SCSI SDP0/ Parity Signal** **0**

This bit represents the active HIGH current status of the SCSI SDP0/ parity signal. This signal is not latched and may be changing as it is read.

Register: 0x0E

SCSI Status One (SSTAT1)

Read Only

7	6	5	4	3	2	1	0
FF3	FF2	FF1	FF0	SDP0L	MSG	C/D	I/O
0	0	0	0	x	x	x	x

FF[3:0] **(FIFO Flags)** **[7:4]**

These four bits, along with SCSI Status Two (SSTAT2), bit 4, define the number of bytes or words that currently reside in the LSI53C895 SCSI synchronous data FIFO. These bits are not latched, and they change as data moves through the FIFO.

FF4 (SSTAT2 bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12

FF4 (SSTAT2 bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

SDP0L **Latched SCSI Parity** **3**

This bit reflects the SCSI parity signal (SDP0/), corresponding to the data latched in the SCSI Input Data Latch (SIDL). It changes when a new byte is latched into the least significant byte of the SCSI Input Data Latch (SIDL) register. This bit is active HIGH, in other words, it is set when the parity signal is active.

MSG	**SCSI MSG/ Signal**	**2**
C/D	**SCSI C_D/ Signal**	**1**
I/O	**SCSI I_O/ Signal** These SCSI phase status bits are latched on the asserting edge of SREQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low-level mode.	**0**

Register: 0x0F

SCSI Status Two (SSTAT2)
Read Only

7	6	5	4	3	2	1	0
ILF1	ORF1	OLF1	FF4	SPL1	DM	LDSC	SDP1
0	0	0	0	x	x	1	x

LF1	**SIDL Most Significant Byte Full** This bit is set when the most significant byte in the SCSI Input Data Latch (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch (SIDL) register before being sent to the DMA FIFO and then to the host bus. The SCSI Input Data Latch (SIDL) register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.	**7**
ORF1	**SODR Most Significant Byte Full** This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. Use this bit to determine how many bytes reside in the chip when an error occurs.	**6**
OLF1	**SODL Most Significant Byte Full** This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SCSI Output Data Latch (SODL) register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output	**5**

Data Latch (SODL) register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. Use this bit to determine how many bytes reside in the chip when an error occurs.

FF4 **FIFO Flags bit 4** **4**
This is the most significant bit in the SCSI FIFO Flags field, with the reset of the bits in SCSI Status One (SSTAT1). For a complete description of this field, see the definition for SCSI Status One (SSTAT1), bits [7:4].

SPL1 **Latched SCSI parity for SD[15:8]** **3**
This active HIGH bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SCSI Input Data Latch (SIDL) register.

DM **DIFFSENS Mismatch** **2**
This bit is set when the DIFFSENS pin detects a SE or LVD SCSI operating voltage level while the LSI53C895 is operating in high-power differential mode (by setting the DIF bit in the SCSI Test Two (STEST2) register). If this bit is reset, the DIFFSENS value matches the DIF bit setting.

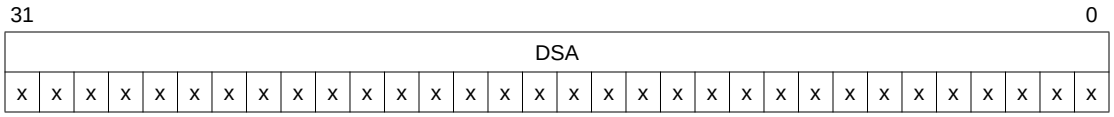
LDSC **Last Disconnect** **1**
This status bit is used in conjunction with the Connected (CON) bit in SCSI Control One (SCNTL1) and allows the user to detect the case in which a target device disconnects, and then another SCSI device selects or reselects, the LSI53C895. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in SCSI Control One (SCNTL1) is cleared. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCSI Control One (SCNTL1) is set.

SDP1 **SCSI SDP1 Signal** **0**

This bit represents the active HIGH current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

Register: 0x10–0x13

Data Structure Address (DSA)
Read/Write



DSA **Data Structure Address** **[31:0]**

This 32-bit register contains the base address used for all table indirect calculations. The Data Structure Address (DSA) register is usually loaded prior to starting an I/O, but it is possible for a SCRIPTS Memory Move to load the DSA during the I/O.

During any Memory to Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register: 0x14

Interrupt Status (ISTAT)
Read/Write

7	6	5	4	3	2	1	0
ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the LSI53C895 is executing SCRIPTS (without interfering in the operation of the LSI53C895). It may be used to poll for interrupts if hardware interrupts are disabled. If there are stacked interrupts pending, read this register after servicing an interrupt to check for stacked interrupts. For more information on interrupt handling refer to Chapter 2, “Functional Description.”

ABRT **Abort Operation** **7**

Setting this bit aborts the current operation being executed by the LSI53C895. If this bit is set and an

interrupt is received, clear this bit before reading the DMA Status (DSTAT) register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit.
2. Wait for an interrupt.
3. Read the Interrupt Status (ISTAT) register.
4. If the SCSI Interrupt Pending bit is set, then read the SCSI Interrupt Status Zero (SIST0) or SCSI Interrupt Status One (SIST1) register to determine the cause of the SCSI Interrupt and go back to Step 2.
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 0x00 value to this register.
6. Read the DMA Status (DSTAT) register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

SRST **Software Reset** **6**

Setting this bit resets the LSI53C895. All operating registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This reset does not clear the LSI53C700 family ID Mode bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).

SIGP **Signal Process** **5**

SIGP is a R/W bit that is writable at any time, and polled and reset using Chip Test Two (CTEST2). The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS instruction.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that instruction to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/reselection condition.

SEM **Semaphore** **4**

This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the LSI53C895 is executing a SCRIPTS operation. This bit enables the LSI53C895 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the LSI53C895 of a predefined condition, and the SCRIPTS processor may take action while SCRIPTS are executing.

CON **Connected** **3**

This bit is automatically set any time the LSI53C895 is connected to the SCSI bus as an initiator or as a target. It is set after successfully completing selection or when the LSI53C895 has responded to a bus-initiated selection or reselection. It is also set after the LSI53C895 wins arbitration when operating in low-level mode. When this bit is clear, the LSI53C895 is not connected to the SCSI bus.

INTF **Interrupt on the Fly** **2**

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs do not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. If this bit is set, when the Interrupt Status (ISTAT) register is read it does not automatically clear. To clear this bit, it must be written to a one. The reset operation is self-clearing.

If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt-on-the-fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

This bit must be written to one in order to clear it after it has been set.

SIP **SCSI Interrupt Pending** **1**

This status bit is set when an interrupt condition is detected in the SCSI portion of the LSI53C895. A SCSI interrupt can occur under these conditions:

- A phase mismatch (initiator mode) or SATN/ becomes active (target mode)
- An arbitration sequence completes
- A selection or reselection timeout occurs
- The LSI53C895 was selected
- The LSI53C895 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- The handshake to handshake timer is expired
- The general purpose timer is expired
- A SCSI bus mode change is detected

To determine exactly which condition(s) caused the interrupt, read the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers.

DIP **DMA Interrupt Pending** **0**

This status bit is set when an interrupt condition is detected in the DMA portion of the LSI53C895. A DMA interrupt can occur under these conditions:

- A PCI parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- An illegal instruction is detected.

To determine exactly which condition(s) caused the interrupt, read the DMA Status (DSTAT) register.

Register: 0x18
Chip Test Zero (CTEST0)
Read/Write

7							0
CTEST0							
x	x	x	x	x	x	x	x

CTEST0 **Chip Test Zero** **[7:0]**
This was a general purpose read/write register in previous LSI53C8XX family chips. Although it is still a read/write register, LSI Logic reserves the right to use these bits for future LSI53C8XX family enhancements.

Register: 0x19
Chip Test One (CTEST1)
Read Only

7	6	5	4	3	2	1	0
FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
1	1	1	1	0	0	0	0

FMT[3:0] **Byte Empty in DMA FIFO** **[7:4]**
These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 is set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

FFL[3:0] **Byte Full in DMA FIFO** **[3:0]**
These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 is set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register: 0x1A
Chip Test Two (CTEST2)
Read/Write

7	6	5	4	3	2	1	0
DDIR	SIGP	CIO	CM	SRTCH	TEOP	DREQ	DACK
0	0	x	x	0	0	0	1

DDIR **Data Transfer Direction (Read only)** **7**
This status bit indicates which direction data is being transferred. When this bit is set, the data is transferred from the SCSI bus to the host bus. When this bit is clear, the data is transferred from the host bus to the SCSI bus.

SIGP **Signal Process (Read only)** **6**
This bit is a copy of the SIGP bit in the Interrupt Status (ISTAT) register (bit 5). Use the SIGP bit to signal a running SCRIPTS instruction. When this register is read, the SIGP bit in the Interrupt Status (ISTAT) register is cleared.

CIO **Configured as I/O (Read only)** **5**
This bit is defined as the Configuration I/O Enable Status bit. This read only bit indicates if the chip is currently enabled as I/O space.

Note: Both bits 4 and 5 may be set if the chip is dual-mapped.

CM **Configured as Memory (Read only)** **4**
This bit is defined as the configuration memory enable status bit. This read only bit indicates if the chip is currently enabled as memory space.

Note: Both bits 4 and 5 may be set if the chip is dual-mapped.

BSRTCH **SCRATCHA/B Operation** **3**
This bit controls the operation of the Scratch Register A (SCRATCHA) and Scratch Register B (SCRATCHB) registers. When it is set, SCRATCHB contains the RAM base address value from the PCI Configuration RAM Base address register. This is the base address for the 4 Kbytes internal RAM. In addition, the Scratch Register A (SCRATCHA) register displays the memory-mapped based address of the chip operating registers. When this bit is clear, the Scratch Register A (SCRATCHA) and

Scratch Register B (SCRATCHB) registers return to normal operation.

Bit 3 is the only writable bit in this register. All other bits are read only. When modifying this register, all other bits must be written to zero. Do not execute a Read-Modify-Write to this register.

TEOP **SCSI True End of Process (Read only)** **2**
This bit indicates the status of the LSI53C895 internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the LSI53C895. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

DREQ **Data Request Status (Read only)** **1**
This bit indicates the status of the LSI53C895 internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

DACK **Data Acknowledge Status (Read only)** **0**
This bit indicates the status of the LSI53C895 internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register: 0x1B
Chip Test Three (CTEST3)
Read/Write

7	6	5	4	3	2	1	0
V3	V2	V1	V0	FLF	CLF	FM	WRIE
x	x	x	x	0	0	0	0

V[3:0] **Chip Revision Level** **[7:4]**
These bits identify the chip revision level for software purposes. The value should be the same as the lower nibble of the PCI Revision ID register, at address 0x08 in configuration space.

FLF **Flush DMA FIFO** **3**
When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the DMA Next Address (DNAD) register. The internal DMAWR signal, controlled by the Chip Test Five (CTEST5) register, determines the direction of the transfer. This bit

is not self clearing; once the LSI53C895 has successfully transferred the data, this bit should be reset.

Polling of FIFO flags is allowed during flush operations.

CLF **Clear DMA FIFO** **2**

When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the LSI53C895 has successfully cleared the appropriate FIFO pointers and registers.

This bit does not clear the data visible at the bottom of the FIFO.

FM **Fetch Pin Mode** **1**

When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ is only active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ is asserted for all bus cycles during instruction fetches.

WRIE **Write and Invalidate Enable** **0**

This bit, when set, causes Memory Write and Invalidate commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in detail in Chapter 3, “PCI Functional Description.”

Register: 0x1C–0x1F

Temporary (TEMP)

Read/Write

31																													0
TEMP																													
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

TEMP **Temporary** **[31:0]**

This 32-bit register stores the Return instruction address pointer from the Call instruction. The address pointer stored in this register is loaded into the DMA SCRIPTS Pointer (DSP) register when a Return instruction is executed. This address points to the next instruction to be

executed. Do not write to this register while the LSI53C895 is executing SCRIPTS.

During any Memory to Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register: 0x20 (A0)

DMA FIFO (DFIFO)

Read Only

7							0
BO[7:0]							
x	0	0	0	0	0	0	0

BO[7:0] **Byte Offset Counter** **[7:0]**

These bits, along with bits [1:0] in the Chip Test Five (CTEST5) register, indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when an interrupt occurs. These bits are unstable while data is being transferred between the two cores. Once the chip has stopped transferring data, these bits are stable.

Since the DMA FIFO (DFIFO) register counts the number of bytes transferred between the DMA core and the SCSI core, and the DMA Byte Counter (DBC) register counts the number of bytes transferred across the host bus, the difference between these two counters represents the number of bytes remaining in the DMA FIFO.

Follow these steps to determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1. If the DMA FIFO size is set to 112 bytes, subtract the seven least significant bits of the DMA Byte Counter (DBC) register from the 7-bit value of the DMA FIFO (DFIFO) register.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the Chip Test Five (CTEST5) register), subtract the 10 least significant bits of the DMA Byte Counter (DBC) register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits [1:0] in the

Chip Test Five (CTEST5) register and bits [7:0] of the DMA FIFO (DFIFO) register.

2. If the DMA FIFO size is set to 112 bytes, AND the result with 0x7F for a byte count between zero and 64. If the DMA FIFO size is set to 816 bytes, AND the result with 0x3FF for a byte count between 0 and 816.

   To calculate the total number of bytes in both the DMA FIFO and SCSI logic, refer to the section on Data Paths in Chapter 2, "Functional Description."

Register: 0x21

Chip Test Four (CTEST4)
Read/Write

7	6	5	4	3	2		0
BDIS	ZMOD	ZSD	SRTM	MPEE	FBL[2:0]		
0	0	0	0	0	0	0	0

BDIS **Burst Disable** **7**
When set, this bit causes the LSI53C895 to perform back to back cycles for all transfers. When reset, the LSI53C895 will perform back to back transfers for op code fetches and burst transfers for data moves.

ZMOD **High Impedance Mode** **6**
Setting this bit causes the LSI53C895 to place all output and bidirectional pins into a high impedance state. In order to read data out of the LSI53C895, this bit must be cleared. This bit is intended for board-level testing only. Do not set this bit during normal system operation.

ZSD **SCSI Data High Impedance** **5**
Setting this bit causes the LSI53C895 to place the SCSI data bus SD[15:0] and the parity lines SDP[1:0] in a high impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

SRTM **Shadow Register Test Mode** **4**
Setting this bit allows access to the shadow registers used by Memory to Memory Move operations. When this bit is set, register accesses to the Temporary (TEMP) and Data Structure Address (DSA) registers are directed to

the shadow copies STEMP (Shadow TEMP) and SDSA (Shadow DSA). The registers are shadowed to prevent them from being overwritten during a Memory to Memory Move operation. The Data Structure Address (DSA) and Temporary (TEMP) registers contain the base address used for table indirect calculations, and the address pointer for a call or return instruction. This bit is intended for manufacturing diagnostics only and should not be set during normal operations.

MPEE **Master Parity Error Enable** **3**

Setting this bit enables parity checking during master data phases. A parity error during a bus master read is detected by the LSI53C895. A parity error during a bus master write is detected by the target, and the LSI53C895 is informed of the error by the PERR/ pin being asserted by the target. When this bit is reset, the LSI53C895 does not interrupt if a master parity error occurs. This bit is reset at power up.

FBL[2:0] **FIFO Byte Control** **[2:0]**

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	x	x	Disabled	N/A
1	0	0	0	D[7:0]
1	0	1	1	D[15:8]
1	1	0	2	D[23:16]
1	1	1	3	D[31:24]

These bits steer the contents of the Chip Test Six (CTEST6) register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. When cleared, the byte lane read or written is determined by the current contents of the DMA Next Address (DNAD) and DMA Byte Counter (DBC) registers. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero.

Register: 0x22

Chip Test Five (CTEST5)

Read/Write

7	6	5	4	3	2	1	0
ADCK	BBCK	DFS	MASR	DDIR	BL2	BO[9:8]	
0	0	0	0	0	x	x	x

ADCK **Clock Address Incrementor** **7**

Setting this bit increments the address pointer contained in the DMA Next Address (DNAD) register. The DMA Next Address (DNAD) register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DMA Next Address (DNAD) register.

BBCK **Clock Byte Counter** **6**

Setting this bit decrements the byte count contained in the 24-bit DMA Byte Counter (DBC) register. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DMA Byte Counter (DBC) register.

DFS **DMA FIFO Size** **5**

This bit controls the size of the DMA FIFO. When clear, the DMA FIFO is 112 bytes deep. When set, the DMA FIFO size increases to 816 bytes. Using a 112-byte FIFO allows software written for other LSI53C8XX family chips to properly calculate the number of bytes residing in the chip after a target disconnect. The default value of this bit is zero.

MASR **Master Control for Set or Reset Pulses** **4**

This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. Bits 4 and 3 should not be changed in the same write cycle.

DDIR **DMA Direction** **3**

Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data is transferred from

the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

BL2 **Burst Length Bit 2** **2**
This bit works with bits 6 and 7 in the DMA Mode (DMODE) register to determine the burst length. For complete definitions of this field, refer to the descriptions of DMA Mode (DMODE), bits 6 and 7. This bit is disabled if an 112-byte FIFO is selected by clearing the DMA FIFO Size bit.

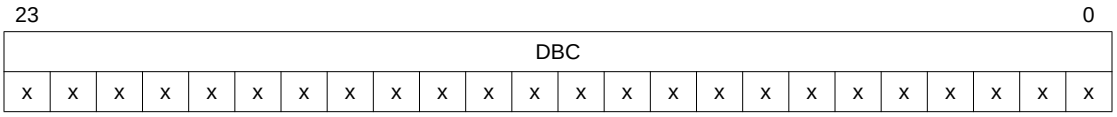
BO[9:8] **DMA FIFO Offset** **[1:0]**
These are the upper two bits of the DMA FIFO byte offset counter. The entire field is described under the DMA FIFO (DFIFO) register, bits [7:0].

Register: 0x23
Chip Test Six (CTEST6)
Read/Write

7							0
DF[7:0]							
0	0	0	0	0	0	0	0

DF[7:0] **DMA FIFO** **[7:0]**
Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. To prevent DMA data from being corrupted, this register should not be accessed during normal operation. This register should only be written when testing the DMA FIFO using the Chip Test Four (CTEST4) register. Reads or writes to this register while the test mode is not enabled will have unexpected results.

Register: 0x24–0x26
DMA Byte Counter (DBC)
Read/Write



DBC **DMA Byte Counter** **[23:0]**

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the LSI53C895. The DBC counter is decremented each time that data is transferred on the PCI bus. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DMA Byte Counter (DBC) register is 0xFFFFFF. If the instruction is a Block Move and a value of 0x000000 is loaded into the DMA Byte Counter (DBC) register, an illegal instruction interrupt occurs if the LSI53C895 is not in target mode, Command phase.

Use the DMA Byte Counter (DBC) register to also hold the least significant 24 bits of the first Dword of a SCRIPT fetch, and to hold the offset value during table indirect I/O SCRIPTS. For a complete description, refer to Section 6.4, “I/O Instruction.” The power-up value of this register is indeterminate.

Register: 0x27
DMA Command (DCMD)
Read/Write

7							0
DCMD							
0	1	x	x	x	x	x	x

DCMD **DMA Command** **[7:0]**
This 8-bit register determines the instruction for the LSI53C895 to execute. This register has a different format for each instruction. For complete descriptions, refer to Section 6.4, “I/O Instruction.”

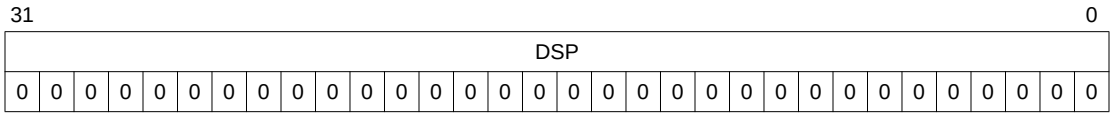
Register: 0x28–0x2B
DMA Next Address (DNAD)
Read/Write

31																													0
DNAD																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DNAD **DMA Next Address** **[31:0]**
This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DMA SCRIPTS Pointer Save (DSPS) register. Its value may not be valid except in certain abort conditions. The default value of this register is zero.

This register should not be used to determine data addresses during a Phase Mismatch interrupt, as its value is not always correct for this use. The DMA Byte Counter (DBC), DMA FIFO (DFIFO), and DMA SCRIPTS Pointer Save (DSPS) registers should be used to calculate residual byte counts and addresses as described in Section 2.2.1.1, “Data Paths.”

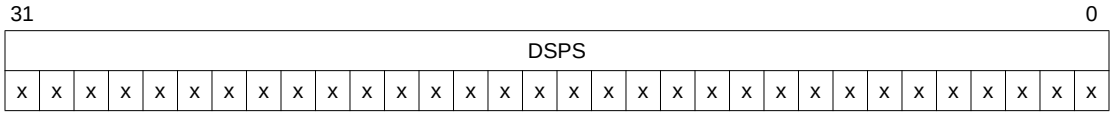
Register: 0x2C–0x2F
DMA SCRIPTS Pointer (DSP)
Read/Write



DSP **DMA SCRIPTS Pointer** **[31:0]**
To execute SCSI SCRIPTS, the address of the first SCRIPTS instruction must be written to this register. In normal SCRIPTS operation, once the starting address of the SCRIPT is written to this register, SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a single step interrupt after each instruction is executed. The DMA SCRIPTS Pointer (DSP) register does not need to be written with the next address, but the Start DMA bit (bit 2, DMA Control (DCNTL) register) must be set each time the step interrupt occurs to fetch and execute the next SCRIPTS command. When writing to this register eight bits at a time, writing the upper eight bits begins execution of SCSI SCRIPTS. The default value of this register is zero.

Register: 0x30–0x33
DMA SCRIPTS Pointer Save (DSPS)
Read/Write



DSPS **DMA SCRIPTS Pointer Save** **[31:0]**
This register contains the second Dword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt instruction is executed, this register holds the interrupt vector. The power-up value of this register is indeterminate.

Register: 0x34–0x37
Scratch Register A (SCRATCHA)
Read/Write

31																													0
SCRATCHA																													
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SCRATCHA **Scratch Register A** **[31:0]**
This is a general purpose, user-definable scratch pad register. Apart from CPU access, only register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The LSI53C895 cannot fetch SCRIPTS instructions from this location. When bit 3 in the Chip Test Two (CTEST2) register is set, this register contains the memory-mapped base address of the operating registers. Setting Chip Test Two (CTEST2), bit 3 only causes the base address to appear in this register. Any information that was previously in the register remains intact. Any writes to this register while Chip Test Two (CTEST2), bit 3 is set passes through to the actual Scratch Register A (SCRATCHA) register. The power-up value of this register is indeterminate.

Register: 0x38
DMA Mode (DMODE)
Read/Write

7	6	5	4	3	2	1	0
BL[1:0]		SIOM	DIOM	ERL	ERMP	BOF	MAN
0	0	0	0	0	0	0	0

BL[1:0] **Burst Length** **[7:6]**
These bits control the maximum number of transfers performed per bus ownership, regardless of whether the transfers are back to back, burst, or a combination of both. The LSI53C895 asserts the Bus Request (REQ/) output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (REQ/) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. The LSI53C895 inserts a “fairness delay” of four CLKs between burst-length

transfers (as set in BL[1:0]) during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access the PCI bus between bursts.

BL2 (CTEST5 bit 2)	BL1	BL0	Burst Length
0	0	0	2-transfer burst
0	0	1	4-transfer burst
0	1	0	8-transfer burst
0	1	1	16-transfer burst
1	0	0	32-transfer burst[1]
1	0	1	64-transfer burst[1]
1	1	0	128-transfer burst[1]
1	1	1	Reserved

1. Only valid if the FIFO size is set to 816 bytes.

SIOM **Source I/O-Memory Enable** **5**

This bit is defined as an I/O Memory Enable bit for the source address of a Memory Move or Block Move Command. If this bit is set, then the source address is in I/O space. If reset, then the source address is in memory space.

This function is useful for register to memory operations using the Memory Move instruction when the LSI53C895 is I/O mapped. Use bits 4 and 5 of the Chip Test Two (CTEST2) register to determine the configuration status of the LSI53C895.

DIOM **Destination I/O-Memory Enable** **4**

This bit is defined as an I/O Memory Enable bit for the destination address of a Memory Move or Block Move Command. If this bit is set, then the destination address is in I/O space. If reset, then the destination address is in memory space.

This function is useful for memory to register operations using the Memory Move instruction when the LSI53C895 is I/O mapped. Bits 4 and 5 of the Chip Test Two (CTEST2) register can be used to determine the configuration status of the LSI53C895.

ERL	**Enable Read Line** This bit enables a PCI Read Line command. If PCI cache mode is enabled by setting bits in the PCI Cache Line Size register, this chip issues a Read Line command on all read cycles if other conditions are met. For more information on these conditions, refer to Section 3.1, “PCI Addressing.”	**3**
ERMP	**Enable Read Multiple** Setting this bit causes Read Multiple commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in Section 3.1, “PCI Addressing.”	**2**
BOF	**Burst Op Code Fetch Enable** Setting this bit causes the LSI53C895 to fetch instructions in burst mode. Specifically, the chip bursts in the first two Dwords of all instructions using a single bus ownership. If the instruction is a Memory to Memory Move type, the third Dword is accessed in a subsequent bus ownership. If the instruction is an indirect type, the additional Dword is accessed in a subsequent bus ownership. If the instruction is a table indirect block move type, the chip accesses the remaining two Dwords in a subsequent bus ownership, thereby fetching the four Dwords required in two bursts of two Dwords each. This bit has no effect if SCRIPTS instruction prefetching is enabled.	**1**
MAN	**Manual Start Mode** Setting this bit prevents the LSI53C895 from automatically fetching and executing SCSI SCRIPTS when the DMA SCRIPTS Pointer (DSP) register is written. When this bit is set, the Start DMA bit in the DMA Control (DCNTL) register must be set to begin SCRIPTS execution. Clearing this bit causes the LSI53C895 to automatically begin fetching and executing SCSI SCRIPTS when the DMA SCRIPTS Pointer (DSP) register is written. This bit normally is not used for SCSI SCRIPTS operations.	**0**

Register: 0x39

DMA Interrupt Enable (DIEN)
Read/Write

7	6	5	4	3	2	1	0
R	MDPE	BF	ABRT	SSI	SIR	R	IID
x	0	0	0	0	0	x	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DMA Status (DSTAT) register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit is still set in the DMA Status (DSTAT) register. Masking an interrupt does not prevent the ISTAT DIP from being set. All DMA interrupts are considered fatal, therefore SCRIPTS stops running when this condition occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt. (A masked nonfatal interrupt does not prevent unmasked or fatal interrupts from getting through; interrupt stacking begins when either the Interrupt Status (ISTAT) SIP or DIP bit is set.)

The LSI53C895 IRQ/ output is latched; once asserted, it remains asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted does not cause IRQ/ to be deasserted.

For more information on interrupts, refer to Chapter 2, “Functional Description.”

R	**Reserved**	**7**
MDPE	**Master Data Parity Error**	**6**
BF	**Bus Fault**	**5**
ABRT	**Aborted**	**4**
SSI	**Single-Step Interrupt**	**3**
SIR	**SCRIPTS Interrupt Instruction Received**	**2**

R	**Reserved**	**1**
IID	**Illegal Instruction Detected**	**0**

Register: 0x3A

Scratch Byte Register (SBR)
Read/Write

This is a general purpose register. Apart from CPU access, only Register Read/Write and Memory Moves into this register alters its contents. The default value of this register is zero. This register was called the DMA Watchdog Timer on previous LSI53C8XX family products.

Register: 0x3B

DMA Control (DCNTL)
Read/Write

7	6	5	4	3	2	1	0
CLSE	PFF	PFEN	SSM	IRQM	STD	IRQD	COM
0	0	0	0	0	0	0	0

CLSE **Cache Line Size Enable** **7**
Setting this bit enables the LSI53C895 to sense and react to cache line boundaries set up by the DMA Mode (DMODE) or PCI Cache Line Size register, whichever contains the smaller value. Clearing this bit disables the cache line size logic and the LSI53C895 monitors the cache line size by using the DMA Mode (DMODE) register.

PFF **Prefetch Flush** **6**
Setting this bit causes the pre-fetch unit to flush its contents. The bit resets after the flush is complete.

PFEN **Prefetch Enable** **5**
Setting this bit enables the pre-fetch unit if the burst size is equal to or greater than four. For more information on SCRIPTS instruction prefetching, refer to Chapter 2, “Functional Description.”

SSM **Single-Step Mode** **4**
Setting this bit causes the LSI53C895 to stop after executing each SCRIPTS instruction, and generate a single step interrupt. When this bit is clear the LSI53C895

does not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the LSI53C895 after it generates a SCRIPTS Step interrupt, the Interrupt Status (ISTAT) and DMA Status (DSTAT) registers should be read to recognize and clear the interrupt and then the START DMA bit in this register should be set.

IRQM **IRQ Mode** **3**

When set, this bit enables a totem pole driver for the IRQ pin. When reset, this bit enables an open drain driver for the IRQ pin with a internal weak pull-up. This bit is reset at power up. This bit should remain clear to retain full PCI compliance.

STD **Start DMA Operation** **2**

The LSI53C895 fetches a SCSI SCRIPTS instruction from the address contained in the DMA SCRIPTS Pointer (DSP) register when this bit is set. This bit is required if the LSI53C895 is in one of the following modes:

- Manual start mode – Bit 0 in the DMA Mode (DMODE) register is set.
- Single-step mode – Bit 4 in the DMA Control (DCNTL) register is set.

When the LSI53C895 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the LSI53C895 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

IRQD **IRQ Disable** **1**

Setting this bit disables the IRQ pin and clearing this bit enables normal operation. As with any other register other than Interrupt Status (ISTAT), this register cannot be accessed except by a SCRIPTS instruction during SCRIPTS execution. For more information on the use of this bit in interrupt handling, refer to Chapter 2, “Functional Description.”

COM **LSI53C700 Family Compatibility** **0**

When this bit is clear, the LSI53C895 behaves in a manner compatible with the LSI53C700 family in that selection/reselection IDs are stored in both the SCSI Selector ID (SSID) and SCSI First Byte Received (SFBR) registers.

When this bit is set, the ID is stored only in the SCSI Selector ID (SSID) register, protecting the SCSI First Byte Received (SFBR) from being overwritten if a selection/reselection occurs during a DMA register to register operation. This bit is not affected by a software reset.

Register: 0x3C–0x3F

Adder Sum Output (ADDER)

Read Only

31																												0
ADDER																												
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

ADDER **Adder Sum Output** **[31:0]**

This register contains the output of the internal adder, and is used primarily for test purposes. The power-up value for this register is indeterminate.

Register: 0x40

SCSI Interrupt Enable Zero (SIEN0)

Read/Write

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SCSI Interrupt Status Zero (SIST0) register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, refer to Chapter 2, “Functional Description.”

M/A	**SCSI Phase Mismatch - Initiator Mode;** **SCSI ATN Condition - Target Mode** Setting this bit allows the LSI53C895 to generate an interrupt when a Phase Mismatch or ATN condition occurs.	
CMP	**Function Complete** Setting this bit allows the LSI53C895 to generate an interrupt when a full arbitration and selection sequence has completed.	**6**
SEL	**Selected** Setting this bit allows the LSI53C895 to generate an interrupt when the LSI53C895 has been selected by a SCSI target device.	**5**
RSL	**Reselected** Setting this bit allows the LSI53C895 to generate an interrupt when the LSI53C895 has been reselected by a SCSI initiator device.	**4**
SGE	**SCSI Gross Error** Setting this bit allows the LSI53C895 to generate an interrupt when a SCSI Gross Error occurs. The following conditions are considered SCSI Gross Errors: • Data underflow – the SCSI FIFO was read when no data was present. • Data overflow – the SCSI FIFO was written to while full. • Offset underflow – in target mode, a SACK/ pulse was received before the corresponding SREQ/ was sent. • Offset overflow – in initiator mode, an SREQ/ pulse was received which caused the maximum offset (Defined by the MO[3:0] bits in the SCSI Transfer (SXFER) register) to be exceeded. • In initiator mode, a phase change occurred with an outstanding SREQ/SACK offset. • Residual data in SCSI FIFO – a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.	**3**

UDC **Unexpected Disconnect** **2**
Setting this bit allows the LSI53C895 to generate an interrupt when an unexpected disconnect occurs. This condition only occurs in initiator mode. It happens when the target to which the LSI53C895 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCSI Control Two (SCNTL2) register for more information on expected versus unexpected disconnects. Any disconnect in low-level mode causes this condition.

RST **SCSI Reset Condition** **1**
Setting this bit allows the LSI53C895 to generate an interrupt when the SRST/ signal has been asserted by the LSI53C895 or any other SCSI device. This condition is edge-triggered, so multiple interrupts cannot occur because of a single SRST/ pulse.

PAR **SCSI Parity Error** **0**
Setting this bit allows the LSI53C895 to generate an interrupt when the LSI53C895 detects a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or SATN/ Condition bits in the SCSI Control One (SCNTL1) register for more information on when this condition will actually be raised.

Register: 0x41
SCSI Interrupt Enable One (SIEN1)
Read/Write

7		5	4	3	2	1	0
R			SBMC	R	STO	GEN	HTH
x	x	x	0	x	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SCSI Interrupt Status One (SIST1) register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, refer to Chapter 2, “Functional Description.”

R	**Reserved**	**[7:5]**
BSBMC	**SCSI Bus Mode Change** Setting this bit allows the LSI53C895 to generate an interrupt when the DIFFSENS pin detects a change in voltage level that indicates the SCSI bus has changed between SE, LVD, or HVD modes. For example, when this bit is clear and the SCSI bus changes modes, IRQ/ does not assert and the SIP bit in the Interrupt Status (ISTAT) register is not set. However, bit 4 in the SCSI Interrupt Status One (SIST1) register is set. Setting this bit allows the interrupt to occur.	**4**
R	**Reserved**	**3**
STO	**Selection or Reselection Timeout** Setting this bit allows the LSI53C895 to generate an interrupt when a selection or reselection timeout occurs. See the description of the SCSI Timer Zero (STIME0) register (bits [3:0]) on page 5-79 for more information on the timeout periods.	**2**
GEN	**General Purpose Timer Expired** Setting this bit allows the LSI53C895 to generate an interrupt when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer One (STIME1) register (bits [3:0]) on page 5-81 for more information on the general purpose timer.	**1**
HTH	**Handshake to Handshake Timer Expired** Setting this bit allows the LSI53C895 to generate an interrupt when the handshake to handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the SCSI Timer Zero (STIME0) register, bits [7:4], for more information on the handshake to handshake timer.	**0**

Register: 0x42
SCSI Interrupt Status Zero (SIST0)
Read Only

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

Reading the SCSI Interrupt Status Zero (SIST0) register returns the status of the various interrupt conditions, whether they are enabled in the SCSI Interrupt Enable Zero (SIEN0) register or not. Each bit set indicates that the corresponding condition has occurred. Reading the SIST0 clears the interrupt status.

Reading this register clears any bits that are set at the time the register is read, but does not necessarily clear the register because additional interrupts may be pending (the LSI53C895 stacks interrupts). SCSI interrupt conditions may be individually masked through the SCSI Interrupt Enable Zero (SIEN0) register.

When performing consecutive 8-bit reads of the DMA Status (DSTAT), SCSI Interrupt Status Zero (SIST0), and SCSI Interrupt Status One (SIST1) registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the Interrupt Status (ISTAT) SIP and DIP bits may not be set, the SCSI Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) registers should be read before the DMA Status (DSTAT) register to avoid missing a SCSI interrupt. For more information on interrupts, refer to Chapter 2, “Functional Description.”

M/A — **Initiator Mode: Phase Mismatch; Target Mode: SATN/ Active** — **7**
In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when SREQ/ is asserted by the target. In target mode, this bit is set when the SATN/ signal is asserted by the initiator.

CMP — **Function Complete** — **6**
This bit is set when an arbitration only or full arbitration sequence has completed.

SEL **Selected** **5**

This bit is set when the LSI53C895 is selected by another SCSI device. The Enable Response to Selection bit must have been set in the SCSI Chip ID (SCID) register (and the Response ID (RESPID) register must hold the chip ID) for the LSI53C895 to respond to selection attempts.

RSL **Reselected** **4**

This bit is set when the LSI53C895 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCSI Chip ID (SCID) register (and the Response ID (RESPID) register must hold the chip ID) for the LSI53C895 to Respond to Reselection attempts.

SGE **SCSI Gross Error** **3**

This bit is set when the LSI53C895 encounters a SCSI Gross Error Condition. These conditions can result in a SCSI Gross Error Condition:

- Data Underflow – the SCSI FIFO register was read when no data was present.
- Data Overflow – too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
- Offset Underflow – the LSI53C895 is operating in target mode and a SACK/ pulse is received when the outstanding offset is zero.
- Offset Overflow – the other SCSI device sent a SREQ/ or SACK/ pulse with data which exceeded the maximum synchronous offset defined by the SCSI Transfer (SXFER) register.
- A phase change occurred with an outstanding synchronous offset when the LSI53C895 was operating as an initiator.
- Residual data in the synchronous data FIFO – a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

UDC **Unexpected Disconnect** **2**

This bit is set when the LSI53C895 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the LSI53C895 operates in the initiator mode. When the

LSI53C895 operates in low-level mode, any disconnect causes an interrupt, even a valid SCSI disconnect. This bit is also set if a selection timeout occurs. It may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected disconnect.

RST **SCSI Reset Received** **1**

This bit is set when the LSI53C895 detects an active SRST/ signal, whether the reset was generated external to the chip or caused by the Assert SRST/ bit in the SCSI Control One (SCNTL1) register. This LSI53C895 SCSI reset detection logic is edge-sensitive, so that multiple interrupts are not generated for a single assertion of the SRST/ signal.

PAR **Parity Error** **0**

This bit is set when the LSI53C895 detects a parity error while receiving SCSI data. The Enable Parity Checking bit (bit 3 in the SCSI Control Zero (SCNTL0) register) must be set for this bit to become active. The LSI53C895 always generates parity when sending SCSI data.

Register: 0x43

SCSI Interrupt Status One (SIST1)
Read Only

7		5	4	3	2	1	0
R			SBMC	R	STO	GEN	HTH
x	x	x	0	x	0	0	0

Reading the SCSI Interrupt Status One (SIST1) register returns the status of the various interrupt conditions, whether they are enabled in the SCSI Interrupt Enable One (SIEN1) register or not. Each bit that is set indicates the corresponding condition has occurred.

Reading the SCSI Interrupt Status One (SIST1) and SCSI Interrupt Status Zero (SIST0) registers clears the interrupt condition.

R	**Reserved**	**[7:5]**
SBMC	**SCSI Bus Mode Change** This bit is set when the DIFFSENS pin detects a change in voltage level that indicates the SCSI bus has switched between SE, LVD, or HVD modes.	**4**
R	**Reserved**	**3**
STO	**Selection or Reselection Timeout** The SCSI device which the LSI53C895 was attempting to select or reselect did not respond within the programmed timeout period. See the description of the SCSI Timer Zero (STIME0) register (bits [3:0]) on page 5-79 for more information on the timeout timer.	**2**
GEN	**General Purpose Timer Expired** This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer One (STIME1) register (bits [3:0]) on page 5-81 for more information on the general purpose timer.	**1**
HTH	**Handshake to Handshake Timer Expired** This bit is set when the handshake to handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the SCSI Timer Zero (STIME0) register, bits [7:4], for more information on the handshake to handshake timer.	**0**

Register: 0x44

SCSI Longitudinal Parity (SLPAR)
Read/Write

7							0
SLPAR							
x	x	x	x	x	x	x	x

SLPAR	**SCSI Longitudinal Parity** The SCSI Longitudinal Parity (SLPAR) register consists of two multiplexed bytes; other register bit settings determine what is displayed at this memory location at	**[7:0]**

any given time. When bit 5 in the SCSI Control Two (SCNTL2) (SLPMD) register is cleared, the chip XORs the high and low bytes of the SCSI Longitudinal Parity (SLPAR) register together to give a single-byte value which is displayed in the SCSI Longitudinal Parity (SLPAR) register. If the SLPMD bit is set, then the SCSI Longitudinal Parity (SLPAR) register shows either the high byte or the low byte of the SLPAR word. The SLPAR High Byte Enable bit, SCSI Control Two (SCNTL2) bit 4, determines which byte of the SCSI Longitudinal Parity (SLPAR) register is visible on the SCSI Longitudinal Parity (SLPAR) register at any given time. If this bit is cleared, the SCSI Longitudinal Parity (SLPAR) register contains the low byte of the SLPAR word. If it is set, the SCSI Longitudinal Parity (SLPAR) register contains the high byte of the SLPAR word.

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active HIGH):

Data Bytes	Running SLPAR
–	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3) Even Parity >>>10010110
4. 10010110	00000000

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SCSI Longitudinal Parity (SLPAR) register can also be used to generate the check bytes for SCSI send operations. If the SCSI Longitudinal Parity (SLPAR) register contains all zeros prior to sending a block move,

it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Note: Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances. The default value of this register is zero.

Register: 0x45

SCSI Wide Residue (SWIDE)
Read Only

7							0
SWIDE							
x	x	x	x	x	x	x	x

SWIDE **SCSI Wide Residue** **[7:0]**
After a wide SCSI data receive operation, this register contains a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide residue message is received. It may also be an overrun data byte. The power-up value of this register is indeterminate.

Register: 0x46

Memory Access Control (MACNTL)
Read/Write

7			4	3	2	1	0
TYP[7:4]				DWR	DRD	PSCPT	SCPTS
1	1	0	1	0	0	0	0

TYP[7:4] **Chip Type** **[7:4]**
These bits identify the chip type for software purposes. This data manual applies to devices that have these bits set to 0xD0.

Bits 3 through 0 of this register determine if an external bus master access is to local or far memory. When bits 3 through 0 are set, the corresponding access is considered local and the MAC/_TESTOUT pin is driven high. When these bits are clear, the corresponding access is to far memory and the MAC/_TESTOUT pin is driven low. This function is enabled after a Transfer Control SCRIPTS instruction is executed.

DWR **Data Write** **3**
This bit defines if a data write is considered local memory access.

DRD **Data Read** **2**
This bit defines if a data read is considered local memory access.

PSCPT **Pointer SCRIPTS** **1**
This bit defines if a pointer to a SCRIPTS indirect or table indirect fetch is considered local memory access.

SCPTS **SCRIPTS** **0**
This bit defines if a SCRIPTS fetch is considered local memory access.

Register: 0x47

General Purpose Pin Control (GPCNTL)
Read/Write

7	6	5	4				0
ME	FE	R	GPIO[4:0]				
0	0	x	0	1	1	1	1

This register determines if the pins controlled by the General Purpose (GPREG) register are inputs or outputs. Bits [4:0] in GPCNTL correspond to bits [4:0] in the General Purpose (GPREG) register.

ME **Master Enable** **7**
The internal bus master signal is presented on GPIO1 if this bit is set, regardless of the state of Bit 1 (GPIO1_EN).

FE **Fetch Enable** **6**
The internal op code fetch signal will be presented on GPIO0 if this bit is set, regardless of the state of Bit 0 (GPIO0_EN).

R **Reserved** **5**

GPIO_EN **GPIO Enable** **[4:2]**
General purpose control, corresponding to bits [4:2] in the General Purpose (GPREG) register and pins [67:65]. GPIO4 powers up as a general purpose output, and GPIO[3:2] power up as general purpose inputs.

GPIO_EN **GPIO Enable** **[1:0]**
These bits power up set, causing the GPIO1 and GPIO0 pins to become inputs. Resetting these bits causes GPIO[1:0] to become outputs.

Register: 0x48
SCSI Timer Zero (STIME0)
Read/Write

7			4	3			0
HTH[7:4]				SEL[3:0]			
0	0	0	0	0	0	0	0

HTH[7:4] **Handshake to Handshake Timer Period** **[7:4]**
These bits select the handshake to handshake timeout period, the maximum time between SCSI handshakes (SREQ/ to SREQ/ in target mode, or SACK/ to SACK/ in initiator mode). When this timing is exceeded, an interrupt is generated and the HTH bit in the SCSI Interrupt Status One (SIST1) register is set. Table 5.8 contains timeout periods for the Handshake to Handshake Timer, the Selection/Reselection Timer (bits [3:0]), and the General Purpose Timer (SCSI Timer One (STIME1), bits [3:0]). For a more detailed explanation of interrupts, refer to Chapter 2, “Functional Description.”

Table 5.8 Timeout Periods[1]

HTH[7:4], SEL[3:0], GEN[3:0]	Minimum Timeout (40 or 160 MHz)[2]
0000	Disabled
0001	125 µs
0010	250 µs
0011	500 µs
0100	1 ms
0101	2 ms
0110	4 ms
0111	8 ms
1000	16 ms
1001	32 ms
1010	64 ms
1011	128 ms
1100	256 ms
1101	512 ms
1110	1.024 s
1111	2.048 s

1. These values are correct if the CCF bits in the SCSI Contr0l Three (SCNTL3) register are set according to the valid combinations in the bit description.
2. A quadrupled 40 MHz clock is required for Ultra2 SCSI operation.

SEL[3:0] **Selection Timeout** **[3:0]**

These bits select the SCSI selection/reselection timeout period. When this timing (plus the 200 µs selection abort time) is exceeded, the STO bit in the SCSI Interrupt Status One (SIST1) register is set. For a more detailed explanation of interrupts, refer to Chapter 2, "Functional Description."

Register: 0x49
SCSI Timer One (STIME1)
Read/Write

7	6	5	4	3			0
R	HTHBA	GENSF	HTHSF	GEN[3:0]			
x	0	0	0	0	0	0	0

R **Reserved** **7**

HTHBA **Handshake to Handshake Timer Bus Activity Enable** **6**
Setting this bit causes this timer to begin testing for SCSI REQ/ACK activity as soon as SBSY/ is asserted, regardless of the agents participating in the transfer.

GENSF **(General Purpose Timer Scale Factor)** **5**
Setting this bit causes this timer to shift by a factor of 16. See Table 5.9 for Timeout Periods, 50 MHz Clock and Table 5.10 for Timeout Periods, 40 MHz Clock.

Table 5.9 Timeout Periods, 50 MHz Clock [1]

HTH[7:4], SEL[3:0], GEN[3:0]	Minimum Timeout (50 MHz Clock)[2]	
	GENSF = 0	GENSF = 1
0000	Disabled	Disabled
0001	100 µs	1.6 ms
0010	200 µs	3.2 ms
0011	400 µs	6.4 ms
0100	800 µs	12.8 ms
0101	1.6 ms	25.6 ms
0110	3.2 ms	51.2 ms
0111	6.4 ms	102.4 ms
1000	12.8 ms	204.8 ms
1001	25.6 ms	409.6 ms
1010	51.2 ms	819.2 ms
1011	102.4 ms	1.6 s
1100	204.8 ms	3.2 s

Table 5.9 Timeout Periods, 50 MHz Clock (Cont.) [1]

HTH[7:4], SEL[3:0], GEN[3:0]	Minimum Timeout (50 MHz Clock)[2]	
	GENSF = 0	GENSF = 1
1101	409.6 ms	6.4 s
1110	819.2 ms	12.8 s
1111	1.6 s	25.6 s

1. These values are correct if the CCF bits in the SCSI Contr0l Three (SCNTL3) register are set according to the valid combinations in the bit description.
2. 50 MHz clock is not supported for Ultra2 SCSI operation.

Table 5.10 Timeout Periods, 40/160 MHz Clock[1]

HTH[7:4], SEL[3:0], GEN[3:0]	Minimum Timeout (40 or 160 MHz Clock)[2]	
	GENSF = 0	GENSF = 1
0000	Disabled	Disabled
0001	125 µs	2 ms
0010	250 µs	4 ms
0011	500 µs	8 ms
0100	1 µs	16 ms
0101	2 ms	32 ms
0110	4 ms	64 ms
0111	8 ms	128 ms
1000	16 ms	256 ms
1001	32 ms	512 ms
1010	64 ms	1 s
1011	128 ms	2 s
1100	256 ms	4.1 s
1101	512 ms	8.2 s
1110	1.024 s	16.4 s
1111	2.048 s	32.8 s

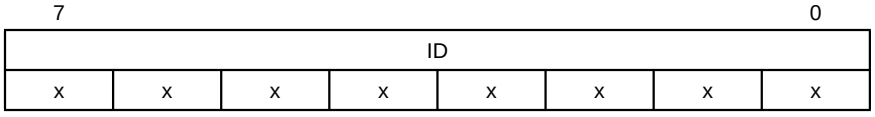
1. These values are correct if the CCF bits in the SCSI Contr0l Three (SCNTL3) register are set according to the valid combinations in the bit description.
2. Ultra2 SCSI operation requires a quadrupled 40 MHz clock.

HTHSF **Handshake to Handshake Timer Scale Factor** **4**
Setting this bit causes this timer to shift by a factor of 16.

GEN[3:0] **General Purpose Timer Period** **[3:0]**
These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SCSI Interrupt Status One (SIST1) register is set. Refer to Table 5.8 on page 80 under the SCSI Timer Zero (STIME0), bits [3:0], for the available timeout periods.

Note: To reset a timer before it has expired and obtain repeatable delays, the time value must be written to zero first, and then written back to the desired value. This is also required when changing from one time value to another. See Chapter 2, "Functional Description," for an explanation of how interrupts will be generated when the timers expire.

Register: 0x4A
Response ID Zero (RESPID0)
Read/Write



RESPID0 **Response ID Zero** **[7:0]**
Response ID Zero (RESPID0) and Response ID One (RESPID1) contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCSI Chip ID (SCID) register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the Response ID One (RESPID1) and Response ID Zero (RESPID0) registers. However, the chip can arbitrate with only one ID value in the SCSI Chip ID (SCID) register.

Register: 0x4B

Response ID One (RESPID1)

Read/Write

15							8
ID							
x	x	x	x	x	x	x	x

RESPID1 **Response ID One** **[15:0]**

Response ID Zero (RESPID0) and Response ID One (RESPID1) contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCSI Chip ID (SCID) register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the Response ID One (RESPID1) and Response ID Zero (RESPID0) registers. However, the chip can arbitrate with only one ID value in the SCSI Chip ID (SCID) register.

Register: 0x4C

SCSI Test Zero (STEST0)

Read Only

7			4	3	2	1	0
SSAID[3:0]				SLT	ART	SOZ	SOM
0	0	0	0	0	x	1	1

SSAID[3:0] **SCSI Selected As ID** **[7:4]**

These bits contain the encoded value of the SCSI ID that the LSI53C895 was selected or reselected as during a SCSI selection or reselection phase. These bits are read only and contain the encoded value of 0–15 possible IDs that could be used to select the LSI53C895. During a SCSI selection or reselection phase when a valid ID has been put on the bus, and the LSI53C895 responds to that ID, the “selected as” ID is written into these bits. These bits are used with the RESPID registers to allow response to multiple IDs on the bus.

SLT **Selection Response Logic Test** **3**
This bit is set when the LSI53C895 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

ART **Arbitration Priority Encoder Test** **2**
This bit is always set when the LSI53C895 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low-level mode operation to determine if the LSI53C895 has won arbitration.

SOZ **SCSI Synchronous Offset Zero**
This bit indicates that the current synchronous SREQ/SACK offset is zero. This bit is not latched and may change at any time. It is used in low-level synchronous SCSI operations. When this bit is set, the LSI53C895, as an initiator, is waiting for the target to request data transfers. If the LSI53C895 is a target, then the initiator has sent the offset number of acknowledges.

SOM **SCSI Synchronous Offset Maximum** **0**
This bit indicates that the current synchronous SREQ/SACK offset is the maximum specified by bits[3:0] in the SCSI Transfer (SXFER) register. This bit is not latched and may change at any time. It is used in low-level synchronous SCSI operations. When this bit is set, the LSI53C895, as a target, is waiting for the initiator to acknowledge the data transfers. If the LSI53C895 is an initiator, then the target has sent the offset number of requests.

Register: 0x4D
SCSI Test One (STEST1)
Read/Write

7	6	5	4	3	2	1	0
SCLK	SISO	R		QEN	QSEL	R	
0	0	x	x	0	0	x	x

SCLK **SCSI Clock** **7**
Setting this bit disables the external SCLK (SCSI Clock) pin and the internal SCSI Clock Quadrupler, and the chip

uses the PCI clock as the internal SCSI clock. If a transfer rate of 10 Mbytes/s (or 20 Mbytes/s on a wide SCSI bus) is to be achieved on the SCSI bus, this bit must be Reset and at least a 40 MHz external SCLK must be provided.

SISO	**SCSI Isolation Mode** This bit allows the LSI53C895 to put the SCSI bidirectional and input pins into a low power mode when the SCSI bus is not in use. When this bit is set, the SCSI bus inputs are logically isolated from the SCSI bus.	**6**
R	**Reserved**	**[5:4]**
QEN	**SCLK Quadrupler Enable** Set this bit to bring the SCSI clock quadrupler out of the powered-down state. The default value of this bit is clear (SCSI clock quadrupler powered down). Set bit 2 after setting this bit, to increase the SCLK frequency to 160 MHz.	**3**
QSEL	**SCLK Quadrupler Select** Set this bit after powering up the SCSI clock quadrupler to increase the SCLK frequency to 160 MHz. This bit has no effect unless bit 3 is set.	**2**
R	**Reserved**	**[1:0]**

5.2.0.1 Quadrupling the SCSI Clock Frequency

The LSI53C895 SCSI clock quadrupler increases the frequency of a 40 MHz SCSI clock to 160 MHz. Follow these steps to use the clock quadrupler:

1. Set the SCLK Quadrupler Enable bit (SCSI Test One (STEST1), bit 3).
2. Poll bit 5 of the SCSI Test 4 (STEST4) register. The LSI53C895 sets this bit as soon as it locks in the 160 MHz frequency. The frequency lockup takes approximately 100 microseconds.
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (SCSI Test Three (STEST3), bit 5).
4. Set the clock conversion factor using the SCF and CCF fields in the SCSI Contr0l Three (SCNTL3) register.

5. Set the SCLK Quadrupler Select bit (SCSI Test One (STEST1), bit 2).
6. Clear the Halt SCSI Clock bit.

Register: 0x4E (0xCE)

SCSI Test Two (STEST2)

Read/Write

7	6	5	4	3	2	1	0
SCE	ROF	DIF	SLB	SZM	AWS	ExT	LOW
0	0	0	0	0	0	0	0

SCE **SCSI Control Enable** **7**

Setting this bit allows all SCSI control and data lines to be asserted through the SCSI Output Control Latch (SOCL) and SCSI Output Data Latch (SODL) registers regardless of whether the LSI53C895 is configured as a target or initiator.

This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

ROF **Reset SCSI Offset** **6**

Setting this bit clears any outstanding synchronous SREQ/SACK offset. If a SCSI gross error condition occurs, set this bit to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

DIF **SCSI Differential Mode** **5**

Setting this bit allows the LSI53C895 to interface properly to external differential transceivers. Its only real effect is to 3-state the SBSY/, SSEL/, and SRST/ pads so that they can be used as pure inputs. This bit must be cleared for SE or LVD operation. This bit should be set in the initialization routine if the HVD interface is used.

SLB **SCSI Loopback Mode** **4**

Setting this bit allows the LSI53C895 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

SZM **SCSI High Impedance Mode** **3**

Setting this bit places all the open drain 48 mA SCSI drivers into a high impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

AWS **Always Wide SCSI** **2**

When this bit is set, all SCSI information transfers are done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, command, and status phases are not supported by the SCSI specifications.

ExT **Extend SREQ/SACK Filtering** **1**

LSI Logic TolerANT SCSI receiver technology includes a special digital filter on the SREQ/ and SACK/ pins that causes glitches on deasserting edges to be disregarded. Setting this bit increases the filtering period from 30 ns to 60 ns on the deasserting edge of the SREQ/ and SACK/ signals.

This bit must never be set during fast SCSI (greater than 5 megatransfers per second) operations, because a valid assertion could be treated as a glitch.

This bit does not affect the filtering period when the Ultra Enable bit in the SCSI Contr0l Three (SCNTL3) register is set. When the LSI53C895 is executing Ultra2 SCSI transfers, the filtering period is automatically set at 8 ns. When the LSI53C895 is executing Ultra SCSI transfers, the filtering period is automatically set at 15 ns.

LOW **(SCSI Low level Mode)** **0**

Setting this bit places the LSI53C895 in low-level mode. In this mode, no DMA operations occur, and no SCRIPTS execute. Arbitration and selection may be performed by setting the start sequence bit as described in the SCSI Control Zero (SCNTL0) register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers).

Register: 0x4F (0xCF)
SCSI Test Three (STEST3)
Read/Write

7	6	5	4	3	2	1	0
TE	STR	HSC	DSI	S16	TTM	CSF	STW
0	0	0	0	0	0	0	0

TE **TolerANT Enable** **7**

Setting this bit enables the active negation portion of LSI Logic TolerANT technology. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively deasserted, instead of relying on external pull-ups, when the LSI53C895 is driving these signals. Active deassertion of these signals will occur only when the LSI53C895 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, TolerANT Active negation should be enabled to improve setup and deassertion times. Active negation is disabled after reset or when this bit is cleared. For more information on LSI Logic TolerANT technology, refer to Chapter 1, "Introduction."

This bit must be set if the Ultra Enable bit in SCNTL3 is set.

This bit must be set to use the LVD Link transceivers.

STR **SCSI FIFO Test Read** **6**

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the least significant byte of the SCSI Output Data Latch (SODL) register causes the FIFO to unload. The functions are summarized in the table below.

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15–0	Unload
SODL0	Read	7–0	Unload
SODL1	Read	15–8	None

HSC **Halt SCSI Clock** **5**

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be

used for test purposes or to lower I_{DD} during a power down mode.

This bit is used when enabling the SCSI clock quadrupler. For additional information on the clock quadrupler, please see Section 2.5.1, “Using the SCSI Clock Quadrupler,” in Chapter 2.

DSI **Disable Single Initiator Response** **4**
If this bit is set, the LSI53C895 ignores all bus-initiated selection attempts that employ the single-initiator option from SCSI-1. In order to select the LSI53C895 while this bit is set, the LSI53C895 SCSI ID and the initiator SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus is not interpreted as a single initiator response.

S16 **16-Bit System** **3**
If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the LSI53C895 to always check the parity bit for SCSI IDs 15–8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the LSI53C895 while this bit is set, the LSI53C895 ignores the selection attempt, because the parity bit for IDs 15–8 will be undriven. See the description of the Enable Parity Checking bit in the SCSI Control Zero (SCNTL0) register on page 5-17 for more information.

TTM **Timer Test Mode** **2**
Asserting this bit facilitates testing of the selection timeout, general purpose, and handshake to handshake timers by greatly reducing all three timeout periods. Setting this bit starts all three timers and if the respective bits in the SCSI Interrupt Enable One (SIEN1) register are asserted, the LSI53C895 generates interrupts at timeout. This bit is intended for internal manufacturing diagnosis and should not be used.

CSF **Clear SCSI FIFO** **1**
Setting this bit causes the “full flags” for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting. In addition to the SCSI FIFO pointers, the SIDL, SODL, and SODR full bits in the SCSI Status Zero

(SSTAT0) and SCSI Status Two (SSTAT2) registers are cleared.

STW **SCSI FIFO Test Write** **0**

Setting this bit places the SCSI core into a test mode in which the FIFO can easily be read or written. While this bit is set, writes to the least significant byte of the SCSI Output Data Latch (SODL) register will cause the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the SCSI Output Data Latch (SODL) register causes the FIFO to load. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Write	15–0	Load
SODL0	Write	7–0	Load
SODL1	Write	15–8	None

Register: 0x50–0x51 (0xD0–0xD1)

SCSI Input Data Latch (SIDL)

Read Only

15															0
SIDL															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SIDL **SCSI Input Data Latch** **[15:0]**

This register is used primarily for diagnostic testing, programmed I/O operation, or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SCSI Output Data Latch (SODL) register and then read back into the LSI53C895 by reading this register to allow loopback testing. When receiving SCSI data, the data flows into this register and out to the host FIFO. This register differs from the SCSI Bus Data Lines (SBDL) register in that SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and causes a parity error interrupt if the data is not valid. The power-up values are indeterminate.

Register: 0x52 (0xD2)
SCSI Test 4 (STEST4)
Read Only

7	6	5	4				0
SMODE		LOCK	R				
x	x	0	x	x	x	x	x

SMODE **SCSI Mode** **[7:6]**
These bits contain the encoded value of the SCSI operating mode that is indicated by the voltage level sensed at the DIFFSENS pin. The incoming SCSI signal goes to a pair of analog comparators that determine the voltage window of the DIFFSENS signal. These voltage windows indicate LVD, SE, or high-power differential operation. The bit values are defined in Table 5.11.

Table 5.11 DIFFSENS Voltage Levels and SCSI Operating Modes

Bit [7:6]	Operating Mode
00	Not possible
01	HVD or powered down (for HVD mode, the DIF bit must also be set)
10	SE
11	LVD SCSI

LOCK **Frequency Lock** **5**
This bit is used when enabling the SCSI clock quadrupler, which allows the LSI53C895 to transfer data at Ultra2 SCSI rates. Poll this bit for a 1 to determine that the clock quadrupler has locked to 160 MHz. For more information on enabling the clock quadrupler, refer to the descriptions about the SCSI Test One (STEST1) register, bits 2 and 3 on page 5-85.

R **Reserved** **[4:0]**

Register: 0x54–0x55 (0xD4–0xD5)

SCSI Output Data Latch (SODL)

Read/Write

15															0
SODL															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SODL **SCSI Output Data Latch** **[15:0]**

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCSI Control One (SCNTL1) register. This register sends data using programmed I/O. Data flows through this register when sending data in any mode. It also writes to the synchronous data FIFO when testing the chip. The power-up value of this register is indeterminate.

Register: 0x56–0x57

Reserved

Register: 0x58–0x59 (0xD8–0xD9)

SCSI Bus Data Lines (SBDL)

Read Only

15															0
SBDL															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SBDL **SCSI Bus Data Lines** **[15:0]**

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data through programmed I/O. This register can also be used for diagnostic testing or in low-level mode. The power-up value of this register is indeterminate.

Register: 0x5A–0x5B

Reserved

Register: 0x5C–0x5F (0xDC–0xDF)
Scratch Register B (SCRATCHB)
Read/Write

SCRATCHB **Scratch Register B** **[31:0]**
This is a general purpose user definable scratch pad register. Apart from CPU access, only register Read/Write and Memory Moves directed at the SCRATCH register will alter its contents. The LSI53C895 cannot fetch SCRIPTS instructions from this location. When bit 3 in the Chip Test Two (CTEST2) register is set, this register contains the base address for the 4 Kbyte internal RAM. Setting Chip Test Two (CTEST2) bit 3 only causes the base address to appear in the Scratch Register B (SCRATCHB) register; any information that was previously in the register remains intact. Any writes to this register while the bit is set passes through to the actual Scratch Register B (SCRATCHB) register. The power-up values are indeterminate.

Register: 0x60–0x7F (0xE0–0xFF)
Scratch Registers C–J (SCRATCHC–SCRATCHJ)
Read/Write

These registers are general-purpose scratch registers for user-defined functions. The LSI53C895 cannot fetch SCRIPTS instructions from this location. The power-up value of these registers is indeterminate.

Chapter 6
SCSI SCRIPTS Instruction Set

The LSI53C895 contains a SCSI SCRIPTS processor that permits both DMA and SCSI commands to be fetched from host memory or internal SCRIPTS RAM. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores. The SCRIPTS processor executes complex SCSI bus sequences independently of the host CPU. This chapter describes the SCSI SCRIPTS Instruction Set used to write these algorithms. This chapter includes these sections, which describe the benefits and use of SCSI SCRIPTS Instructions:

After power up and initialization of the LSI53C895, the chip can be operated in the low-level register interface mode or in the high-level SCSI SCRIPTS mode.

6.1 Low-Level Register Interface Mode

With the low-level register interface mode, the user has access to the DMA control logic and the SCSI bus control logic. An external processor has access to the SCSI bus signals and the low-level DMA signals, which allows creation of complicated board level test algorithms. The low-level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low-level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip pins.

6.2 High-Level SCSI SCRIPTS Mode

To operate in the SCSI SCRIPTS mode, the LSI53C895 requires only a SCRIPTS start address. The start address must be at a Dword (four byte) boundary to align all the following SCRIPTS at a Dword boundary since all SCRIPTS are 8 or 12 bytes long. Instructions are fetched until an interrupt instruction is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the LSI53C895 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer (DSP) register to restart the automatic fetching and execution of instructions.

The SCSI SCRIPTS mode of execution allows the LSI53C895 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI-oriented features included in the instruction set, and the ability to re-enter the SCSI algorithm at any point, this high-level interface is all that is required for both normal and exception conditions. Switching to low-level mode for error recovery should never be required.

Table 6.1 shows the types of SCRIPTS instructions are implemented in the LSI53C895:

Table 6.1 SCRIPTS Instructions

Instruction	Description
Block Move	Block Move instruction moves data between the SCSI bus and memory
I/O or Read/Write	I/O or Read/Write instructions cause the LSI53C895 to trigger common SCSI hardware sequences, or to move registers
Transfer Control	Transfer Control instruction allows SCRIPTS instructions to make decisions based on real time SCSI bus conditions
Memory Move	Memory Move instruction causes the LSI53C895 to execute block moves between different parts of main memory
Load and Store	Load and Store instructions provide a more efficient way to move data to/from memory from/to an internal register in the chip without using the Memory Move instruction

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DMA Command (DCMD) and DMA Byte Counter (DBC) registers, the second into the DMA SCRIPTS Pointer Save (DSPS) register. The third word, used only by Memory Move instructions, is loaded into the Temporary (TEMP) shadow register. In an indirect I/O or Move instruction, the first two 32-bit opcode fetches are followed by one or two more 32-bit fetch cycles.

6.2.1 Sample Operation

This sample operation describes execution of a SCRIPTS instruction for a Block Move instruction.

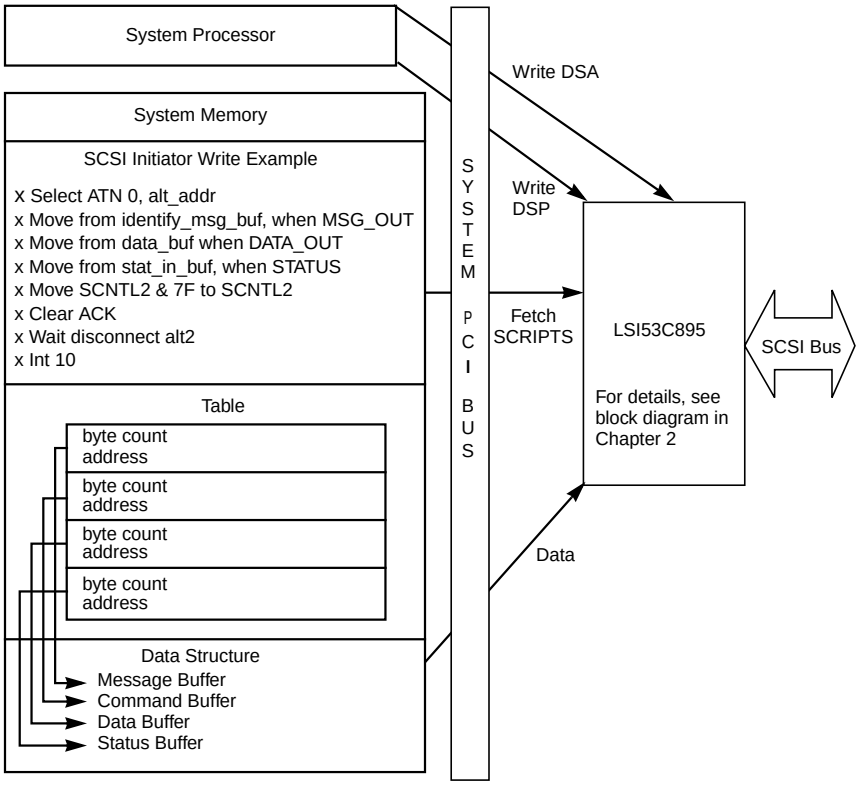
1. The host CPU, through programmed I/O, gives the DMA SCRIPTS Pointer (DSP) register (in the Operating Register file) the starting address in main memory that points to a SCSI SCRIPTS program for execution.
2. Loading the DMA SCRIPTS Pointer (DSP) register causes the LSI53C895 to fetch its first instruction at the address just loaded.

This is from main memory or the internal RAM, depending on the address.

3. The LSI53C895 typically fetches two Dwords (64 bits) and decodes the high order byte of the first longword as a SCRIPTS instruction. If the instruction is a Block Move, the lower three bytes of the first longword are stored and interpreted as the number of bytes to be moved. The second longword is stored and interpreted as the 32-bit beginning address in main memory to which the move is directed.
4. For a SCSI send operation, the LSI53C895 waits until there is enough space in the DMA FIFO to transfer a programmable size block of data. For a SCSI receive operation, it waits until enough data is collected in the DMA FIFO for transfer to memory. At this point, the LSI53C895 requests use of the PCI bus again to transfer the data.
5. When the LSI53C895 is granted the PCI bus, it executes (as a bus master) a burst transfer (programmable size) of data, decrements the internally stored remaining byte count, increments the address pointer, and then releases the PCI bus. The LSI53C895 stays off the PCI bus until the FIFO can again hold (for a write) or has collected (for a read) enough data to repeat the process.

The process repeats until the internally stored byte count has reached zero. The LSI53C895 releases the PCI bus and then performs another SCRIPTS instruction fetch cycle, using the incremented stored address maintained in the DMA SCRIPTS Pointer (DSP) register. Execution of SCRIPTS instructions continues until an error condition occurs or an interrupt SCRIPTS instruction is received. At this point, the LSI53C895 interrupts the host CPU and waits for further servicing by the host system. It can execute independent Block Move instructions specifying new byte counts and starting locations in main memory. In this manner, the LSI53C895 performs scatter/gather operations on data without requiring help from the host program, generating a host interrupt, or requiring an external DMA controller to be programmed. Figure 6.1 shows a SCRIPTS overview.

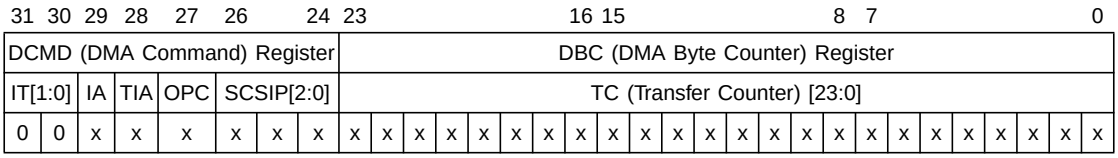
Figure 6.1 SCRIPTS Overview



6.3 Block Move Instruction

Performing a Block Move instruction, bit 5, Source I/O - Memory Enable (SIOM) and bit 4, Destination I/O - Memory Enable (DIOM) in the DMA Mode (DMODE) register determines whether the source/destination address resides in memory or I/O space. When data is being moved onto the SCSI bus, SIOM controls whether that data comes from I/O or memory space. When data is being moved off of the SCSI bus, DIOM controls whether that data goes to I/O or memory space.

6.3.1 First Dword



IT[1:0] **Instruction Type - Block Move** **[31:30]**
The IT bit configuration (00) defines a Block Move Instruction Type.

IA **Indirect Addressing** **29**
This bit determines if addressing is direct or indirect. If IA bit is (0), use destination field as an address (direct addressing). If IA bit is (1), use destination field as a pointer to an address (indirect addressing).

When this bit is zero, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip address register and incremented as data is transferred. The address of the data to move is in the second Dword of this instruction.

When this bit is one, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip DMA Next Address (DNAD) register using a third longword fetch (4-byte transfer across the host computer bus).

Direct Addressing

The byte count and absolute address are:

Command	Byte Count
Address of Data	

Indirect Addressing

Use the fetched byte count, but fetch the data address from the address in the instruction.

Command	Byte Count
Address of Pointer to Data	

Once the data pointer address is loaded, it is executed as when the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the LSI Logic SCSI SCRIPTS assembler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Note: Do not use indirect and table indirect addressing simultaneously; use only one addressing method at a time.

TIA **Table Indirect** **28**
32-Bit Addressing

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the Data Structure Address (DSA) register. Both the transfer count and the source/ destination address are fetched from this location.

Use the signed integer offset in bits [23:0] of the second four bytes of the instruction, added to the value in the Data Structure Address (DSA) register, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from

the data structure. Sign-extended values of all ones for negative values are allowed, but bits [31:24] are ignored.

Command	Not Used
Don't Care	Table Offset

Note: Do not use indirect and table indirect addressing simultaneously; use only one addressing method at a time.

Prior to the start of an I/O, the Data Structure Address (DSA) register should be loaded with the base address of the I/O data structure. The address may be any address on a longword boundary.

After a Table Indirect opcode is fetched, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

For a MOVE instruction, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the LSI53C895. Execution of the move begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries.

There are two restrictions on the placement of pointer data in system memory:

- The eight bytes of data in the MOVE instruction must be contiguous, as shown below, and
- Indirect data fetches are not available during execution of a Memory to Memory DMA operation.

00	Byte Count
Physical Data Address	

OPC **Op Code** **27**

This 1-bit Op Code field defines the type of Block Move (MOVE) Instruction to be preformed in Target and Initiator mode.

Target Mode

In Target mode, the Op Code bit defines the following operations:

OPC	Instruction Defined
0	MOVE/MOVE64
1	CHMOV/CHMOV64

These instructions perform the following steps:

1. The LSI53C895 verifies that it is connected to the SCSI bus as a Target before executing this instruction.
2. The LSI53C895 asserts the SCSI phase signals (SMSG/, SC_D/, and SI_O/) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the command phase, the LSI53C895 receives the first command byte and decodes its SCSI Group Code.
   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, and if the Vendor Unique Enhancement 1 (VUE1) bit (SCSI Control Two (SCNTL2), bit 1) is clear, then the LSI53C895 overwrites the DMA Byte Counter (DBC) register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b) If the Vendor Unique Enhancement 1 (VUE1) bit (SCSI Control Two (SCNTL2), bit 1) is set, the LSI53C895 receives the number of bytes in the byte count regardless of the group code.
   c) If the Vendor Unique Enhancement 1 bit is clear and group code is vendor unique, the LSI53C895 receives the number of bytes in the count.
   d) If any other Group Code is received, the DMA Byte Counter (DBC) register is not modified and the LSI53C895 requests the number of bytes specified in

the DMA Byte Counter (DBC) register. If the DMA Byte Counter (DBC) register contains 0x000000, an illegal instruction interrupt is generated.

4. The LSI53C895 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address specified in the DMA Next Address (DNAD) register. If the opcode bit is set and a data transfer ends on an odd byte boundary, the LSI53C895 stores the last byte in the SCSI Wide Residue (SWIDE) register during a receive operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

5. If the SATN/ signal is asserted by the Initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCSI Control One (SCNTL1) register controls whether the LSI53C895 halts on these conditions immediately, or waits until completion of the current Move.

Initiator Mode

In Target mode, the Op Code bit defines the following operations:

OPC	Instruction Defined
0	CHMOV
1	MOVE

These instructions perform the following steps:

1. The LSI53C895 verifies that it is connected to the SCSI bus as an Initiator before executing this instruction.

2. The LSI53C895 waits for an unserviced phase to occur. An unserviced phase is any phase (with SREQ/ asserted) for which the LSI53C895 has not yet transferred data by responding with a SACK/.

3. The LSI53C895 compares the SCSI phase bits in the DMA Command (DCMD) register with the latched SCSI phase lines stored in the SCSI Status One (SSTAT1)

register. These phase lines are latched when SREQ/ is asserted.

4. If the SCSI phase bits match the value stored in the SCSI Status One (SSTAT1) register, the LSI53C895 transfers the number of bytes specified in the DMA Byte Counter (DBC) register starting at the address pointed to by the DMA Next Address (DNAD) register. If the opcode bit is cleared and a data transfer ends on an odd byte boundary, the LSI53C895 stores the last byte in the SCSI Wide Residue (SWIDE) register during a receive operation, or in the SCSI Output Data Latch (SODL) register during a send operation. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can complete.

5. If the SCSI phase bits do not match the value stored in the SCSI Status One (SSTAT1) register, the LSI53C895 generates a phase mismatch interrupt and the instruction is not executed.

6. During a Message-Out phase, after the LSI53C895 has performed a select with Attention (or SATN/ is manually asserted with a Set ATN instruction), the LSI53C895 deasserts SATN/ during the final SREQ/SACK/ handshake.

7. When the LSI53C895 is performing a block move for Message-In phase, it does not deassert the SACK/ signal for the last SREQ/SACK/ handshake. Clear the SACK/ signal using the Clear SACK I/O instruction.

SCSIP[2:0] **SCSI Phase** **[26:24]**

This 3-bit field defines the SCSI information transfer phase. When the LSI53C895 operates in Initiator mode, these bits are compared with the latched SCSI phase bits in the SCSI Status One (SSTAT1) register. When the LSI53C895 operates in Target mode, it asserts the phase defined in this field. Table 6.2 describes the possible combinations and the corresponding SCSI phase.

Table 6.2 SCSI Information Transfer Phase

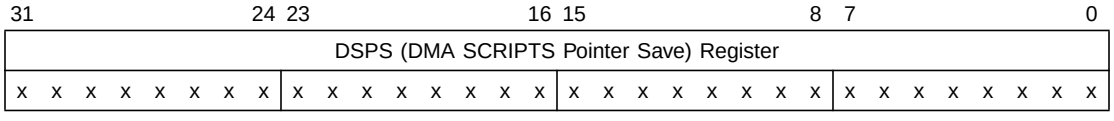
MSG	C_D	I_O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved-Out
1	0	1	Reserved-In
1	1	0	Message-Out
1	1	1	Message-In

TC[23:0] **Transfer Counter** **[23:0]**

This 24-bit field specifies the number of data bytes to be moved between the LSI53C895 and system memory. The field is stored in the DMA Byte Counter (DBC) register. When the LSI53C895 transfers data to/from memory, the DMA Byte Counter (DBC) register is decremented by the number of bytes transferred. In addition, the DMA Next Address (DNAD) register is incremented by the number of bytes transferred. This process is repeated until the DMA Byte Counter (DBC) register is decremented to zero. At this time, the LSI53C895 fetches the next instruction.

If bit 28 is set, indicating table indirect addressing, this field is not used. The byte count is instead fetched from a table pointed to by the Data Structure Address (DSA) register.

6.3.2 Second Dword



Start Address **[31:0]**

This 32-bit field specifies the starting address of the data to move to/from memory. This field is copied to the DMA Next Address (DNAD) register. When the LSI53C895

transfers data to or from memory, the DMA Next Address (DNAD) register is incremented by the number of bytes transferred.

When bit 29 is set, indicating indirect addressing, this address is a pointer to an address in memory that points to the data location. When bit 28 is set, indicating table indirect addressing, the value in this field is an offset into a table pointed to by the Data Structure Address (DSA). The table entry contains byte count and address information.

6.4 I/O Instruction

I/O Instructions perform the following SCSI operations in Target and Initiator mode. These I/O operations are chosen with the op code bits in the DMA Command (DCMD) register. All reserved bits are shaded.

OPC2	OPC1	OPC0	Target Mode	Initiator Mode
0	0	0	Reselect	Select
0	0	1	Disconnect	Wait Disconnect
0	1	0	Wait Select	Wait Reselect
0	1	1	Set	Set
1	0	0	Clear	Clear

This section describes these I/O operations.

6.4.1 First Dword

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCMD (DMA Command) Register								DBC (DMA Byte Counter) Register																							
IT[1:0]		OPC[2:0]			RA	TI	Sel	R				ENDID[3:0]				R						CC	TM	R		ACK	R		ATN	R		
0	1	x	x	x	x	x	x	0	0	0	0	x	x	x	x	0	0	0	0	0		x	x	0	0	x	0	0	x	0	0	0

IT[1:0] **Instruction Type - I/O Instruction** **[31:30]**
The IT bit configuration (01) defines an I/O Instruction Type.

OPC[2:0] **Op Code** **[29:27]**

The Op Code bit configurations define the I/O operation performed but the Op Code bit meanings change in Target mode compared to Initiator mode. Op Code bit configuration (101, 110, and 111) are considered Read/Write instructions, and are described in that section. This section describes Target mode operations.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1. The LSI53C895 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If it loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the LSI53C895 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the LSI53C895 wins arbitration, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register. This way the SCRIPTS can move on to the next instruction before the reselection completes. It continues executing SCRIPTS until a SCRIPT that requires a response from the Initiator is encountered.
3. If the LSI53C895 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register. Manually set the LSI53C895 to Initiator mode if it is reselected, or to Target mode if it is selected.

Disconnect Instruction

The LSI53C895 disconnects from the SCSI bus by deasserting all SCSI signal outputs.

Wait Select Instruction

1. If the LSI53C895 is selected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.
2. If reselected, the LSI53C895 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register. Manually set the LSI53C895 to Initiator mode when it is reselected.
3. If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the LSI53C895 aborts the Wait Select instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. Do not set SACK/ or SATN/ except for testing purposes. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set. When the carry bit is set, the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Note: None of the signals are set on the SCSI bus in Target mode.

Clear Instruction

When the SACK/ or SATN/ bits are cleared, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. Do not set SACK/ or SATN/ except for testing purposes. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

Note: None of the signals are cleared on the SCSI bus in the Target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1. The LSI53C895 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCSI Chip ID (SCID) register. If it loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the LSI53C895 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. Once the LSI53C895 wins arbitration, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register. This way the SCRIPTS can move to the next instruction before the selection completes. It continues executing SCRIPTS until a SCRIPT that requires a response from the Target is encountered.
3. If the LSI53C895 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register. Manually set the LSI53C895 to Initiator mode if it is reselected, or to Target mode if it is selected.
4. If the Select with SATN/ field is set, the SATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

The LSI53C895 waits for the Target to perform a “legal” disconnect from the SCSI bus. A “legal” disconnect

occurs when SBSY/ and SSEL/ are inactive for a minimum of one Bus Free delay (400 ns), after the LSI53C895 receives a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1. If the LSI53C895 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register. Manually set the LSI53C895 to Target mode when it is selected.
2. If the LSI53C895 is reselected, it fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register.
3. If the CPU sets the SIGP bit in the Interrupt Status (ISTAT) register, the LSI53C895 aborts the Wait Reselect instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DMA Next Address (DNAD) register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SCSI Output Control Latch (SOCL) register are set. When the target bit is set, the corresponding bit in the SCSI Control Zero (SCNTL0) register is also set. When the carry bit is set, the corresponding bit in the ALU is set.

Clear Instruction

When the SACK/ or SATN/ bits are cleared, the corresponding bits are cleared in the SCSI Output Control Latch (SOCL) register. When the target bit is cleared, the corresponding bit in the SCSI Control Zero (SCNTL0) register is cleared. When the carry bit is cleared, the corresponding bit in the ALU is cleared.

RA **Relative Addressing Mode** **26**

When this bit is set, the 24-bit signed value in the DMA Next Address (DNAD) register is used as a relative displacement from the current DMA SCRIPTS Pointer (DSP) address. Use this bit only in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can

contain an absolute alternate jump address or a relative transfer address.

TI **Table Indirect Mode** **25**

When this bit is set, the 24-bit signed value in the DMA Byte Counter (DBC) register is added to the value in the Data Structure Address (DSA) register, and used as an offset relative to the value in the Data Structure Address (DSA) register. The SCSI Contr0l Three (SCNTL3) value, SCSI ID, synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, load the Data Structure Address (DSA) with the base address of the I/O data structure. Any address on a Dword boundary is allowed. After a Table Indirect op code is fetched, the Data Structure Address (DSA) is added to the 24-bit signed offset value from the op code to generate the address of the required data. Both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any Dword boundary and may cross system segment boundaries. There are two restrictions on the placement of data in system memory:

- The I/O data structure must lie within the 8 Mbytes above or below the base address.
- An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SCSI Transfer (SXFER) register. The configuration bits are ordered as in the SCSI Contr0l Three (SCNTL3) register.

Config	ID	Offset/period	00

Use bit 25 only in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Use bits 25 and 26 individually or in combination to produce the following conditions:

Bit 25	Bit 26	Addressing Mode
0	0	Direct
0	1	Table Indirect
1	0	Relative
1	1	Table Relative

Direct

Uses the device ID and physical address in the instruction.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect

Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative

Uses the device ID in the instruction, but treats the alternate address as a relative jump.

Command	ID	Not Used	Not Used
Absolute Jump Offset			

Table Relative

Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. The value in bits [23:0] of the first four bytes of the SCRIPTS instruction is added to the data structure base address to form the fetch address.

Command	Table Offset
Alternate Jump Offset	

Sel	**Select with ATN/** This bit specifies whether SATN/ is asserted during the selection phase when the LSI53C895 is executing a Select instruction. When operating in Initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.	**24**
R	**Reserved**	**[23:20]**
ENDID[3:0]	**Encoded SCSI Destination ID** This 4-bit field specifies the destination SCSI ID for an I/O instruction.	**[19:16]**
R	**Reserved**	**[15:11]**
CC	**Set/Clear Carry** This bit is used in conjunction with a Set or Clear instruction to set or clear the Carry bit. Setting this bit with a Set instruction asserts the Carry bit in the ALU. Clearing this bit with a Clear instruction deasserts the Carry bit in the ALU.	**10**
TM	**Set/Clear Target Mode** This bit is used in conjunction with a Set or Clear instruction to set or clear Target mode. Setting this bit with a Set instruction configures the LSI53C895 as a Target device (this sets bit 0 of the SCSI Control Zero (SCNTL0) register). Clearing this bit with a Clear instruction configures the LSI53C895 as an Initiator device (this clears bit 0 of the SCSI Control Zero (SCNTL0) register).	**9**
R	**Reserved**	**[8:7]**
ACK	**Set/Clear SACK/**	**6**
R	**Reserved**	**[5:4]**
ATN	**Set/Clear SATN/** These two bits (6 and 3)are used in conjunction with a Set or Clear instruction to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI SACK/ signal. Bit 3 controls the SCSI SATN/ signal.	**3**

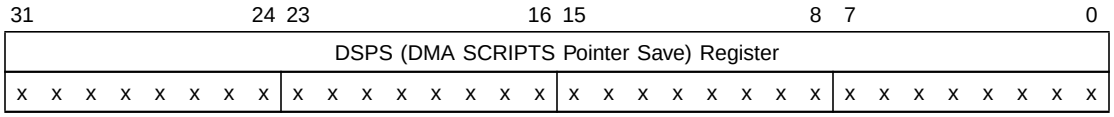
The Set instruction asserts SACK/ and/or SATN/ on the SCSI bus. The Clear instruction deasserts SACK/ and/or SATN/ on the SCSI bus. The corresponding bit in the SCSI Output Control Latch (SOCL) register is set or cleared depending on the instruction used.

Since SACK/ and SATN/ are Initiator signals, they are not asserted on the SCSI bus unless the LSI53C895 is operating as an Initiator or the SCSI Loopback Enable bit is set in the SCSI Test Two (STEST2) register.

The Set/Clear SCSI ACK/, ATN/ instruction is used after message phase Block Move operations to give the Initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the Initiator wishes to reject a message, it issues an Assert SCSI ATN instruction before a Clear SCSI ACK instruction.

R **Reserved** **[2:0]**

6.4.2 Second Dword



SA **Start Address** **[31:0]**

This 32-bit field contains the memory address to fetch the next instruction if the selection or reselection fails.

If relative or table relative addressing is used, this value is a 24-bit signed offset relative to the current DMA SCRIPTS Pointer (DSP) register value.

6.5 Read/Write Instructions

The Read/Write instruction supports addition, subtraction, and comparison of two separate values within the chip. It performs the desired operation on the specified register and the SCSI First Byte Received (SFBR) register, then stores the result back to the specified register or the SFBR. If the COM bit DMA Control (DMA Control (DCNTL), bit 0) is cleared, Read/Write instructions cannot be used.

6.5.1 First Dword

31 30	29 27	26 24	23	22 16	15 8	7 0
DCMD (DMA Command) Register			DBC (DMA Byte Counter) Register			
IT[1:0]	OPC[2:0]	Oper[2:0]	D8	A[6:0]	ImmD	Reserved - Must be 0
0 1	x x x	x x x	x	x x x x x x x	x x x x x x x x	0 0 0 0 0 0 0 0

IT[1:0] **Instruction Type - Read/Write Instruction** **[31:30]**
The configuration of the IT bits, the Op code bits and the Operator bits define the Read/Write Instruction Type. The configuration of all these bits determine which instruction is currently selected.

OPC[2:0] **Op Code** **[29:27]**
The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Op codes 0b000 through 0b100 are considered I/O instructions.

Oper[2:0] **Operator** **[26:24]**
These bits are used in conjunction with the opcode bits to determine which instruction is currently selected. Refer to Table 6.1 for field definitions.

D8 **Use data8/SFBR** **23**
When this bit is set, SCSI First Byte Received (SFBR) is used instead of the data8 value during a Read-Modify-Write instruction (see Table 6.1). This allows the user to add two register values.

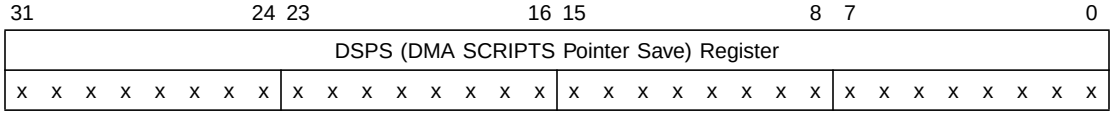
A[6:0] **Register Address - A[6:0]** **[22:16]**
It is possible to change register values from SCRIPTS in read-modify-write cycles or move to/from SCSI First Byte Received (SFBR) cycles. A[6:0] selects an 8-bit source/destination register within the LSI53C895.

ImmD **Immediate Data** **[15:8]**
This 8-bit value is used as a second operand in logical and arithmetic functions.

A7 **Upper Register Address Line [A7]** **7**
This bit is used to access registers 0x80–0xFF.

R **Reserved** **[6:0]**

6.5.2 Second Dword



Destination Address **[31:0]**
This field contains the 32-bit destination address where the data is to move.

6.5.3 Read-Modify-Write Cycles

During these cycles the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation is used to increment or decrement register values (or memory values if used in conjunction with a Memory to Register Move operation) for use as loop counters.

Subtraction is not available when SCSI First Byte Received (SFBR) is used instead of data8 in the instruction syntax. To subtract one value from another when using SCSI First Byte Received (SFBR), first XOR the value to subtract (subtrahend) with 0xFF, and add 1 to the resulting value. This creates the 2's complement of the subtrahend. The two values are then added to obtain the difference.

6.5.4 Move To/From SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SCSI First Byte Received (SFBR). See Table 6.3 for these Read/Write instructions. The possible functions of this instruction are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SCSI First Byte Received (SFBR) from/to any other register.
- Alter the value of a register with AND, OR, ADD, XOR, SHIFT LEFT, or SHIFT RIGHT operators.
- After moving values to the SCSI First Byte Received (SFBR), the compare and jump, call, or similar instructions are used to check the value.
- A Move to SFBR followed by a Move from SFBR is used to perform a register to register move.

Table 6.3 Read/Write Instructions

Operator	Op Code 111 Read Modify Write	Op Code 110 Move to SFBR	Op Code 101 Move from SFBR
000	Move data into register. Syntax: “Move data8 to RegA”	Move data into SCSI First Byte Received (SFBR) register. Syntax: “Move data8 to SFBR”	Move data into register. Syntax: “Move data8 to RegA”
001[1]	Shift register one bit to the left and place the result in the same register. Syntax: “Move RegA SHL RegA”	Shift register one bit to the left and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA SHL SFBR”	Shift the SFBR register one bit to the left and place the result in the register. Syntax: “Move SFBR SHL RegA”
010	OR data with register and place the result in the same register. Syntax: “Move RegA | data8 to RegA”	OR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA | data8 to SFBR”	OR data with SFBR and place the result in the register. Syntax: “Move SFBR | data8 to RegA”

Table 6.3 Read/Write Instructions (Cont.)

Operator	Op Code 111 Read Modify Write	Op Code 110 Move to SFBR	Op Code 101 Move from SFBR
011	XOR data with register and place the result in the same register. Syntax: “Move RegA XOR data8 to RegA”	XOR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA XOR data8 to SFBR”	XOR data with SFBR and place the result in the register. Syntax: “Move SFBR XOR data8 to RegA”
100	AND data with register and place the result in the same register. Syntax: “Move RegA & data8 to RegA”	AND data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA & data8 to SFBR”	AND data with SFBR and place the result in the register. Syntax: “Move SFBR & data8 to RegA”
101[1]	Shift register one bit to the right and place the result in the same register. Syntax: “Move RegA SHR RegA”	Shift register one bit to the right and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA SHR SFBR”	Shift the SFBR register one bit to the right and place the result in the register. Syntax: “Move SFBR SHR RegA”
110	Add data to register without carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA”	Add data to register without carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA + data8 to SFBR”	Add data to SFBR without carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA”
111	Add data to register with carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA with carry”	Add data to register with carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: “Move RegA + data8 to SFBR with carry”	Add data to SFBR with carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA with carry”

1. Data is shifted through the Carry bit and the Carry bit is shifted into the data byte.

Miscellaneous Notes:

- Substitute the desired register name or address for “RegA” in the syntax examples.
- data8 indicates eight bits of data.
- Use SCSI First Byte Received (SFBR) instead of data8 to add two register values.

6.6 Transfer Control Instruction

This section describes the Transfer Control Instructions. The configuration of the Op Code bits define which Transfer Control Instruction to perform.

6.6.1 First Dword

31 30	29 27	26 24	23	22	21	20	19	18	17	16	15 8	7 0
DCMD (DMA Command) Register			DBC (DMA Byte Counter) Register									
IT[1:0]	OPC[2:0]	SCSIP[2:0]	RA	R	CT	IF	JMP	CD	CP	WVP	DCM-Data Compare Mask	DCV-Data Compare Value
1 0	x x x	x x x	x	0	x	x	x	x	x	x	x x x x x x x x	x x x x x x x x

IT[1:0] **Instruction Type - Transfer Control Instruction [31:30]**
The IT bit configuration (10) defines the Transfer Control Instruction Type.

OPC [2:0] **Op Code [29:27]**
This 3-bit field specifies the type of Transfer Control Instruction to execute. All Transfer Control Instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in Initiator or Target mode. Transfer Control Instructions are shown in Table 6.4.

Table 6.4 Transfer Control Instructions

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	x	x	Reserved

Jump Instruction

The LSI53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields.

If the comparisons are true, then it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register. The DMA SCRIPTS Pointer (DSP) register now contains the address of the next instruction.

If the comparisons are false, the LSI53C895 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register, leaving the instruction pointer unchanged.

Call Instruction

The LSI53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register and that address value becomes the address of the next instruction.

When the LSI53C895 executes a Call instruction, the instruction pointer contained in the DMA SCRIPTS Pointer (DSP) register is stored in the Temporary (TEMP) register. Since the Temporary (TEMP) register is not a stack and can only hold one Dword, nested call instructions are not allowed.

If the comparisons are false, the LSI53C895 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Return Instruction

The LSI53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, it loads the DMA SCRIPTS Pointer (DSP) register with the contents of the DMA SCRIPTS Pointer Save (DSPS) register. That address value becomes the address of the next instruction.

When a Return instruction is executed, the value stored in the Temporary (TEMP) register is returned to the DMA SCRIPTS Pointer (DSP) register. The LSI53C895 does not check to see whether the Call instruction has already been executed. It does not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

If the comparisons are false, the LSI53C895 fetches the next instruction from the address pointed to by the DMA SCRIPTS Pointer (DSP) register and the instruction pointer is not modified.

Interrupt Instruction

The LSI53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, the LSI53C895 generates an interrupt by asserting the IRQ/ signal.

The 32-bit address field stored in the DMA SCRIPTS Pointer Save (DSPS) register can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the Interrupt Service Routine to quickly identify the point at which the interrupt occurred.

The LSI53C895 halts and the DMA SCRIPTS Pointer (DSP) register must be written to before starting any further operation.

Interrupt on the Fly Instruction

The LSI53C895 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields.

If the comparisons are true, and the Interrupt-on-the-Fly bit (Interrupt Status (ISTAT), bit 2) is set, the LSI53C895 asserts the Interrupt-on-the-Fly bit.

SCSIP[2:0] **SCSI Phase** **[26:24]**

This 3-bit field corresponds to the three SCSI bus phase signals that are compared with the phase lines latched when SREQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. Table 6.5 describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the LSI53C895 is operating in Initiator mode. Clear these bits when the LSI53C895 is operating in Target mode.

Table 6.5 SCSI Phase Comparisons

MSG	C/D	I/O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved-Out
1	0	1	Reserved-In
1	1	0	Message-Out
1	1	1	Message-In

RA **Relative Addressing Mode** **23**

When this bit is set, the 24-bit signed value in the DMA SCRIPTS Pointer Save (DSPS) register is used as a relative offset from the current DMA SCRIPTS Pointer (DSP) address (which is pointing to the next instruction, not the one currently executing). The relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address

Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address

Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
Don't Care	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently under execution by the LSI53C895. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (2's complement), the jump can be forward or backward.

A relative transfer can be to any address within a 16 Mbyte segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it does not require any run time alteration of physical addresses, and can be stored in and executed from a PROM.

R **Reserved** **22**

CT **Carry Test** **21**
When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

IF **Interrupt-on-the-Fly** **20**
When this bit is set, the interrupt instruction does not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt-on-the-Fly bit (Interrupt Status (ISTAT), bit 2) is asserted.

JMP **Jump If True/False** **19**

This bit determines whether the LSI53C895 branches when a comparison is true or when a comparison is false. This bit applies to phase compares, data compares, and carry tests. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Result of Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

CD **Compare Data** **18**

When this bit is set, the first byte received from the SCSI data bus (contained in the SCSI First Byte Received (SFBR) register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare occurs. The Jump if True/False bit determines the condition (true or false) to branch on.

CP **Compare Phase** **17**

When the LSI53C895 is in Initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by SREQ/) are compared to the Phase Field in the Transfer Control instruction. If they match, the comparison is true. The Wait for Valid Phase bit controls when the compare occurs. When the LSI53C895 is operating in Target mode and this bit is set it tests for an active SCSI SATN/ signal.

WVP **Wait For Valid Phase** **16**

If the Wait for Valid Phase bit is set, the LSI53C895 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is cleared, the LSI53C895 compares the SCSI phase and data immediately.

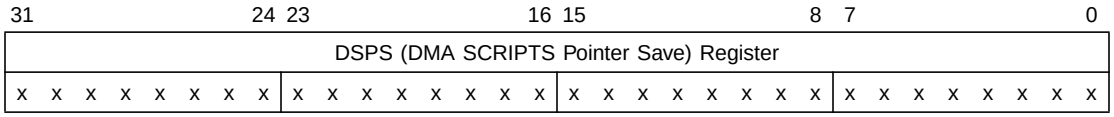
DCM **Data Compare Mask** **[15:8]**

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, if any mask bits are set, the corresponding bit in the SCSI First Byte Received (SFBR) data byte is ignored. For instance, a mask of 0b01111111 and data compare value of 0b1XXXXXXX allows the SCRIPTS processor to determine whether or not the high order bit is set while ignoring the remaining bits.

DCV **Data Compare Value** **[7:0]**

This 8-bit field is the data compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

6.6.2 Second Dword



Jump Address **[31:0]**

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the LSI53C895 fetches the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DMA SCRIPTS Pointer (DSP) register and becomes the current instruction pointer.

6.7 Memory Move Instructions

For Memory Move instructions, bits 5 and 4 (SIOM and DIOM) in the DMA Mode (DMODE) register determine whether the source or destination addresses reside in memory or I/O space. By setting these bits appropriately, data may be moved within memory space, within I/O space, or between the two address spaces.

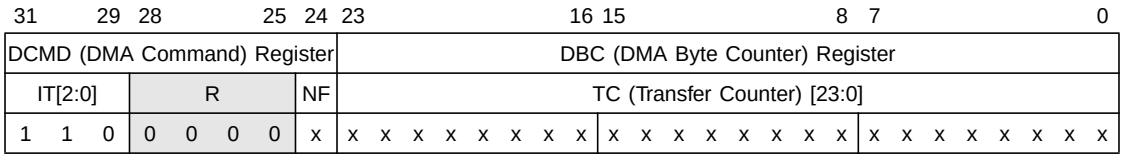
The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the LSI53C895 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 Mbytes may be transferred with one instruction. There are two restrictions:

- Both the source and destination addresses must start with the same address alignment (A[1:0]) must be the same). If the source and destination are not aligned, then an illegal instruction interrupt occurs. For the PCI Cache Line Size register setting to take effect, the source and destination must be the same distance from a cache line boundary.
- Indirect addresses are not allowed. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

The DMA SCRIPTS Pointer Save (DSPS) and Data Structure Address (DSA) registers are additional holding registers used during the Memory Move. However, the contents of the Data Structure Address (DSA) register are preserved.

6.7.1 First Dword



IT[2:0] **Instruction Type - Memory Move** **[31:29]**
The IT bit configuration (110) defines a Memory Move Instruction Type.

R **Reserved** **[28:25]**
These bits are reserved and must be zero. If any of these bits are set, an illegal instruction interrupt occurs.

NF **No Flush** **24**
When this bit is set, the LSI53C895 performs a Memory Move without flushing the prefetch unit. When this bit is cleared, the Memory Move instruction automatically flushes the prefetch unit. Use the No Flush option if the source and destination are not within four instructions of the current Memory Move instruction.

Note: This bit has no effect unless the Prefetch Enable bit in the DMA Control (DCNTL) register is set. For information on SCRIPTS instruction prefetching, see Chapter 2, "Functional Description."

TC[23:0] **Transfer Counter** **[23:0]**
The number of bytes to transfer is stored in the lower 24 bits of the first instruction word.

6.7.2 Read/Write System Memory from a SCRIPT

By using the Memory Move instruction, single or multiple register values are transferred to or from system memory.

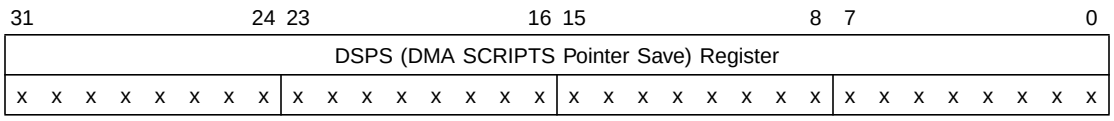
Because the LSI53C895 responds to addresses as defined in the Base Address Register Zero (I/O) or Base Address One (Memory) registers, it can be accessed during a Memory Move operation if the source or destination address decodes to within the chip register space. If this occurs, the register indicated by the lower seven bits of the address is taken as the data source or destination. In this way, register values are

saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SCSI First Byte Received (SFBR) is not writable using the CPU, and therefore not by a Memory Move. However, it can be loaded using SCRIPTS Read/Write operations. To load the SCSI First Byte Received (SFBR) with a byte stored in system memory, first move the byte to an intermediate LSI53C895 register (for example, a SCRATCH register), and then to the SCSI First Byte Received (SFBR).

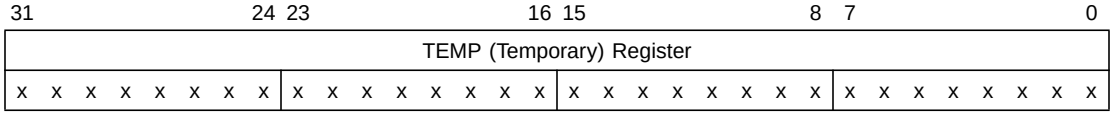
The same address alignment restrictions apply to register access operations as to normal memory to memory transfers.

6.7.3 Second Dword



DSPS Register **[31:0]**
These bits contain the source address of the Memory Move.

6.7.4 Third Dword



TEMP Register **[31:0]**
These bits contain the destination address for the Memory Move.

6.8 Load and Store Instructions

The Load and Store instructions provide a more efficient way to move data from/to memory to/from an internal register in the chip without using the normal memory move instruction.

The load and store instructions are represented by two-Dword op codes. The first Dword contains the DMA Command (DCMD) and DMA Byte Counter (DBC) register values. The second Dword contains the DMA SCRIPTS Pointer Save (DSPS) value. This is either the actual memory location of where to load/store, or the offset from the Data Structure Address (DSA), depending on the value of bit 28 (DSA Relative).

A maximum of 4 bytes may be moved with these instructions. The register address and memory address must have the same byte alignment, and the count set such that it does not cross Dword boundaries. The memory address may not map back to the chip, excluding RAM and ROM. If it does, a PCI read/write cycle occurs (the data does not actually transfer to/from the chip), and the chip issues an interrupt (Illegal Instruction Detected) immediately following.

Bit A1	Bit A0	Number of Bytes Allowed to Load/Store
0	0	One, two, three or four
0	1	One, two, or three
1	0	One or two
1	1	One

The SIOM and DIOM bits in the DMA Mode (DMODE) register determine whether the destination or source address of the instruction is in Memory space or I/O space, as illustrated in the following table. The Load/Store utilizes the PCI commands for I/O read and I/O write to access the I/O space.

Bit	Source	Destination
SIOM (Load)	Memory	Register
DIOM (Store)	Register	Memory

6.8.1 First Dword

31 29	28	27 26	25	24	23	16 15	8 7	3 2 0
DCMD (DMA Command) Register					DBC (DMA Byte Counter) Register			
IT[2:0]	DSA	R	NF	LS	R	RA[6:0]	R	BC
1 1 1	x	0 0	x	x	0	x x x x x x x	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	x x x

IT[2:0] **Instruction Type** **[31:29]**
These bits should be 0b111, indicating the Load and Store instruction.

DSA **DSA Relative** **28**
When this bit is cleared, the value in the DMA SCRIPTS Pointer Save (DSPS) is the actual 32-bit memory address used to perform the Load/Store to/from. When this bit is set, the chip determines the memory address to perform the Load/Store to/from by adding the 24 bit signed offset value in the DMA SCRIPTS Pointer Save (DSPS) to the Data Structure Address (DSA).

R **Reserved** **[27:26]**

NF **No Flush (Store Instruction Only)** **25**
When this bit is set, the LSI53C895 performs a Store without flushing the prefetch unit. When this bit is cleared, the Store instruction automatically flushes the prefetch unit. Use No Flush if the source and destination are not within four instructions of the current Store instruction. This bit has no effect on the Load instruction.

Note: This bit has no effect unless the Prefetch Enable bit in the DMA Control (DCNTL) register is set. For information on SCRIPTS instruction prefetching, see Chapter 2, "Functional Description."

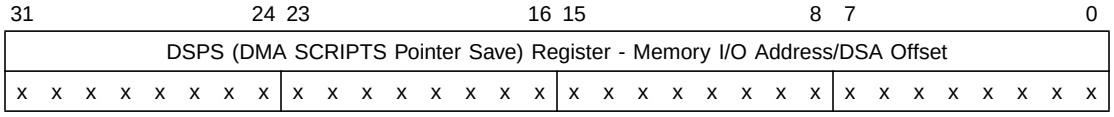
LS **Load/Store** **24**
When this bit is set, the instruction is a Load. When cleared, it is a Store.

R **Reserved** **[23]**

RA[6:0] **Register Address** **[22:16]**
A[6:0] selects the register to load/store to/from within the LSI53C895.

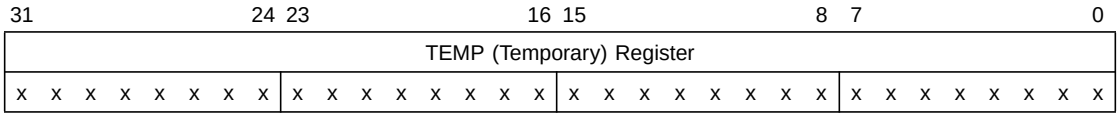
R	**Reserved**	**[15:3]**
BC	**Byte Count** This value is the number of bytes to load/store.	**[2:0]**

6.8.2 Second Dword



Memory I/O Address/DSA Offset **[31:0]**
This is the actual memory location of where to load/store, or the offset from the Data Structure Address (DSA) register value.

6.8.3 Third Dword



TEMP Register **[31:0]**
These bits contain the destination address for the Memory Move.

Chapter 7
Electrical Characteristics

This chapter specifies the LSI53C895 electrical and mechanical characteristics. It is divided into the following sections:

7.1 DC Characteristics

This section of the manual describes LSI53C895 DC characteristics. Table 7.1 through Table 7.13 give current and voltage specifications. Figure 7.1 and Figure 7.2 are driver schematics.

Table 7.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	–55	150	°C	–
V_{DD}	Supply voltage	–0.5	5.0	V	–
V_{IN}	Input voltage	V_{SS} –0.3	V_{DD} +0.3	V	–
I_{LP}[2]	Latch-up current	±150	–	mA	–
ESD[3]	Electrostatic discharge	–	2 k	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
2. $-2\ V < V_{PIN} < 8\ V$.
3. SCSI pins only.

Table 7.2 Operating Conditions

Symbol	Parameter	Min	Max[1]	Unit	Test Conditions
V_{DD}	Supply voltage	3.135	3.465	V	–
I_{DD}	Supply current (dynamic) Supply current (static)	– –	130 1	mA mA	– –
$I_{DD\text{-}SCSI}$	LVD pad supply current	–	600	mA	RBIAS = 2.2 KΩ, V_{DD} = 3.3 V
T_A	Operating free air	0	70	°C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	67	°C/W	–

1. Conditions that exceed the operating limits may cause the device to function incorrect.

Table 7.3 SCSI Signals, LVD Drivers—SD[15:0]+/–, SDP[1:0]+/–, SREQ+/–, SACK+/–, SMSG+/–, SIO+/–, SCD+/–, SATN+/–, SBSY+/–, SSEL+/–, SRST+/–*

Symbol	Parameter[1]	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	13	mA	Asserted state
I_O-	Sink (–) current	–7	–13	mA	Asserted state
I_O+	Sink (–) current	–3.5	–6.5	mA	Negated state
I_O-	Source (+) current	3.5	6.5	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	–
I_{OZ} (SRST– only)	3-state leakage	–500	–50	µA	–

1. V_{CM} = 0.7–1.8 V, R_L = 0–110 Ω, R_{BIAS} = 2.2 KΩ. Positive current is into SCSI I/O processor.

Figure 7.1 LVD Transmitter

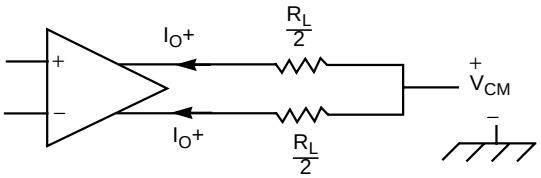


Table 7.4 SCSI Signals, LVD Receivers—SD[15:0]+/–, SDP[1:0]+/–, SREQ+/–, SACK+/–, SMSG+/–, SIO+/–, SCD+/–, SATN+–, SBSY+/–, SSEL+/–, SRST+/–

Symbol	Parameter[1]	Min	Max	Units
V_I	LVD receiver voltage asserting	60	–	mV
V_I	LVD receiver voltage negating	–	–60	mV

1. VCM = 0.7 – 1.8 V.

Figure 7.2 LVD Receiver

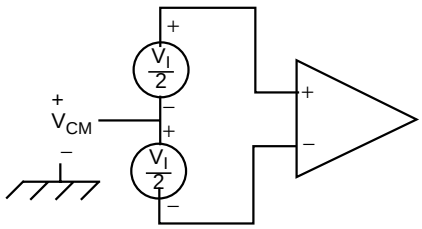


Table 7.5 SCSI Signal—DIFFSENS

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	HVD sense voltage	2.4	V_{DD} +0.3	V	–
V_S	LVD sense voltage	0.7	1.9	V	–
V_{IL}	SE sense voltage	V_{SS} –0.3	0.5	V	–
I_{OZ}	3-State leakage	–10	10	µA	–

Table 7.6 SCSI Signals—RBIAS+/–

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IN}	Input voltage	V_{DD} –0.2	–	V	–125 µA

Table 7.7 Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	15	pF	–

Table 7.8 Output Signal—MAC/_TESTOUT

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	–16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	3-state leakage	–10	10	µA	–

Table 7.9 Input Signals—CLK[1], RST/[1], IDSEL, GNT/, SCLK/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V5BIAS(PCI)	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.3 V_{DD}	V	–
I_{IN}	Input current	–10	10	µA	–
I_{PULL}	Pull-up current	25	–	µA	–

1. I_{PULL} not possible.

Table 7.10 Bidirectional Signals—AD[31:0], C_BE/[3:0], FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR, REQ/, IRQ/, SERR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V5BIAS(PCI)	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.3 V_{DD}	V	–
V_{OH}	Output high voltage	0.9 V_{DD}	V_{DD}	V	–0.5 µA
V_{OL}	Output low voltage	V_{SS}	0.1 V_{DD}	V	1.5 µA
I_{OZ}	3-state leakage	–10	10	µA	–
I_{PULL}	Pull-up current	25		µA	–

Table 7.11 Bidirectional Signals—GPIO0_FETCH/, GPIO1_MASTER/, GPIO2, GPIO3, GPIO4, MAD[7:0]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS(MEM)	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	–8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	–

Table 7.12 Bidirectional Signals—MAS/[1:0], MCE/, MOE/, MWE/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS (PCI or MEM)	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	–4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{OZ}	3-state leakage	–10	10	µA	–
I_{PULL}	Pull-up current	25	–	µA	–

Table 7.13 Input Signal—BIG_LIT/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS(PCI)	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IN}	Input current	–10	10	µA	–
I_{PULL}	Pull-up current	25	–	µA	–

7.2 3.3 Volt PCI DC Characteristics

Table 7.14 through Table 7.17 list characteristics that apply whenever a V_{DD} source of 3.3 volts is supplied to the V_{DD}–I pins of the LSI53C895.

Table 7.14 Bidirectional Signals—AD[31:0], C_BE[3:0]/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR, BYTEPAR[3:0]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	–0.5	0.3 V_{DD}	V	–
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	–0.5 mA
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1.5 mA
I_{OZ}	3-state leakage	–10	10	V	–

Table 7.15 Input Signals—CLK, GNT/, IDSEL, RST/

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	–0.5	0.3 V_{DD}	V	–
I_{IN}	Input leakage	–10	10	µA	–

Table 7.16 Output Signals—IRQ/, REQ/

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	–0.5 mA
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1.5 mA
I_{OZ}	3-state leakage	–10	10	µA	–

Table 7.17 Output Signal—SERR/

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1.5 mA
I_{OZ}	3-state leakage	–10	10	µA	–

7.3 TolerANT Technology Electrical Characteristics

The LSI53C895 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Table 7.18 provides electrical characteristics for SE SCSI signals. Figure 7.3 through Figure 7.7 provide reference information for testing SCSI signals.

Table 7.18 TolerANT Technology Electrical Characteristics[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.0	V_{DD} +0.3	V	I_{OH} = 7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, high to low	1.0	1.2	V	–
V_{TL}	Threshold, low to high	1.4	1.6	V	–
V_{TH}-V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V

Table 7.18 TolerANT Technology Electrical Characteristics[1] (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	$-0.5 < V_{DD} < 5.25$ V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	–20	µA	$-0.5 < V_{DD} < 5.25$ V_{PIN} = 0.5 V
R_I	Input resistance	20	–	MΩ	SCSI pins[4]
C_P	Capacitance per pin	–	15	pF	PQFP
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 7.1
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 7.1
dV_H/dt	Slew rate, low to high	0.15	0.50	V/ns	Figure 7.1
dV_L/dt	Slew rate, high to low	0.15	0.50	V/ns	Figure 7.1
ESD	Electrostatic discharge	2	–	KV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 7.2
	Ultra filter delay	10	15	ns	Figure 7.2
	Ultra2 filter delay	5	8	ns	Figure 7.2
	Extended filter delay	40	60	ns	Figure 7.2

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, SACK/.
3. Single pin only; irreversible damage may occur if sustained for one second.
4. SCSI RESET pin has 10 KΩ pull-up resistor.

Figure 7.3 Rise and Fall Time Test Conditions

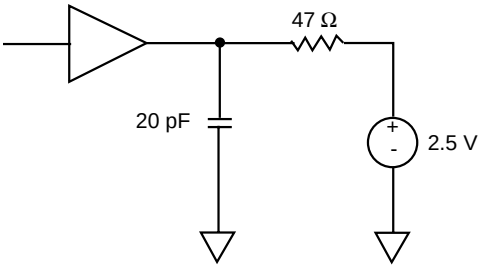
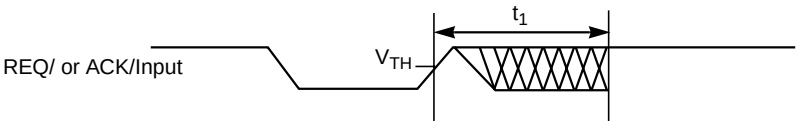


Figure 7.4 Input Filtering



* t_1 is the input filtering period

Figure 7.5 Hysteresis of SCSI Receiver

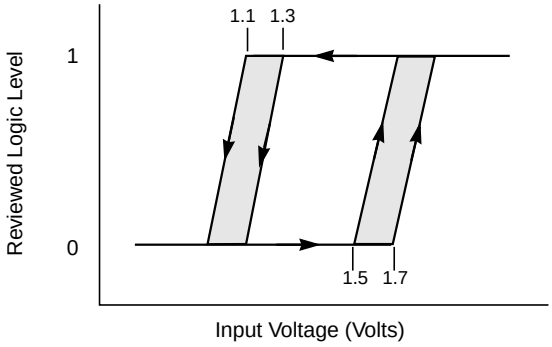


Figure 7.6 Input Current as a Function of Input Voltage

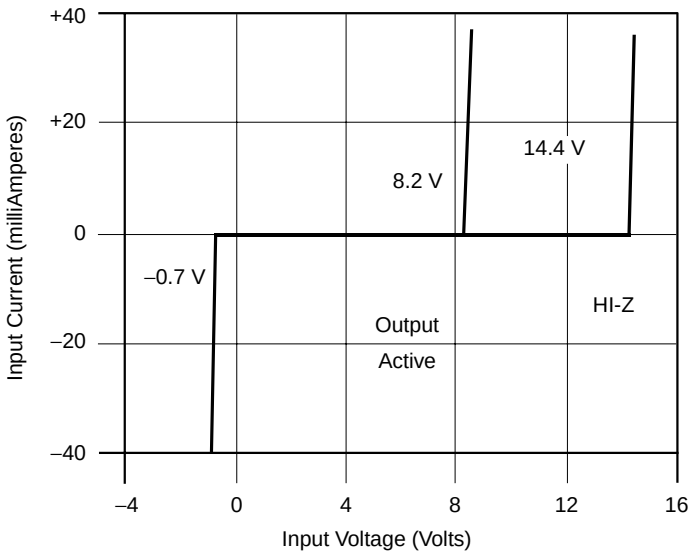
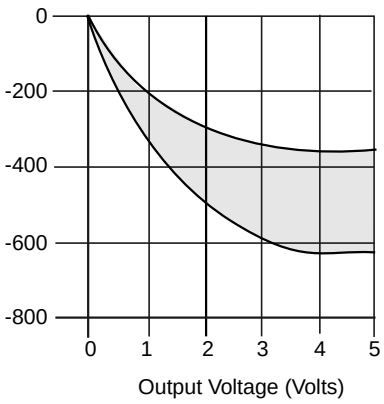
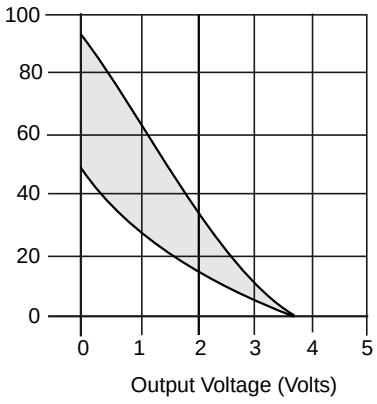


Figure 7.7 Output Current as a Function of Output Voltage





7.4 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 7.1, “DC Characteristics”). Chip timing is based on simulation at worst case voltage, temperature, and processing. The timing was developed with a load capacitance of 50 pF. Table 7.19 and Figure 7.8 provide External Clock timing data.

Table 7.19 External Clock[1]

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time	30	DC	ns
	SCSI clock cycle time (SCLK)[2]	25	60	ns
t_2	CLK low time[3]	10	–	ns
	SCLK low time[3]	6	33	ns
t_3	CLK high time[3]	12	–	ns
	SCLK high time[3]	10	33	ns
t_4	CLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. The timing are for an external 40 MHz clock. A quadrupled 40 MHz clock is required for Ultra2 SCSI operation.
2. This parameter must be met to ensure SCSI timing are within specification.
3. Duty cycle not to exceed 60/40.

Figure 7.8 External Clock

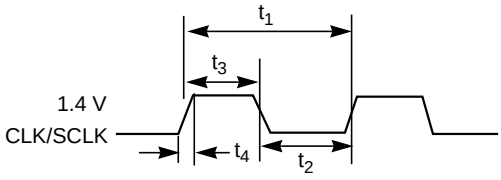


Table 7.20 and Figure 7.9 provide Reset Input timing data.

Table 7.20 Reset Input

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	–	t_{CLK}
t_2	Reset deasserted setup to CLK HIGH	0	–	ns
t_3	MAD setup time to CLK HIGH (for configuring the MAD bus only)	20	–	ns
t_4	MAD hold time from CLK HIGH (for configuring the MAD bus only)	20	–	ns

Figure 7.9 Reset Input

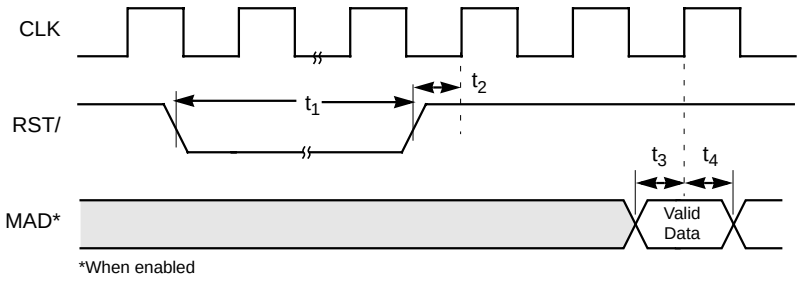
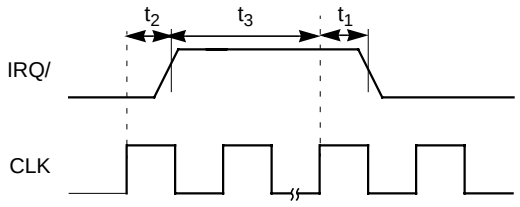


Table 7.21 and Figure 7.10 provide Interrupt Output timing data.

Table 7.21 Interrupt Output

Symbol	Parameter	Min	Max	Units
t_1	CLK HIGH to IRQ/ LOW	2	11	ns
t_2	CLK HIGH to IRQ/ high	2	11	ns
t_3	IRQ/ deassertion time	3	–	CLKs

Figure 7.10 Interrupt Output



7.5 PCI and External Memory Interface Timing Diagram

Figure 7.11 through Figure 7.38 represent signal activity when the LSI53C895 accesses the PCI bus. This section includes timing diagrams for access to three groups of external memory configurations. The first group applies to systems with memory size of 64 Kbytes and above; one byte read or write cycle, and fast or normal ROMs. The second group applies to systems with memory size of 64 Kbytes and above, one-byte read or write cycles, and slow ROMs. The third group applies to systems with memory size of 64 Kbytes or less, one-byte read or write cycles, and normal or fast ROM.

Note: Multiple byte accesses to the external memory bus increase the read or write cycle by 11 clocks for each additional byte.

Timing diagrams included in this section are:

- Target Timing
  - PCI Configuration Register Read
  - PCI Configuration Register Write
  - Operating Register/SCRIPTS RAM Read
  - Operating Register/SCRIPTS RAM Write
- Initiator Timing
  - Op Code Fetch, Nonburst
  - Burst Op Code Fetch
  - Back to Back Read
  - Back to Back Write
  - Burst Read
  - Burst Write
- External Memory Timing
  - External Memory Read
  - External Memory Write
  - Read Cycle, Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access
  - Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access, Write Cycle
  - Normal/Fast Memory (≥ 128 Kbytes), Multiple Byte Access, Read Cycle
  - Normal/Fast Memory (≥ 128 Kbytes) Multiple Byte Access, Write Cycle
  - Read Cycle, Slow Memory (≥ 128 Kbytes)
  - Write Cycle, Slow Memory (≥ 128 Kbytes)
  - Read cycle, ≤ 64 Kbytes ROM
  - Write Cycle, ≤ 64 Kbytes ROM

7.5.1 Target Timing

Tables 7.22 through 7.25 and figures 7.11 through 7.14 describe LSI53C895 target timing.

Table 7.22 Configuration Register Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns

Figure 7.11 PCI Configuration Register Read

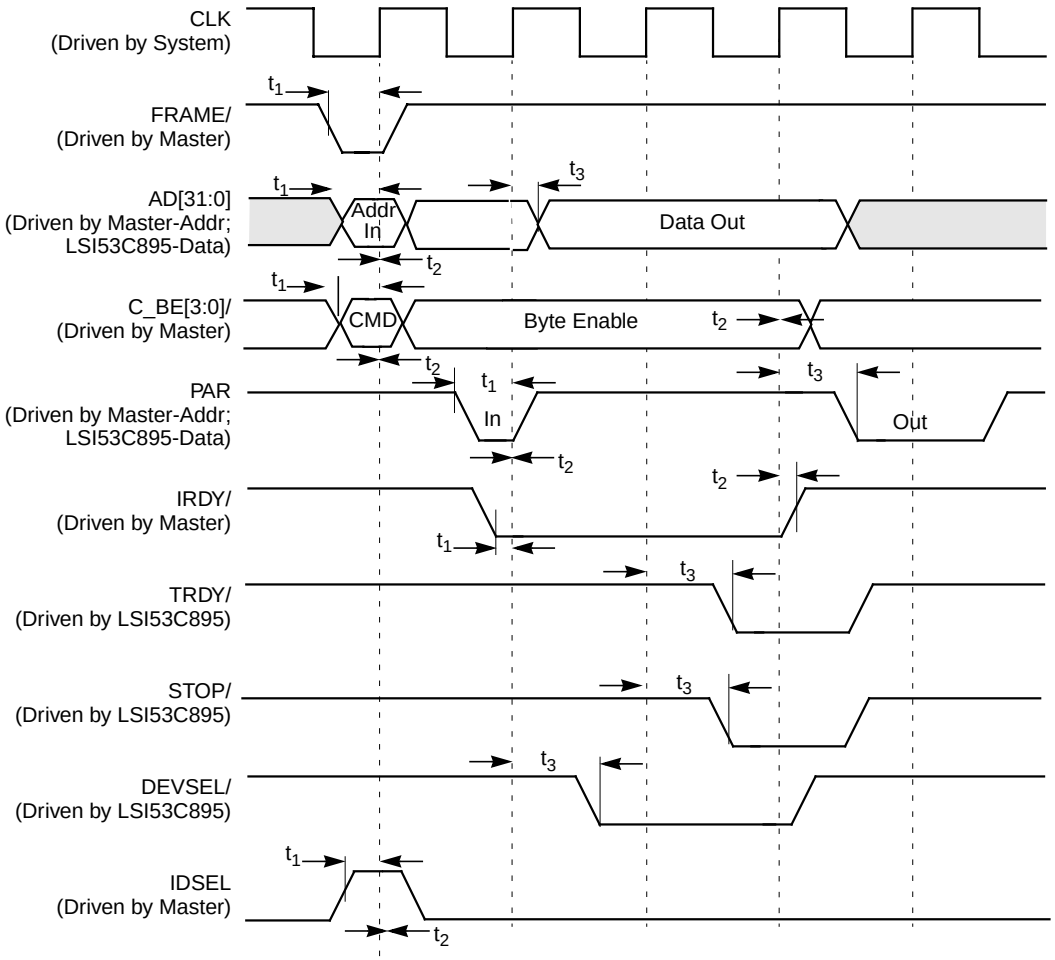


Table 7.23 Configuration Register Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns

Figure 7.12 PCI Configuration Register Write

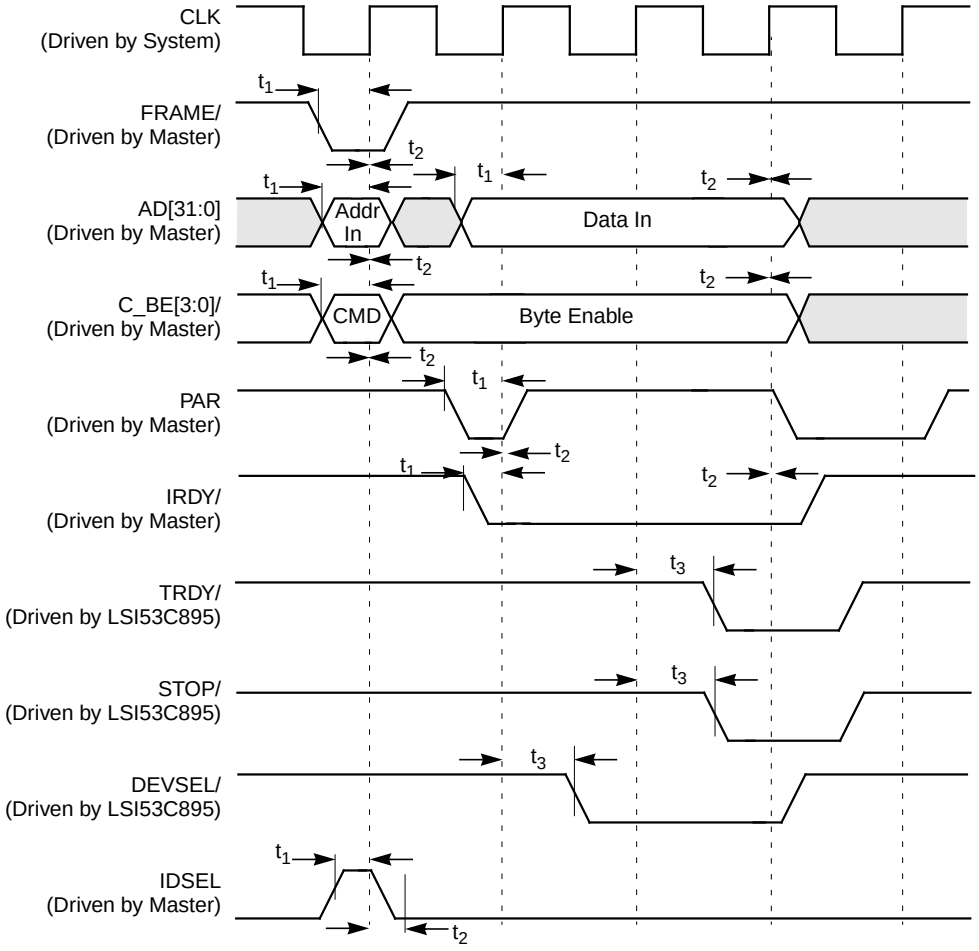


Table 7.24 Operating Register/SCRIPTS RAM Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns

Figure 7.13 Operating Register/SCRIPTS RAM Read

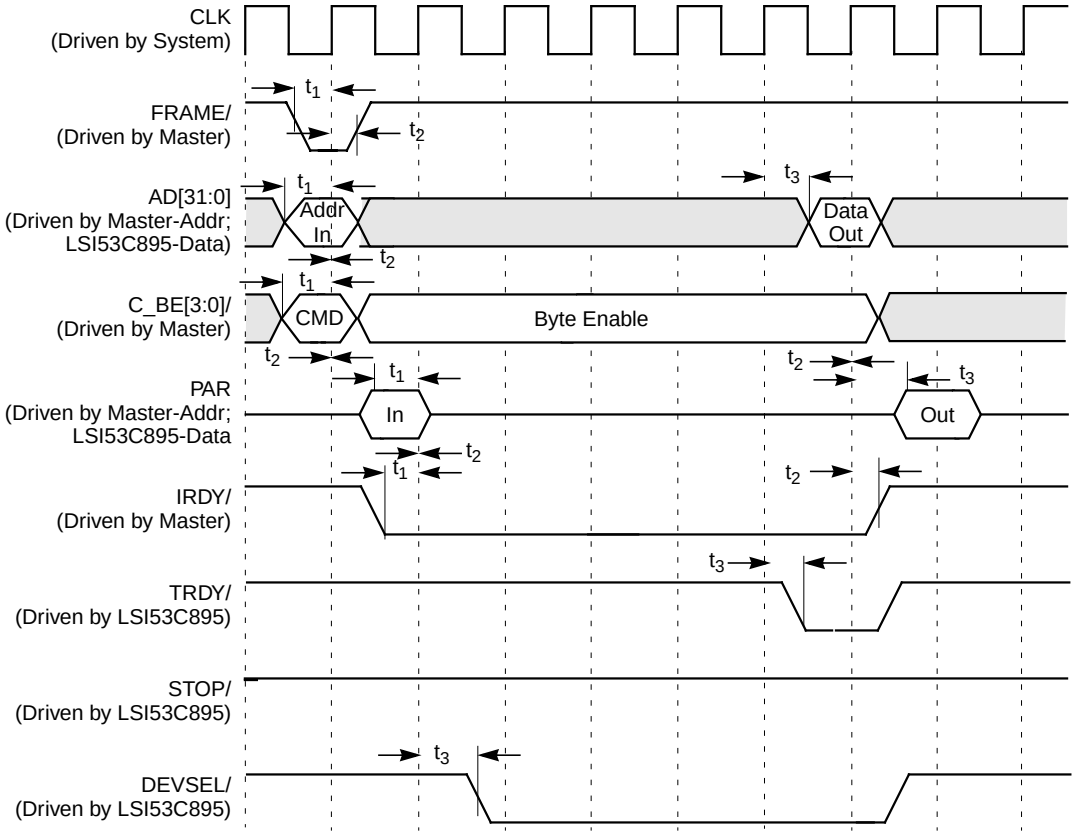
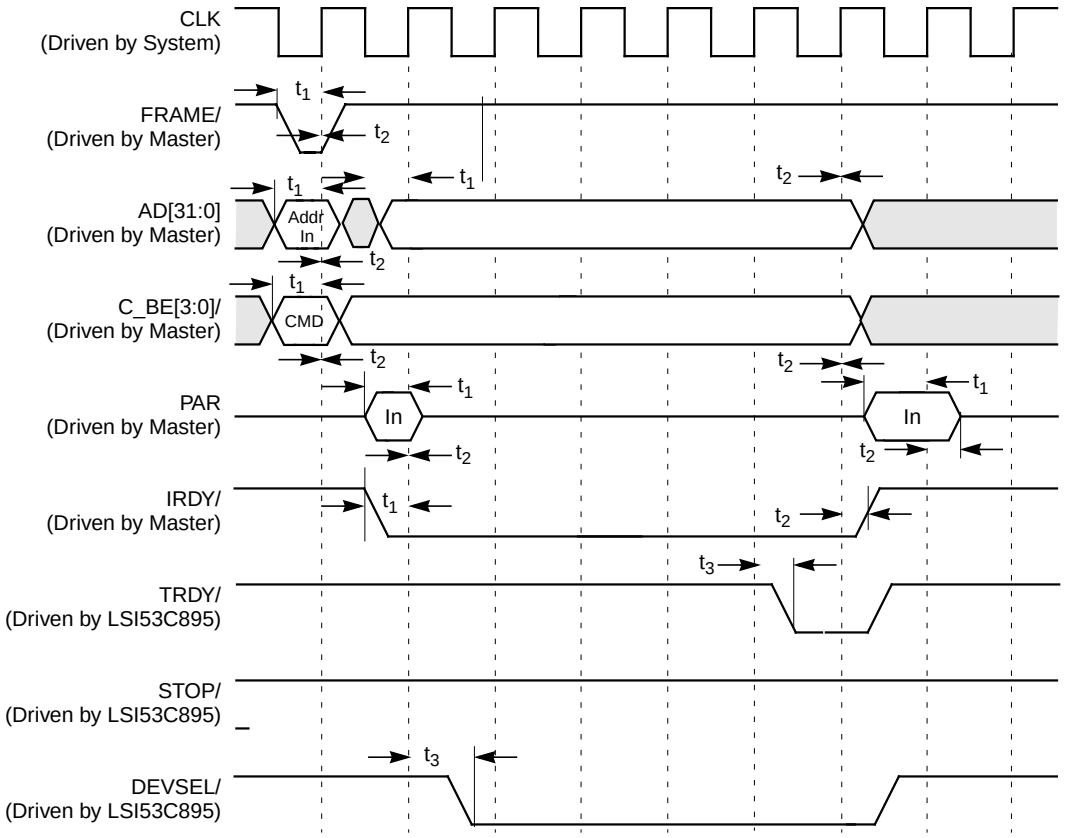


Table 7.25 Operating Register/SCRIPTS RAM Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns

Figure 7.14 Operating Register/SCRIPTS RAM Write



7.5.2 Initiator Timing

Tables 7.26 through 7.31 and figures 7.15 through 7.20 describe LSI53C895 initiator timing.

Table 7.26 Op Code Fetch, Nonburst

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_7	CLK HIGH to FETCH/ LOW	–	20	ns
t_8	CLK HIGH to FETCH/ HIGH	–	20	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGH	–	20	ns

Figure 7.15 Op Code Fetch, Nonburst

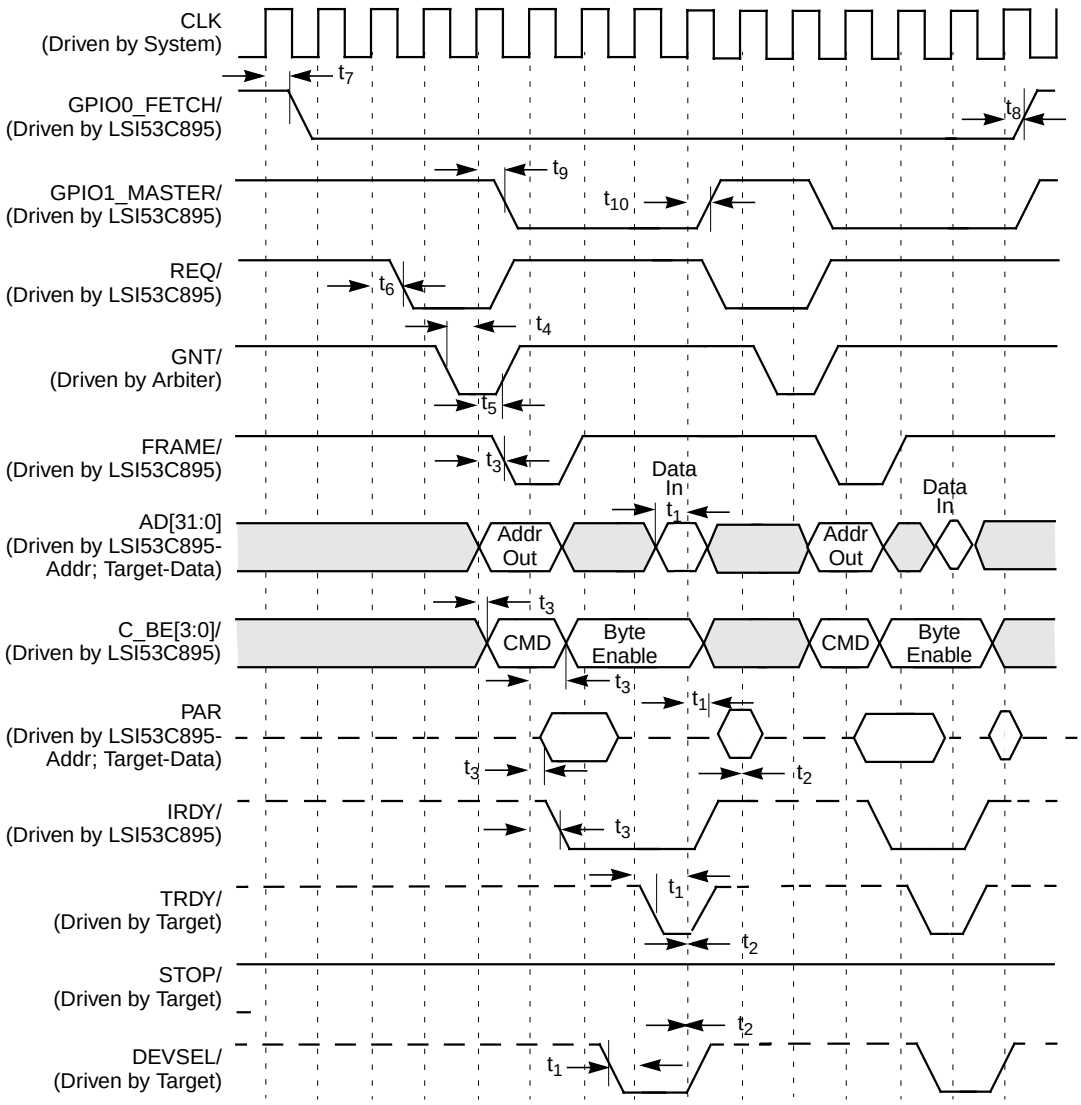


Table 7.27 Burst Op Code Fetch

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_7	CLK HIGH to FETCH/ LOW	–	20	ns
t_8	CLK HIGH to FETCH/ HIGH	–	20	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGh	–	20	ns

Figure 7.16 Burst Op Code Fetch

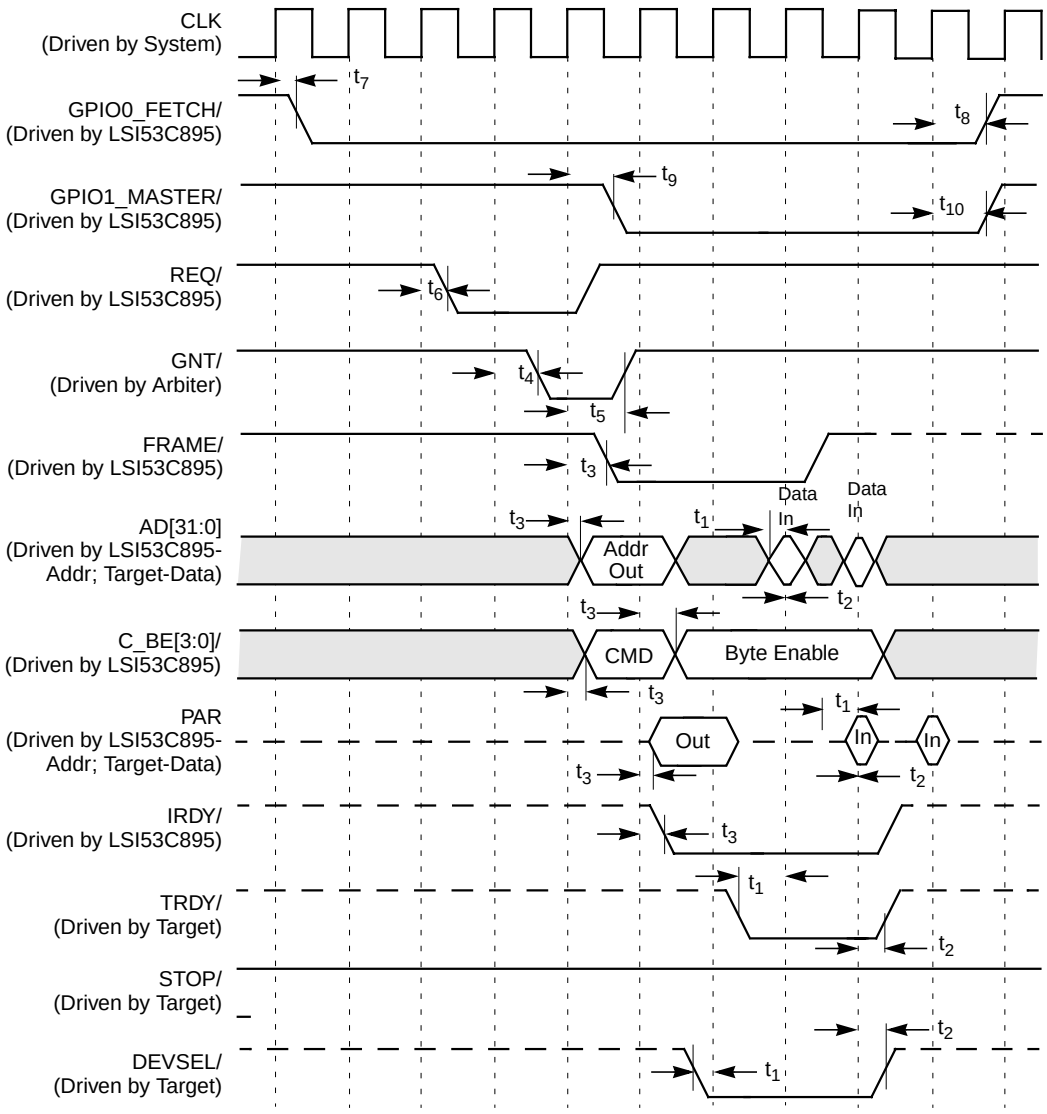


Table 7.28 Back to Back Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGH	–	20	ns

Figure 7.17 Back to Back Read

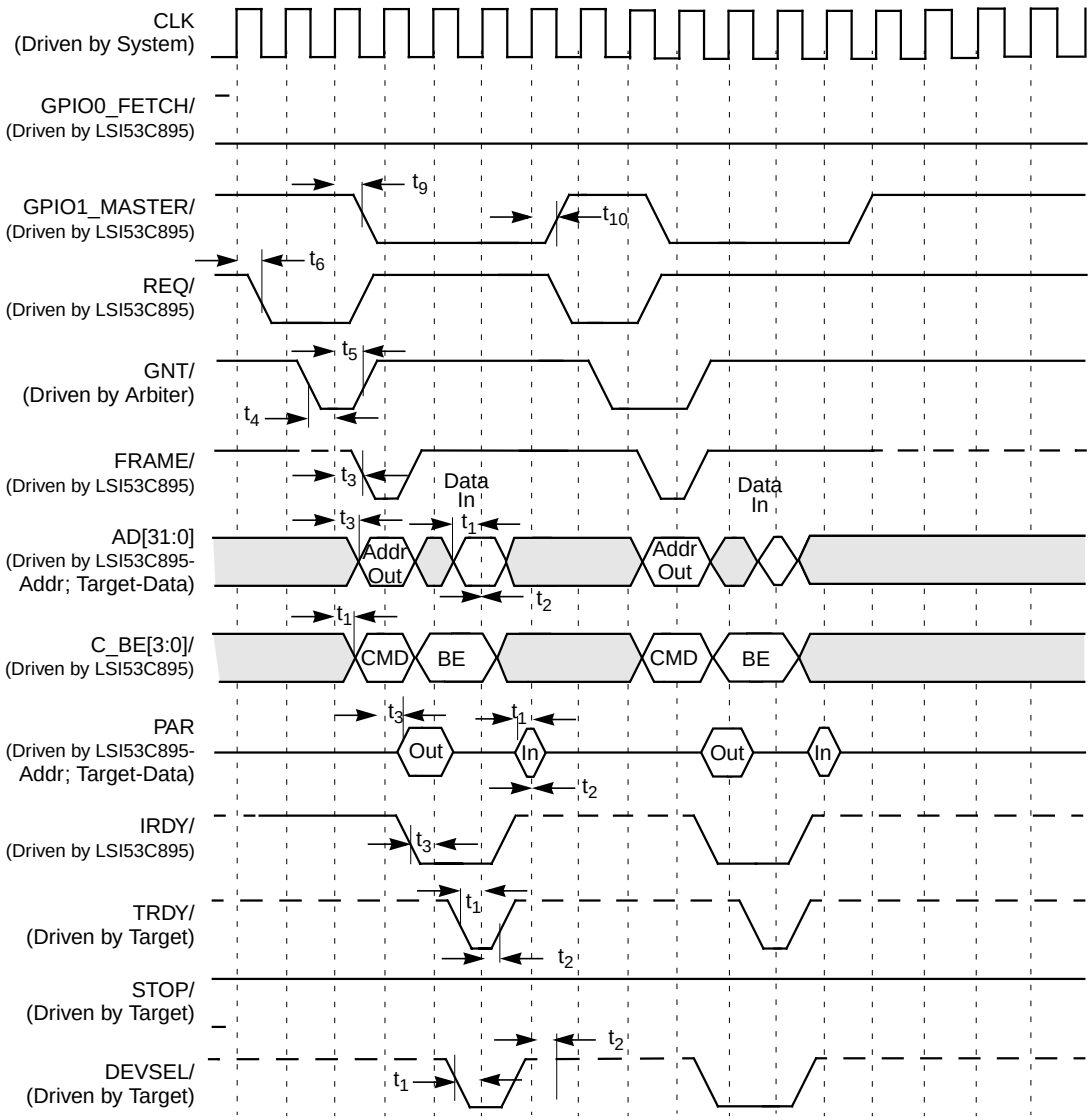


Table 7.29 Back to Back Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGH	–	20	ns

Figure 7.18 Back to Back Write

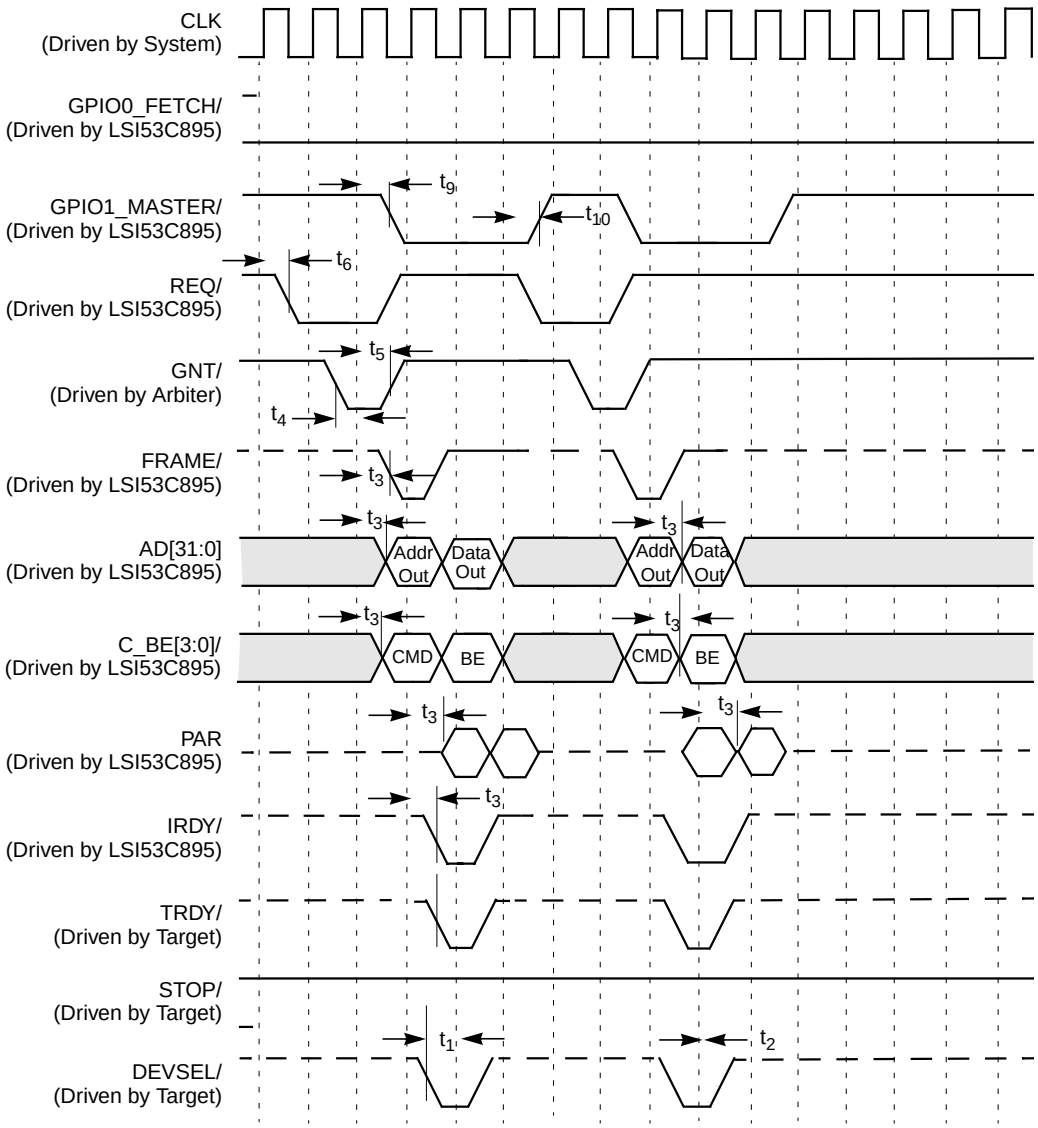


Table 7.30 Burst Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGH	–	20	ns

Figure 7.19 Burst Read

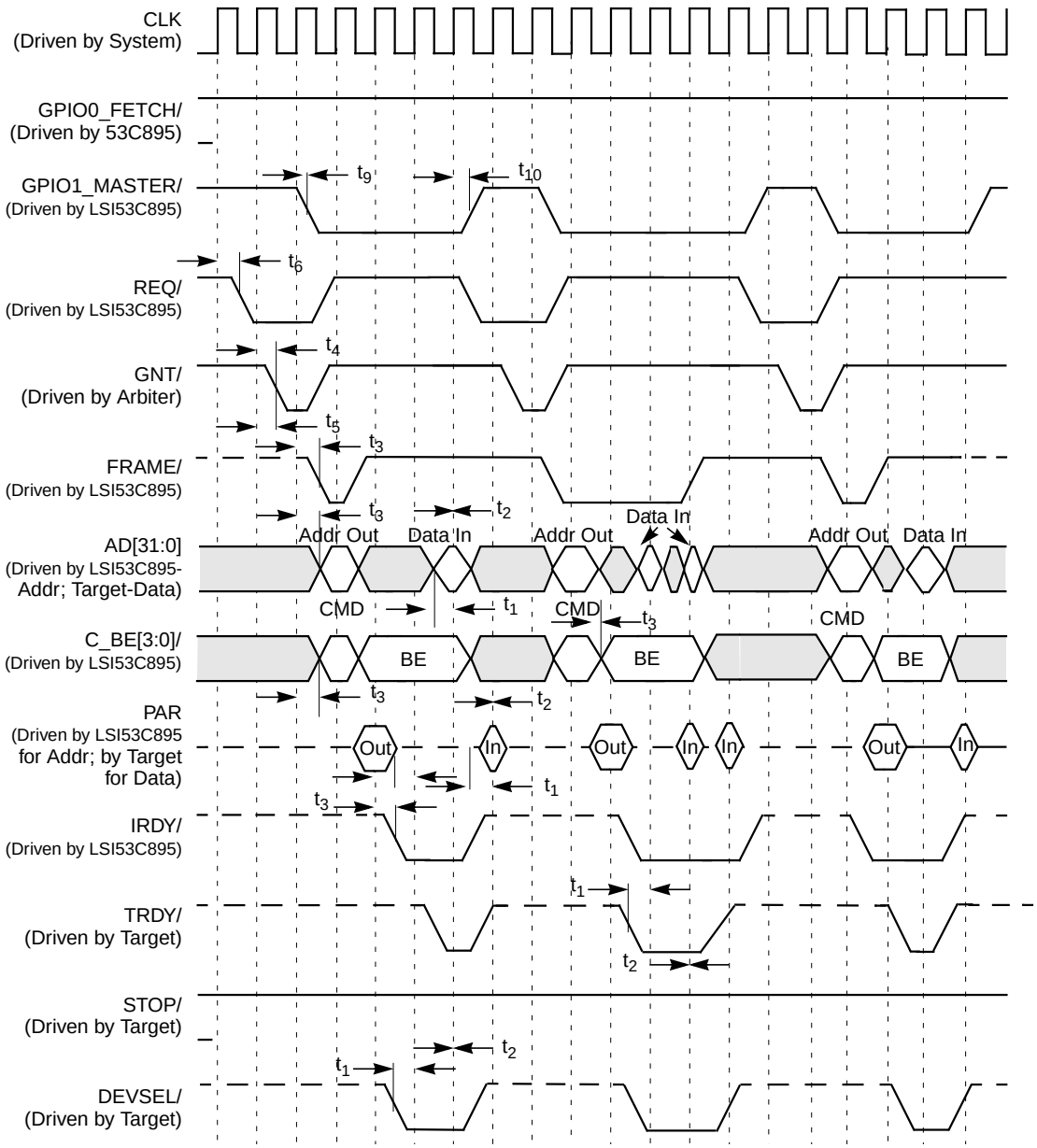
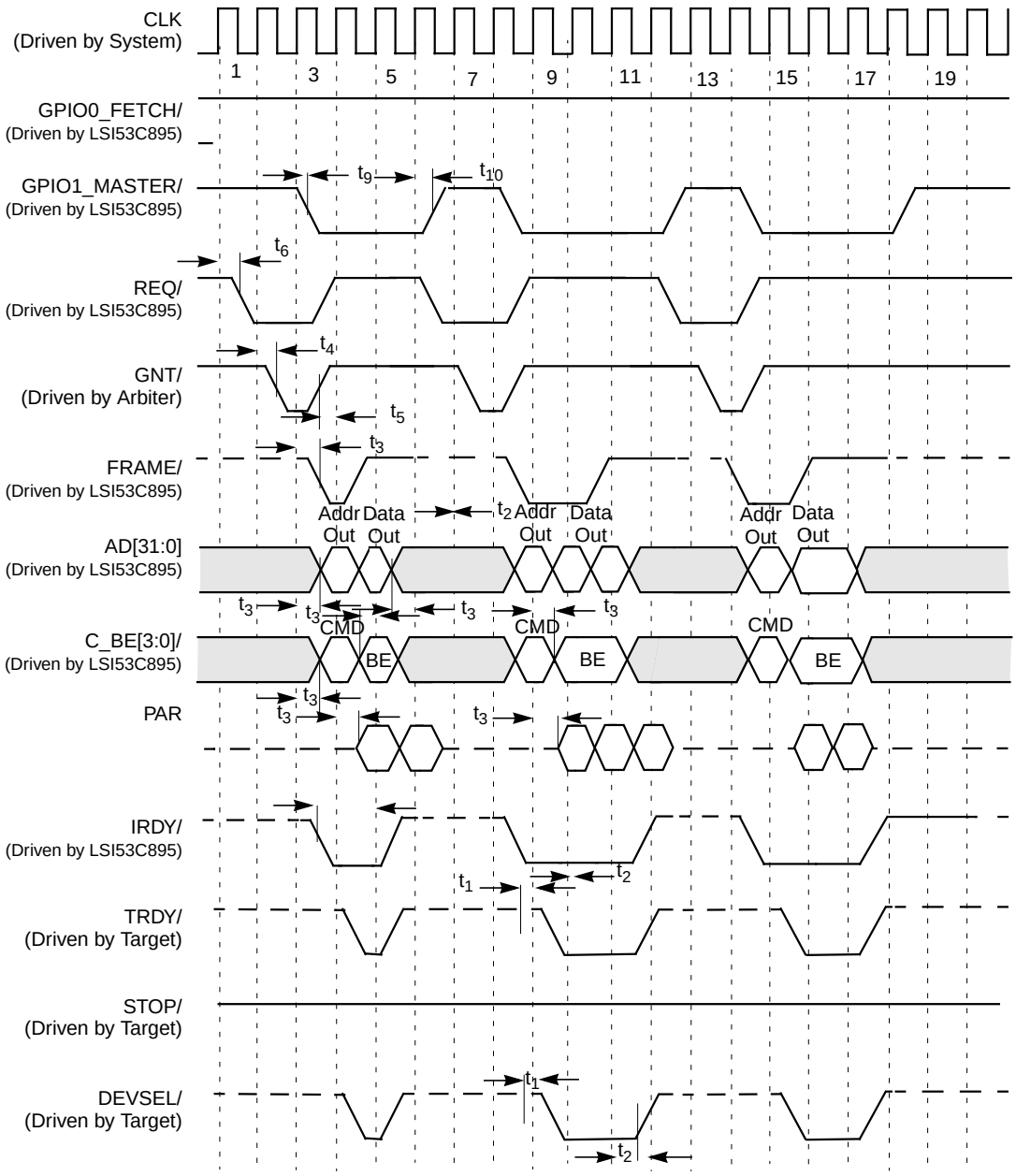


Table 7.31 Burst Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns
t_9	CLK HIGH to MASTER/ LOW	–	20	ns
t_{10}	CLK HIGH to MASTER/ HIGH	–	20	ns

Figure 7.20 Burst Write



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7.5.3 External Memory Timing

Tables 7.32 through 7.39 and figures 7.21 through 7.33 describe LSI53C895 external memory timing.

Table 7.32 External Memory Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns
t_4	Side signal input setup time	10	–	ns
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{14}	MCE/ LOW to data clocked in	160	–	ns
t_{15}	Address valid to data clocked in	205	–	ns
t_{16}	MOE/ LOW to data clocked in	100	–	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	–	ns
t_{18}	Address out from MOE/, MCE/ HIGH	50	–	ns
t_{19}	Data setup to CLK HIGH	5	–	ns

Figure 7.21 External Memory Read

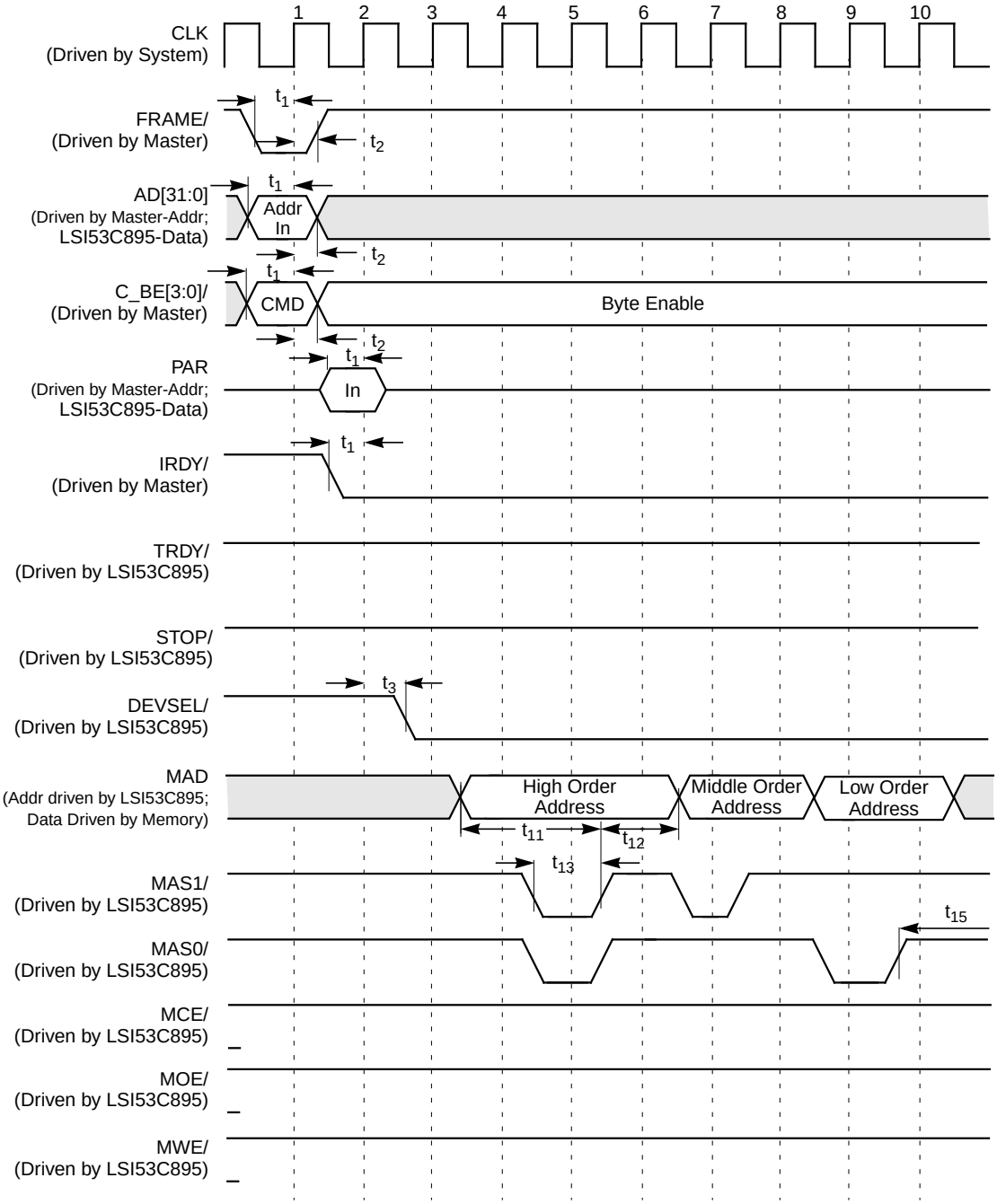

Figure 7.22 External Memory Read (Cont.)

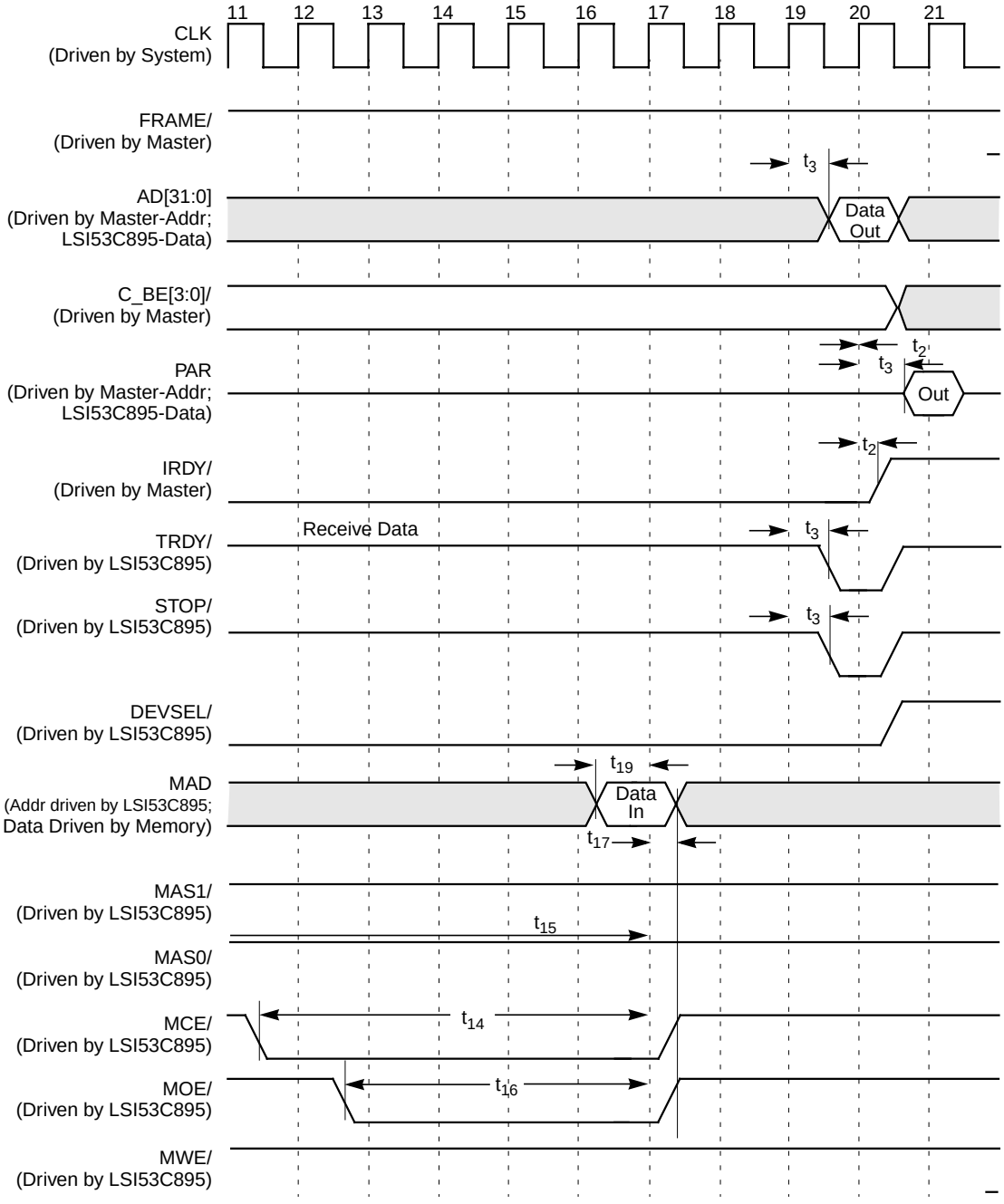

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Table 7.33 External Memory Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	–	11	ns
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{20}	Data setup to MWE/ LOW	30	–	ns
t_{21}	Data hold from MWE/ HIGH	20	–	ns
t_{22}	MWE/ pulse width	100	–	ns
t_{23}	Address setup to MWE/ LOW	75	–	ns
t_{24}	MCE/ LOW to MWE/ HIGH	120	–	ns
t_{25}	MCE/ LOW to MWE/ LOW	25	–	ns
t_{26}	MWE/ HIGH to MCE/ HIGH	25	–	ns

Figure 7.23 External Memory Write

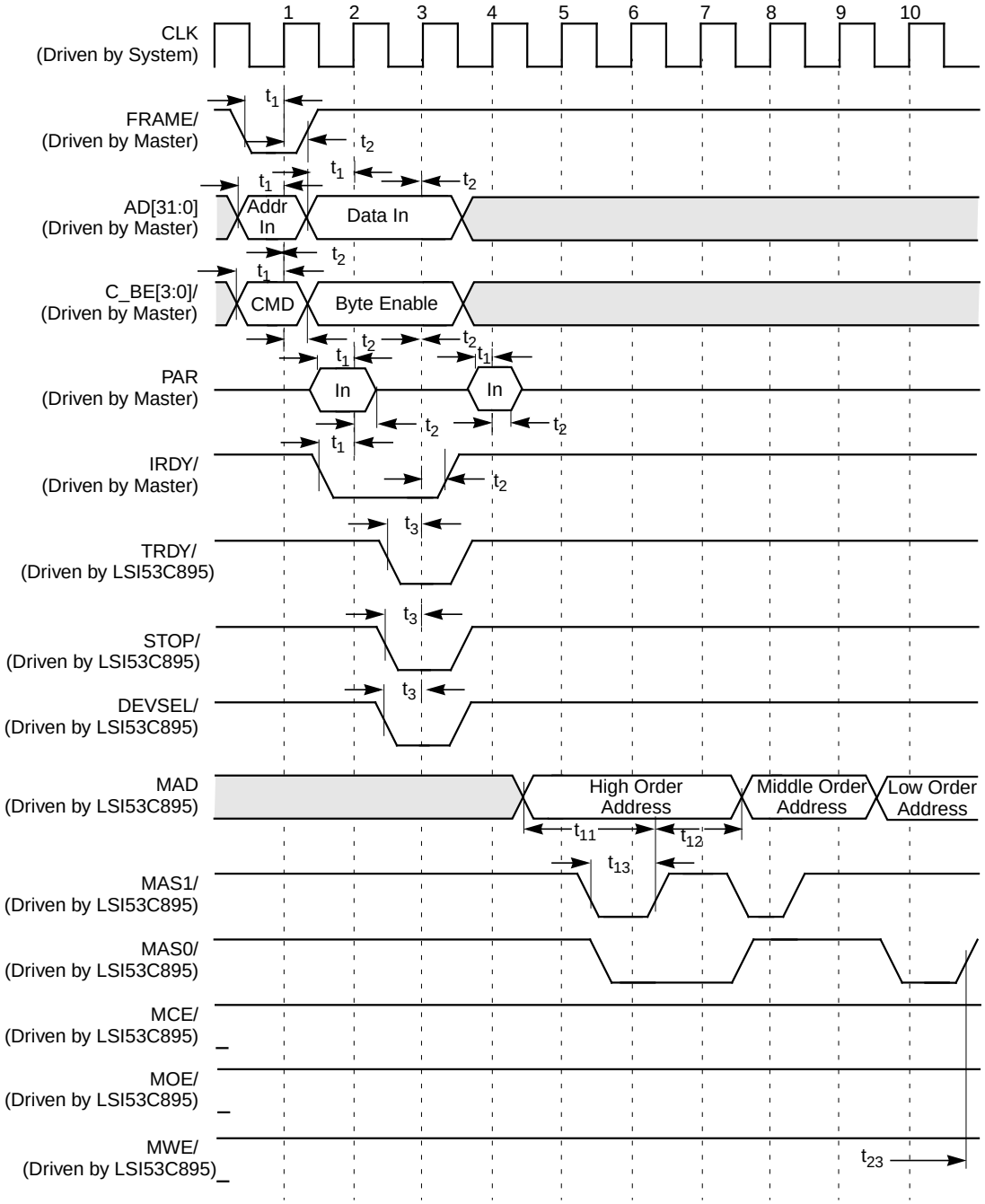


Figure 7.24 External Memory Write (Cont.)

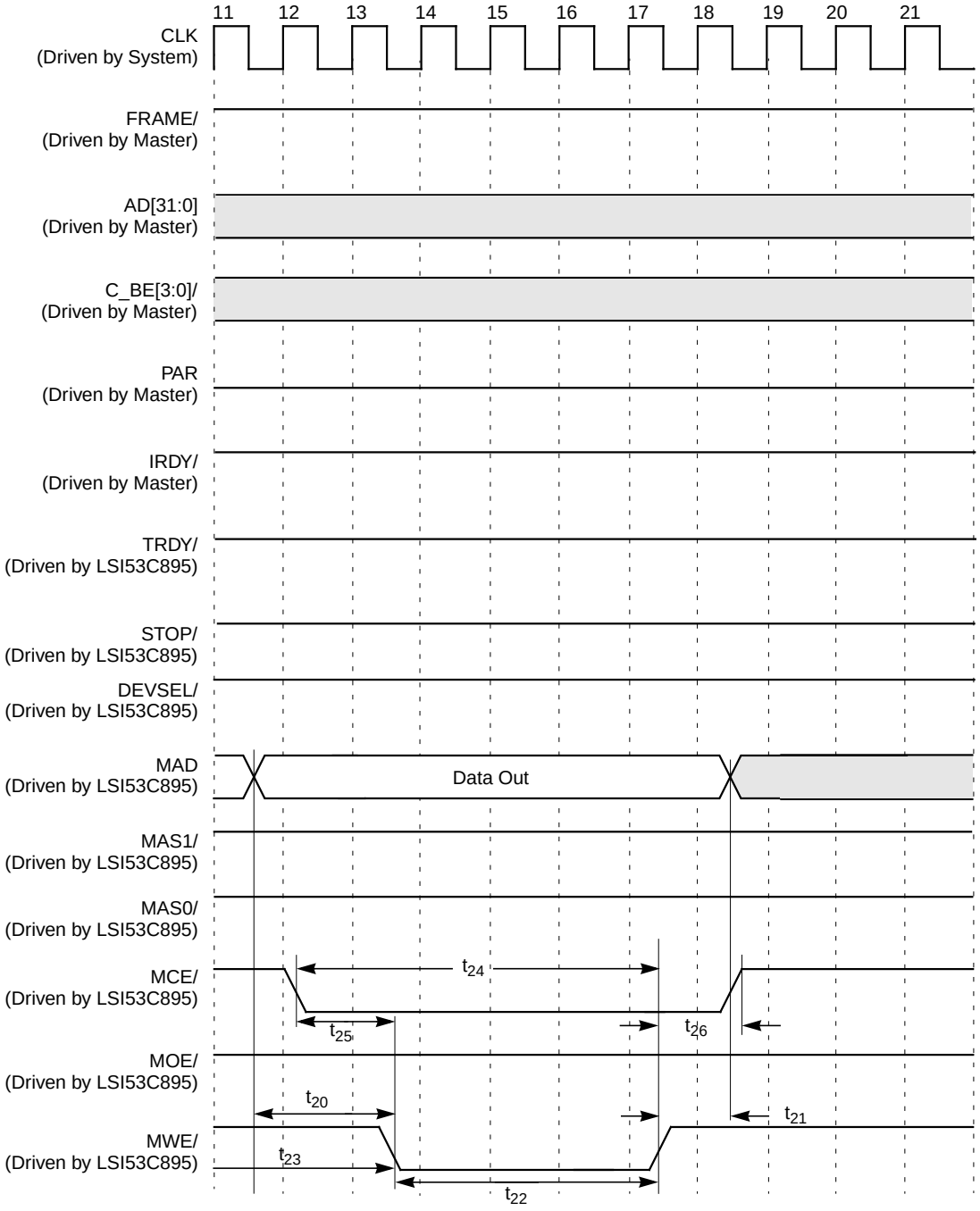


Table 7.34 Read Cycle TIming, Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGh	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{14}	MCE/ LOW to data clocked in	160	–	ns
t_{15}	Address valid to data clocked in	205	–	ns
t_{16}	MOE/ LOW to data clocked in	100	–	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	–	ns
t_{18}	Address out from MOE/, MCE/ HIGH	50	–	ns
t_{19}	Data setup to CLK HIGH	5	–	ns

Figure 7.25 Read Cycle, Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access

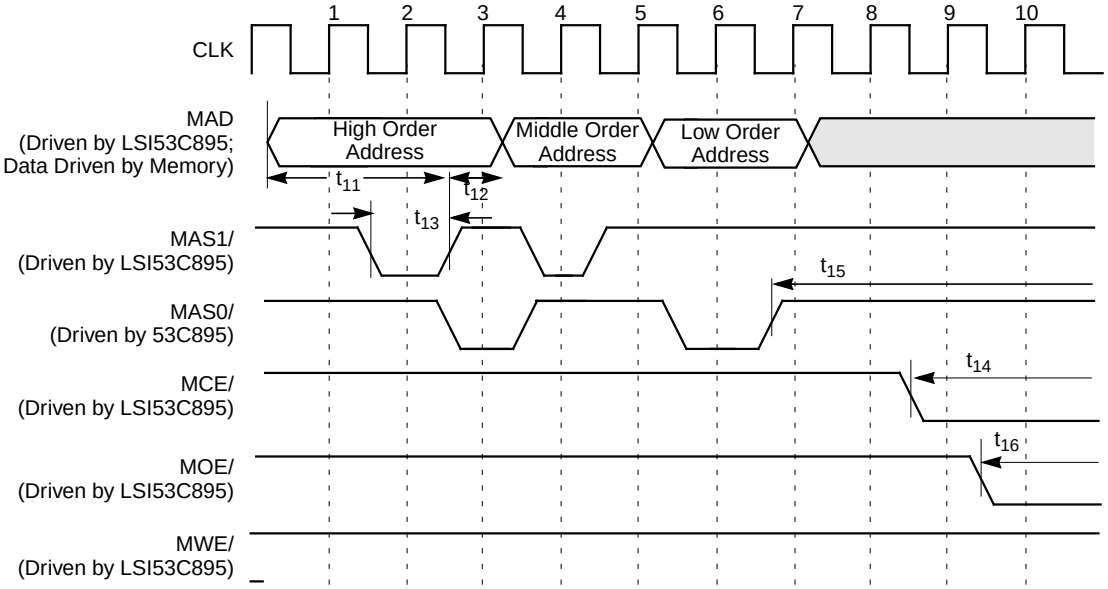


Figure 7.25 Read Cycle, Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access (Cont.)

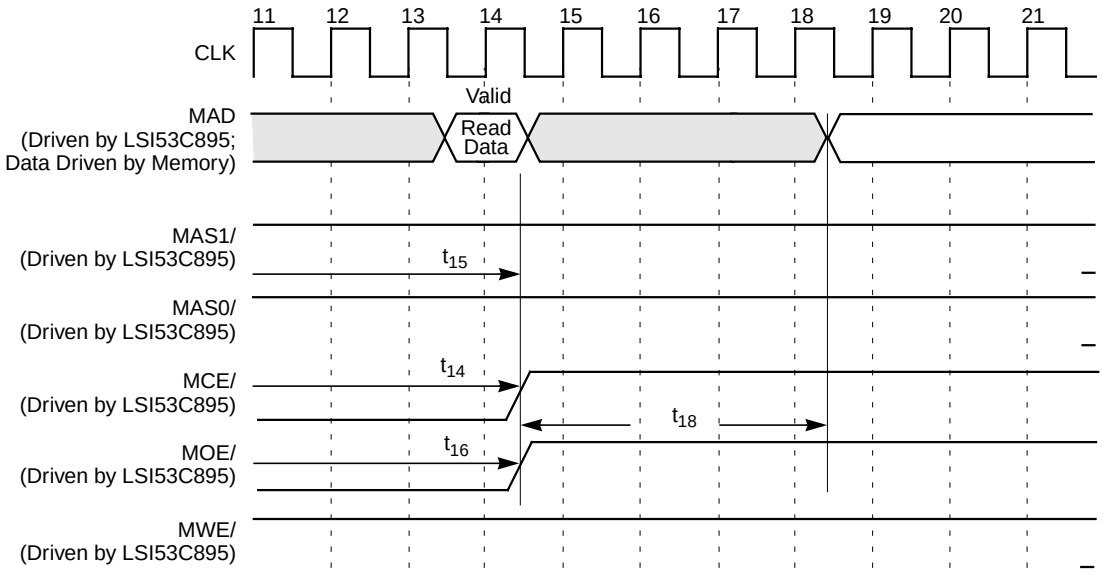


Table 7.35 Write Cycle Timing, Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{20}	Data setup to MWE/ LOW	30	–	ns
t_{21}	Data hold from MWE/ HIGH	20	–	ns
t_{22}	MWE/ pulse width	100	–	ns
t_{23}	Address setup to MWE/ LOW	75	–	ns
t_{24}	MCE/ low to MWE/ HIGH	120	–	ns
t_{25}	MCE/ low to MWE/ LOW	25	–	ns
t_{26}	MWE/ high to MCE/ HIGH	25	–	ns

Figure 7.26 Normal/Fast Memory (≥ 128 Kbytes), Single Byte Access, Write Cycle

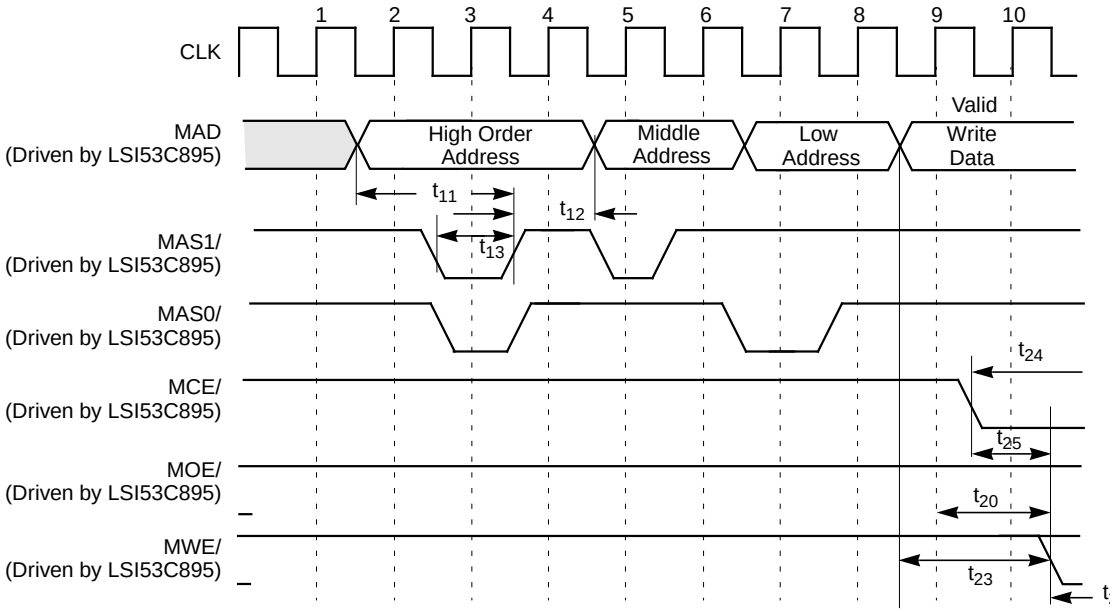


Figure 7.26 Normal/Fast Memory (≥ 128 Kbytes) Single Byte Access Write Cycle (Cont.)

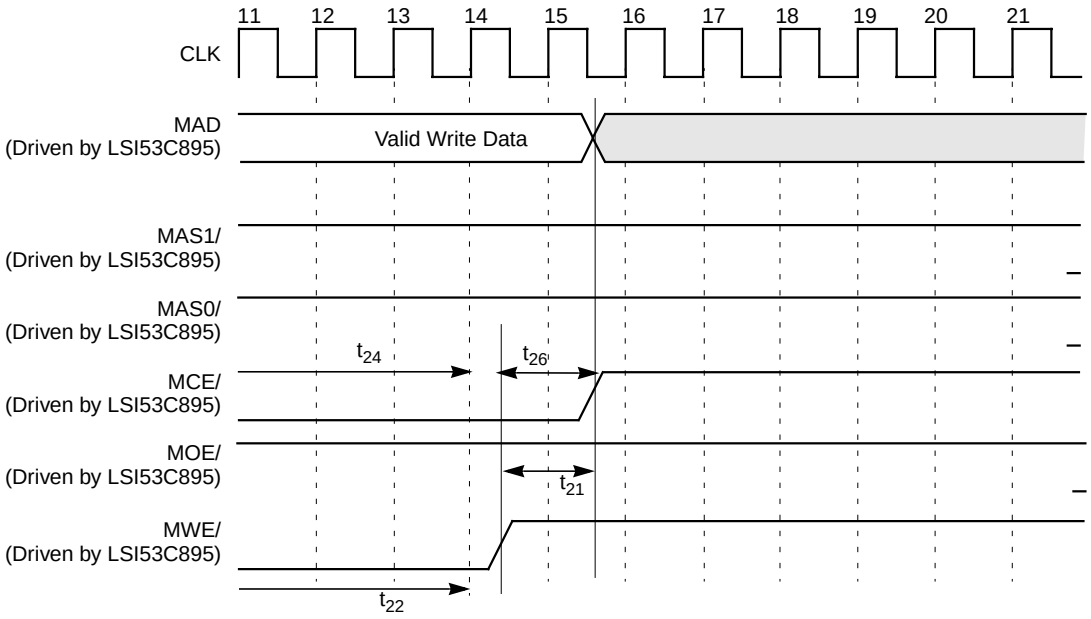


Figure 7.27 Normal/Fast Memory (≥ 128 Kbytes), Multiple Byte Access, Read Cycle

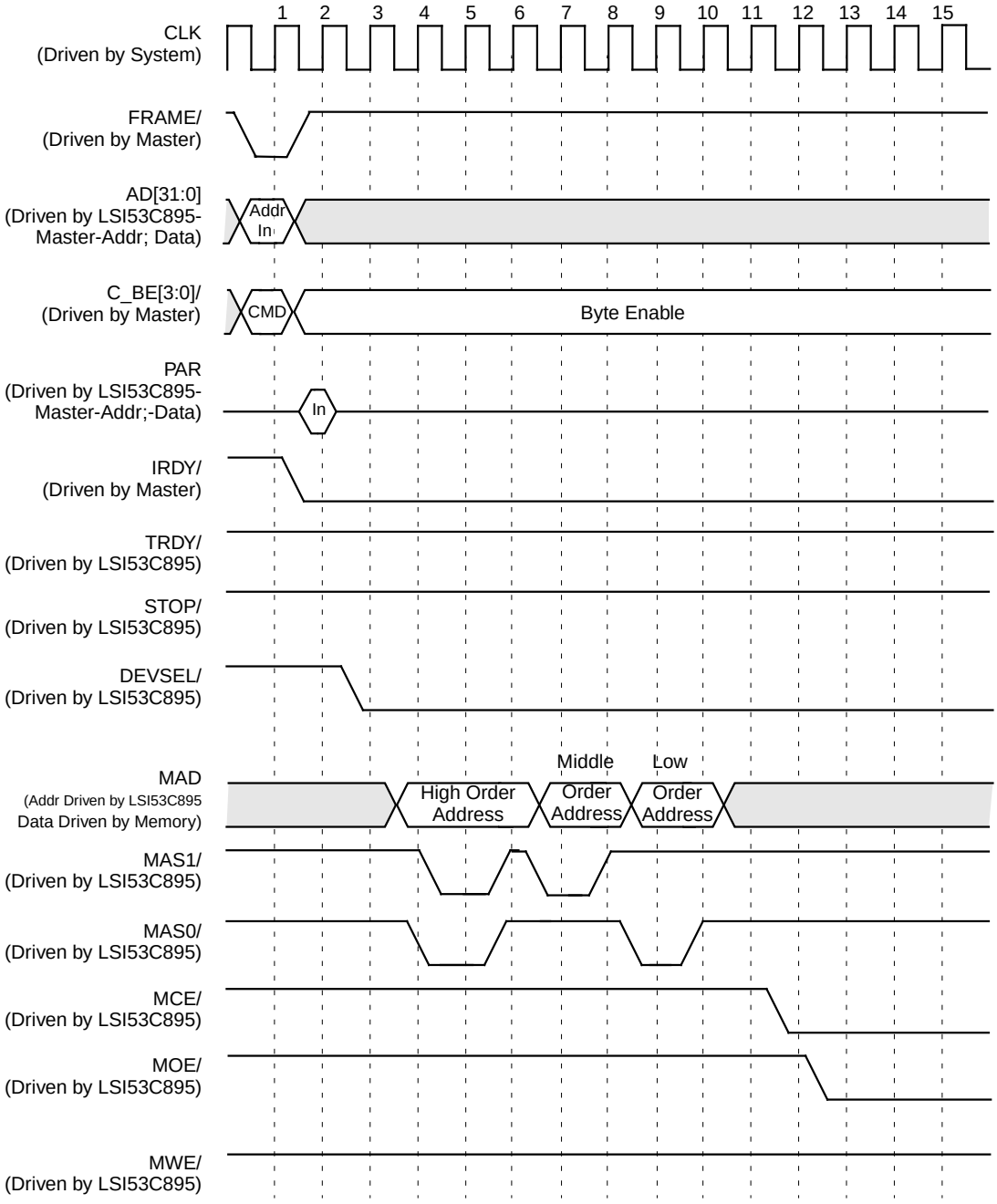


Figure 7.27 Normal/Fast Memory (≥ 128 Kbytes) Multiple Byte Access, Read Cycle (Cont.)

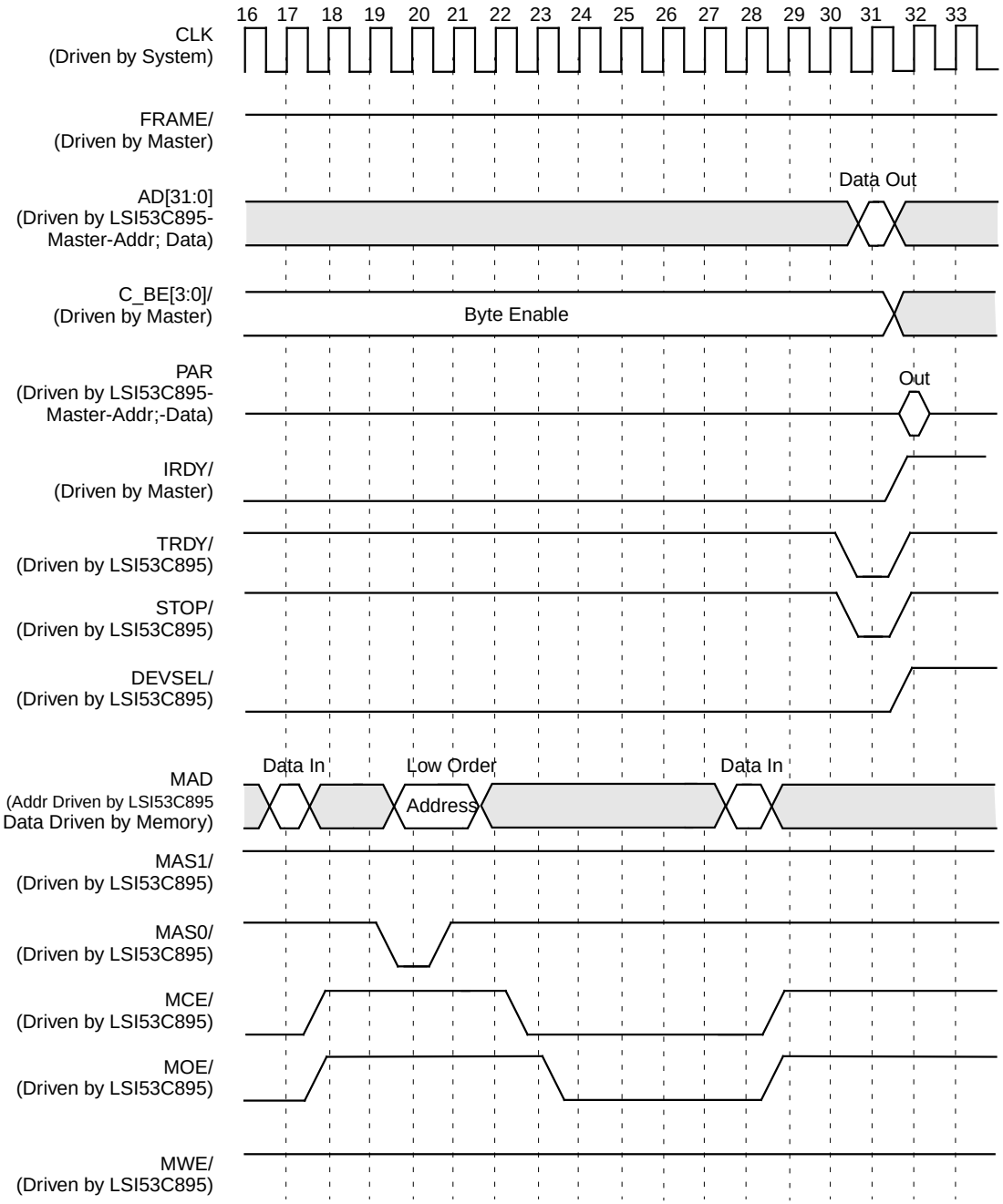


Figure 7.28 Normal/Fast Memory (≥ 128 Kbytes) Multiple Byte Access, Write Cycle

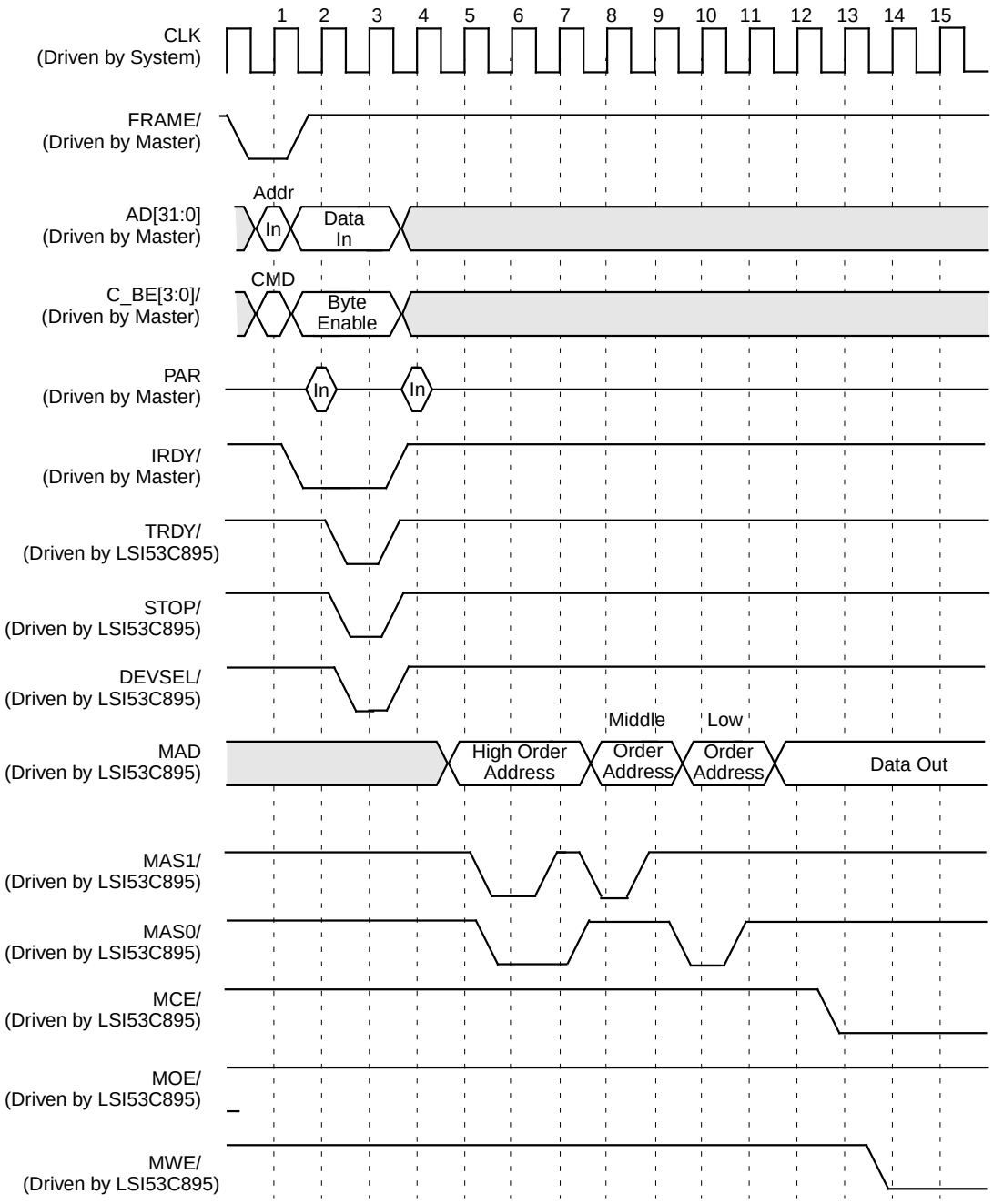


Figure 7.28 Normal/Fast Memory (≥ 128 Kbytes) Multiple Byte Access, Write Cycle (Cont.)

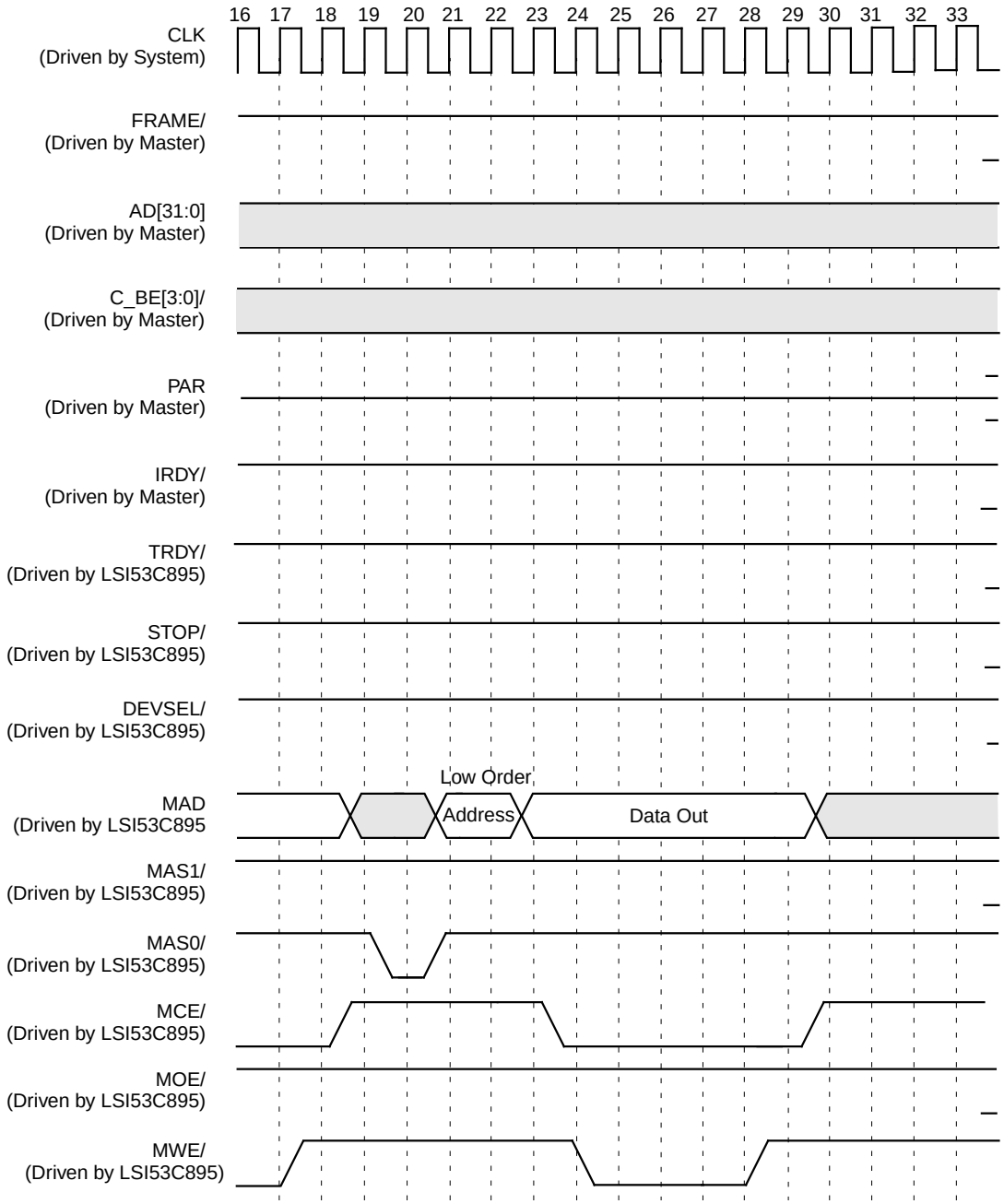


Table 7.36 Read Cycle, Slow Memory (≥ 128 Kbytes)

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{14}	MCE/ LOW to data clocked in	160	–	ns
t_{15}	Address valid to data clocked in	205	–	ns
t_{16}	MOE/ LOW to data clocked in	100	–	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	–	ns
t_{18}	Address out from MOE/, MCE/ HIGH	50	–	ns
t_{19}	Data setup to CLK HIGH	5	–	ns

Figure 7.29 Read Cycle, Slow Memory (≥ 128 Kbytes)

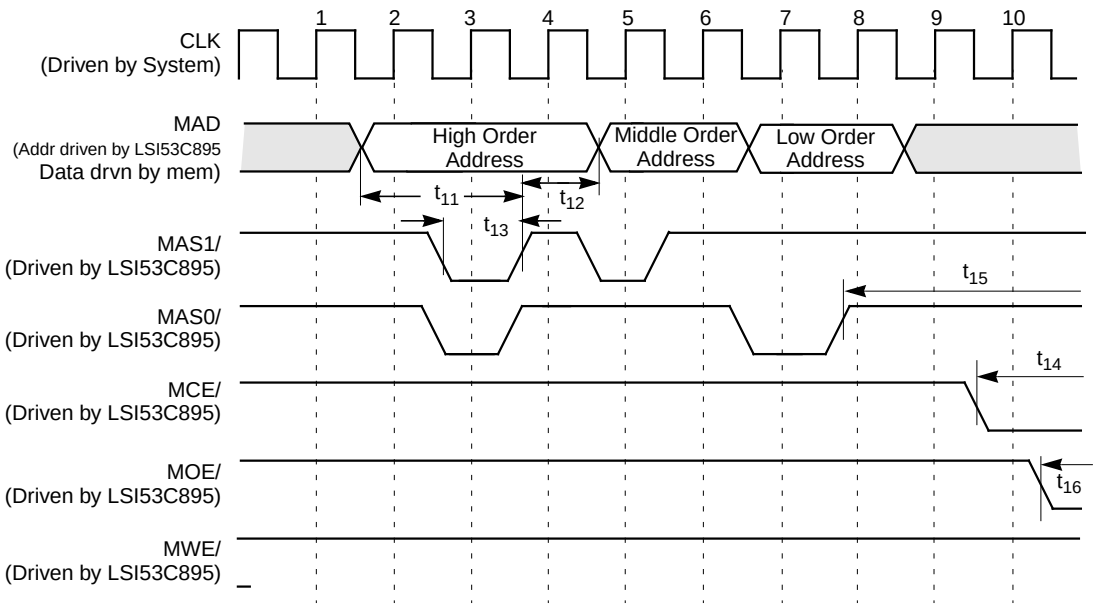


Figure 7.30 Read Cycle, Slow Memory (≥ 128 Kbytes) (Cont.)

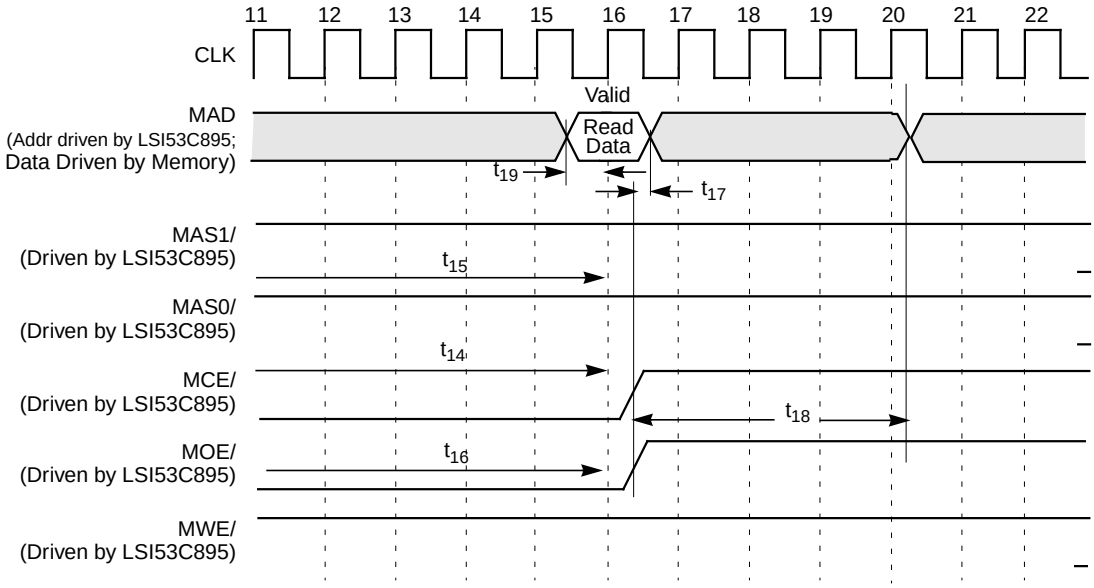


Table 7.37 Write Cycle Timing, Slow Memory (≥ 128 Kbytes)

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{20}	Data setup to MWE/ LOW	30	–	ns
t_{21}	Data hold from MWE/ HIGH	20	–	ns
t_{22}	MWE/ pulse width	100	–	ns
t_{23}	Address setup to MWE/ LOW	75	–	ns
t_{24}	MCE/ LOW to MWE/ HIGH	120	–	ns
t_{25}	MCE/ LOW to MWE/ LOW	25	–	ns
t_{26}	MWE/ HIGH to MCE/ HIGH	25	–	ns

Figure 7.31 Write Cycle, Slow Memory (≥ 128 Kbytes)

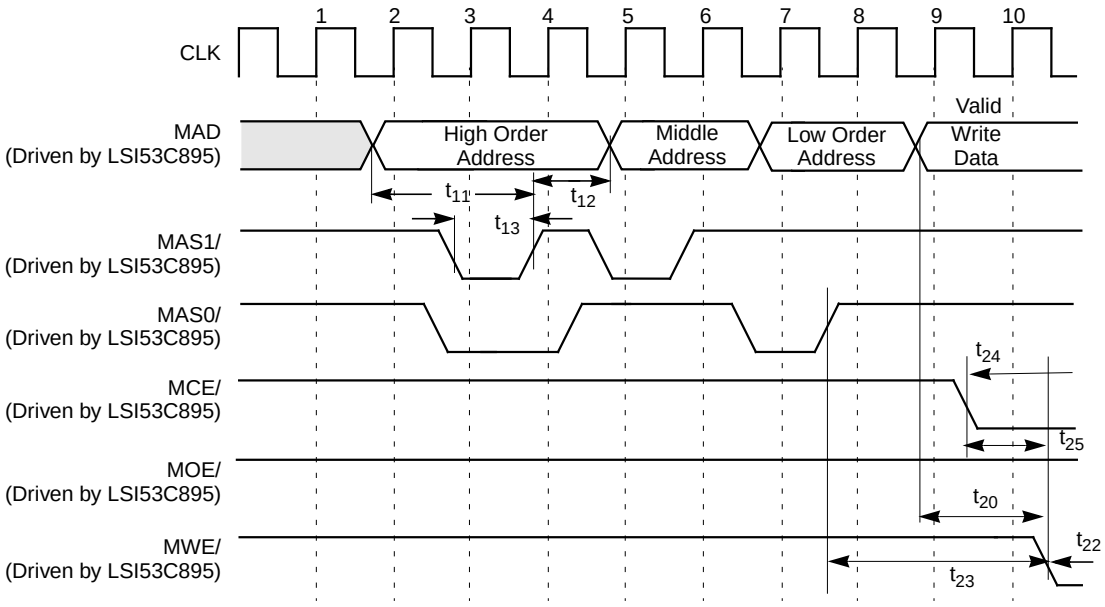


Figure 7.31 Write Cycle, Slow Memory (≥ 128 Kbytes) (Cont.)

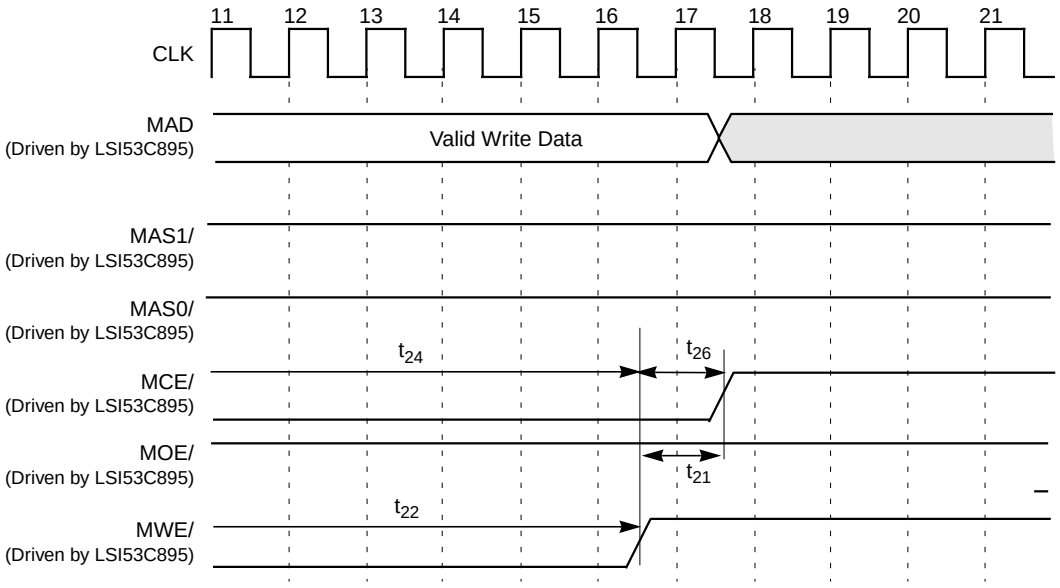


Table 7.38 Read Cycle Timing, ≤ 64 Kbytes ROM

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{14}	MCE/ LOW to data clocked in	160	–	ns
t_{15}	Address valid to data clocked in	205	–	ns
t_{16}	MOE/ LOW to data clocked in	100	–	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	–	ns
t_{18}	Address out from MOE/, MCE/ HIGH	50	–	ns
t_{19}	Data setup to CLK HIGH	5	–	ns

Figure 7.32 Read cycle, ≤ 64 Kbytes ROM

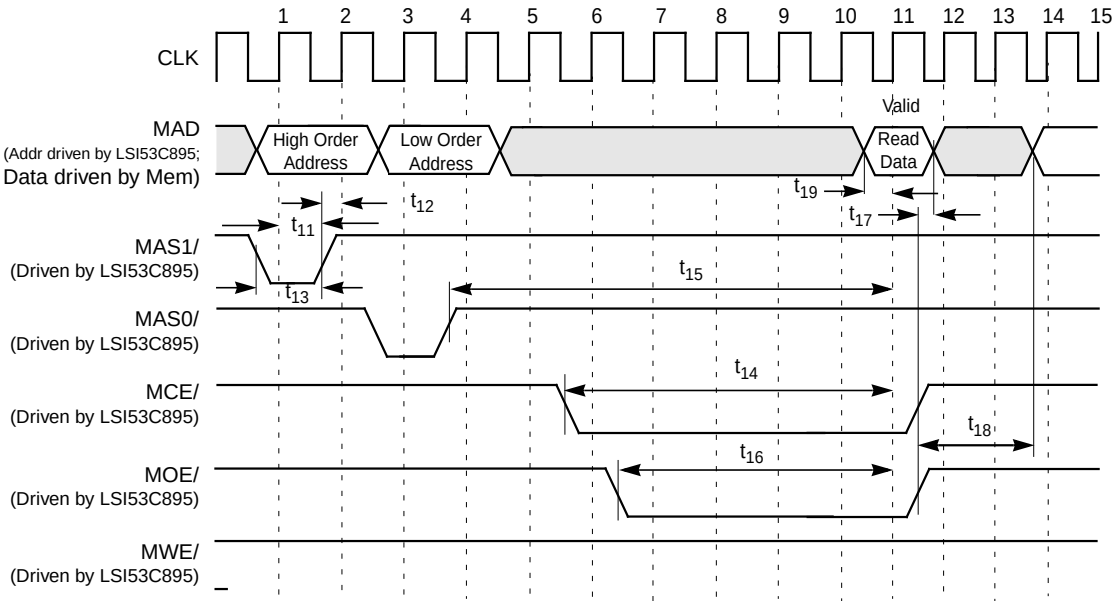
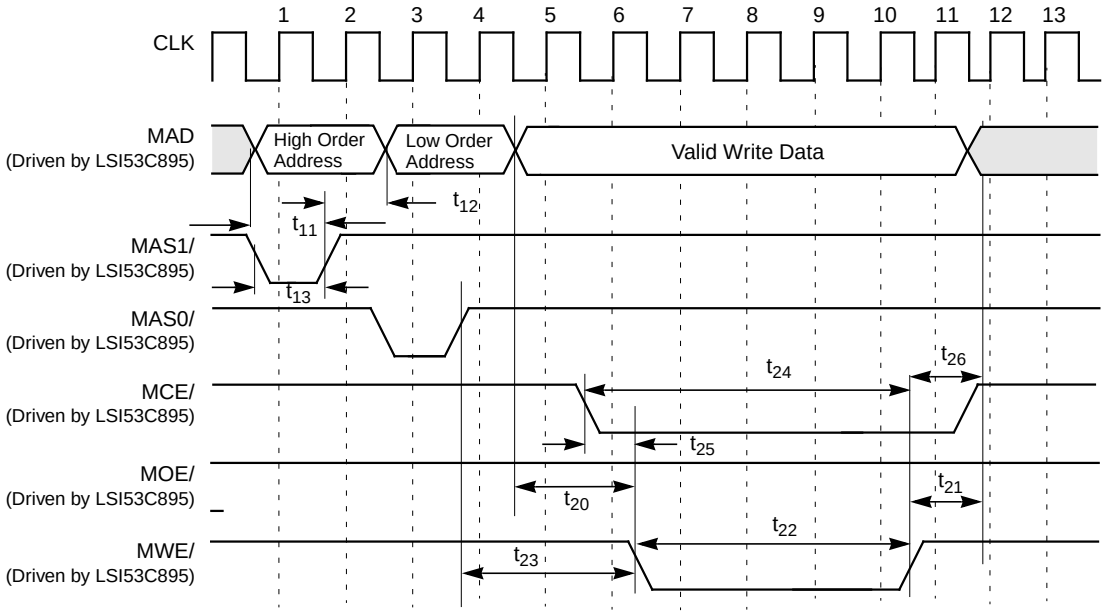


Table 7.39 Write Cycle Timing, ≤ 64 Kbytes ROM

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ HIGH	25	–	ns
t_{12}	Address hold from MAS/ HIGH	15	–	ns
t_{13}	MAS/ pulse width	25	–	ns
t_{20}	Data setup to MWE/ LOW	30	–	ns
t_{21}	Data hold from MWE/ HIGH	20	–	ns
t_{22}	MWE/ pulse width	100	–	ns
t_{23}	Address setup to MWE/ LOW	75	–	ns
t_{24}	MCE/ LOW to MWE/ HIGH	120	–	ns
t_{25}	MCE/ LOW to MWE/ LOW	25	–	ns
t_{26}	MWE/ HIGH to MCE/ HIGH	25	–	ns

Figure 7.33 Write Cycle, ≤ 64 Kbytes ROM



7.6 SCSI Timing

Tables 7.40 through 7.50 and figures 7.34 through 7.38 describe LSI53C895 SCSI timing.

Table 7.40 Initiator Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	–	ns
t_3	Data setup to SACK/ asserted	55	–	ns
t_4	Data hold from SREQ/ deasserted	20	–	ns

Figure 7.34 Initiator Asynchronous Send

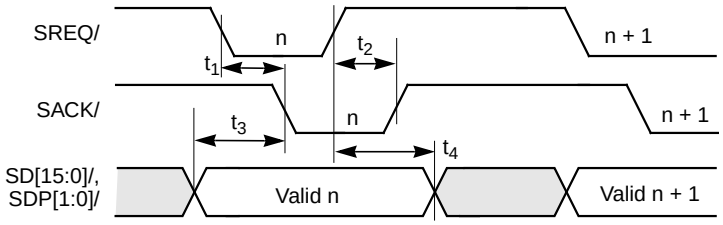


Table 7.41 Initiator Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	–	ns
t_3	Data setup to SREQ/ asserted	0	–	ns
t_4	Data hold from SACK/ asserted	0	–	ns

Figure 7.35 Initiator Asynchronous Receive

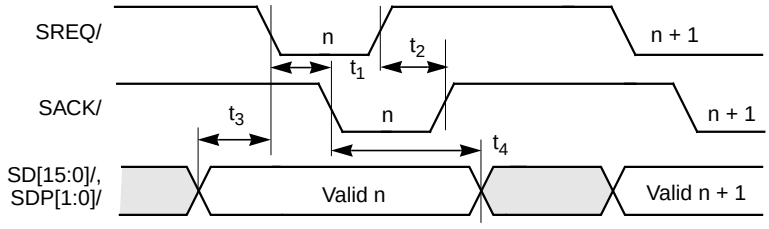


Table 7.42 Target Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	–	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	–	ns
t_3	Data setup to SREQ/ asserted	55	–	ns
t_4	Data hold from SACK/ asserted	20	–	ns

Figure 7.36 Target Asynchronous Send

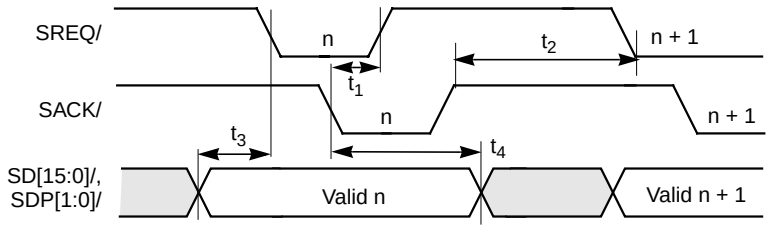


Table 7.43 Target Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	–	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	–	ns
t_3	Data setup to SACK/ asserted	0	–	ns
t_4	Data hold from SREQ/ deasserted	0	–	ns

Figure 7.37 Target Asynchronous Receive

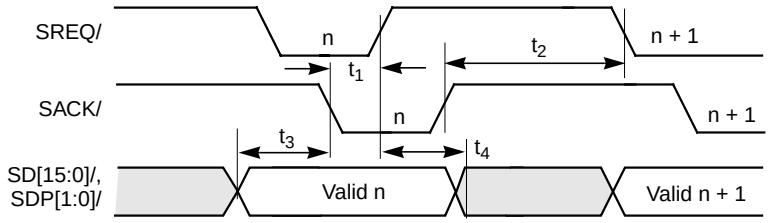


Figure 7.38 Initiator and Target Synchronous Transfers

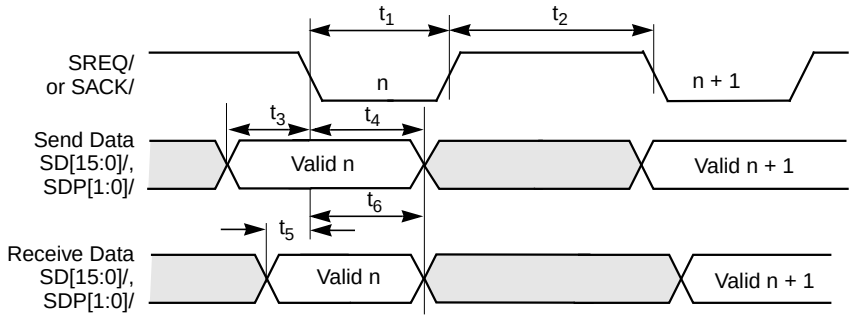


Table 7.44 SCSI-1 Transfers (SE, 5.0 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	55	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	100	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	–	ns

Table 7.45 SCSI-1 Transfers (Differential, 4.17 Mbytes/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	96	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	96	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	84	–	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	84	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	65	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	110	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	–	ns

Table 7.46 SCSI-2 Fast Transfers 10.0 Mbytes/s (8-Bit Transfers) or 20.0 Mbytes/s (16-Bit Transfers), 40 MHz Clock

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	35	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	45	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	–	ns

Table 7.47 SCSI-2 Fast Transfers 10.0 Mbytes/s (8-Bit Transfers) or 20.0 Mbytes/s (16-Bit Transfers), 50 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	35	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	40[3]	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	–	ns

1. Transfer period bits (bits [6:4] in the SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCSI Control One (SCNTL1)) is set.
2. For fast SCSI, set the TolerANT Enable bit (bit 7 in SCSI Test Three (STEST3)).
3. Analysis of system configuration is recommended due to reduced driver skew margin in differential systems

Table 7.48 Ultra SCSI SE Transfers 20.0 Mbytes/s (8-Bit Transfers) or 40.0 Mbytes/s (16-Bit Transfers), Quadrupled 40 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	7	–	ns

1. Transfer period bits (bits [6:4] in the SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCSI Control One (SCNTL1)) is set.
2. For fast SCSI, set the TolerANT Enable bit (bit 7 in SCSI Test Three (STEST3)). During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (SCSI Test Two (STEST2), bit 1) has no effect

Table 7.49 Ultra SCSI HVD Transfers 20.0 Mbytes/s (8-Bit Transfers) or 40.0 Mbytes/s (16-Bit Transfers), 80 MHz Clock[1]

Symbol	Parameter[1]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	16	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	21	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

1. During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (SCSI Test Two (STEST2), bit 1) has no effect.

Table 7.50 Ultra2 SCSI Transfers 40.0 Mbytes/s (8-Bit Transfers) or 80.0 Mbytes/s (16-Bit Transfers), Quadrupled 40 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	8	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	8	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	6	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	6	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	10	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	10	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	4.5	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	4.5	–	ns

1. Transfer period bits (bits [6:4] in the SCSI Transfer (SXFER) register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCSI Control One (SCNTL1)) is set.
2. During Ultra2 SCSI transfers, the value of the Extend REQ/ACK Filtering bit (SCSI Test Two (STEST2), bit 1) has no effect.

7.7 Package Diagrams

The signal locations on the 272 BGA are illustrated in Figure 7.39. The signal names are listed alphabetically in Table 7.51, and numerically in Table 7.52. Figure 7.40 is the 208-pin QFP diagram. The signals names for the QFP are listed by pin number in Table 7.53, and numerically in Table 7.54. Figure 7.41 is the package drawing for the 208-pin QFP. Figure 7.42 is the package drawing for the 272 BGA.

Figure 7.39 LSI53C895 Pin Diagram, 272-Ball BGA (Top View)

A1 VSS	A2 N/C	A3 SD2+	A4 SD3+	A5 SD4+	A6 N/C	A7 SD5-	A8 SD6-	A9 SD7-	A10 RBIAS	A11 VDD_ BIAS	A12 SATN+	A13 SBSY+	A14 SACK+	A15 SRST+	A16 SMSG+	A17 SSEL+	A18 SSEL-	A19 N/C	A20 N/C
B1 N/C	B2 SD1+	B3 SD1-	B4 SD2-	B5 SD3-	B6 SD4-	B7 SD5+	B8 SD6+	B9 SD7+	B10 SDP0-	B11 N/C	B12 SATN-	B13 SBSY-	B14 SACK-	B15 SRST-	B16 SMSG-	B17 N/C	B18 N/C	B19 N/C	B20 N/C
C1 SD0-	C2 N/C	C3 N/C	C4 N/C	C5 N/C	C6 N/C	C7 N/C	C8 N/C	C9 N/C	C10 SDP0+	C11 N/C	C12 N/C	C13 N/C	C14 N/C	C15 N/C	C16 N/C	C17 SCD-	C18 N/C	C19 SREQ+	C20 SIO-
D1 SD0+	D2 N/C	D3 N/C	D4 VSS	D5 N/C	D6 VDD	D7 N/C	D8 VSS	D9 N/C	D10 N/C	D11 VDD	D12 N/C	D13 VSS	D14 N/C	D15 VDD	D16 SCD+	D17 VSS	D18 SREQ-	D19 SD8+	D20 SD8-
E1 SDP1-	E2 N/C	E3 N/C	E4 N/C													E17 SIO+	E18 N/C	E19 SD9+	E20 SD9-
F1 SD15+	F2 SD15-	F3 SDP1+	F4 VDD													F17 VDD	F18 N/C	F19 SD10+	F20 SD10-
G1 SD14+	G2 SD14-	G3 N/C	G4 N/C													G17 N/C	G18 N/C	G19 SD11+	G20 SD11-
H1 SD13+	H2 SD13-	H3 N/C	H4 VSS													H17 VSS	H18 N/C	H19 VDDA	H20 DIFFSENS
J1 LVDSMODE (TEST)	J2 SD12+	J3 SD12-	J4 N/C					J9 VSS	J10 VSS	J11 VSS	J12 VSS					J17 N/C	J18 VSSA	J19 TEST_ HSC/	J20 SCLK
K1 TEST	K2 TESTIN	K3 N/C	K4 VDD					K9 VSS	K10 VSS	K11 VSS	K12 VSS					K17 N/C	K18 N/C	K19 MAC/_ TESTOUT	K20 MAD0
L1 TEST	L2 TEST	L3 TEST	L4 N/C					L9 VSS	L10 VSS	L11 VSS	L12 VSS					L17 VDD	L18 N/C	L19 MAD2	L20 MAD1
M1 MAS1/	M2 MAS0/	M3 VSS_ CORE	M4 N/C					M9 VSS	M10 VSS	M11 VSS	M12 VSS					M17 N/C	M18 MAD5	M19 MAD4	M20 MAD3
N1 VSS_ CORE2	N2 MWE/	N3 MOE/	N4 VSS													N17 VSS	N18 VSS_ CORE	N19 MAD7	N20 MAD6
P1 VDD_ CORE	P2 VDD_ CORE	P3 BIG_LIT/	P4 N/C													P17 VDD_ CORE	P18 GPIO3	P19 GPIO4	P20 VSS_ CORE
R1 MCE/	R2 RST/	R3 N/C	R4 VDD													R17 VDD	R18 GPIO_ MASTER/	R19 VDD_ CORE	R20 GPIO2
T1 CLK	T2 GNT/	T3 N/C	T4 N/C													T17 N/C	T18 N/C	T19 GPIO0_ FETCH/	T20 V5BIAS (MEM)
U1 REQ/	U2 AD31	U3 N/C	U4 VSS	U5 N/C	U6 VDD	U7 N/C	U8 VSS	U9 C_BE2/	U10 VDD	U11 SERR/	U12 N/C	U13 VSS	U14 N/C	U15 VDD	U16 N/C	U17 VSS	U18 AD1	U19 N/C	U20 IRQ/
V1 AD30	V2 AD29	V3 AD27	V4 N/C	V5 AD25	V6 IDSEL	V7 AD21	V8 AD18	V9 FRAME/	V10 N/C	V11 PERR/	V12 AD15	V13 AD12	V14 N/C	V15 N/C	V16 N/C	V17 AD4	V18 AD2	V19 N/C	V20 AD0
W1 AD28	W2 N/C	W3 N/C	W4 N/C	W5 AD24	W6 AD23	W7 AD20	W8 AD17	W9 IRDY/	W10 TRDY/	W11 STOP/	W12 C_BE1/	W13 AD13	W14 AD10	W15 AD8	W16 N/C	W17 AD6	W18 V5BIAS (PCI)	W19 N/C	W20 N/C
Y1 N/C	Y2 N/C	Y3 AD26	Y4 V5BIAS (PCI)	Y5 C_BE3/	Y6 AD22	Y7 AD19	Y8 AD16	Y9 N/C	Y10 DEVSEL/	Y11 N/C	Y12 PAR	Y13 AD14	Y14 AD11	Y15 AD9	Y16 C_BE0/	Y17 AD7	Y18 AD5	Y19 AD3	Y20 N/C

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Table 7.51 BGA Position and Signal Name Alphabetically

BGA #	Signal	BGA #	Signal	BGA #	Signal	BGA #	Signal	BGA #	Signal
V20	AD0	M2	MAS0/	T17	N/C	A3	SD2+	D17	VSS
U18	AD1	M1	MAS1/	T18	N/C	A4	SD3+	D4	VSS
V18	AD2	R1	MCE/	T3	N/C	A5	SD4+	D8	VSS
Y19	AD3	N3	MOE/	T4	N/C	B7	SD5+	H10	VSS
V17	AD4	N2	MWE/	U12	N/C	B8	SD6+	H11	VSS
Y18	AD5	A19	N/C	U14	N/C	B9	SD7+	H12	VSS
W17	AD6	A2	N/C	U16	N/C	D19	SD8+	H13	VSS
Y17	AD7	A20	N/C	U19	N/C	E19	SD9+	H17	VSS
W15	AD8	A6	N/C	U3	N/C	F19	SD10+	H4	VSS
Y15	AD9	B1	N/C	U5	N/C	G19	SD11+	H8	VSS
W14	AD10	B11	N/C	U7	N/C	J2	SD12+	H9	VSS
Y14	AD11	B17	N/C	V10	N/C	H1	SD13+	J10	VSS
V13	AD12	B18	N/C	V14	N/C	G1	SD14+	J11	VSS
W13	AD13	B19	N/C	V15	N/C	F1	SD15+	J12	VSS
Y13	AD14	B20	N/C	V16	N/C	B10	SDP0–	J13	VSS
V12	AD15	C11	N/C	V19	N/C	E1	SDP1–	J8	VSS
Y8	AD16	C12	N/C	V4	N/C	C10	SDP0+	J9	VSS
W8	AD17	C13	N/C	W16	N/C	F3	SDP1+	K10	VSS
V8	AD18	C14	N/C	W19	N/C	U11	SERR/	K11	VSS
Y7	AD19	C15	N/C	W2	N/C	C20	SIO–	K12	VSS
W7	AD20	C16	N/C	W20	N/C	E17	SIO+	K13	VSS
V7	AD21	C18	N/C	W3	N/C	B16	SMSG–	K8	VSS
Y6	AD22	C2	N/C	W4	N/C	A16	SMSG+	K9	VSS
W6	AD23	C3	N/C	Y1	N/C	D18	SREQ–	L10	VSS
W5	AD24	C4	N/C	Y11	N/C	C19	SREQ+	L11	VSS
V5	AD25	C5	N/C	Y2	N/C	B15	SRST–	L12	VSS
Y3	AD26	C6	N/C	Y20	N/C	A15	SRST+	L13	VSS
V3	AD27	C7	N/C	Y9	N/C	A18	SSEL–	L8	VSS
W1	AD28	C8	N/C	Y12	PAR	A17	SSEL+	L9	VSS
V2	AD29	C9	N/C	V11	PERR/	W11	STOP/	M10	VSS
V1	AD30	D10	N/C	A10	RBIAS	K1	TEST	M11	VSS
U2	AD31	D12	N/C	U1	REQ/	L1	TEST	M12	VSS
P3	BIG_LIT/	D14	N/C	R2	RST/	L2	TEST	M13	VSS
Y16	C_BE0/	D2	N/C	B14	SACK-	L3	TEST	M8	VSS
W12	C_BE1/	D3	N/C	A14	SACK+	J19	TEST_HSC/	M9	VSS
U9	C_BE2/	D5	N/C	B12	SATN–	K2	TESTIN	N10	VSS
Y5	C_BE3/	D7	N/C	A12	SATN+	W10	TRDY/	N11	VSS
T1	CLK	D9	N/C	B13	SBSY–	T20	V5BIAS(MEM)	N12	VSS
Y10	DEVSEL/	E18	N/C	A13	SBSY+	W18	V5BIAS(PCI)	N13	VSS
H20	DIFFSENS	E2	N/C	C17	SCD–	Y4	V5BIAS(PCI)	N17	VSS
V9	FRAME/	E3	N/C	D16	SCD+	D11	VDD	N4	VSS
T2	GNT/	E4	N/C	J20	SCLK	D15	VDD	N8	VSS
T19	GPIO0_FETCH/	F18	N/C	C1	SD0–	D6	VDD	N9	VSS
R18	GPIO1_MASTER/	G17	N/C	B3	SD1–	F17	VDD	U13	VSS
R20	GPIO2	G18	N/C	B4	SD2–	F4	VDD	U17	VSS
P18	GPIO3	G3	N/C	B5	SD3–	K4	VDD	U4	VSS
P19	GPIO4	G4	N/C	B6	SD4–	L17	VDD	U8	VSS
V6	IDSEL	H18	N/C	A7	SD5–	R17	VDD	J18	VSSA
W9	IRDY/	H3	N/C	A8	SD6–	R4	VDD	M3	VSSCORE
U20	IRQ/	J17	N/C	A9	SD7–	U10	VDD	N18	VSSCORE
J1	LVDSMODE(TEST)	J4	N/C	D20	SD8–	U15	VDD	P20	VSSCORE
K19	MAC/_TESTOUT	K17	N/C	E20	SD9–	U6	VDD	N1	VSSCORE2
K20	MAD0	K18	N/C	F20	SD10–	A11	VDD_RBIAS		
L20	MAD1	K3	N/C	G20	SD11–	H19	VDDA		
L19	MAD2	L18	N/C	J3	SD12–	P1	VDDCORE		
M20	MAD3	L4	N/C	H2	SD13–	P17	VDDCORE		
M19	MAD4	M17	N/C	G2	SD14–	P2	VDDCORE		
M18	MAD5	M4	N/C	F2	SD15–	R19	VDDCORE		
N20	MAD6	P4	N/C	D1	SD0+	A1	VSS		
N19	MAD7	R3	N/C	B2	SD1+	D13	VSS		

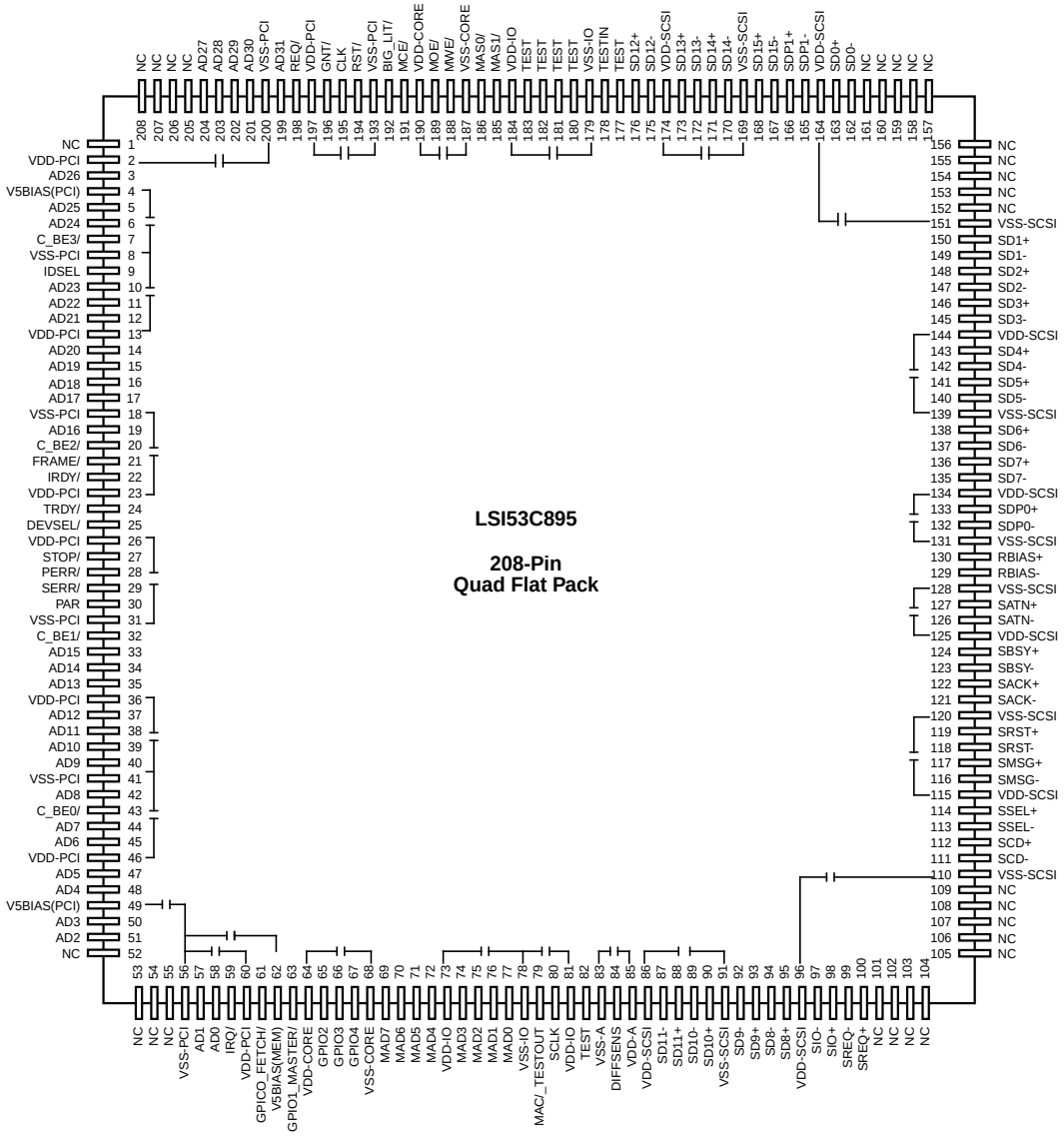
1. *NC* pins are not connected.

Table 7.52 BGA Position Numerically and Signal Name

BGA #	Signal	BGA #	Signal	BGA #	Signal	BGA #	Signal	BGA #	Signal
A1	VSS	D1	SD0+	J3	SD12–	N10	VSS	V9	FRAME/
A2	N/C	D2	N/C	J4	N/C	N11	VSS	V10	N/C
A3	SD2+	D3	N/C	J8	VSS	N12	VSS	V11	PERR/
A4	SD3+	D4	VSS	J9	VSS	N13	VSS	V12	AD15
A5	SD4+	D5	N/C	J10	VSS	N17	VSS	V13	AD12
A6	N/C	D6	VDD	J11	VSS	N18	VSSCORE	V14	N/C
A7	SD5–	D7	N/C	J12	VSS	N19	MAD7	V15	N/C
A8	SD6–	D8	VSS	J13	VSS	N20	MAD6	V16	N/C
A9	SD7–	D9	N/C	J17	N/C	P1	VDDCORE	V17	AD4
A10	RBIAS	D10	N/C	J18	VSSA	P2	VDDCORE	V18	AD2
A11	VDD_RBIAS	D11	VDD	J19	TEST_HSC/	P3	BIG_LIT/	V19	N/C
A12	SATN+	D12	N/C	J20	SCLK	P4	N/C	V20	AD0
A13	SBSY+	D13	VSS	K1	TEST	P17	VDDCORE	W1	AD28
A14	SACK+	D14	N/C	K2	TESTIN	P18	GPIO3	W2	N/C
A15	SRST+	D15	VDD	K3	N/C	P19	GPIO4	W3	N/C
A16	SMSG+	D16	SCD+	K4	VDD	P20	VSSCORE	W4	N/C
A17	SSEL+	D17	VSS	K8	VSS	R1	MCE/	W5	AD24
A18	SSEL–	D18	SREQ–	K9	VSS	R2	RST/	W6	AD23
A19	N/C	D19	SD8+	K10	VSS	R3	N/C	W7	AD20
A20	N/C	D20	SD8–	K11	VSS	R4	VDD	W8	AD17
B1	N/C	E1	SDP1–	K12	VSS	R17	VDD	W9	IRDY/
B2	SD1+	E2	N/C	K13	VSS	R18	GPIO1_MASTER/	W10	TRDY/
B3	SD1–	E3	N/C	K17	N/C	R19	VDDCORE	W11	STOP/
B4	SD2–	E4	N/C	K18	N/C	R20	GPIO2	W12	C_BE1/
B5	SD3–	E17	SIO+	K19	MAC/_TESTOUT	T1	CLK	W13	AD13
B6	SD4–	E18	N/C	K20	MAD0	T2	GNT/	W14	AD10
B7	SD5+	E19	SD9+	L1	TEST	T3	N/C	W15	AD8
B8	SD6+	E20	SD9–	L2	TEST	T4	N/C	W16	N/C
B9	SD7+	F1	SD15+	L3	TEST	T17	N/C	W17	AD6
B10	SDP0–	F2	SD15–	L4	N/C	T18	N/C	W18	V5BIAS(PCI)
B11	N/C	F3	SDP1+	L8	VSS	T19	GPIO0_FETCHN	W19	N/C
B12	SATN–	F4	VDD	L9	VSS	T20	V5BIAS(MEM)	W20	N/C
B13	SBSY–	F17	VDD	L10	VSS	U1	REQ/	Y1	N/C
B14	SACK–	F18	N/C	L11	VSS	U2	AD31	Y2	N/C
B15	SRST–	F19	SD10+	L12	VSS	U3	N/C	Y3	AD26
B16	SMSG–	F20	SD10–	L13	VSS	U4	VSS	Y4	V5BIAS(PCI)
B17	N/C	G1	SD14+	L17	VDD	U5	N/C	Y5	C_BE3/
B18	N/C	G2	SD14–	L18	N/C	U6	VDD	Y6	AD22
B19	N/C	G3	N/C	L19	MAD2	U7	N/C	Y7	AD19
B20	N/C	G4	N/C	L20	MAD1	U8	VSS	Y8	AD16
C1	SD0–	G17	N/C	M1	MAS1/	U9	C_BE2/	Y9	N/C
C2	N/C	G18	N/C	M2	MAS0/	U10	VDD	Y10	DEVSEL/
C3	N/C	G19	SD11+	M3	VSSCORE	U11	SERR/'	Y11	N/C
C4	N/C	G20	SD11–	M4	N/C	U12	N/C	Y12	PAR
C5	N/C	H1	SD13+	M8	VSS	U13	VSS	Y13	AD14
C6	N/C	H2	SD13–	M9	VSS	U14	N/C	Y14	AD11
C7	N/C	H3	N/C	M10	VSS	U15	VDD	Y15	AD9
C8	N/C	H4	VSS	M11	VSS	U16	N/C	Y16	C_BE0/
C9	N/C	H8	VSS	M12	VSS	U17	VSS	Y17	AD7
C10	SDP0+	H9	VSS	M13	VSS	U18	AD1	Y18	AD5
C11	N/C	H10	VSS	M17	N/C	U19	N/C	Y19	AD3
C12	N/C	H11	VSS	M18	MAD5	U20	IRQ/	Y20	N/C
C13	N/C	H12	VSS	M19	MAD4	V1	AD30		
C14	N/C	H13	VSS	M20	MAD3	V2	AD29		
C15	N/C	H17	VSS	N1	VSSCORE2	V3	AD27		
C16	N/C	H18	N/C	N2	MWE/	V4	N/C		
C17	SCD–	H19	VDDA	N3	MOE/	V5	AD25		
C18	N/C	H20	DIFFSENS	N4	VSS	V6	IDSEL		
C19	SREQ+	J1	LVDSMODE(TEST)	N8	VSS	V7	AD21		
C20	SIO–	J2	SD12+	N9	VSS	V8	AD18		

1. *NC* pins are not connected.

Figure 7.40 LSI53C895 Pin Diagram, 208-Pin QFP



1. The decoupling capacitor arrangement shown above is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the LSI53C895, a multilayer PC board with power and ground planes is required.
2. A 2.2 kΩ resistor is required between RBIAS+ and RBIAS– pins. RBIAS– must be connected to 3.3 V as well.

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Table 7.53 Signal Name by Pin Number QFP

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
NC	1	AD7	44	SD11–	87	RBIAS+	130	VDD-SCSI	174
VDD-PCI	2	AD6	45	SD11+	88	VSS-SCSI	131	SD12-	175
AD26	3	VDD-PCI	46	SD10-	89	SDP0-	132	SD12+	176
V5BIAS(PCI)	4	AD5	47	SD10+	90	SDP0+	133	TEST	177
AD25	5	AD4	48	VSS-SCSI	91	VDD-SCSI	134	TESTIN	178
AD24	6	V5BIAS(PCI)	49	SD9-	92	SD7-	135	VSS-IO	179
C_BD3/	7	AD3	50	SD9+	93	SD7+	136	TEST	180
VSS-PCI	8	AD2	51	SD8-	94	SD6-	137	TEST	181
IDSEL	9	NC	52	SD8+	95	SD6+	138	TEST	182
AD23	10	NC	53	VDD-SCSI	96	VSS-SCSI	139	TEST	183
AD22	11	NC	54	SIO-	97	SD5-	140	VDD-IO	184
AD21	12	NC	55	SIO+	98	SD5+	141	MAS1/	185
VDD-PCI	13	VSS-PCI	56	SREQ-	99	SD4-	142	MAS0	186
AD20	14	AD1	57	SREQ+	100	SD4+	143	VSS-CORE	187
AD19	15	AD0	58	NC	101	VDD-SCSI	144	MWE/	188
AD18	16	IR$Q/	59	NC	102	SD3-	145	MOE/	189
AD17	17	VDD-PCI	60	NC	103	SD3+	146	VDD-CORE	190
VSS-PCI	18	GPIC0_FETCH	61	NC	104	SD2-	147	MCE/	191
AD16	19	V5BIAS(MEM)	62	NC	105	SD2+	148	BIT_LIT	192
C_BE2/	20	GPIO1_MASTER	63	NC	106	SD1-	149	VSS-PCI	193
FRAME/	21	VDD-CORE	64	NC	107	SD1+	150	RST/	194
IRDY/	22	GPIO2	65	NC	108	VSS-SCSI	151	CLK	195
VDD-PCI	23	GPIO3	66	NC	109	NC	153	GNT/	196
TRDY/	24	GPIO4	67	VSS-SCSI	110	NC	154	VDD-PCI	197
DEVSEL/	25	VSS-CORE	68	SCD-	111	NC	155	REQ/	198
VDD-PCI	26	MAD7	69	SCD+	112	NC	156	AD31	199
STOP/	27	MAD6	70	SSEL-	113	NC	157	VSS-PCI	200
PERR/	28	MAD5	71	SSEL+	114	NC	158	AD30	201
SERR/	29	MAD4	72	VDD-SCSI	115	NC	159	AD29	202
PAR	30	VDD-IO	73	SMSG-	116	NC	160	AD28	203
VSS-PCI	31	MAD3	74	SMSG+	117	NC	161	AD27	204
C_BE1/	32	MAD2	75	SRST-	118	SD0-	162	NC	205
AD15	33	MAD1	76	SRST+	119	SD0+	163	NC	206
AD14	34	MAD0	77	VSS-SCSI	120	VDD-SCSI	164	NC	207
AD13	35	VSS-IO	78	SACK-	121	SDP1-	165	NC	208
VDD-PCI	36	MAC/_TESTOUT	79	SACK+	122	SDP1+	166		
AD12	37	SCLK	80	SBSY-	123	SD15-	167		
AD11	38	VDD-IO	81	SBSY+	124	SD15+	168		
AD10	39	TEST	82	VDD-SCSI	125	VSS-SCSI	169		
AD9	40	VSS-A	83	SATN-	126	SD14-	170		
VSS-PCI	41	DIFFSENS	84	SATN+	127	SD14+	171		
AD8	42	VDD-A	85	VSS-SCSI	128	SD13-	172		
C_BE0/	43	VDD-SCSI	86	RBIAS-	129	SD13+	173		

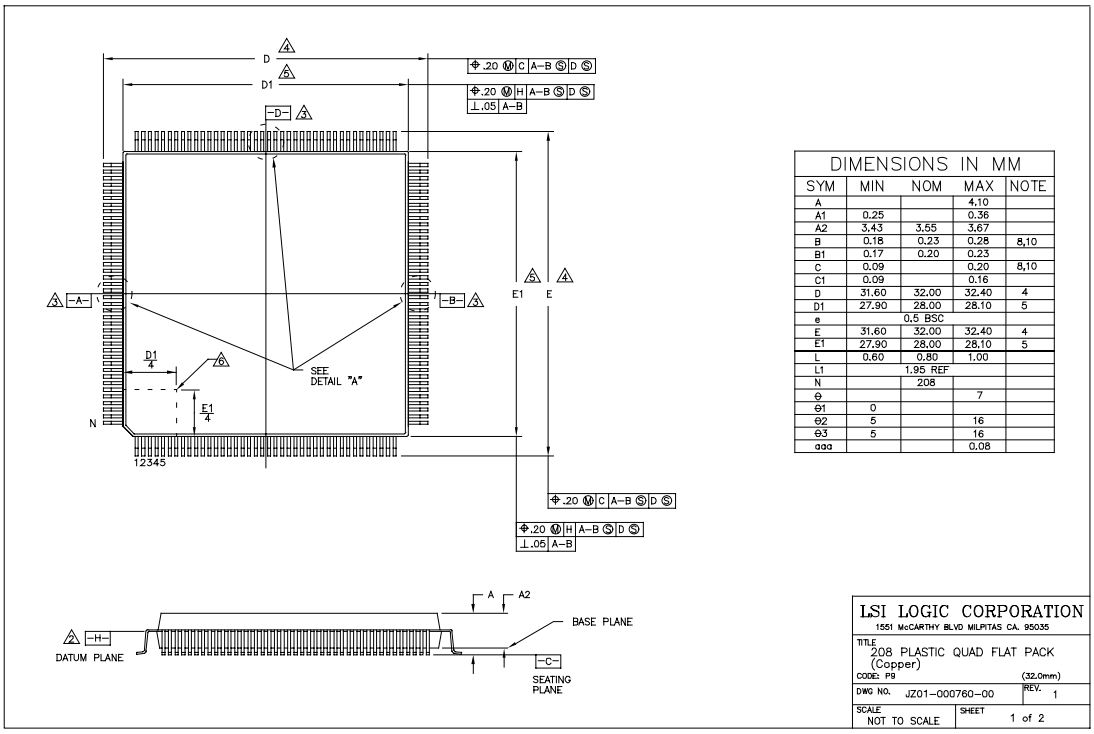
1. *NC* pins are not connected.

Table 7.54 Alphabetical Signal Name and Pin Number QFP

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD0	58	GPIO1_MASTER	63	NC	161	SD5-	140	VDD-PCI	13
AD2	51	GPIO2	65	NC	205	SD6+	138	VDD-PCI	23
AD3	50	GPIO3	66	NC	206	SD6-	137	VDD-PCI	26
AD1	57	GPIO4	67	NC	207	SD7+	136	VDD-PCI	36
AD4	48	IDSEL	9	NC	208	SD7-	135	VDD-PCI	46
AD5	47	IR$Q/	59	PAR	30	SD8+	95	VDD-PCI	60
AD6	45	IRDY/	22	PERR/	28	SD8-	94	VDD-PCI	197
AD7	44	MAC/_TESTOUT	79	RBIAS+	130	SD9+	93	VDD-SCSI	86
AD8	42	MAD0	77	RBIAS-	129	SD9-	92	VDD-SCSI	96
AD9	40	MAD1	76	REQ/	198	SDP0+	133	VDD-SCSI	115
AD10	39	MAD2	75	RST/	194	SDP0-	132	VDD-SCSI	125
AD11	38	MAD3	74	SACK+	122	SDP1+	166	VDD-SCSI	134
AD12	37	MAD4	72	SACK-	121	SDP1-	165	VDD-SCSI	144
AD13	35	MAD5	71	SATN+	127	SERR/	29	VDD-SCSI	164
AD14	34	MAD6	70	SATN-	126	SIO+	98	VDD-SCSI	174
AD15	33	MAD7	69	SBSY+	124	SIO-	97	VSS-A	83
AD16	19	MAS0	186	SBSY-	123	SMSG+	117	VSS-CORE	68
AD17	17	MAS1/	185	SCD+	112	SMSG-	116	VSS-CORE	187
AD18	16	MCE/	191	SCD-	111	SREQ+	100	VSS-IO	78
AD19	15	MOE/	189	SCLK	80	SREQ-	99	VSS-IO	179
AD20	14	MWE/	188	SD0+	163	SRST+	119	VSS-PCI	8
AD21	12	NC	1	SD0-	162	SRST-	118	VSS-PCI	18
AD22	11	NC	52	SD1+	150	SSEL+	114	VSS-PCI	31
AD23	10	NC	53	SD1-	149	SSEL-	113	VSS-PCI	41
AD24	6	NC	54	SD10+	90	STOP/	27	VSS-PCI	56
AD25	5	NC	55	SD10-	89	TEST	82	VSS-PCI	193
AD26	3	NC	101	SD11+	88	TEST	177	VSS-PCI	200
AD27	204	NC	102	SD11–	87	TEST	180	VSS-SCSI	91
AD28	203	NC	103	SD12+	176	TEST	181	VSS-SCSI	110
AD29	202	NC	104	SD12-	175	TEST	182	VSS-SCSI	120
AD30	201	NC	105	SD13+	173	TEST	183	VSS-SCSI	128
AD31	199	NC	106	SD13-	172	TESTIN	178	VSS-SCSI	131
BIT_LIT	192	NC	107	SD14+	171	TRDY/	24	VSS-SCSI	139
C_BD3/	7	NC	108	SD14-	170	V5BIAS(MEM)	62	VSS-SCSI	151
C_BE0/	43	NC	109	SD15+	168	V5BIAS(PCI)	4	VSS-SCSI	169
C_BE1/	32	NC	153	SD15-	167	V5BIAS(PCI)	49		
C_BE2/	20	NC	154	SD2+	148	VDD-A	85		
CLK	195	NC	155	SD2-	147	VDD-CORE	64		
DEVSEL/	25	NC	156	SD3+	146	VDD-CORE	190		
DIFFSENS	84	NC	157	SD3-	145	VDD-IO	73		
FRAME/	21	NC	158	SD4+	143	VDD-IO	81		
GNT/	196	NC	159	SD4-	142	VDD-IO	184		
GPIC0_FETCH	61	NC	160	SD5+	141	VDD-PCI	2		

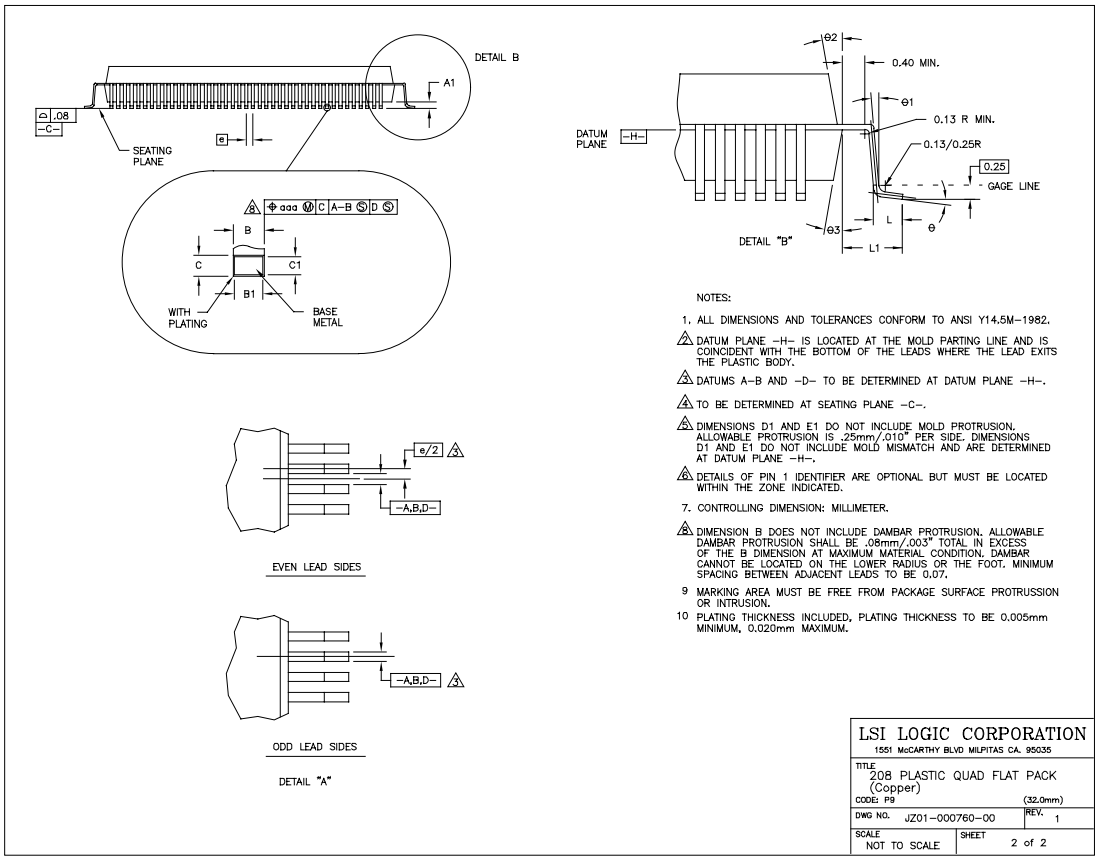
1. *NC* pins are not connected.

Figure 7.41 LSI53C895 Mechanical Drawing, 208-Pin QFP



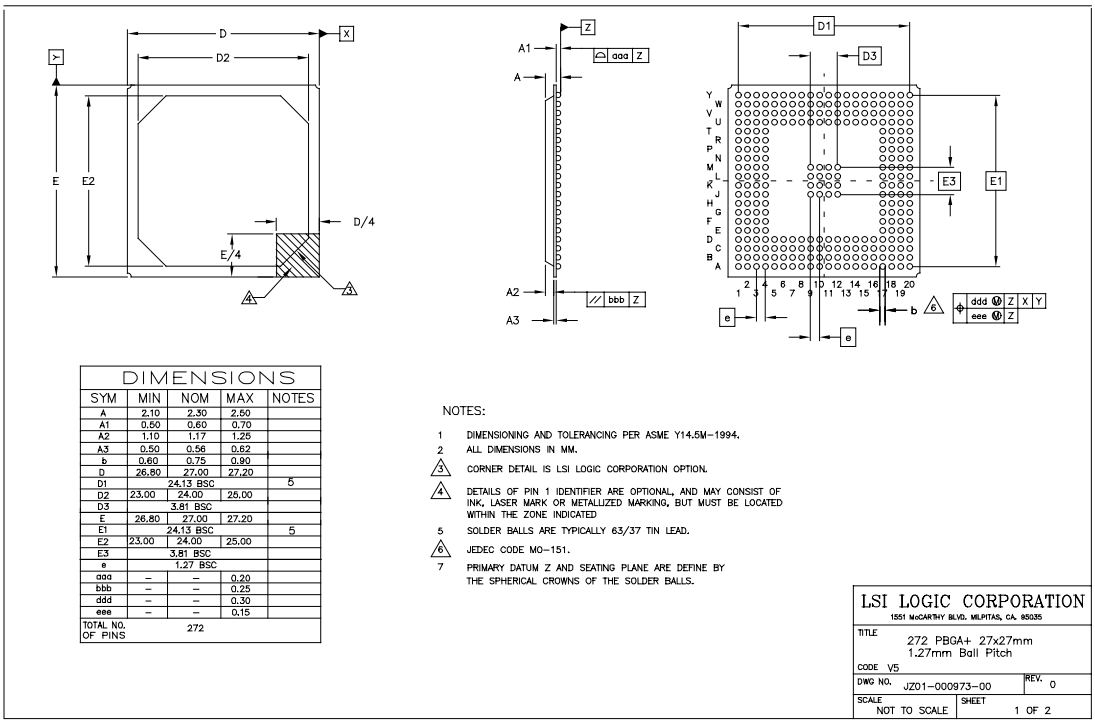
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code P9.**

Figure 7.41 LSI53C895 Mechanical Drawing, 208-Pin QFP (cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code P9.**

Figure 7.42 LSI53C895 Mechanical Drawing, 272 BGA



DIMENSIONS				
SYM	MIN	NOM	MAX	NOTES
A	2.10	2.30	2.50	
A1	0.50	0.60	0.70	
A2	1.10	1.17	1.25	
A3	0.50	0.56	0.62	
b	0.60	0.75	0.90	
D	26.80	27.00	27.20	
D1		24.13 BSC		5
D2	23.00	24.00	25.00	
D3		3.81 BSC		
E	26.80	27.00	27.20	
E1		24.13 BSC		5
E2	23.00	24.00	25.00	
E3		3.81 BSC		
e		1.27 BSC		
aaa	–	–	0.20	
bbb	–	–	0.25	
ddd	–	–	0.30	
eee	–	–	0.15	
TOTAL NO. OF PINS		272		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS IN MM.
3. CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
5. SOLDER BALLS ARE TYPICALLY 63/37 TIN LEAD.
6. JEDEC CODE MO–151.
7. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINE BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

LSI LOGIC CORPORATION
1551 McCARTHY BLVD. MILPITAS, CA. 95035

TITLE: 272 PBGA+ 27x27mm 1.27mm Ball Pitch
CODE V5
DWG NO. JZ01–000973–00 REV. 0
SCALE NOT TO SCALE SHEET 1 OF 2

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code V5.**

Appendix A
Register Summary

Table A.1 lists the PCI and SCSI registers by register name.

Table A.1 LSI53C895 Register Map

Register Name	Address	Read/Write	Page
PCI Registers			
Base Address One (Memory)	0x14–0x17	Read/Write	5-9
Base Address Register Zero (I/O)	0x10–0x13	Read/Write	5-9
Cache Line Size	0x0C	Read/Write	5-7
Class Code	0x09–0x0B	Read Only	5-7
Command	0x04–0x05	Read/Write	5-3
Device ID	0x02–0x03	Read Only	5-3
Expansion ROM Base Address	0x30–0x33	Read/Write	5-12
Header Type	0x0E	Read Only	5-8
Interrupt Line	0x3C	Read/Write	5-13
Interrupt Pin	0x3D	Read Only	5-13
Latency Timer	0x0D	Read/Write	5-8
Max_Lat	0x3F	Read Only	5-14
Min_Gnt	0x3E	Read Only	5-14
Not Supported	0x1C–0x1F	–	5-10
Not Supported	0x20–0x23	–	5-10
Not Supported	0x24–0x27	–	5-10
RAM Base Address	0x18–0x1B	Read/Write	5-10

Table A.1 LSI53C895 Register Map (Cont.)

Register Name	Address	Read/Write	Page
Reserved	0x28–0x31	–	5-10
Reserved	0x34–0x3B	–	5-13
Revision ID (Rev ID)	0x08	Read Only	5-6
Status	0x06–0x07	Read/Write	5-5
Subsystem ID	0x2E–0x2F	Read Only	5-11
Subsystem Vendor ID	0x2C–0x2D	Read Only	5-10
Vendor ID	0x00–0x01	Read Only	5-3
SCSI Registers			
Adder Sum Output (ADDER)	0x3C–0x3F	Read Only	5-68
Chip Test Five (CTEST5)	0x22	Read/Write	5-57
Chip Test Four (CTEST4)	0x21	Read/Write	5-55
Chip Test One (CTEST1)	0x19	Read Only	5-50
Chip Test Six (CTEST6)	0x23	Read/Write	5-58
Chip Test Three (CTEST3)	0x1B	Read/Write	5-52
Chip Test Two (CTEST2)	0x1A	Read/Write	5-51
Chip Test Zero (CTEST0)	0x18	Read/Write	5-50
Data Structure Address (DSA)	0x10–0x13	Read/Write	5-46
DMA Byte Counter (DBC)	0x24–0x26	Read/Write	5-59
DMA Command (DCMD)	0x27	Read/Write	5-60
DMA Control (DCNTL)	0x3B	Read/Write	5-66
DMA FIFO (DFIFO)	0x20 (A0)	Read Only	5-54
DMA Interrupt Enable (DIEN)	0x39	Read/Write	5-65
DMA Mode (DMODE)	0x38	Read/Write	5-62
DMA Next Address (DNAD)	0x28–0x2B	Read/Write	5-60
DMA SCRIPTS Pointer (DSP)	0x2C–0x2F	Read/Write	5-61

Table A.1 LSI53C895 Register Map (Cont.)

Register Name	Address	Read/Write	Page
DMA SCRIPTS Pointer Save (DSPS)	0x30–0x33	Read/Write	5-61
DMA Status (DSTAT)	0x0C	Read Only	5-38
General Purpose (GPREG)	0x07	Read/Write	5-33
General Purpose Pin Control (GPCNTL)	0x47	Read/Write	5-78
Interrupt Status (ISTAT)	0x14	Read/Write	5-46
Memory Access Control (MACNTL)	0x46	Read/Write	5-77
Reserved	0x56–0x57	–	5-93
Reserved	0x5A–0x5B	–	5-93
Response ID One (RESPID1)	0x4B	Read/Write	5-84
Response ID Zero (RESPID0)	0x4A	Read/Write	5-83
Scratch Byte Register (SBR)	0x3A	Read/Write	5-66
Scratch Register A (SCRATCHA)	0x34–0x37	Read/Write	5-62
Scratch Register B (SCRATCHB)	0x5C–0x5F (0xDC–0xDF)	Read/Write	5-94
Scratch Registers C–J (SCRATCHC–SCRATCHJ)	0x60–0x7F (0xE0–0xFF)	Read/Write	5-94
SCSI Bus Control Lines (SBCL)	0x0B	Read Only	5-37
SCSI Bus Data Lines (SBDL)	0x58–0x59 (0xD8–0xD9)	Read Only	5-93
SCSI Chip ID (SCID)	0x04	Read/Write	5-28
SCSI Contr0l Three (SCNTL3)	0x03	Read/Write	5-25
SCSI Control One (SCNTL1)	0x01	Read/Write	5-20
SCSI Control Two (SCNTL2)	0x02	Read/Write	5-23
SCSI Control Zero (SCNTL0)	0x00	Read/Write	5-17
SCSI Destination ID (SDID)	0x06	Read/Write	5-33
SCSI First Byte Received (SFBR)	0x08	Read/Write	5-34

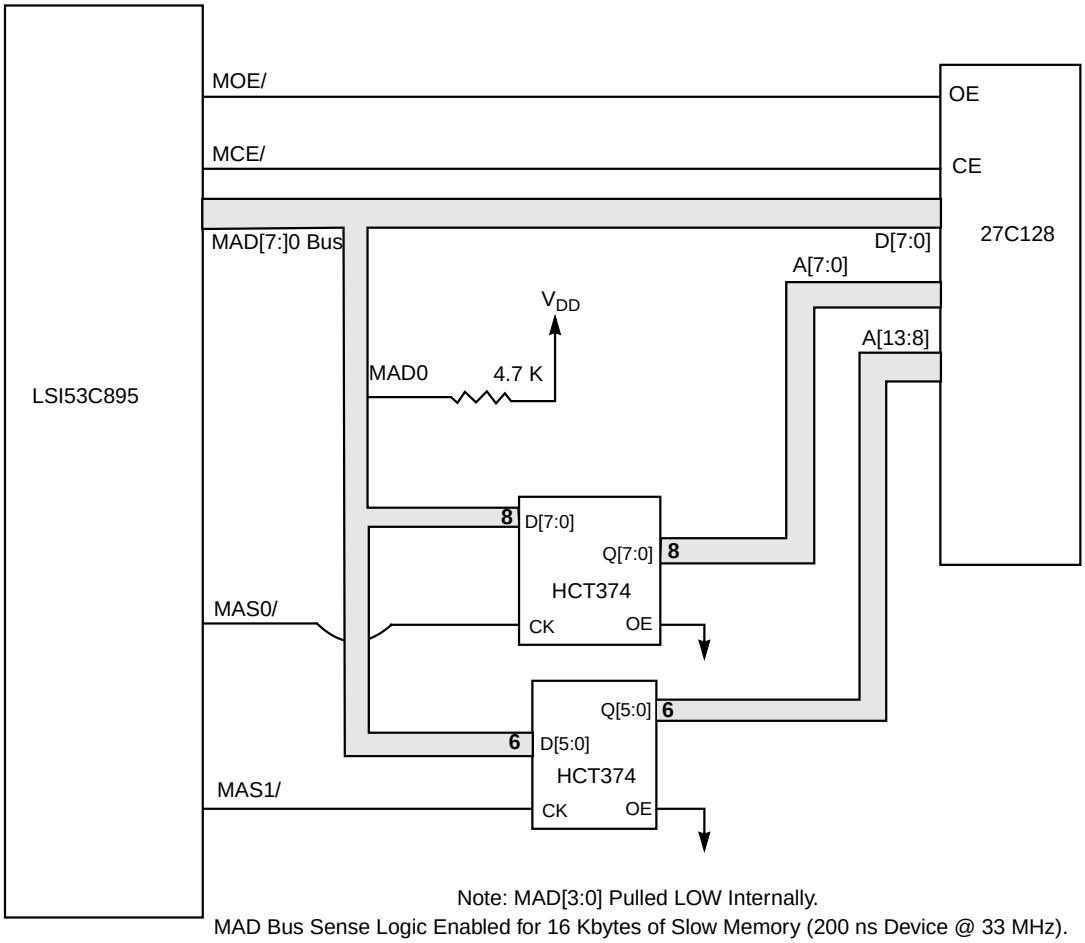
Table A.1 LSI53C895 Register Map (Cont.)

Register Name	Address	Read/Write	Page
SCSI Input Data Latch (SIDL)	0x50–0x51 (0xD0–0xD1)	Read Only	5-91
SCSI Interrupt Enable One (SIEN1)	0x41	Read/Write	5-70
SCSI Interrupt Enable Zero (SIEN0)	0x40	Read/Write	5-68
SCSI Interrupt Status One (SIST1)	0x43	Read Only	5-74
SCSI Interrupt Status Zero (SIST0)	0x42	Read Only	5-72
SCSI Longitudinal Parity (SLPAR)	0x44	Read/Write	5-75
SCSI Output Control Latch (SOCL)	0x09	Read /Write	5-35
SCSI Output Data Latch (SODL)	0x54–0x55 (0xD4–0xD5)	Read/Write	5-93
SCSI Selector ID (SSID)	0x0A	Read Only	5-36
SCSI Status One (SSTAT1)	0x0E	Read Only	5-42
SCSI Status Two (SSTAT2)	0x0F	Read Only	5-44
SCSI Status Zero (SSTAT0)	0x0D	Read Only	5-40
SCSI Test 4 (STEST4)	0x52 (0xD2)	Read Only	5-92
SCSI Test One (STEST1)	0x4D	Read/Write	5-85
SCSI Test Three (STEST3)	0x4F (0xCF)	Read/Write	5-89
SCSI Test Two (STEST2)	0x4E (0xCE)	Read/Write	5-87
SCSI Test Zero (STEST0)	0x4C	Read Only	5-84
SCSI Timer One (STIME1)	0x49	Read/Write	5-81
SCSI Timer Zero (STIME0)	0x48	Read/Write	5-79
SCSI Transfer (SXFER)	0x05	Read/Write	5-29
SCSI Wide Residue (SWIDE)	0x45	Read Only	5-77
Temporary (TEMP)	0x1C–0x1F	Read/Write	5-53

Appendix B
External Memory Interface Diagram Examples

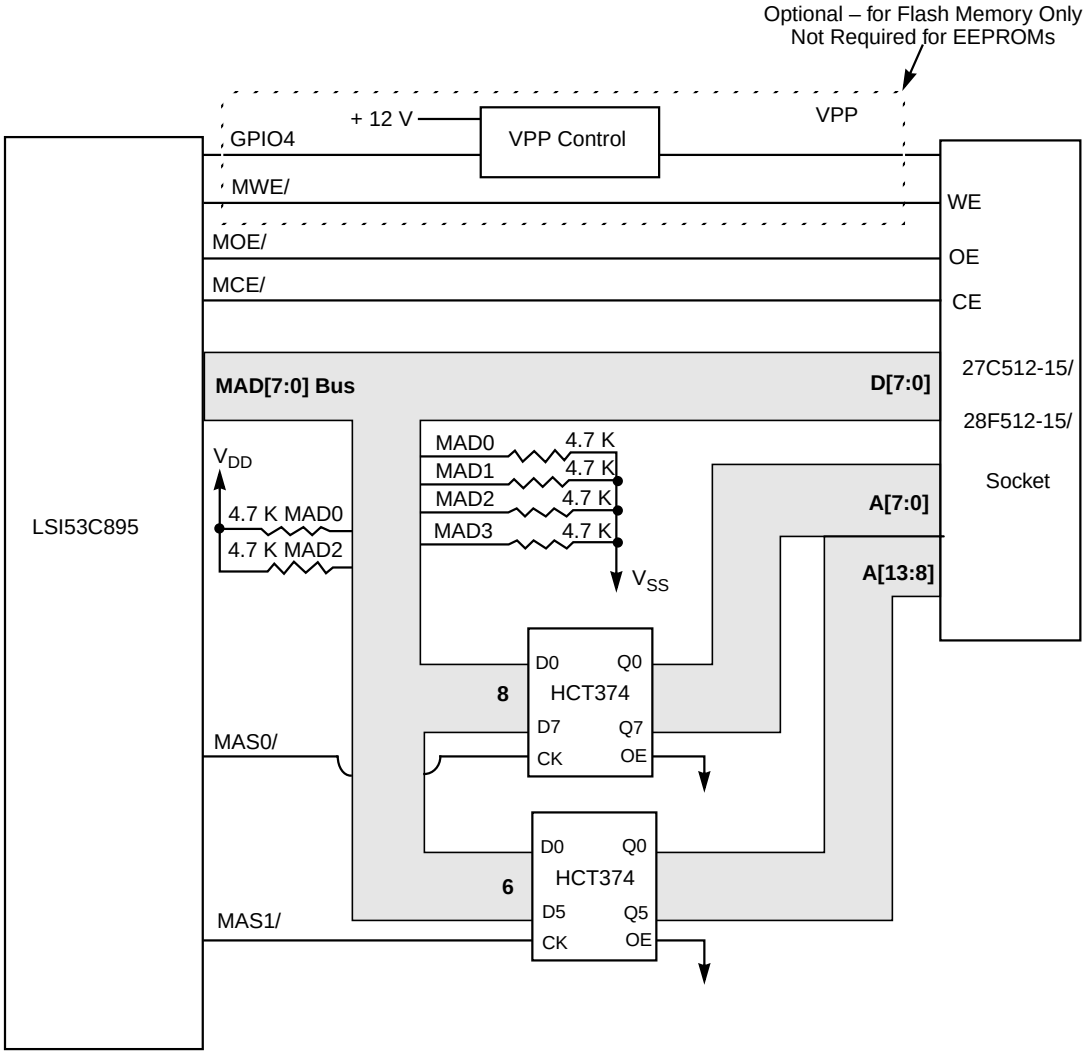
Appendix B has example external memory interface diagrams.

Figure B.1 16 Kbytes Interface with 200 ns Memory



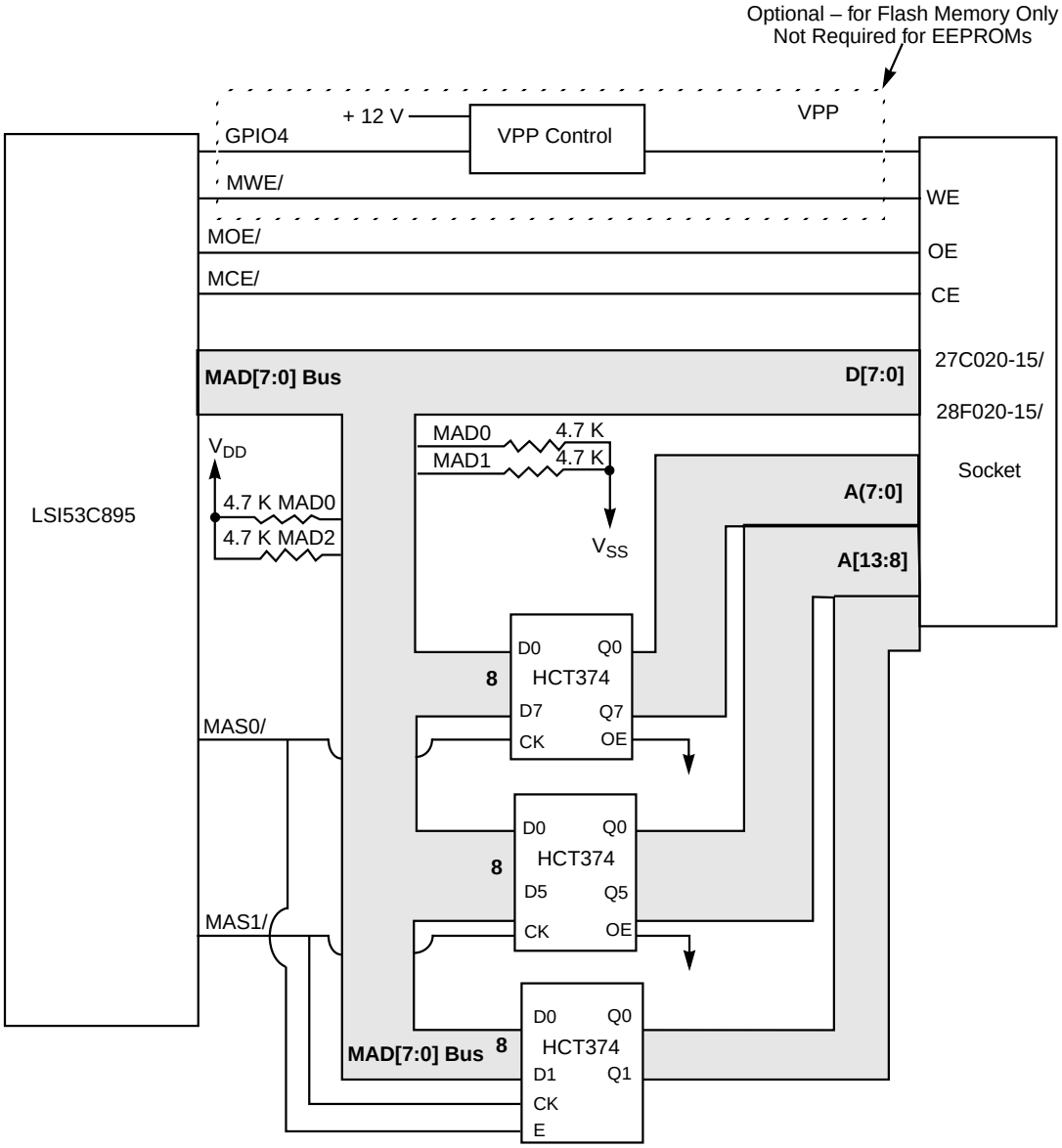
Note: MAD[3:0] Pulled LOW Internally.
MAD Bus Sense Logic Enabled for 16 Kbytes of Slow Memory (200 ns Device @ 33 MHz).

Figure B.2 64 Kbytes Interface with 200 ns Memory



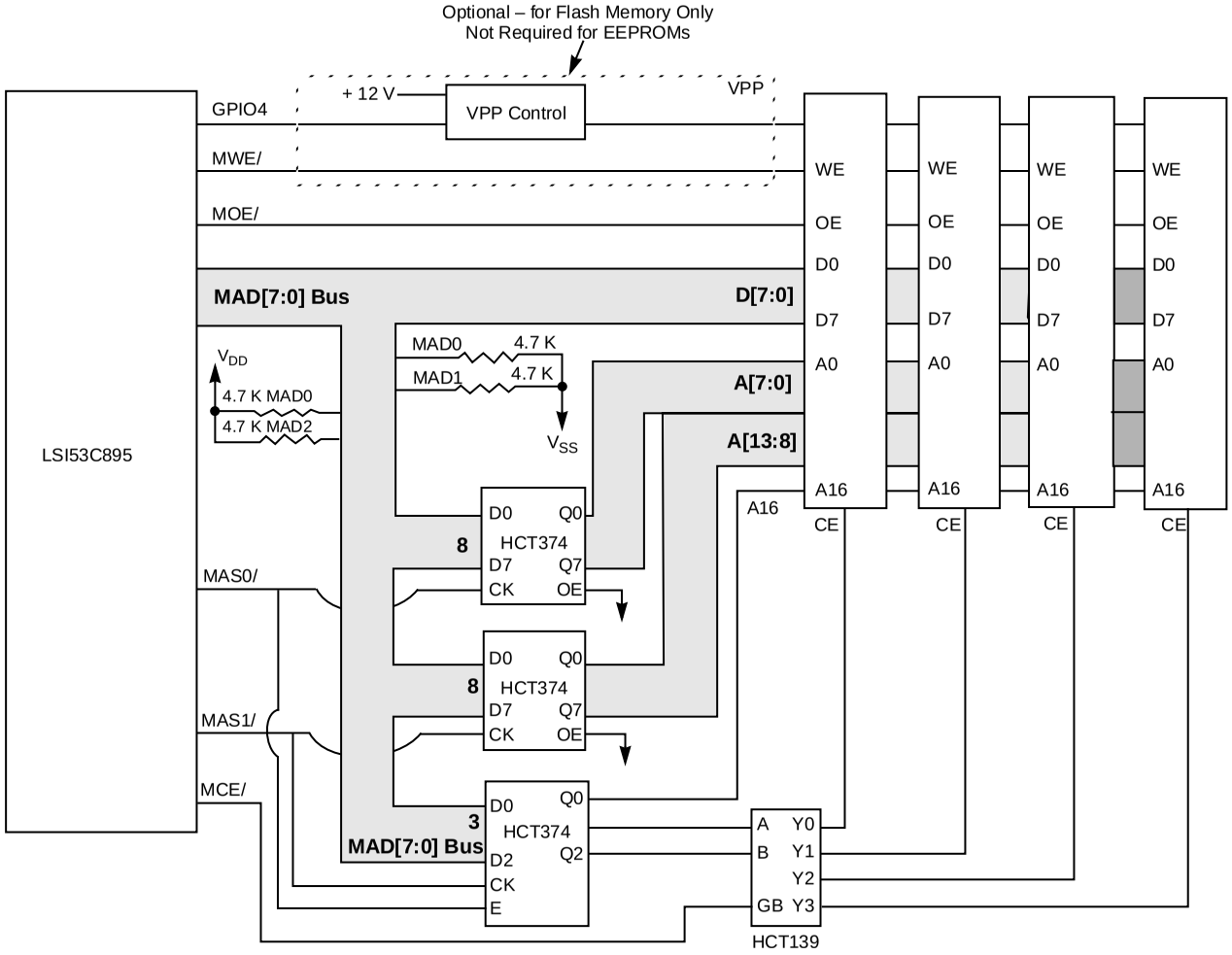
MAD Bus Sense Logic Enabled for 64 Kbytes of Slow Memory (200 ns Device @ 33 MHz).

Figure B.3 256 Kbytes Interface with 150 ns Memory



MAD Bus Sense Logic Enabled for 256 Kbytes for Fast Memory (150 ns Device @ 33 MHz).
The HCT374s may be replaced with HCT377s.

Figure B.4 512 Kbytes Interface with 150 ns Memory



MAD Bus Sense Logic Enabled for 512 Kbytes of Slow Memory (150 ns Devices, Additional Time Required for HCT139 @ 33 MHz).
The HCT374s may be replaced with HCT377s.

Appendix C
Circuit Board Layout Issues

Higher data transfer rates, such as Ultra2 SCSI, make good Printed Circuit Board (PCB) layout practices more critical than ever. Some of the layout design criteria that need to be considered are separation of LVD and TTL/CMOS signals, routing of the differential pairs, trace impedance, stub lengths, decoupling power supplies and the dielectric constant of the board material. When certain PCB layout guidelines are not followed, various signal degradation effects can result. Impedance mismatches cause reflections. Crosstalk, dielectric loss, skin effects, dispersion loss and reduction of noise margin are some other unwanted by-products of poor PCB layout practices.

Note: This information was originally published in System Engineering Notes 893 (PCB Layout for LSI53C895) and 898 (Analog Power Filtering for LSI53C895).

This appendix contains these topics:

C.1 Signal Separation

Avoid crosstalk problems by providing a good separation between LVD and TTL/CMOS signals. Crosstalk is proportional to dv/dt. TTL/CMOS

signals have larger voltage swings than LVD and can effect them if lines are running in close proximity. The best means of separation is to provide a ground trace between the two types of signals. Another means of keeping the two kinds of signals apart is to place them on separate layers. If LVD and TTL/CMOS signals need to be on the same layer, they should be separated by as much distance as possible.

C.2 Routing Signal Lines

Routing of differential lines is an important factor in maintaining signal integrity. Differentially paired traces must be kept equidistant. Each line should be kept as parallel as possible to its counterpart. To avoid skew issues, the two lines should be exactly the same in length. Abiding by these rules ensures that the rejection of common mode noise, inherent to differentially paired signals, remains intact. Another consideration in laying out these traces is to avoid sharp orthogonal turns. This type of turn needs to be angled to avoid sharp changes in impedance.

C.3 Impedance Matching

Trace impedance should match the impedance of the media as close as possible to avoid signal reflections. A typical differential impedance for the cable is about 120 Ω. The impedance of a trace on the PCB is controlled by its height and width, as well as the thickness of the dielectric. The impedance of a trace pair is controlled by the distance between the two traces.

C.4 Termination and Stub Length

The impedance of the terminator should match that of the cable. Terminators need to be placed at the far ends of the cable and as close to the receiver inputs as possible. Stub lengths of any device placed along the bus needs to be kept short to avoid impedance mismatches that result in reflections. The Ultra2 SCSI standard stipulates that stub lengths for LVD busses should not exceed 0.1 m. Additionally differences in stub lengths between REQ, ACK, DATA, and PARITY signals shall not exceed 1.27 cm.

C.5 Decoupling

Decoupling caps need to be as close to the chip V_{DD} pins as possible. The main power supply line should also be decoupled. SMT parts are preferred. The long lead lengths of axial leaded parts add inductance to the line.

C.6 Dielectric

Another design criteria that should be considered is that the dielectric constant of the board material should be as low as possible. Teflon has a dielectric constant rating twice as low as FR-4, which is a common material used in PCBs and so has lower losses. The disadvantage of Teflon is that it is more expensive.

C.7 Considerations Specific to the LSI53C895

This section discusses specific issues that relate to the LSI53C895 device.

C.7.1 RBIAS +/– Pins

The RBIAS +/– pins, 130 and 129, need to have a 2.2 KΩ resistor between them to provide the correct bias current to the LVD pads. Additionally + 3.3 V needs to be connected to RBIAS–, pin 129.

- SCSI lines should be short, with no Ts and all of them are about the same length.
- All PCI lines need to be less than 1.5 inches long.
- All GND and PWR traces need to be short, wide, and doubled.

C.7.2 Physical Dimensions

Refer to the mechanical drawing in the data manual for specific dimensions.

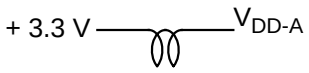
C.7.3 Power Requirements

A 3.3 V regulator (LT1086) derives the V_{DD} supply voltage.

C.7.4 V_{DD-A} Pin

The V_{DD-A} pin (pin 85 or H19) on the LSI53C895 SCSI I/O processor (SIOP) provides power to the phase locked loop (PLL) and is sensitive to noise. Board configurations that expose V_{DD-A} to noise above 90 mV at frequencies above 120 MHz are susceptible. External AC filtering is required to prevent high frequency noise from reaching the PLL. Neglecting to incorporate this filter may result in unpredictable SCSI bus behavior. This is particularly problematic during SCSI DATA OUT and DATA IN phases at Ultra2 speeds.

Analog power noise affects the ability of the SIOP to accurately clock REQ/ and ACK/ signals. As a result, the SIOP may double clock an incoming REQ/ signal or generate an extra ACK/ signal. This miscounting manifests itself as a data underrun or a data overrun. A ferrite bead is required to perform this filtering. The bead should be placed in series between V_{DD-A} and the 3.3 V power supply as follows:



The bead should provide between 50 W and 90 W impedance above 120 MHz and should be rated to handle currents up to 25 mA. No decoupling capacitor is needed in this configuration.

C.7.5 Terminators

Unitrode terminators (UCC5630) are recommended. They provide both LVD and single-ended termination, depending on what mode of operation is detected by the DIFFSENS pin. All GND's to the terminators should be short, wide and doubled. REG is tied to ground through five 1 µF caps.

C.7.6 Capacitive Load

The total capacitance budget dictated by the SCSI Parallel Interconnect – 2 (SPI-2) standard is presently 25 pF. The LSI53C895 is about 13 pF. A high density (68 pin) connector is about 3 pF. That leaves a budget of about 10pF for traces. Calculations show that the trace lengths should

be held to about 4 inches maximum under these conditions. Further calculations to determine allowable deltas in trace length between different signals show that +/– 1.46 inches is the maximum. This accommodates less than 200 ps of skew between signals.

C.7.7 SPI-2 Document

Refer to the SCSI Parallel Interconnect 2 (SPI-2) standard on Ultra2 SCSI for specific definitions of LVD technology as it pertains to SCSI. It also talks about requirements for Ultra2 SCSI data rates, VHDCI connectors, SCA-2 connectors, DIFFSENS and TERMPWR signals.

Index

Symbols

Numerics

A

B

C

D

E

F

G

H

I

J

L

M

N

O

P

Q

R

S

T

U

V

W

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W. E. Tel: 800.933.9953
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A. E. Tel: 727.507.5000

Georgia
Atlanta
A. E. Tel: 770.623.4400
B. M. Tel: 770.980.4922
W. E. Tel: 800.876.9953
Duluth
I. E. Tel: 678.584.0812

Hawaii
A. E. Tel: 800.851.2282

Idaho
A. E. Tel: 801.365.3800
W. E. Tel: 801.974.9953

Illinois
North/South
A. E. Tel: 847.797.7300
Tel: 314.291.5350
Chicago
B. M. Tel: 847.413.8530
W. E. Tel: 800.853.9953
Schaumburg
I. E. Tel: 847.885.9700

Indiana
Fort Wayne
I. E. Tel: 219.436.4250
W. E. Tel: 888.358.9953
Indianapolis
A. E. Tel: 317.575.3500

Iowa
W. E. Tel: 612.853.2280
Cedar Rapids
A. E. Tel: 319.393.0033

Kansas
W. E. Tel: 303.457.9953
Kansas City
A. E. Tel: 913.663.7900
Lenexa
I. E. Tel: 913.492.0408

Kentucky
W. E. Tel: 937.436.9953
Central/Northern/ Western
A. E. Tel: 800.984.9503
Tel: 800.767.0329
Tel: 800.829.0146

Louisiana
W. E. Tel: 713.854.9953
North/South
A. E. Tel: 800.231.0253
Tel: 800.231.5775

Maine
A. E. Tel: 800.272.9255
W. E. Tel: 781.271.9953

Maryland
Baltimore
A. E. Tel: 410.720.3400
W. E. Tel: 800.863.9953
Columbia
B. M. Tel: 800.673.7461
I. E. Tel: 410.381.3131

Massachusetts
Boston
A. E. Tel: 978.532.9808
W. E. Tel: 800.444.9953
Burlington
I. E. Tel: 781.270.9400
Marlborough
B. M. Tel: 800.673.7459
Woburn
B. M. Tel: 800.552.4305

Michigan
Brighton
I. E. Tel: 810.229.7710
Detroit
A. E. Tel: 734.416.5800
W. E. Tel: 888.318.9953
Clarkston
B. M. Tel: 877.922.9363

Minnesota
Champlin
B. M. Tel: 800.557.2566
Eden Prairie
B. M. Tel: 800.255.1469
Minneapolis
A. E. Tel: 612.346.3000
W. E. Tel: 800.860.9953
St. Louis Park
I. E. Tel: 612.525.9999

Mississippi
A. E. Tel: 800.633.2918
W. E. Tel: 256.830.1119

Missouri
W. E. Tel: 630.620.0969
St. Louis
A. E. Tel: 314.291.5350
I. E. Tel: 314.872.2182

Montana
A. E. Tel: 800.526.1741
W. E. Tel: 801.974.9953

Nebraska
A. E. Tel: 800.332.4375
W. E. Tel: 303.457.9953

Nevada
Las Vegas
A. E. Tel: 800.528.8471
W. E. Tel: 702.765.7117

New Hampshire
A. E. Tel: 800.272.9255
W. E. Tel: 781.271.9953

New Jersey
North/South
A. E. Tel: 201.515.1641
Tel: 609.222.6400
Mt. Laurel
I. E. Tel: 856.222.9566
Pine Brook
B. M. Tel: 973.244.9668
W. E. Tel: 800.862.9953
Parsippany
I. E. Tel: 973.299.4425
Wayne
W. E. Tel: 973.237.9010

New Mexico
W. E. Tel: 480.804.7000
Albuquerque
A. E. Tel: 505.293.5119

U.S. Distributors by State (Continued)

New York
Hauppauge
I. E. Tel: 516.761.0960
Long Island
A. E. Tel: 516.434.7400
W. E. Tel: 800.861.9953
Rochester
A. E. Tel: 716.475.9130
I. E. Tel: 716.242.7790
W. E. Tel: 800.319.9953
Smithtown
B. M. Tel: 800.543.2008
Syracuse
A. E. Tel: 315.449.4927

North Carolina
Raleigh
A. E. Tel: 919.859.9159
I. E. Tel: 919.873.9922
W. E. Tel: 800.560.9953

North Dakota
A. E. Tel: 800.829.0116
W. E. Tel: 612.853.2280

Ohio
Cleveland
A. E. Tel: 216.498.1100
W. E. Tel: 800.763.9953
Dayton
A. E. Tel: 614.888.3313
I. E. Tel: 937.253.7501
W. E. Tel: 800.575.9953
Strongsville
B. M. Tel: 440.238.0404
Valley View
I. E. Tel: 216.520.4333

Oklahoma
W. E. Tel: 972.235.9953
Tulsa
A. E. Tel: 918.459.6000
I. E. Tel: 918.665.4664

Oregon
Beaverton
B. M. Tel: 503.524.1075
I. E. Tel: 503.644.3300
Portland
A. E. Tel: 503.526.6200
W. E. Tel: 800.879.9953

Pennsylvania
Mercer
I. E. Tel: 412.662.2707
Philadelphia
A. E. Tel: 800.526.4812
B. M. Tel: 877.351.2355
W. E. Tel: 800.871.9953
Pittsburgh
A. E. Tel: 412.281.4150
W. E. Tel: 440.248.9996

Rhode Island
A. E. 800.272.9255
W. E. Tel: 781.271.9953

South Carolina
A. E. Tel: 919.872.0712
W. E. Tel: 919.469.1502

South Dakota
A. E. Tel: 800.829.0116
W. E. Tel: 612.853.2280

Tennessee
W. E. Tel: 256.830.1119
East/West
A. E. Tel: 800.241.8182
Tel: 800.633.2918

Texas
Arlington
B. M. Tel: 817.417.5993
Austin
A. E. Tel: 512.219.3700
B. M. Tel: 512.258.0725
I. E. Tel: 512.719.3090
W. E. Tel: 800.365.9953
Dallas
A. E. Tel: 214.553.4300
B. M. Tel: 972.783.4191
W. E. Tel: 800.955.9953
El Paso
A. E. Tel: 800.526.9238
Houston
A. E. Tel: 713.781.6100
B. M. Tel: 713.917.0663
W. E. Tel: 800.888.9953
Richardson
I. E. Tel: 972.783.0800
Rio Grande Valley
A. E. Tel: 210.412.2047
Stafford
I. E. Tel: 281.277.8200

Utah
Centerville
B. M. Tel: 801.295.3900
Murray
I. E. Tel: 801.288.9001
Salt Lake City
A. E. Tel: 801.365.3800
W. E. Tel: 800.477.9953

Vermont
A. E. Tel: 800.272.9255
W. E. Tel: 716.334.5970

Virginia
A. E. Tel: 800.638.5988
W. E. Tel: 301.604.8488
Haymarket
B. M. Tel: 703.754.3399
Springfield
B. M. Tel: 703.644.9045

Washington
Kirkland
I. E. Tel: 425.820.8100
Maple Valley
B. M. Tel: 206.223.0080
Seattle
A. E. Tel: 425.882.7000
W. E. Tel: 800.248.9953

West Virginia
A. E. Tel: 800.638.5988

Wisconsin
Milwaukee
A. E. Tel: 414.513.1500
W. E. Tel: 800.867.9953
Wauwatosa
I. E. Tel: 414.258.5338

Wyoming
A. E. Tel: 800.332.9326
W. E. Tel: 801.974.9953

Direct Sales Representatives by State (Components and Boards)

E. A. Earle Associates
E. L. Electrodyne - UT
GRP Group 2000
I. S. Infinity Sales, Inc.
ION ION Associates, Inc.
R. A. Rathsburg Associates, Inc.
SGY Synergy Associates, Inc.

Arizona
Tempe
E. A. Tel: 480.921.3305

California
Calabasas
I. S. Tel: 818.880.6480
Irvine
I. S. Tel: 714.833.0300
San Diego
E. A. Tel: 619.278.5441

Illinois
Elmhurst
R. A. Tel: 630.516.8400

Indiana
Cicero
R. A. Tel: 317.984.8608
Ligonier
R. A. Tel: 219.894.3184
Plainfield
R. A. Tel: 317.838.0360

Massachusetts
Burlington
SGY Tel: 781.238.0870

Michigan
Byron Center
R. A. Tel: 616.554.1460
Good Rich
R. A. Tel: 810.636.6060
Novi
R. A. Tel: 810.615.4000

North Carolina
Cary
GRP Tel: 919.481.1530

Ohio
Columbus
R. A. Tel: 614.457.2242
Dayton
R. A. Tel: 513.291.4001
Independence
R. A. Tel: 216.447.8825

Pennsylvania
Somerset
R. A. Tel: 814.445.6976

Texas
Austin
ION Tel: 512.794.9006
Arlington
ION Tel: 817.695.8000
Houston
ION Tel: 281.376.2000

Utah
Salt Lake City
E. L. Tel: 801.264.8050

Wisconsin
Muskego
R. A. Tel: 414.679.8250
Saukville
R. A. Tel: 414.268.1152

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
1551 McCarthy Blvd
Milpitas CA 95035
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Irvine
18301 Von Karman Ave
Suite 900
Irvine, CA 92612
♦ Tel: 949.809.4600
Fax: 949.809.4444

Pleasanton Design Center
5050 Hopyard Road, 3rd Floor
Suite 300
Pleasanton, CA 94588
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
7585 Ronson Road
Suite 100
San Diego, CA 92111
Tel: 858.467.6981
Fax: 858.496.0548

Silicon Valley
1551 McCarthy Blvd
Sales Office
M/S C-500
Milpitas, CA 95035
♦ Tel: 408.433.8000
Fax: 408.954.3353
Design Center
M/S C-410
Tel: 408.433.8000
Fax: 408.433.7695

Wireless Design Center
11452 El Camino Real
Suite 210
San Diego, CA 92130
Tel: 858.350.5560
Fax: 858.350.0171

Colorado
Boulder
4940 Pearl East Circle
Suite 201
Boulder, CO 80301
♦ Tel: 303.447.3800
Fax: 303.541.0641

Colorado Springs
4420 Arrowswest Drive
Colorado Springs, CO 80907
Tel: 719.533.7000
Fax: 719.533.7020

Fort Collins
2001 Danfield Court
Fort Collins, CO 80525
Tel: 970.223.5100
Fax: 970.206.5549

Florida
Boca Raton
2255 Glades Road
Suite 324A
Boca Raton, FL 33431
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Alpharetta
2475 North Winds Parkway
Suite 200
Alpharetta, GA 30004
Tel: 770.753.6146
Fax: 770.753.6147

Illinois
Oakbrook Terrace
Two Mid American Plaza
Suite 800
Oakbrook Terrace, IL 60181
Tel: 630.954.2234
Fax: 630.954.2235

Kentucky
Bowling Green
1262 Chestnut Street
Bowling Green, KY 42101
Tel: 270.793.0010
Fax: 270.793.0040

Maryland
Bethesda
6903 Rockledge Drive
Suite 230
Bethesda, MD 20817
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
200 West Street
Waltham, MA 02451
♦ Tel: 781.890.0180
Fax: 781.890.6158

Burlington - Mint Technology
77 South Bedford Street
Burlington, MA 01803
Tel: 781.685.3800
Fax: 781.685.3801

Minnesota
Minneapolis
8300 Norman Center Drive
Suite 730
Minneapolis, MN 55437
♦ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Red Bank
125 Half Mile Road
Suite 200
Red Bank, NJ 07701
Tel: 732.933.2656
Fax: 732.933.2643

Cherry Hill - Mint Technology
215 Longstone Drive
Cherry Hill, NJ 08003
Tel: 856.489.5530
Fax: 856.489.5531

New York
Fairport
550 Willowbrook Office Park
Fairport, NY 14450
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Phase II
4601 Six Forks Road
Suite 528
Raleigh, NC 27609
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
15455 NW Greenbrier Parkway
Suite 235
Beaverton, OR 97006
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
9020 Capital of TX Highway North
Building 1
Suite 150
Austin, TX 78759
Tel: 512.388.7294
Fax: 512.388.4171

Plano
500 North Central Expressway
Suite 440
Plano, TX 75074
♦ Tel: 972.244.5000
Fax: 972.244.5001

Houston
20405 State Highway 249
Suite 450
Houston, TX 77070
Tel: 281.379.7800
Fax: 281.379.7818

Canada
Ontario
Ottawa
260 Hearst Way
Suite 400
Kanata, ON K2L 3H1
♦ Tel: 613.592.1263
Fax: 613.592.3253

INTERNATIONAL

France
Paris
LSI Logic S.A.
Immeuble Europa
53 bis Avenue de l'Europe
B.P. 139
78148 Velizy-Villacoublay
Cedex, Paris
♦ Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
LSI Logic GmbH
Orleansstrasse 4
81669 Munich
♦ Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
Mittlerer Pfad 4
D-70499 Stuttgart
♦ Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Italy
Milan
LSI Logic S.P.A.
Centro Direzionale Colleoni Palazzo
Orione Ingresso 1
20041 Agrate Brianza, Milano
♦ Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
LSI Logic K.K.
Rivage-Shinagawa Bldg. 14F
4-1-8 Kounan
Minato-ku, Tokyo 108-0075
♦ Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
Crystal Tower 14F
1-2-27 Shiromi
Chuo-ku, Osaka 540-6014
♦ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Sales Offices and Design Resource Centers (Continued)

Korea
Seoul
LSI Logic Corporation of Korea Ltd
10th Fl., Haesung 1 Bldg.
942, Daechi-dong,
Kangnam-ku, Seoul, 135-283
Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
LSI Logic Europe Ltd
World Trade Center Eindhoven
Building 'Rijder'
Bogert 26
5612 LZ Eindhoven
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
LSI Logic Pte Ltd
7 Temasek Boulevard
#28-02 Suntec Tower One
Singapore 038987
Tel: 65.334.9061
Fax: 65.334.4749

Sweden
Stockholm
LSI Logic AB
Finlandsgatan 14
164 74 Kista
♦ Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Taiwan
Taipei
LSI Logic Asia, Inc.
Taiwan Branch
10/F 156 Min Sheng E. Road
Section 3
Taipei, Taiwan R.O.C.
Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

United Kingdom
Bracknell
LSI Logic Europe Ltd
Greenwood House
London Road
Bracknell, Berkshire RG12 2UB
♦ Tel: 44.1344.426544
Fax: 44.1344.481039

♦ Sales Offices with Design Resource Centers

International Distributors

Australia
New South Wales
Reptechnic Pty Ltd
3/36 Bydown Street
Neutral Bay, NSW 2089
♦ Tel: 612.9953.9844
Fax: 612.9953.9683

Belgium
Acal nv/sa
Lozenberg 4
1932 Zaventem
Tel: 32.2.7205983
Fax: 32.2.7251014

China
Beijing
LSI Logic International Services Inc.
Beijing Representative Office
Room 708
Canway Building
66 Nan Li Shi Lu
Xicheng District
Beijing 100045, China
Tel: 86.10.6804.2534 to 38
Fax: 86.10.6804.2521

France
Rungis Cedex
Azzurri Technology France
22 Rue Saarinen
Sillic 274
94578 Rungis Cedex
Tel: 33.1.41806310
Fax: 33.1.41730340

Germany
Haar
EBV Elektronik
Hans-Pinsel Str. 4
D-85540 Haar
Tel: 49.89.4600980
Fax: 49.89.46009840

Munich
Avnet Emg GmbH
Stahlgruberring 12
81829 Munich
Tel: 49.89.45110102
Fax: 49.89.42.27.75

Wuennenberg-Haaren
Peacock AG
Graf-Zepplin-Str 14
D-33181 Wuennenberg-Haaren
Tel: 49.2957.79.1692
Fax: 49.2957.79.9341

Hong Kong
Hong Kong
AVT Industrial Ltd
Unit 608 Tower 1
Cheung Sha Wan Plaza
833 Cheung Sha Wan Road
Kowloon, Hong Kong
Tel: 852.2428.0008
Fax: 852.2401.2105

Serial System (HK) Ltd
2301 Nanyang Plaza
57 Hung To Road, Kwun Tong
Kowloon, Hong Kong
Tel: 852.2995.7538
Fax: 852.2950.0386

India
Bangalore
Spike Technologies India Private Ltd
951, Vijayalakshmi Complex,
2nd Floor, 24th Main,
J P Nagar II Phase,
Bangalore, India 560078
♦ Tel: 91.80.664.5530
Fax: 91.80.664.9748

Israel
Tel Aviv
Eastronics Ltd
11 Rozanis Street
P.O. Box 39300
Tel Aviv 61392
Tel: 972.3.6458777
Fax: 972.3.6458666

Japan
Tokyo
Daito Electron
Sogo Kojimachi No.3 Bldg
1-6 Kojimachi
Chiyoda-ku, Tokyo 102-8730
Tel: 81.3.3264.0326
Fax: 81.3.3261.3984

Global Electronics Corporation
Nichibei Time24 Bldg. 35 Tansu-cho
Shinjuku-ku, Tokyo 162-0833
Tel: 81.3.3260.1411
Fax: 81.3.3260.7100
Technical Center
Tel: 81.471.43.8200

Marubeni Solutions
1-26-20 Higashi
Shibuya-ku, Tokyo 150-0001
Tel: 81.3.5778.8662
Fax: 81.3.5778.8669

Shinki Electronics
Myuru Daikanyama 3F
3-7-3 Ebisu Minami
Shibuya-ku, Tokyo 150-0022
Tel: 81.3.3760.3110
Fax: 81.3.3760.3101

Yokohama-City
Innotech
2-15-10 Shin Yokohama
Kohoku-ku
Yokohama-City, 222-8580
Tel: 81.45.474.9037
Fax: 81.45.474.9065

Macnica Corporation
Hakusan High-Tech Park
1-22-2 Hadusan, Midori-Ku,
Yokohama-City, 226-8505
Tel: 81.45.939.6140
Fax: 81.45.939.6141

The Netherlands
Eindhoven
Acal Nederland b.v.
Beatrix de Rijkweg 8
5657 EG Eindhoven
Tel: 31.40.2.502602
Fax: 31.40.2.510255

Switzerland
Brugg
LSI Logic Sulzer AG
Mattenstrasse 6a
CH 2555 Brugg
Tel: 41.32.3743232
Fax: 41.32.3743233

Taiwan
Taipei
Avnet-Mercuries Corporation, Ltd
14F, No. 145,
Sec. 2, Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2516.7303
Fax: 886.2.2505.7391

Lumax International Corporation, Ltd
7th Fl., 52, Sec. 3
Nan-Kang Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2788.3656
Fax: 886.2.2788.3568

Prospect Technology Corporation, Ltd
4Fl., No. 34, Chu Luen Street
Taipei, Taiwan, R.O.C.
Tel: 886.2.2721.9533
Fax: 886.2.2773.3756

Wintech Microeletronics Co., Ltd
7F., No. 34, Sec. 3, Pateh Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2579.5858
Fax: 886.2.2570.3123

United Kingdom
Maidenhead
Azzurri Technology Ltd
16 Grove Park Business Estate
Waltham Road
White Waltham
Maidenhead, Berkshire SL6 3LW
Tel: 44.1628.826826
Fax: 44.1628.829730

Milton Keynes
Ingram Micro (UK) Ltd
Garamonde Drive
Wymbush
Milton Keynes
Buckinghamshire MK8 8DF
Tel: 44.1908.260422

Swindon
EBV Elektronik
12 Interface Business Park
Bincknoll Lane
Wootton Bassett,
Swindon, Wiltshire SN4 8SY
Tel: 44.1793.849933
Fax: 44.1793.859555

♦ Sales Offices with Design Resource Centers