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GENERAL SEMICONDUCTOR®

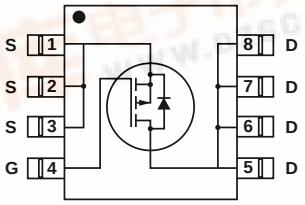
GF4435

P-Channel Enhancement-Mode MOSFET

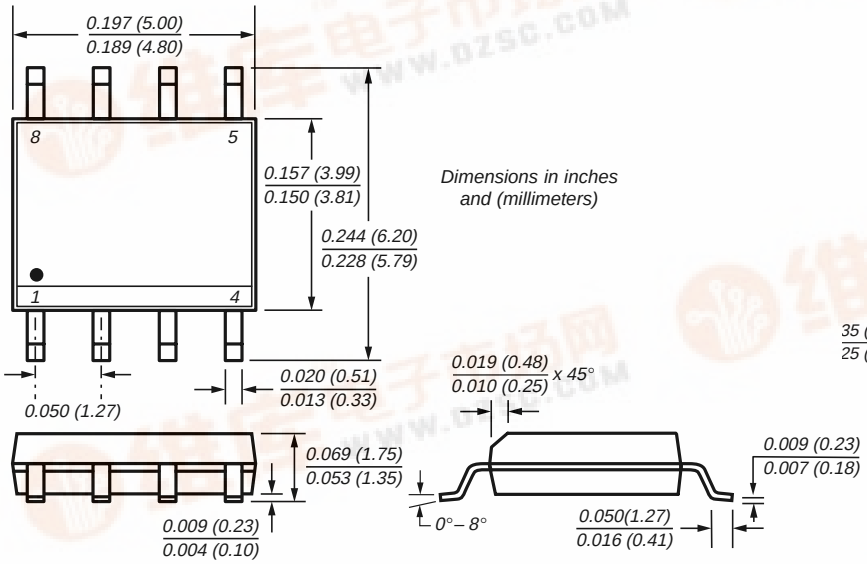
V_{DS} −30V $R_{DS(ON)}$ 20mΩ I_D −8.0A

TRENCH GENFET™

New Product

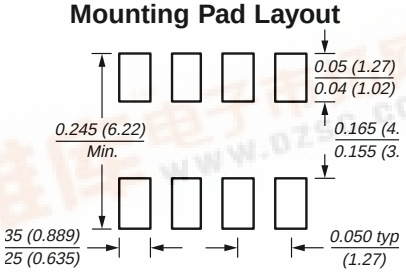


SO-8



Dimensions in inches and (millimeters)

Mounting Pad Layout



Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency
- High temperature soldering in accordance with CECC802/Reflow guaranteed

Mechanical Data

Case: SO-8 molded plastic body

Terminals: Leads solderable per MIL-STD-750, Method 2026

Mounting Position: Any

Weight: 0.5g

Packaging Codes/Options:
5B/2.5K per reel, 12.5K/carton

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current		I_D	–8.0	A
Pulsed Drain Current		I_{DM}	–50	
Maximum Power Dissipation	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Maximum Junction-to-Ambient(1)		$R_{\theta JA}$	50	°C/W

Notes: (1) Surface Mounted on FR4 Board, t ≤ 10 sec.

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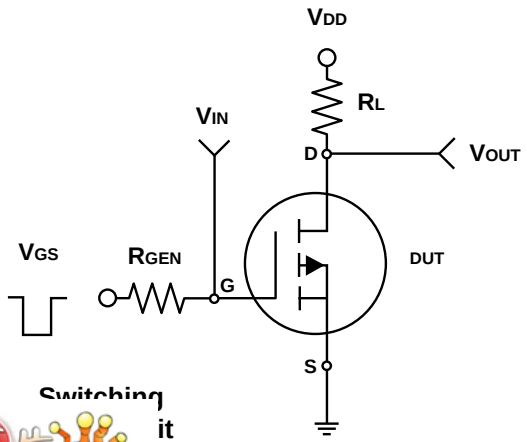
Electrical Characteristics (T_J = 25°C unless otherwise noted)

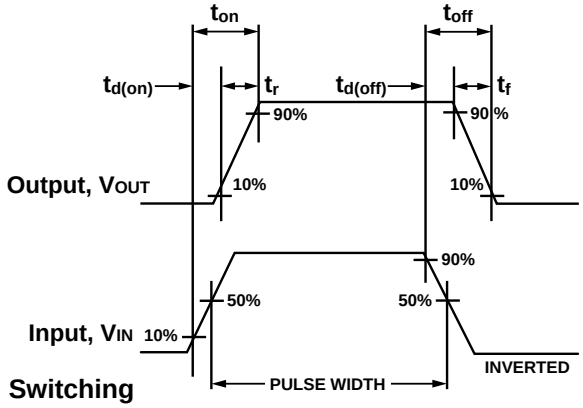
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250µA	–1.0		–3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30V, V_{GS} = 0V			–1.0	µA
On-State Drain Current[1]	$I_{D(on)}$	V_{DS} ≥ –5V, V_{GS} = –10V	–40			A
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = –250µA	–30			V
Drain-Source On-State Resistance[1]	$R_{DS(on)}$	V_{GS} = –10V, I_D = –8.0A		15.3	20	mΩ
		V_{GS} = –4.5V, I_D = –5.0A		25.3	35	
Forward Transconductance[1]	g_{fs}	V_{DS} = –15V, I_D = –8.0A		22		S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = –15V, V_{GS} = –10V I_D = –4.6A		54	60	nC
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}			10.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –15V, R_L = 15Ω I_D ≈ –1A, V_{GEN} = –10V R_G = 6Ω		24	30	ns
Rise Time	t_r			12	30	
Turn-Off Delay Time	$t_{d(off)}$			78	120	
Fall Time	t_f			37	80	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = –15V f = 1.0MHz		2520		pF
Output Capacitance	C_{oss}			490		
Reverse Transfer Capacitance	C_{rss}			335		
Source-Drain Diode						
Maximum Diode Forward Current	I_S				–2.1	A
Diode Forward Voltage	V_{SD}	I_S = –2.1A, V_{GS} = 0V		–0.75	–1.2	V

Note:
(1) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%



Switching

it



Switching Waveforms

P-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

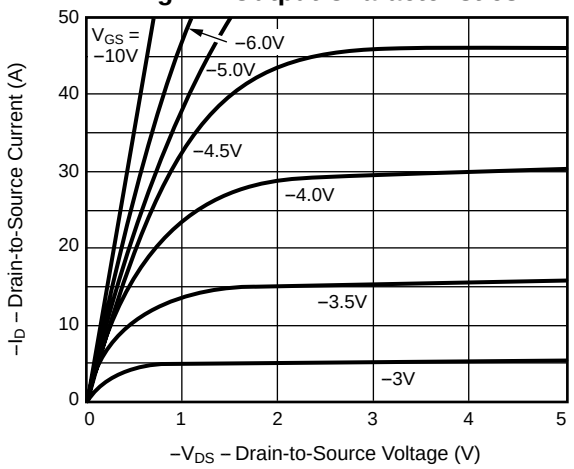


Fig. 2 – Transfer Characteristics

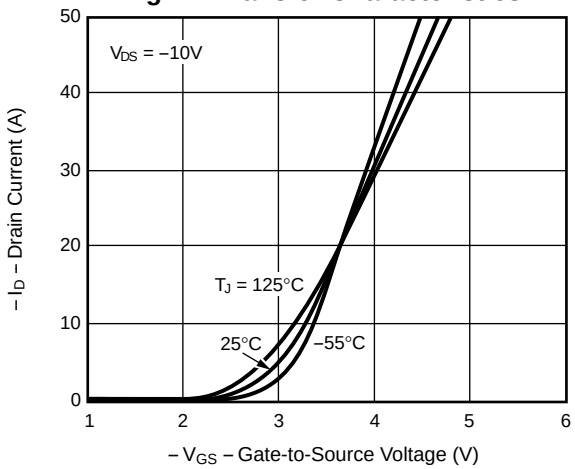


Fig. 3 – Threshold Voltage vs. Temperature

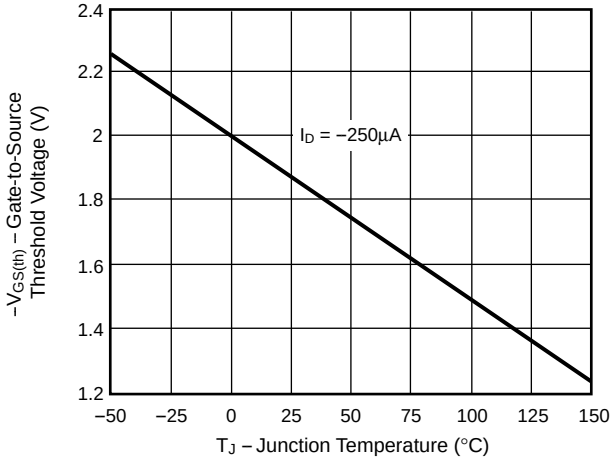


Fig. 4 – On-Resistance vs. Drain Current

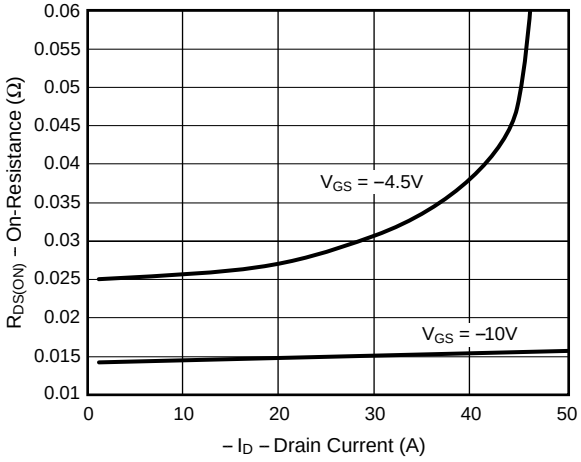


Fig. 5 – On-Resistance vs. Junction Temperature

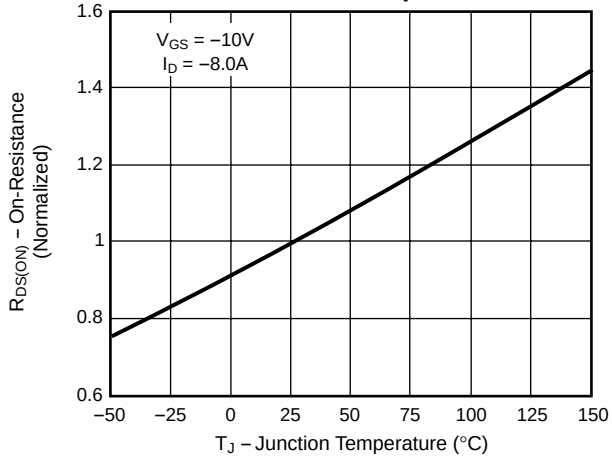
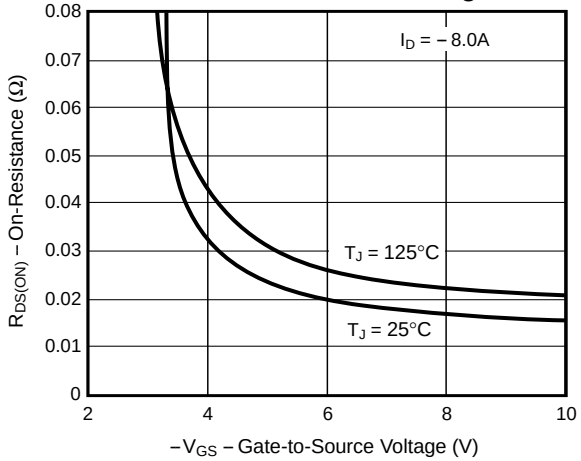


Fig. 6 – On-Resistance vs. Gate-to-Source Voltage



P-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 7 – Gate Charge

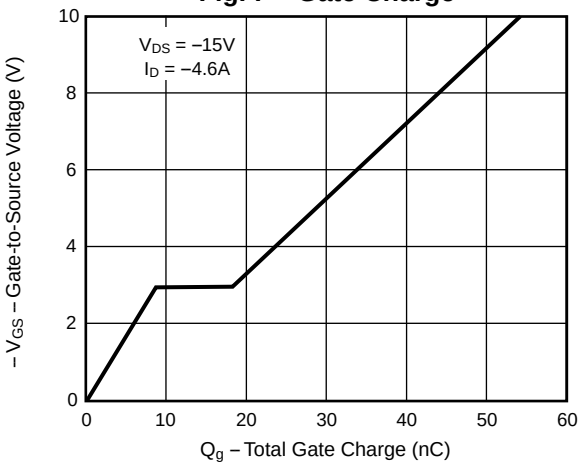


Fig. 8 – Capacitance

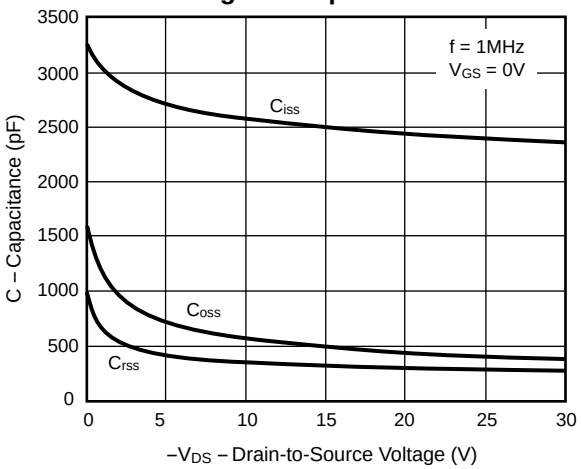


Fig. 9 – Source-Drain Diode Forward Voltage

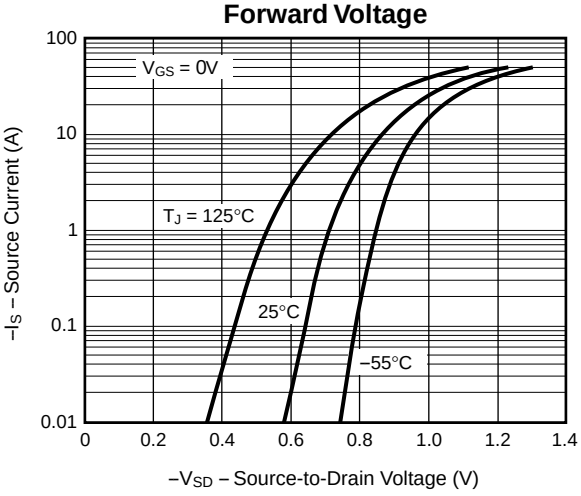


Fig. 10 – Breakdown Voltage vs. Junction Temperature