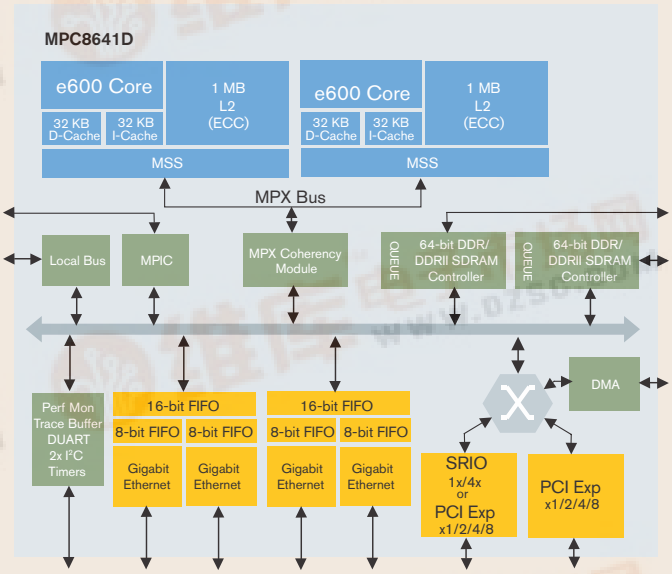
High-Performance Processors

MPC8641D Dual-Core PowerPC® Processor

Based on the e600 PowerPC® system-on-chip (SoC) platform, Freescale's MPC8641D dual-core processor is engineered to deliver breakthrough performance, connectivity and integration for embedded networking, telecom, military, storage and pervasive computing applications. The MPC8641D combines two e600 cores—each designed to deliver greater than 1.5 GHz performance. Two 1 MB L2 caches (four times more L2 cache than available from current single-core MPC74xx PowerPC processors) and dual AltiVec™ vector processing engines provide additional performance acceleration.



Note: A pin-for-pin compatible single-core implementation of the dual-core device is also available called the MPC8641. This device offers the same level of bus and interface integration, but it includes only one e600 PowerPC core.

One of the significant advantages of the MPC8641D is the fully integrated MPX bus that can run three to four times faster than an external MPX bus. Because MPX bus speed is proportional to memory bandwidth and inversely proportional to memory latency, this integrated bus has the potential to provide a huge performance increase to applications limited by either condition—relieving system bottlenecks. In addition, the MPC8641D features an integrated dual-memory controller that provides support for both DDR and DDRII memories, providing more bandwidth and reduced latency during memory accesses.

In addition to its performance enhancements, the highly integrated MPC8641D can replace multiple devices on the line card, resulting in huge savings in board cost and space. In many existing applications, two processors run in symmetric multiprocessing (SMP) mode connected to a system controller by a system bus. These three separate chips can be replaced by one MPC8641D device. With its on-chip, high-speed interfaces, including the standard RapidIO® fabric interface, PCI Express interfaces and Gigabit Ethernet interfaces, the MPC8641D also reduces the bridging/control devices on a board.

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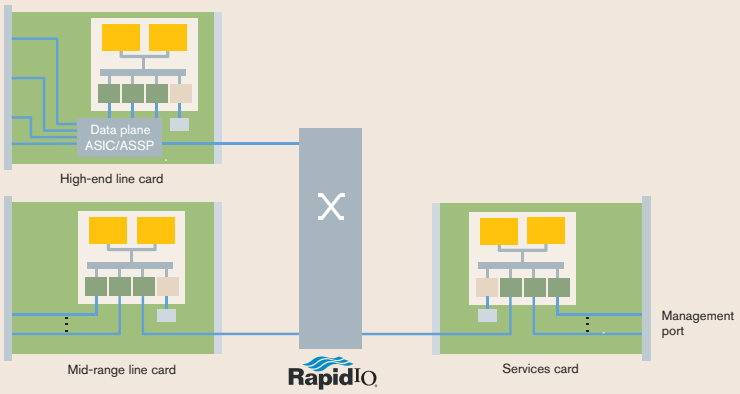
SYSTEM EXAMPLE USING THE MPC8641D PROCESSOR



MPC8641D Processor Highlights	
CPU Speeds (internal)	> At least 1.5 GHz per e600 core
MPX Bus (integrated)	> Up to 667 MHz, 64 bits
L1 Cache (integrated)	> 32 KB instruction, 32 KB data per core
L2 Cache (integrated)	> 1 MB per core with optional ECC
Package	> High-thermal coefficient of expansion (HiTCE) ceramic package
Process Technology	> 90 nm silicon on insulator (SOI)
Execution Units	> Integer (4), floating-point, AltiVec (4), branch, load/store per core
RapidIO Interface	> 1x/4x serial at Gbaud/lane intervals of 1.25, 2.5 and 3.125 > DMA and message-based programming models > Message unit supports SARing up to 4 KB messages into 256-byte packets > Hardware-based error recovery
PCI Express Interface	> One or two 1x/4x/8x serial at 2.5 Gbaud/lane > Configurable as root complex or endpoint > Maximum supported packet payload size is 256 bytes
Ethernet Interface	> 4 10/100/1000 Ethernet controllers > Supports MII, RMII, GMII, RGMII, TBI and RTBI > Accelerates TCP/IP stack checksum operations > 64 receive queues and 8 transmit queues per GMAC with QoS features > Classification and filtering capabilities > High-efficiency FIFO mode for ASIC connectivity
Memory Controller	> Supports dual 64-bit DDR and DDRII with up to 667 MHz data rate with ECC
DMA Controller	> 4 channels
Multiprocessor Interrupt Controller	> Four inter-core messaging interrupts > Steering of interrupts to either core
Local Bus	> 32-bit multiplexed address/data

The MPC8641D processor provides extensive application flexibility for developers, offering various options for assigning distinct processing resources to distinct tasks that need guaranteed performance.

Card 1: A high-end line card uses an ASIC or ASSP for the data path and the MPC8641D for control plane. The two cores can operate in SMP mode, or two separate operating systems may be used for separate control plane tasks, such as off-loading security, classification and quality-of-service (QoS) tasks from the data plane.

Card 2: A mid-range line card uses the MPC8641D to implement both the control and data plane and can be organized in a variety of ways, including splitting functionality directionally (one core per direction) or splitting functionality vertically (one core for handling data plane, one for control plane).

Card 3: A service card, leveraging the MPC8641D, supports a new feature set in a centralized manner, receiving traffic from all line cards—fast processing time is key. The RapidIO port connects to the fabric and the Gigabit Ethernet ports implement a management interface.

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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