



# G8870

## Microcircuits

### CMOS DTMF Integrated Receiver

#### Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

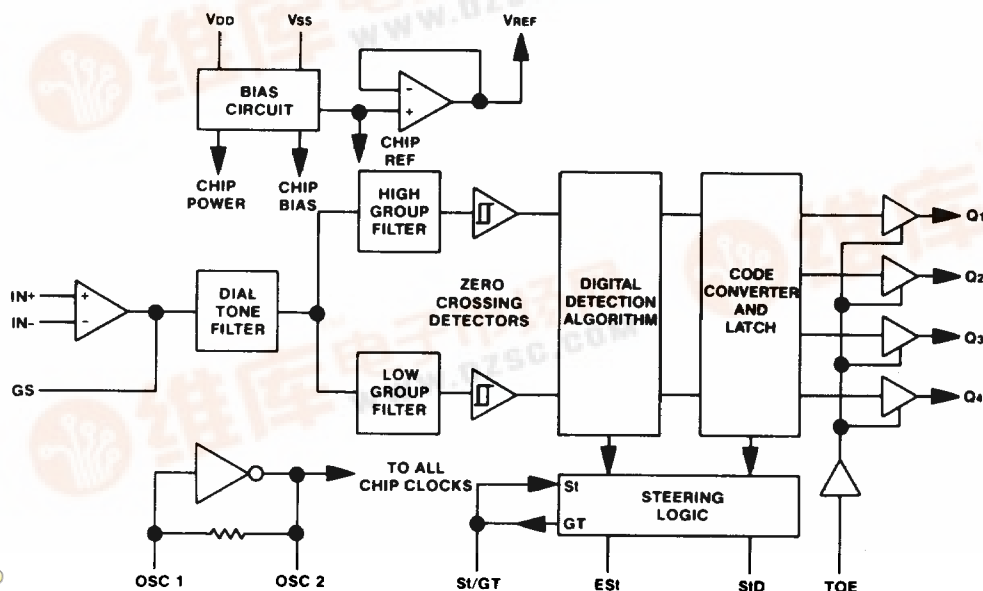
#### Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

#### General Description

The GTE G8870 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

#### Block Diagram



**Absolute Maximum Ratings: (Note 1)**

| Parameter                      | Symbol | Value             |
|--------------------------------|--------|-------------------|
| Power Supply Voltage (VDD-VSS) | VDD    | 6.0V Max          |
| Voltage on any Pin             | Vdc    | VSS-0.3, VDD+0.3  |
| Current on any Pin             | IDD    | 10 mA Max         |
| Operating Temperature          | TA     | -40° C to +85° C  |
| Storage Temperature            | TS     | -65° C to +150° C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

**Notes:**

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

**DC Characteristics:** All voltages referenced to VSS unless otherwise noted. VDD = 5.0V, VSS = 0V, TA = 25° C.

| Parameter                          | Symbol                           | Min  | Typ | Max  | Units | Test Conditions            |
|------------------------------------|----------------------------------|------|-----|------|-------|----------------------------|
| Operating Supply Voltage           | VDD                              | 4.75 |     | 5.25 | V     |                            |
| Operating Supply Current           | IDD                              |      | 3.0 | 7.0  | mA    |                            |
| Power Consumption                  | PO                               |      | 15  | 35   | mW    | f = 3.579 MHz; VDD = 5.0V  |
| Low Level Input Voltage            | VIL                              |      |     | 1.5  | V     |                            |
| High Level Input Voltage           | VIH                              | 3.5  |     |      | V     |                            |
| Input Leakage Current              | I <sub>IH</sub> /I <sub>IL</sub> |      |     | 0.1  | μA    | VIN = VSS or VDD (Note 11) |
| Pull Up (Source) Current on TOE    | ISO                              |      | 6.5 | 15.0 | μA    | TOE = 0 V                  |
| Input Impedance, Signal Inputs 1,2 | RIN                              | 8    | 10  |      | Meg Ω | @ 1KHz                     |
| Steering Threshold Voltage         | VTst                             | 2.2  |     | 2.5  | V     |                            |
| Low Level Output Voltage           | VOL                              |      |     | 0.03 | V     | No Load                    |
| High Level Output Voltage          | VOH                              | 4.97 |     |      | V     | No Load                    |
| Output Low (Sink) Current          | IOL                              | 1.0  | 2.5 |      | mA    | VOUT = 0.4 V               |
| Output High (Source) Current       | IOH                              | 0.4  | 0.8 |      | mA    | VOUT = 4.6 V               |
| Output Voltage                     | VREF                             | VREF | 2.4 | 2.7  | V     | No Load                    |
| Output Resistance                  |                                  | ROR  |     | 10   | KΩ    |                            |

**Operating Characteristics:** All voltages referenced to VSS unless otherwise noted. VDD = 5.0V, VSS = 0V, TA = 25° C.

**Gain Setting Amplifier**

| Parameter                      | Symbol | Min | Typ | Max  | Units | Test Conditions     |
|--------------------------------|--------|-----|-----|------|-------|---------------------|
| Input Leakage Current          | IIN    |     |     | ±100 | nA    | VSS < VIN < VDD     |
| Input Resistance               | RIN    | 10  |     |      | MΩ    |                     |
| Input Offset Voltage           | Vos    |     |     | ±25  | mV    |                     |
| Power Supply Rejection         | PSRR   | 50  |     |      | dB    | 1 KHz (Note 12)     |
| Common Mode Rejection          | CMRR   | 55  |     |      | dB    | -3.0 V < VIN < 3.0V |
| DC Open Loop Voltage Gain      | AVOL   | 60  |     |      | dB    |                     |
| Open Loop Unity Gain Bandwidth | fc     | 1.2 | 1.5 |      | MHz   |                     |
| Output Voltage Swing           | Vo     | 3.5 |     |      | Vp-p  | RL ≥ 100KΩ to VSS   |
| Tolerable Capacitive Load (GS) | CL     |     |     | 100  | pF    |                     |
| Tolerable Resistive Load (GS)  | RL     |     |     | 50   | KΩ    |                     |
| Common Mode Range              | Vcm    | 2.5 |     |      | Vp-p  | No Load             |



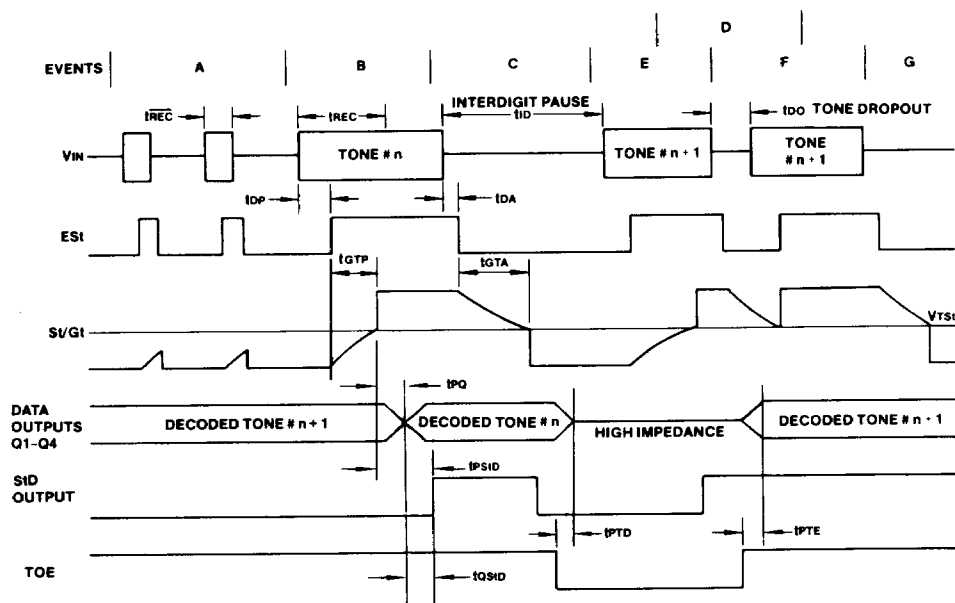
**AC Characteristics:** All voltages referenced to VSS unless otherwise noted. VDD = 5.0V, VSS = 0V, TA = 25° C, fCLK = 3.579545 MHz using test circuit (Fig. 1).

| Parameter                                                    | Symbol             | Min    | Typ    | Max       | Units | Notes                                                                      |
|--------------------------------------------------------------|--------------------|--------|--------|-----------|-------|----------------------------------------------------------------------------|
| Valid Input Signal Levels<br>(each tone of composite signal) |                    | -29    |        | +1        | dBm   | 1,2,3,4,5,8                                                                |
|                                                              |                    | 27.5   |        | 869       | mVRMS |                                                                            |
| Positive Twist Accept                                        |                    |        |        | 10        | dB    | 2,3,4,8                                                                    |
| Negative Twist Accept                                        |                    |        |        | 10        | dB    |                                                                            |
| Freq. Deviation Accept Limit                                 |                    |        |        | 1.5%±2 Hz | Nom.  | 2,3,5,8,10                                                                 |
| Freq. Deviation Reject Limit                                 |                    | ±3.5%  |        |           | Nom.  | 2,3,5                                                                      |
| Third Tone Tolerance                                         |                    | -25    | -16    |           | dB    | 2,3,4,5,8,9,13,14                                                          |
| Noise Tolerance                                              |                    |        | -12    |           | dB    | 2,3,4,5,6,8,9                                                              |
| Dial Tone Tolerance                                          |                    | +18    | +22    |           | dB    | 2,3,4,5,7,8,9                                                              |
| Tone Present Detection Time                                  | tDP                | 5      | 8      | 14        | mS    | Refer to<br>Timing Diagram                                                 |
| Tone Absent Detection Time                                   | tDA                | 0.5    | 3      | 8.5       | mS    |                                                                            |
| Min. Tone Duration Accept                                    | tREC               |        |        | 40        | mS    | (User Adjustable)<br>Times shown are<br>obtained with<br>circuit in Fig. 1 |
| Max. Tone Duration Reject                                    | tREC               | 20     |        |           | mS    |                                                                            |
| Min. Interdigit Pause Accept                                 | tID                |        |        | 40        | mS    |                                                                            |
| Max. Interdigit Pause Reject                                 | tDO                | 20     |        |           | mS    |                                                                            |
| Propagation Delay (St to Q)                                  | tPQ                |        | 6      | 11        | μS    | TOE = VDD                                                                  |
| Propagation Delay (St to StD)                                | tPSID              |        | 9      |           | μS    |                                                                            |
| Output Data Set Up (Q to StD)                                | tQStD              | 4.0    |        |           | μS    |                                                                            |
| Propagation Delay<br>(TOE to Q)                              | Enable.            | tPTE   | 50     | 60        | nS    | RL = 10KΩ<br>CL = 50pF                                                     |
|                                                              | Disable            | tPTD   | 300    |           | nS    |                                                                            |
| Crystal/Clock Frequency                                      | fCLK               | 3.5759 | 3.5795 | 3.5831    | MHz   |                                                                            |
| Clock Output<br>(OSC2)                                       | Capacitive<br>Load | CLO    |        | 30        | pF    |                                                                            |

# NOTES:

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.



**Timing Diagram**

**Explanation of Events**

- A) Tone bursts detected, tone duration invalid, outputs not updated.
- B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
- C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
- D) Outputs switched to high impedance state.
- E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
- F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
- G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

**Explanation of Symbols**

- VIN DTMF composite input signal.
- EST Early Steering Output. Indicates detection of valid tone frequencies.
- St/GT Steering input/guard time output. Drives external RC timing circuit.
- Q1-Q4 4-bit decoded tone output.
- StD Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
- TOE Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
- tREC Maximum DTMF signal duration not detected as valid.
- tREC Minimum DTMF signal duration required for valid recognition.
- tID Minimum time between valid DTMF signals.
- tDO Maximum allowable drop-out during valid DTMF signal.
- tDP Time to detect the presence of valid DTMF signals.
- tDA Time to detect the absence of valid DTMF signals.
- tGTP Guard time, tone present.
- tGTA Guard time, tone absent.



## Functional Description

The GTE G8870 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP or 20-pin PLCC package configuration. The G8870's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

## Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

## Decoder Section

The G8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (EST). Any subsequent loss of signal condition will cause EST to fall.

## Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by EST. A logic high on EST causes Vc (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (EST remains high) for the validation period (tgTP), Vc reaches the threshold (VTS) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives Vc to VDD. GT continues to drive high as long as EST remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by

raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

## Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$TREC = TDP + tgTP$$

$$tgTP \approx 0.67 RC$$

The value of TDP is a parameter of the device and TREC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1  $\mu$ F is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a TREC of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (tgTP) and tone-absent (tgTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing TREC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short TREC with a long too would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

## Input Configuration

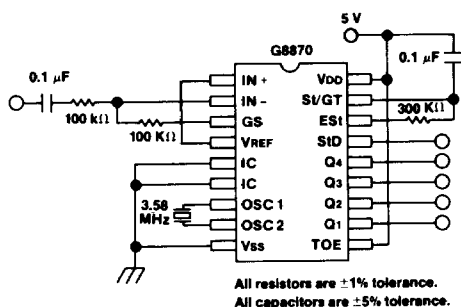
The input arrangement of the G8870 provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and VREF biasing the input at  $\frac{1}{2}VDD$ . Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

**Pin Function Table**

| Name  | Description                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                  |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| IN+   | Non-inverting input                                                                                                                                                                                                                                                                                                                                                                                    | Connections to the front-end differential amplifier                              |
| IN-   | Inverting input                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                  |
| GS    | Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.                                                                                                                                                                                                                                                                                           |                                                                                  |
| VREF  | Reference voltage output (nominally $V_{DD}/2$ ). May be used to bias the inputs at mid-rail.                                                                                                                                                                                                                                                                                                          |                                                                                  |
| IC    | Internal connection. Must be tied to Vss.                                                                                                                                                                                                                                                                                                                                                              |                                                                                  |
| IC    | Internal connection. Must be tied to Vss.                                                                                                                                                                                                                                                                                                                                                              |                                                                                  |
| OSC1  | Clock input                                                                                                                                                                                                                                                                                                                                                                                            | 3.579545 MHz crystal connected between these pins completes internal oscillator. |
| OSC2  | Clock output                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                  |
| Vss   | Negative power supply (Normally connected to 0V).                                                                                                                                                                                                                                                                                                                                                      |                                                                                  |
| TOE   | Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.                                                                                                                                                                                                                                                                                                             |                                                                                  |
| Q1    | Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)                                                                                                                                                                                                                                                                          |                                                                                  |
| Q2    |                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                  |
| Q3    |                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                  |
| Q4    |                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                  |
| StD   | Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below $V_{TSt}$ .                                                                                                                                                                                                   |                                                                                  |
| Est   | Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause Est to return to a logic low.                                                                                                                                                                               |                                                                                  |
| St/GT | Steering input/guard time output (bidirectional). A voltage greater than $V_{TSt}$ detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than $V_{TSt}$ frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of Est and the voltage on St. (See Fig. 2.) |                                                                                  |
| VDD   | Positive power supply                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                  |


**Figure 1. Single Ended Input Configuration**

| FLOW | HIGH | KEY | TOE | Q4 | Q3 | Q2 | Q1 |
|------|------|-----|-----|----|----|----|----|
| 697  | 1209 | 1   | H   | 0  | 0  | 0  | 1  |
| 697  | 1336 | 2   | H   | 0  | 0  | 1  | 0  |
| 697  | 1477 | 3   | H   | 0  | 0  | 1  | 1  |
| 770  | 1209 | 4   | H   | 0  | 1  | 0  | 0  |
| 770  | 1336 | 5   | H   | 0  | 1  | 0  | 1  |
| 770  | 1477 | 6   | H   | 0  | 1  | 1  | 0  |
| 852  | 1209 | 7   | H   | 0  | 1  | 1  | 1  |
| 852  | 1336 | 8   | H   | 1  | 0  | 0  | 0  |
| 852  | 1477 | 9   | H   | 1  | 0  | 0  | 1  |
| 941  | 1336 | 0   | H   | 1  | 0  | 1  | 0  |
| 941  | 1209 | *   | H   | 1  | 0  | 1  | 1  |
| 941  | 1477 | #   | H   | 1  | 1  | 0  | 0  |
| 697  | 1633 | A   | H   | 1  | 1  | 0  | 1  |
| 770  | 1633 | B   | H   | 1  | 1  | 1  | 0  |
| 852  | 1633 | C   | H   | 1  | 1  | 1  | 1  |
| 941  | 1633 | D   | H   | 0  | 0  | 0  | 0  |
| —    | —    | ANY | L   | Z  | Z  | Z  | Z  |

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

**Figure 2. Functional Decode Table**

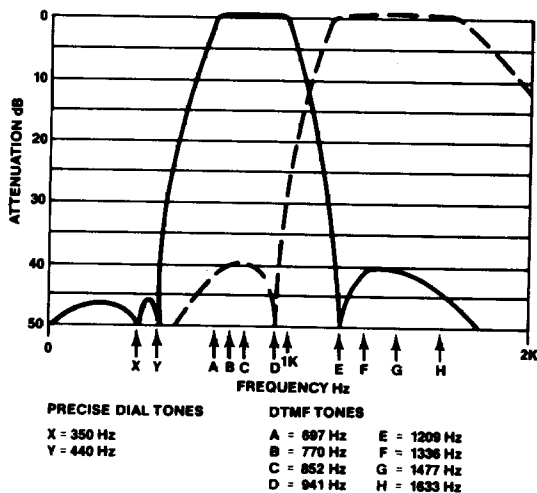


Figure 3. Typical Filter Characteristic

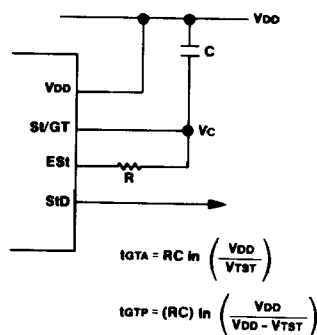


Figure 4. Basic Steering Circuit

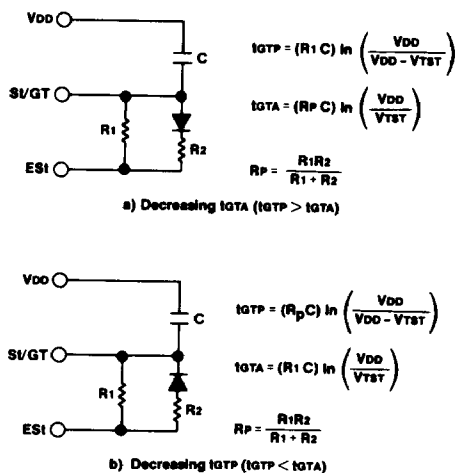
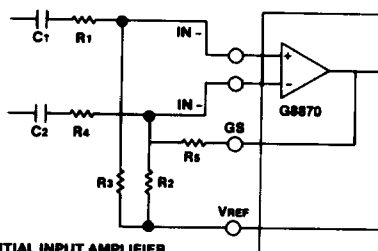


Figure 5. Guard Time Adjustment


**DIFFERENTIAL INPUT AMPLIFIER**

$C_1 = C_2 = 10 \text{ nF}$   
 $R_1 = R_4 = R_5 = 100 \text{ K}\Omega$   
 $R_2 = 60 \text{ K}\Omega, R_3 = 37.5 \text{ K}\Omega$

$R_3 = \frac{R_2 R_5}{R_2 + R_5}$   
**VOLTAGE GAIN ( $A_v$  dBF)** =  $\frac{R_5}{R_1}$

**INPUT IMPEDANCE**  
 $(Z_{INOFF}) = 2 \sqrt{R_1^2 + \left( \frac{1}{\omega C} \right)^2}$

All resistors are — 1% tolerance.  
 All capacitors are — 5% tolerance.

Figure 6. Differential Input Configuration

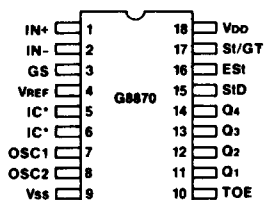


## Pin Function

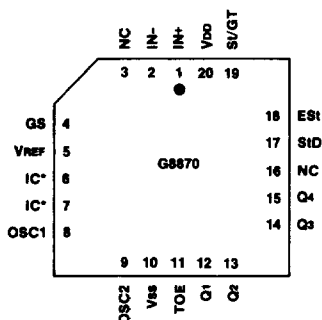
| Pin  | Description               |
|------|---------------------------|
| IN+  | Non-Inverting Input       |
| IN-  | Inverting Input           |
| GS   | Gain Select               |
| IC   | Internal Connection       |
| OSC1 | Clock Input               |
| OSC2 | Clock Output              |
| TOE  | Three-State Output Enable |

| Pin   | Description                     |
|-------|---------------------------------|
| Q1-4  | Three-State Data Outputs        |
| StD   | Delayed Steering Output         |
| ESi   | Early Steering Output           |
| St/GT | Steering Input/Guard Time Input |
| VREF  | Reference Voltage Output        |
| VSS   | Negative Power Supply           |
| VDD   | Positive Power Supply           |

## Pin Configuration



\*CONNECT TO Vss



## Ordering Information

