FUJITSU

AV CMOS SERIES GATE ARRAYS

MB65xxxx MB66xxxx MB67xxxx

T-42-11-09

June 1986
Edition 2.0

DESCRIPTION

The Fujitsu MB65xxxx/MB66xxxx/MB67xxxx family are a series of high performance CMOS gate arrays designed to provide high density, low power, and operating speeds that are comparable to standard bipolar logic. The AV (MB65xxxx) series is an ideal choice for LSI and VLSI applications that require up to 8000 gates, 2304 bits of RAM, 4608 bits of ROM or for bus interface circuits with high-drive requirements. The AVB (MB67xxxx) series include optional 10 mA buffered outputs and input pull-up/pull-down resistors for easy interfacing with bus organized logic.The AVM (MB66xxxx) series of memory arrays include, in addition to the 1.5K, 2.3K, and 4K gates of logic, two basic sizes of static registered memories:

The C4002 and C1502 have up to 2304 bits of RAM organized in an optional by-nine memory configuration that is system compatible with most modern designs. The 2301 has 1024 bits of RAM that may be configured into any by-four multiple from 256-by-4 to 32-by-32.

The AVM memories contain duplicate decoder and address register logic so that they may be split and used as two independent memories without borrowing any of the unit cells.

All AV, AVB and AVM arrays use the same basic internal cell structure and common logic Macros.

FEATURES

- 1.4 ns gate delay typical. (2-input NAND gate, F.O.=2)
- Static RAM or ROM on chip.
- Silicon-gate 1.8 micron dual metal.
- 100% automatic placement and routing with guaranteed 90% cell utilization.
- Three-state and bidirectional outputs available.
- High-drive output. Buffers, I_{OL} = 10.0 mA, available.
- Pull-up/pull-down input buffers available.
- Single 5V power supply.
- TTL compatible I/O, CMOS input and Schmitt trigger input.
- Popular CAE workstations supported.
- Over 100 unit cells available for design.
- Predesigned software macros available. (F-Macros).
- Fast turnaround: 5 weeks after final validation.
- Evaluation samples available.
- Extended temperature range available.

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	Device	Part No.	Gates	I/O	Gate Speed	Features
AV-CMOS SERIES	C2600AV	MB654xxx	2640	106	1.4 ns	High Density
	C3900AV	MB653xxx	3900	127	1.4 ns	High Density
	C5000AV	MB652xxx	5022	127	1.4 ns	High Density
	C6600AV	MB651xxx	6664	160	1.4 ns	High Density
	C8000AV	MB650xxx	8000	160	1.4 ns	High Density
AVB-CMOS SERIES	C350AVB	MB675xxx	357	38 (42)[1]	1.4 ns	High-Drive
	C540AVB	MB674xxx	549	48 (50)[1]	1.4 ns	High-Drive
	C850AVB	MB673xxx	852	58 (60)[1]	1.4 ns	High-Drive
	C1200AVB	MB672xxx	1245	68 (68)[1]	1.4 ns	High-Drive
	C1600AVB	MB671xxx	1674	74 (76)[1]	1.4 ns	High-Drive
	C2000AVB	MB670xxx	2052	88 (92)[1]	1.4 ns	High-Drive
AVM-CMOS SERIES	C1502AVM	MB662xxx	1564	107 (109)[2]	1.4 ns	4K ROM/2K RAM [3]
	C2301AVM	MB661xxx	2375	117 (119)[2]	1.4 ns	2K ROM/1K RAM [3]
	C4002AVM	MB660xxx	4087	120 (122)[2]	1.4 ns	4K ROM/2K RAM [3]

Notes:
1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.
2. When ROM is provided.
3. Available options.

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MB66xxxx
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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS [1]

(V_{ss} = 0V.)

Rating	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	V_{ss} - 0.5	-	6.0	volts
Input Voltage	V_I	V_{ss} - 0.5	-	V_{DD} + 0.5	volts
Output Voltage	V_O	V_{ss} - 0.5	-	V_{DD} + 0.5	volts
Output Current [2] AVB	I_{OS}	-80	-	140	mA
Output Current [2] AV, AVM	I_{OS}	-40	-	70	mA
Storage Temperature	T_{STG}	-65 Ceramic	-	150 Ceramic	°C
		-40 Plastic	-	125 Plastic	°C
Bias Temperature	T_{bias}	-40 Ceramic	-	125 Ceramic	°C
		-25 Plastic	-	85 Plastic	°C

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Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions of recommended operation. Exposure to absolute maximum ratings for extended periods may affect device reliability.
2. No more than one output can be shorted at a time and no output can be shorted for more than one second.

RECOMMENDED OPERATING CONDITIONS

(V_{ss} = 0V.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	volts
Input High Voltage	V_{IH}	2.2	-	-	volts
for CMOS Inputs	V_{IH}	V_{DD} x 0.7	-	-	volts
Input Low Voltage	V_{IL}	-	-	0.8	volts
for CMOS Inputs	V_{IL}	-	-	V_{DD} x 0.3	volts
Ambient Temperature	T_A	0	-	70	°C

AV, AVM SERIES CAPACITANCE

(Ta = 25 °C, V_{DD} = V_I = 0 volts, f = 1 MHz.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	C_{IN}	-	-	9	pF
Output Capacitance	C_{OUT}	-	-	9	pF
I/O Pin Capacitance	$C_{I/O}$	-	-	11	pF

AVB SERIES CAPACITANCE

(Ta = 25 °C, V_{DD} = V_I = 0 volts, f = 1 MHz.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance	C_{IN}	-	-	8	pF
Output Capacitance	C_{OUT}	-	-	16	pF
I/O Pin Capacitance	$C_{I/O}$	-	-	21	pF

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Current (Steady state, V_I = 0V or V_{DD})	I_{DDS}	–	–	100	µA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	4.2	–	V_{DD}	volts
for Driver Output (I_{OH} = -0.4 mA)	V_{OH}	4.2	–	V_{DD}	volts
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	V_{ss}	–	0.4	volts
for Driver Output (I_{OL} = 10.0 mA)	V_{OL}	V_{ss}	–	0.5	volts
Input High Voltage	V_{IH}	2.2	–	–	volts
for CMOS Input	V_{IH}	V_{DD} x 0.7	–	–	volts
Input Low Voltage	V_{IL}	–	–	0.8	volts
for CMOS Input	V_{IL}	–	–	V_{DD} x 0.3	volts
Input Leakage Current (V_I = 0 – V_{DD})	I_{LI}	-10	–	10	µA
Input Leakage Current (3-state, V_I = 0 – V_{DD})	I_{LZ}	-10	–	10	µA
Input Pull-Up/Down Resistor (Pull up: V_{IL} = 0V, Pull down V_{IH} = V_{DD})	RP	25	50	100	kΩ

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AC CHARACTERISTICS DELAY MULTIPLIERS FOR PRE-LAYOUT SIMULATION

(See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Propagation Delay	t_{pd}				
Enable Time	t_{PZL}/t_{PZH}				
Disable Time	t_{PLZ}/t_{PHZ}	Typ x 0.45		Typ x 1.6	ns
Set-up Time	t_{SD}				
Hold Time	t_{HD}				
Pulse Width	t_{CW}				

AC CHARACTERISTICS DELAY MULTIPLIERS FOR POST-LAYOUT SIMULATION

(See AV Series Gate Arrays Unit Cell Library)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
–	–	Typ x 0.50	–	Typ x 1.55	ns

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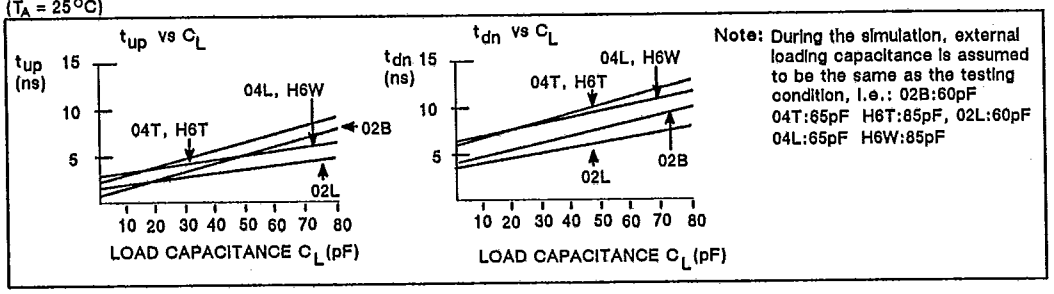
OUTPUT BUFFER PROPAGATION DELAY CHARACTERISTIC
(T_A = 25°C)



Note: During the simulation, external loading capacitance is assumed to be the same as the testing condition, i.e.: 02B:60pF
04T:65pF H6T:85pF, 02L:60pF
04L:65pF H6W:85pF

AV AND AVB-CMOS GATE ARRAY CHIP LAYOUT AND ORGANIZATION

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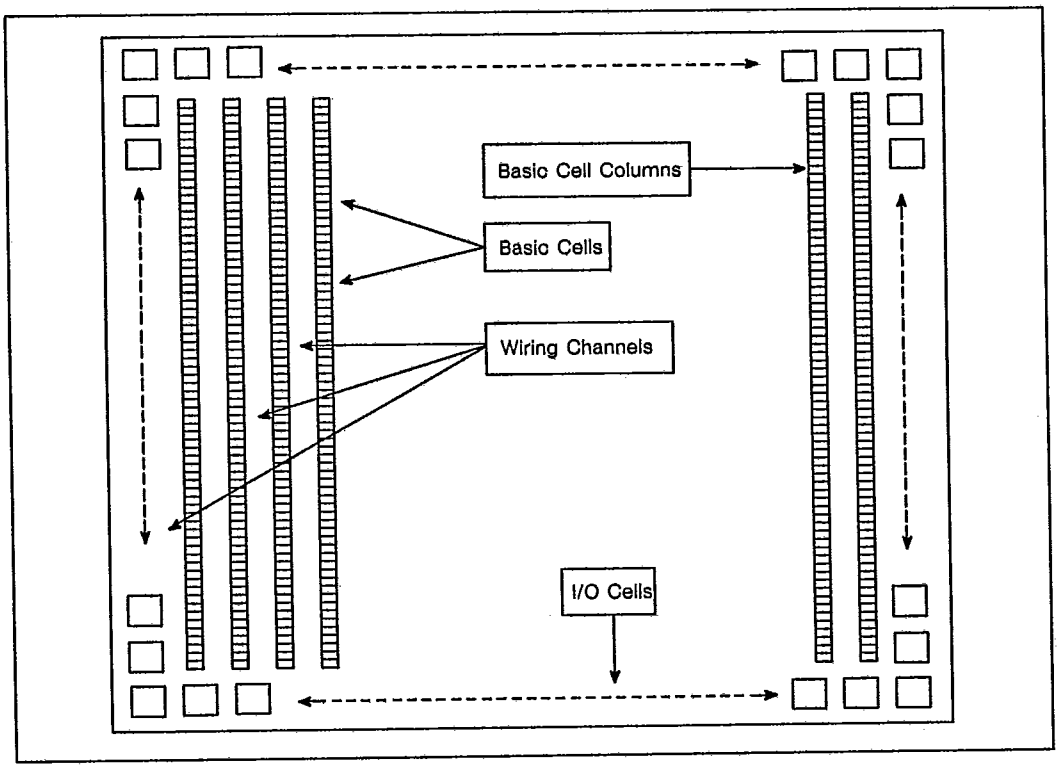
CHIP LAYOUT AV AND AVB SERIES EXCEPT C6600AV AND C8000AV



AV AND AVB ORGANIZATION

Device	Total Basic Cells	Columns	Basic Cells per Column	Total I/O Cells
C350AVB	357	7	51	38 (42)[1]
C540AVB	549	9	61	48 (50)[1]
C850AVB	852	12	71	58 (60)[1]
C1200AVB	1245	15	83	68 (68)[1]
C1600AVB	1674	18	93	74 (76)[1]
C2000AVB	2052	18	114	88 (92)[1]
C2600AV	2640	22	120	106
C3900AV	3900	25	156	127
C5000AV	5022	27	186	127

Note:

1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.

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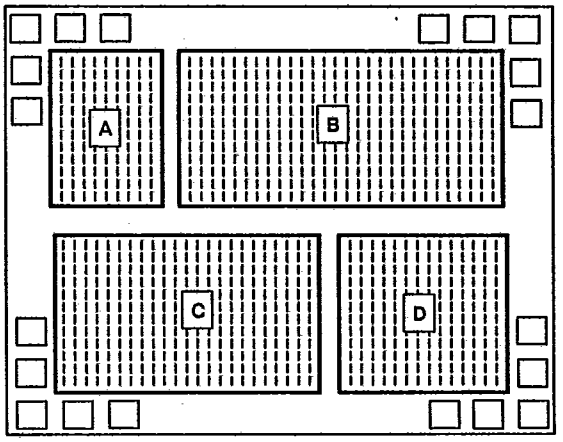
C6600AV, C8000AV AND AVM GATE ARRAY CHIP LAYOUT AND ORGANIZATION

C6600AV, C8000AV CHIP LAYOUT

For C6600AV each block may vary from 1000 to 2000 basic cells.

For C8000AV each block is fixed at 2000 basic cells.

For automatic placement and routing, the maximum basic cells used for each block should not exceed 90% of the total available in that block.



C6600AV, C8000AV ORGANIZATION

Device	Total Basic Cells	Blocks	BC/Block	Rows/Block	Columns/Block	Total I/O Cells
C6600AV	6664	4	1000 – 2000	–	Variable	160
C8000AV	8000	4	2000	100	20	160

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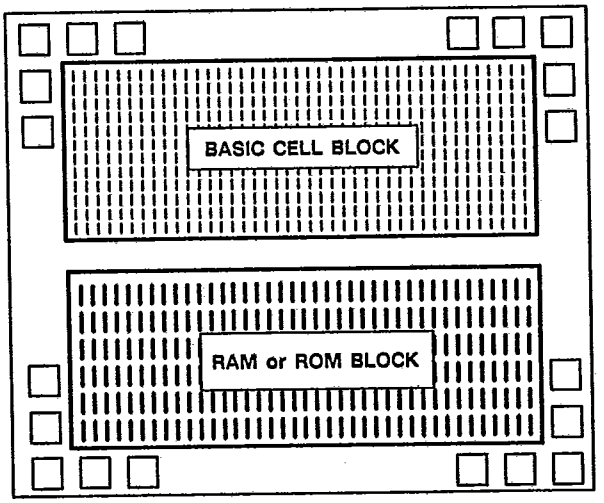
C1502AVM, C2301AVM CHIP LAYOUT

The maximum basic cells used for the basic cell block should not exceed 90% of the total available.

The block is configurable for either 1024 or 2304 total bits organized from 2-bits per word to 32-bits per word, or 9-bits per word to 36-bits per word.

8-bit word sizes and larger (for C2301AVM) or 18-bit word sizes and larger (for C1502AVM) allow division of the RAM block into two separate RAMSs.

ROM can be provided in place of RAM. The ROM block is configurable for either 2048 or 4608 total bits.



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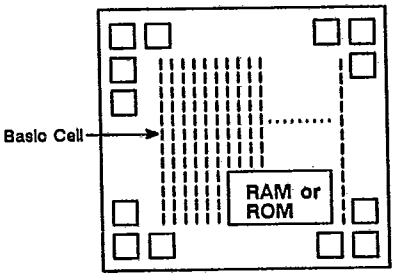
C4002AVM CHIP LAYOUT

For automatic placement and routing the maximum basic cells should not exceed 90% of the total available.

The RAM block is configurable for 2304 total bits organized from 9 bits per word to 36 bits per word.

18-bit word sizes and larger allow division of the RAM block into two separate RAMs.

ROM can be provided in place of RAM. The ROM block is configured for 4608 total bits.



C1502AVM, C2301AVM, C4002AVM ORGANIZATION

Device	Total Basic Cells	Columns	BC/Column	RAM Size	Total I/O Cells
C1502AVM	1564	23	68	2K, 9-bit to 36-bit	107 (109) [1]
C2301AVM	2375	25	95	1K, 4-bit to 32-bit	117 (119) [1]
C4002AVM	4087	6 25	202 115	2K, 9-bit to 36-bit	120 (122) [1]

Note:

1. When ROM is provided.

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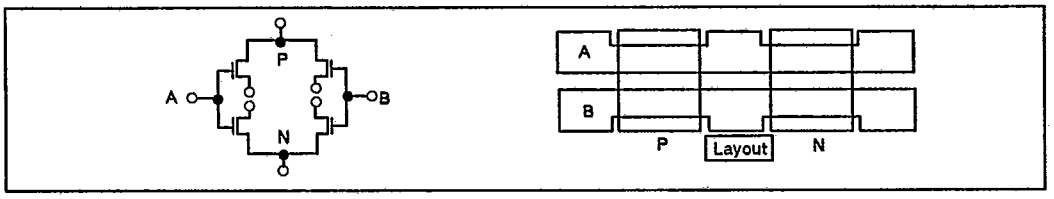
DESIGN COMPONENTS

BASIC CELL

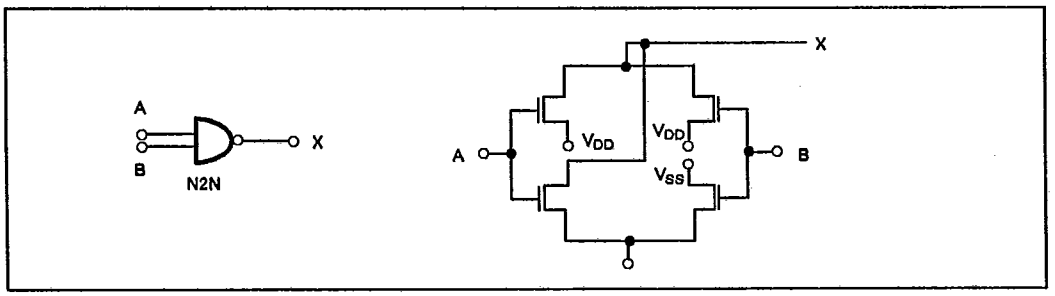
An unprogrammed gate array is an array of basic cells. Thus the "gates" in a gate array are actually the basic cells which will make up final logic. Fujitsu's basic cell contains enough transistors to form a two-input NAND gate.



Unprogrammmed Basic Cell

UNIT CELL

A design is implemented in a gate array by logically combining unit cells from the Fujitsu unit cell library to form the logic. Fujitsu provides unit cells to perform most common logic functions and the designer need only name the unit cells required to form the higher level logic functions of his design.

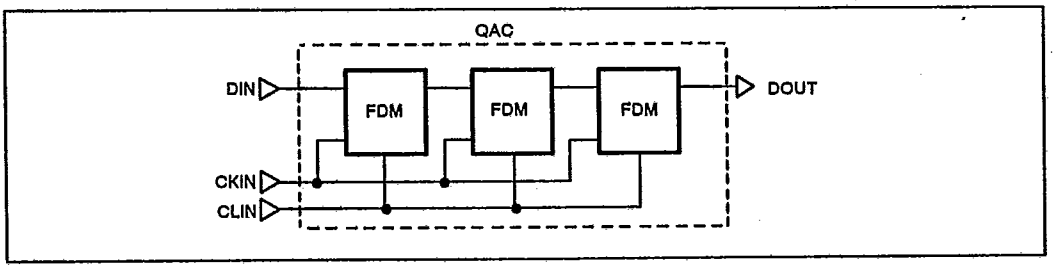


Two-Input NAND Gate Unit Cell (One Basic Cell)

A two-input NAND gate requires only one basic cell to implement. Other unit cells may require as many as 60 or more basic cells. (C47, a counter, requires 68.) Over 100 unit cells are available for design with AV/AVB/AVM-CMOS arrays.

USER MACROS

User Macros are groups of unit cells which perform an identifiable function within the design. It is a user macro because it is defined by the designer. The primary utility of a user macro is that it allows the designer to compose a macro function from unit cells once, then use it any number of times simply by calling it by name.



User Macro QAC is Composed of Three FDM Unit Cells

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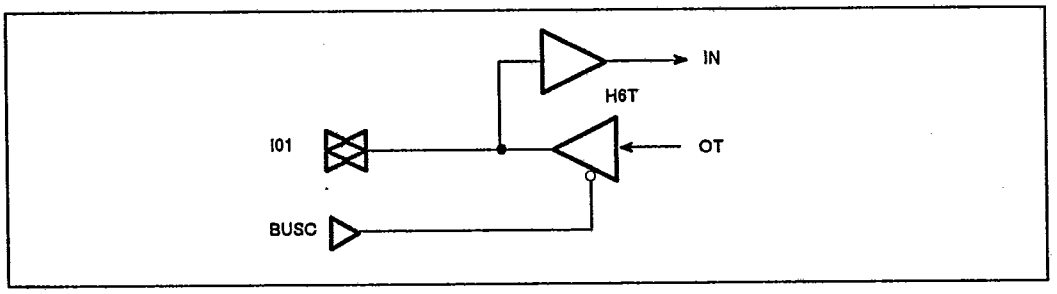
F-MACROS

F-Macros are created and offered by Fujitsu to emulate the function of popular industry-standard TTL devices. They are identical in application to user macros. Using F-Macros, a designer may convert an existing design directly into gate array. For example, the 74LS191 function is emulated by the Fujitsu F191 F-Macro.

I/O Cells

The I/O cells located on the periphery of the gate array chip are programmable to any of the input or output buffers available. The actual location of an I/O buffer on the chip is determined by the location on the chip of the associated circuitry and any pin location requirements that may be in effect.



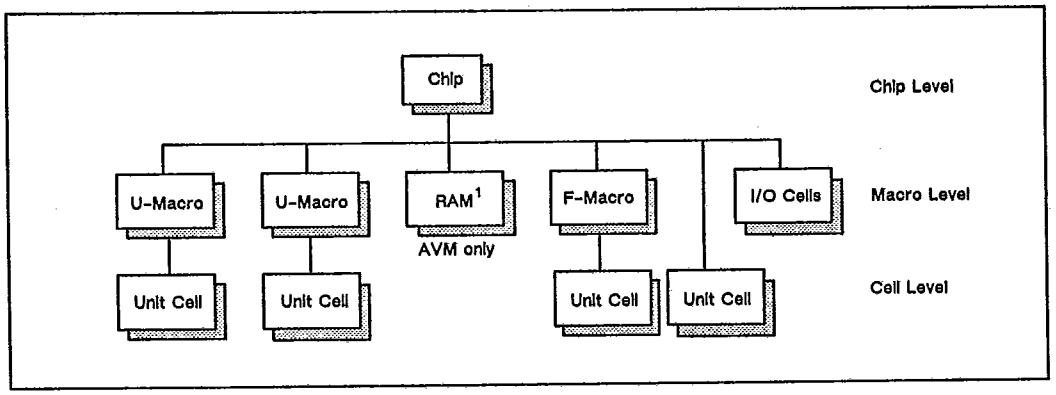
Bidirectional Buffer

DESIGN DESCRIPTION

DESIGN DESCRIPTION

Fujitsu requires only two basic inputs to complete a gate array design: A **Logic Description** and a **Test Description**. The logic description defines the logical function of the circuit to be implemented in the array. The test description defines the electrical operation required.

AV, AVB AND AVM LOGIC HIERARCHY



Note:

1. ROM can be made available in place of RAM.

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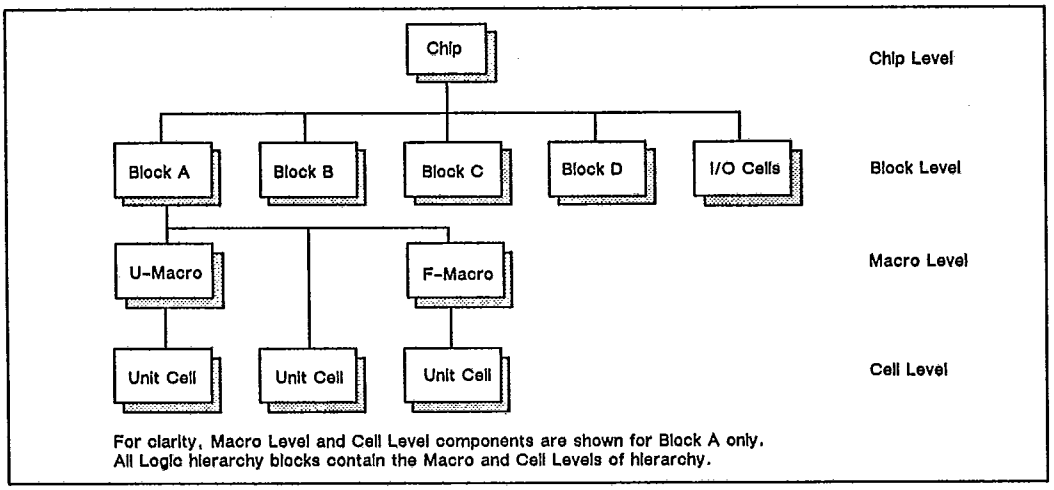
C6600AV, C8000AV LOGIC HIERARCHY



For clarity, Macro Level and Cell Level components are shown for Block A only. All Logic hierarchy blocks contain the Macro and Cell Levels of hierarchy.

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LOGIC DESCRIPTION

The Logic Description, sometimes called a "netlist," calls out the unit cells utilized and their interconnection to form the designer's circuit. Fujitsu uses a proprietary description language, the Fujitsu Logic Description Language (FLDL), to enter the logic description language into the design flow to produce the array design. Designers may prepare their logic description using FLDL or use other description media which Fujitsu will convert to FLDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. In all cases, the design description must follow the fundamental design description structure provided by the logic hierarchy. In many cases Fujitsu will provide turnkey design services.

LOGIC HIERARCHY

The Logic Description is organized into a hierarchy of design components. The logic hierarchy provides the fundamental structure for all logic description inputs and allows a designer to divide his logic into major macro functions and follow a step-by-step approach in describing their interconnection. User Macros may be created to allow repeating the same logic function many times in the design without describing the entire function each time. Fujitsu provides predefined macros (F-Macros) which duplicate the function of many popular industry-standard TTL devices and RAM macros which provide from 1K to 2K of single-port static RAM on chip. Also, ROM macros can be provided. The C6600AV and C8000AV are further divided into "blocks" of cells to ease the layout operations.

CHIP LEVEL

The Chip Level of the logic description defines the interconnection of the design components to each other and the I/O cells. For most AV-CMOS family devices, all types of design components including user macros, F-Macros, RAM macros, ROM macros, and unit cells may be interconnected with each other and the I/O cells to form the chip level logic provided the basic cells total required does not exceed 90% of the basic cell total on the array. For the C6600AV and C8000AV, the same basic cells total restriction applies; the chip level of hierarchy describes only the interconnection of the blocks with the I/O cells to form the chip level logic.

BLOCK LEVEL

The Block Level of the logic description defines the interconnection of design components to form each block of the logic description. C6600AV and C8000AV allow up to 90% of the available basic cells to be utilized for each block. Designers may utilize any of the available design components, including user macros, F-Macros and unit cells for interconnection within the blocks provided the basic cell total required to implement the block design does not exceed the maximum allowed for the block. C6600AV provides a flexible block arrangement, allowing block sizes to range between 1000 and 2000 basic cells provided the total does not exceed 90% of the total available on the array.

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MACRO LEVEL

The Macro Level of the logic description defines the interconnection of unit cells to form user macros. F-Macros may not be used to form user macros. Nor may user macros be nested to form other user macros. The total number of basic cells included in one User Macro can be larger than the total number of basic cells available in one column of the array provided the number of BCs in any of the Unit Cells used in the User Macro does not exceed the total number of basic cells available in one column of the array.

TEST DESCRIPTION

The Test Description defines the electrical performance required of the finished array. Test descriptions are used for all simulation operations and are ultimately converted into final test programs for prototype and production testing. Fujitsu utilizes the proprietary Fujitsu Test Data Description Language (FTDL) for all test description inputs to the design operation. As with the logic description, designers may submit test descriptions utilizing other media and Fujitsu will convert to FTDL. Designers using Daisy, Valid or Mentor design workstations are provided with conversion programs as part of the Fujitsu Design Kits for these workstations. Turnkey services may be available. A complete test description will include D.C. testing and functional testing. Delay testing may be performed under some conditions.

DESIGN DEVELOPMENT FLOW

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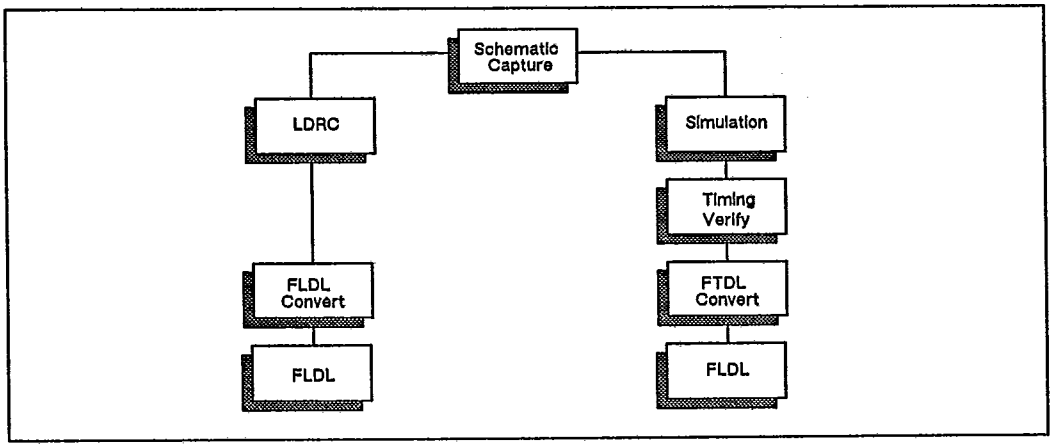
DESIGN WORKSTATION SIMPLIFIED FLOW



WORKSTATION DESIGN

Fujitsu provides workstation support software free of charge to designers using workstations manufactured by Daisy, Valid or Mentor. This software includes a complete design library of unit cells, I/O cells, and memory macros for AV-CMOS gate arrays and conversion programs which generate the logic and test descriptions in the FLDL and FTDL languages required for design input to Fujitsu.

FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY

Fujitsu accepts a variety of design input media but all media must be converted to logic and test descriptions using the FLDL and FTDL description languages. Fujitsu may request additional engineering fees for conversion. Logic and test descriptions are collected into data files for access by the Fujitsu CAD system. The test data file provides the basic information used to conduct simulations and generate the final test program.

LDRC

The Logic Design Rule Check conducts a verification that no design rule violations for interconnect, hierarchy or design description language syntax have occurred, and that the description is complete. Fujitsu will work with the designer to resolve any discrepancies before proceeding with the design development.

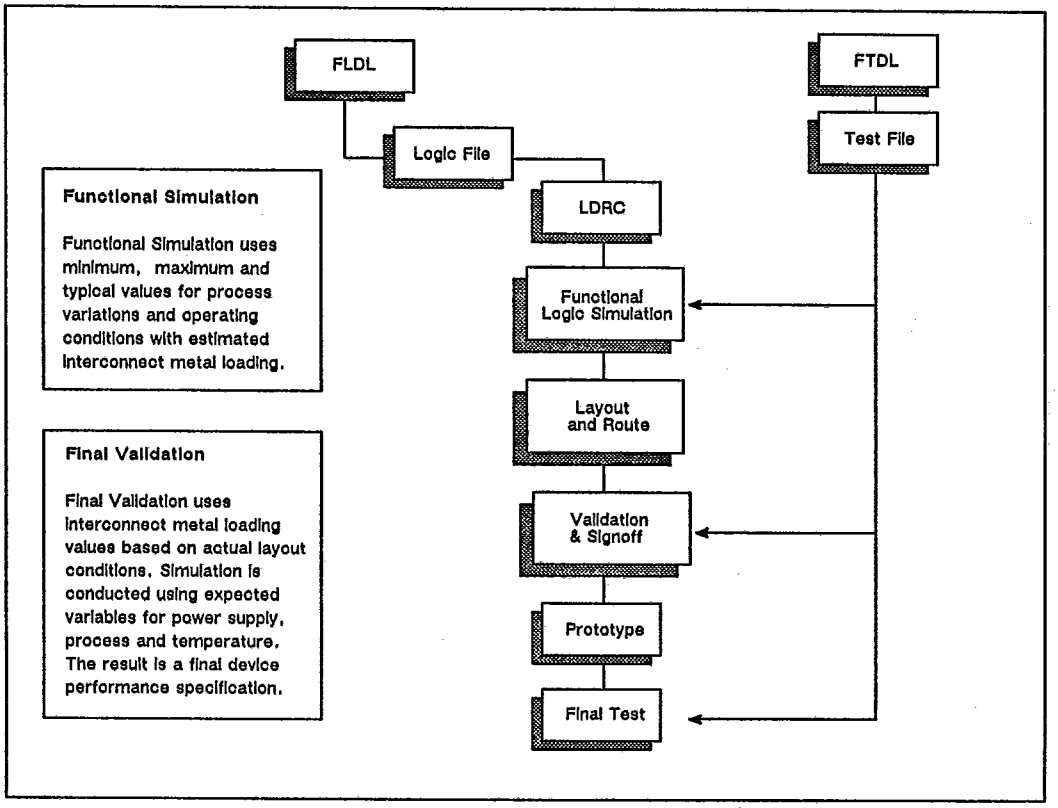
SIMULATION

The Functional Logic Simulation is conducted using minimum, maximum and typical values for process, power supply and temperature conditions, with estimated interconnect metal loading. The functional logic simulation must successfully demonstrate device operation according to the designer's test description before any layout operations are attempted.

FINAL VALIDATION

Final Validation is conducted to produce the device operating specification for approval and signoff by the designer. The simulation is conducted using values for interconnect metal loading based on the actual layout. Full range values for process, temperature and power supply variation are also used. A final operating specification is presented to the designer which defines the parameters which will be guaranteed by Fujitsu in the prototype and production devices.

FUJITSU DESIGN DEVELOPMENT FLOW SUMMARY



PROTOTYPES

At the completion of the design development Fujitsu provides the designer with prototypes for on-site design evaluation. Ten prototype devices (Five for C8000AV) are provided with the development fee. Additional prototypes may be provided for an additional fee.

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UNIT CELL LIBRARY

INVERTER, CLOCK BUFFER FAMILY

Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
V1N	Inverter	1	K3B	Gated Clock Buffer (AND)	3
V2B	Power Inverter	1	K4B	Gated Clock Buffer (OR)	3
K1B	Clock Buffer	2	KCB	Block Clock Buffer	11
K2B	Power Clock Buffer	3	–	–	–

NAND FAMILY

N2N	2-Input NAND	1	N6B	6-Input Power NAND	5
N3N	3-Input NAND	2	N8B	8-Input Power NAND	6
N4N	4-Input NAND	2	N9B	9-Input Power NAND	7
N2B	2-Input Power NAND	3	NCB	12-Input Power NAND	9
N3B	3-Input Power NAND	3	NGB	16-Input Power NAND	11
N4B	4-Input Power NAND	4	–	–	–

AND FAMILY

N2P	2-Input Power AND	2	N4P	4-Input Power AND	3
N3P	3-Input Power AND	3	–	–	–

NOR FAMILY

R2N	2-Input NOR	1	R6B	6-Input Power NOR	5
R3N	3-Input NOR	2	R8B	8-Input Power NOR	6
R4N	4-Input NOR	2	R9B	9-Input Power NOR	7
R2B	2-Input Power NOR	3	RCB	12-Input Power NOR	9
R3B	3-Input Power NOR	3	RGB	16-Input Power NOR	11
R4B	4-Input Power NOR	4	–	–	–

OR FAMILY

R2P	2-Input Power OR	2	R4P	4-Input Power OR	3
R3P	3-Input Power OR	3	–	–	–

ENOR/EOR

X1B	Power ENOR	4	X2B	Power EOR	4

AND-NOR FAMILY

D14	2-wide 3-AND 4-Input AND-OR Invert	2	D34	3-wide 2-AND 4-Input AND-OR Invert	2
D23	2-wide 2-AND 3-Input AND-OR Invert	2	D44	2-wide 2-OR 2 AND 4-Input AND-OR Invert	2
D24	2-wide 2-AND 4-Input AND-OR Invert	2	–	–	–

OR-NAND FAMILY

G14	2-wide 3-OR 4-Input OR-AND Invert	2	G34	3-wide 2-OR 4-Input OR-AND Invert	2
G23	2-wide 2-OR 3-Input OR-AND Invert	2	G44	2-wide 2-AND 2-OR 4-Input OR-AND Invert	2
G24	2-wide 2-OR 4-Input OR-AND Invert	2	–	–	–

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UNIT CELL LIBRARY

MULTIPLEXER FAMILY

Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
T24	Power 2-AND 4-wide	6	U24	Power 2-OR 4-wide	6
T26	Power 2-AND 6-wide	9	U26	Power 2-OR 6-wide	9
T28	Power 2-AND 8-wide	11	U28	Power 2-OR 8-wide	11
T32	Power 3-AND 2-wide	5	U32	Power 3-OR 2-wide	5
T33	Power 3-AND 3-wide	7	U33	Power 3-OR 3-wide	7
T34	Power 3-AND 4-wide	9	U34	Power 3-OR 4-wide	9
T42	Power 4-AND 2-wide	6	U42	Power 4-OR 2-wide	6
T43	Power 4-AND 3-wide	9	U43	Power 4-OR 3-wide	9
T44	Power 4-AND 4-wide	11	U44	Power 4-OR 4-wide	11

FLIP-FLOP FAMILY

FD2	Power DFF	8	FDD	Positive Edge Power DFF with Clear/Preset	11
FD3	Power DFF with Preset	9	FDE	Positive Edge Power DFF with Clear	10
FD4	Power DFF with Clear/ Preset	10	FDG	Positive Edge with Clear	9
FD5	Power DFF with Clear	9	FJD	Positive Edge Power JKFF with Clear	12
FD6	DFF	7	FJ4	Power JKFF with Clear	11
FD7	DFF with Clear	8	FJ5	Power JKFF with Clear/ Preset	12
FD8	DFF with Latch	9	–	–	–

FLIP-FLOP FAMILY USING TRANSMISSION GATES

FDM	DFF	6	FDP	DFF with Set/Reset	8
FDN	DFF with Set	7	FDQ	4-bit DFF	21
FDO	DFF with Reset	7	FDR	4-bit DFF with Clear	26
FDS	4-Bit DFF	20	–	–	–

LATCH FAMILY

LT1	SET-RESET with Clear	4	LT3	4-bit Data Latch	15
LT2	1-bit Data Latch	4	LT4	4-bit Data Latch	13
LTK	Data Latch	4	LTL	Data Latch with Clear	5
LTM	4-Bit Data Latch with Clear	15	–	–	–

SHIFT REGISTER FAMILY

FS1	4-bit S_{in} -P_{out}	18	FS3	4-bit with Asyno Load	34
FS2	4 bit S_{in} -P_{out} with Syno Load	30	–	–	–

DECODER FAMILY

DE2	2:4 Decoder	5	DE3	3:8 Decoder	15

COUNTER FAMILY

C11	Flip-Flop for Counter	11	C43	4-bit Syno UP with Clear	48
C41	4-bit Asyno	24	C45	4-bit Syno UP	48
C42	4-bit Syno	32	C47[1]	4-bit Syno UP/DOWN	68

Note:

1. C47 is not available for C-350AVB and C540AVB.

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UNIT CELL LIBRARY

SELECTOR FAMILY

Unit Cell	Function	Basic Cells	Unit Cell	Function	Basic Cells
T2B	2:1 Selector	2	V3A	1:2 Selector	2
T2C	Dual 2:1 Selector	4	V3B	Dual 1:2 Selector	3
T2D	2:1 Selector	2	T5A	4:1 Selector	5

COMPARATOR

MC4	4-bit Magnitude Comparator	42	–	–	–

ADDER FAMILY

A1N	1-bit Full Adder	8	A4H	4-bit Full Adder	50
A2N	2-bit Full Adder	16	–	–	–

SCHMITT TRIGGER

SM1 [1]	Schmitt Trigger	8	SM2 [1]	Schmitt Trigger	7

DELAY UNIT CELLS

BD3	Buffer (Delay Cell)	5	BD6	Buffer (Delay Cell)	17
BD5	Buffer (Delay Cell)	9	–	–	–

I/O CELL FAMILY

I2B	Input Buffer	0	IKB	Clocked Input Buffer(Inverting)	0
I2BU [2]	I2B with Input Pull-up	0	IKBU [2]	IKB with Input Pull-up	0
I2BD [2]	I2B with Input Pull-down	0	IKBD [2]	IKB with Input Pull-down	0
ILB	Clocked Input Buffer	0	I2C	CMOS Interface Input Buffer (True & Inverter)	0
ILBU [2]	ILB with Input Pull-up	0			
ILBD [2]	ILB with Input Pull-down	0	I2CU [2]	I2C with Input Pull-up	0
IT1	Input Buffer for Schmitt-Trigger Input	0	I2CD [2]	I2C with Input Pull-down	0
			H6T	Tri-state Output & Input Buffer	0
IT1U [2]	IT1 with Input Pull-up	0	H6TU [2]	H6T with Input Pull-up	0
IT1D [2]	IT1 with Input Pull-down	0	H6TD [2]	H6T with Input Pull-down	0
O2B	Output Buffer	0	O4T	Tri-state Output Buffer	0
02L [2]	Power Output Buffer (True)	0	O4W [2]	Power Tri-state Output Buffer (True)	0
H6W [2]	Power Tri-state Output and Input Buffer (True)	0	H6C [2]	Tri-state Output and CMOS Interface Input Buffer (True)	0
H6WU [2]	H6W with Input Pull-up	0			
H6WD [2]	H6W with Input Pull-down	0	H6CU [2]	H6C with Input Pull-up	0
H6E [2]	Power Tri-state Output and CMOS Interface Input Buffer (True)	0	H6CD [2]	H6C with Input Pull-down	0
			H6EU [2]	H6E with Input Pull-up	0
			H6ED [2]	H6E with Input Pull-down	0

Note:

1. SM1 and SM2 must not be used together in one chip.
2. Available only for AVB.

F-MACRO LIBRARY

F-MACRO FUNCTION

Fujitsu's F-Macros are direct software macro implementations of popular industry-standard TTL functions. They may be used in the design exactly the same as user macros. Designers's converting existing TTL designs to gate array will find the F-Macro a particularly useful implementation.

F-MACROS AVAILABLE TO REPLACE THESE TTL DEVICES

Device	Basic Cells	Device	Basic Cells	Device	Basic Cells
7400		7498	36	74176	76
7402		7499		74177	72
7404		74100	60	74178	63
7408		74101		74179	71
7410		74102		74180	33
7411		74103		74181	
7420		74106		74182	49
7421		74107		74183	36
7425		74108		74190	106
7427		74109		74191	73[1]
7430		74112		74192	92
7432		74113		74193	82
7442	32	74114		74194	78
7443	32	74116	82	74195	51
7444	32	74120	34	74198	132
7451	7	74135		74199	98
7454	9	74137	48	74260	
7455	6	74138	28	74261	107
7456		74139	26	74273	
7457		74147	49	74278	46
7464	9	74148	53	74279	18
7468	89	74150	112	74280	57
7469	79	74151	54	74283	50
7473		74152	29	74290	45
7474		74153	24	74293	33
7475	32	74154	96	74298	36
7476		74155	29	74352	28
7477	18	74157	23	74375	18
7478		74158	23	74377	71
7482	16	74160	82	74378	55
7483	50	74161	48	74379	39
7485	42	74162	83	74381	192
7486		74163	48	74382	201
7487		74164	70	74386	
7490	41	74165	73	74390	82
7491	43	74166	80	74393	52
7492	64	74168	111	74396	60
7493	33	74169	74[1]	74398	37
7494	47	74171		74399	37
7495	42	74174	46		
7496	56	74175	32		
7497					

Note:
1. These F-Macros utilize complex unit cells and may not be available for smaller arrays.

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RAM MACRO LIBRARY

C2301AVM

	RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration
32-WORD RAM MACROS	R51	32-word x 32-bit	-
	R51A	32-word x 28-bit	32-word x 4-bit
	R51B	32-word x 24-bit	32-word x 8-bit
	R51C	32-word x 20-bit	32-word x 12-bit
	R51D	32-word x 16-bit	32-word x 16-bit
64-WORD RAM MACROS	R61	64-word x 16-bit	-
	R61A	64-word x 12-bit	64-word x 4-bit
	R61B	64-word x 8-bit	64-word x 8-bit
128-WORD RAM MACROS	R71	128-word x 8-bit	-
	R71A	128-word x 4-bit	128-word x 4-bit
256-WORD RAM MACROS	R83	256-word x 4-bit	-
	R83A	256-word x 2-bit	256-word x 2-bit

C1502AVM/C4002AVM

	RAM Macro Name	RAM 1 Configuration	RAM 2 Configuration
64-WORD RAM MACROS	R610	64-word x 36-bit	-
	R611	64-word x 20-bit	64-word x 16-bit
128-WORD RAM MACROS	R711	128-word x 18-bit	-
	R712	128-word x 9-bit	128-word x 9-bit
256-WORD RAM MACROS	R87	256-word x 9-bit	-

ROM MACRO LIBRARY

C2301AVM

	ROM Macro Name	Configuration	
256-WORD ROM MACROS	YRn	256-word x 8-bit	-

Note:
Contact nearest Fujitsu Design Center for additional ROM data.

PACKAGE AVAILABILITY MATRIX

DUAL IN-LINE PACKAGES, PLASTIC (PDIP)

	PACKAGE PRODUCT	PDIP-16	PDIP-18	PDIP-20	PDIP-22	PDIP-24	PDIP-28	PDIP-40	PDIP-42	PDIP-48
CMOS	350AVB	●	●	●	●	●	●	●	●	
	540AVB	●	●	●	●	●	●	●	●	
	850AVB			●	●	●	●	●	●	
	1200AVB				●	●	●	●	●	●
	1502AVM					●	●	●	●	
	1600AVB				●	●	●	●	●	●
	2000AVB					●	●	●	●	●
	2301AVM					●		●	●	
	2600AV					●	●	●	●	●
	3900AV					●		●	●	
	4002AVM									
	5000AV							●		
	6600AV									
	8000AV									

DUAL IN-LINE PACKAGES, PLASTIC SHRINK TYPE (SH-DIP)

DUAL IN-LINE PACKAGES PLASTIC SKINNY TYPE (SK-DIP)

PACKAGE PRODUCT	DIP-28SH SHRINK	DIP-42SH SHRINK	DIP-48SH SHRINK	DIP-64SH SHRINK	DIP-24SK SKINNY
350AVB	●	●	●		
540AVB	●	●	●	●	
850AVB	●	●	●	●	
1200AVB	●	●	●	●	
1502AVM		●	●	●	
1600AVB	●	●	●	●	
2000AVB		●	●	●	
2301AVM			●	●	
2600AV		●	●	●	
3900AV			●	●	
4002AVM					
5000AV				□	
6600AV					
8000AV					

PLASTIC LEADED CHIP CARRIERS (PLCC)

	PACKAGE PRODUCT	PLCC-28	PLCC-44	PLCC-68	PLCC-84
CMOS	350AVB	●	●		
	540AVB	●	●		
	850AVB	●	●		
	1200AVB	●	●		
	1502AVM		●	●	●
	1600AVB	●	●	●	
	2000AVB		●	●	
	2301AVM		●	●	●
	2600AV	●	●	●	●
	3900AV		●	●	●
	4002AVM				
	5000AV			●	●
	6600AV				
	8000AV				

FLAT PACKS, PLASTIC (FPT)

PACKAGE PRODUCT	FPT-16	FPT-20	FPT-24	FPT-28	FPT-48	FPT-64	FPT-80	FPT-100	FPT-120	FPT-160
350AVB	●	●	●	●	●					
540AVB	●	●	●	●	●	●				
850AVB			●	●	●	●				
1200AVB			●	●	●	●	●			
1502AVM					●	●	●	●		
1600AVB					●	●	●			
2000AVB					●	●	●	●		
2301AVM					●	●	●	●		
2600AV					●	●	●	●	□	
3900AV					●	●	●	●	□	
4002AVM										
5000AV							●	●	□	□
6600AV							□	□	□	□
8000AV							□	□	□	□

● – QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW

□ – PACKAGE COMBINATION UNDER DEVELOPMENT

Note:
Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions.
Plastic PGA packages (64, 88, 135, 179-pin) are now under development.

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PACKAGE AVAILABILITY MATRIX

DUAL IN-LINE PACKAGES, CERAMIC (CDIP)

	PACKAGE PRODUCT	CDIP-16	CDIP-18	CDIP-20	CDIP-22	CDIP-24	CDIP-28	CDIP-40	CDIP-42	CDIP-48
CMOS	350AVB	●	●	●	●	●	●	●		
	540AVB	●	●	●	●	●	●	●		
	850AVB				●	●	●	●		
	1200AVB				●	●	●	●	●	●
	1502AVM							●	●	●
	1600AVB				●	●	●	●	●	●
	2000AVB						●	●	●	●
	2301AVM							●	●	●
	2600AV						●	●	●	●
	3900AV							●	●	●
	4002AVM									
	5000AV									
	6600AV									
	8000AV									

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CERAMIC LEADLESS CHIP CARRIERS (LCC)
CERAMIC J-LEADED CHIP CARRIERS (JLCC)
CERAMIC PIN GRID ARRAY (PGA)

	PACKAGE PRODUCT	LCC-28	LCC-48	LCC-64	LCC-68	JLCC-68	JLCC-84	PGA-64	PGA-88	PGA-135	PGA-179	PGA-256
CMOS	350AVB	●	●									
	540AVB	●	●	●	□			●				
	850AVB	●	●	●	□			●				
	1200AVB	●	●	●	□			●				
	1502AVM		●	●	□	□	□	●	●	●		
	1600AVB	●	●	●	□	□		●	●			
	2000AVB		●	●	□	□		●	●			
	2301AVM		●	●	□	□	□	●	●	●		
	2600AV		●	●	□	□	□	●	●	●		
	3900AV		●	●	□	□	□	●	●	●		
	4002AVM			●	●			●	●	●		
	5000AV		●	●	□	□	□	●	●	●		
	6600AV			●	□			●	●	●	●	
	8000AV			●	□			●	●	●	●	

● – QUALIFIED PRODUCTION OFFICIALLY AVAILABLE NOW
□ – PACKAGE COMBINATION UNDER DEVELOPMENT

Note:
Contact nearest Fujitsu Design Center for current package information and power supply pin restrictions.