DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78P054, 78P058

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P054 and 78P058 are the members of the μPD78054 Subseries of 78K/0 Series products, in which the on-chip mask ROM of the μPD78054 and 78058 is replaced with one-time PROM or EPROM.

Because these devices can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

Caution The reliability of the μPD78P054KK-T and 78P058KK-T is not guaranteed when used in mass-production applications. Please use this device only experimentally or for evaluation during trial manufacture.

Details are given in the following User's Manuals. Be sure to read them before starting design.

μPD78054, 78054Y Subseries User's Manual : U11747E

78K/0 Series User's Manual Instructions : U12326E

FEATURES

- Pin compatible with mask ROM versions (except the V_{PP} pin)
- Internal high-capacity PROM and RAM

Parameter / Part Number	Program Memory (PROM)	Internal Data Memory		
		High-speed RAM	Buffer RAM	Expansion RAM
μPD78P054	32 Kbytes[Note 1]	1024 bytes[Note 1]	32 bytes	None
μPD78P058	60 Kbytes[Note 1]			1024 bytes[Note 2]

  - μPD78P05xKK-T : Reprogrammable (ideal for system evaluation)
  - μPD78P05xGC, 78P05xGK : Programmable once only (ideal for small-scale production)
- Operable in the same supply voltage as mask ROM versions (V_{DD} = 2.0 to 6.0 V)
- Corresponding to QTOP™ microcontrollers

Notes 1. Internal PROM and internal high-speed RAM capacity can be changed by memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

Remarks 1. QTOP microcontroller is the general name of the microcontrollers with one-time PROM that are totally supported by the NEC writing service (from writing to marking, screening, and testing).

2. For the differences between PROM versions and mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78P054, 78P058 AND MASK ROM VERSIONS**.

In this document, "PROM" is used in parts common to one-time PROM and EPROM versions.

★ ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade
μPD78P054GC-3B9	80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)	One-time PROM	Standard
μPD78P054GC-8BT[Note]	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	One-time PROM	Standard
μPD78P054GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	One-time PROM	Standard
μPD78P054KK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM	Not applicable
μPD78P058GC-8BT	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	One-time PROM	Standard
μPD78P058KK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM	Not applicable

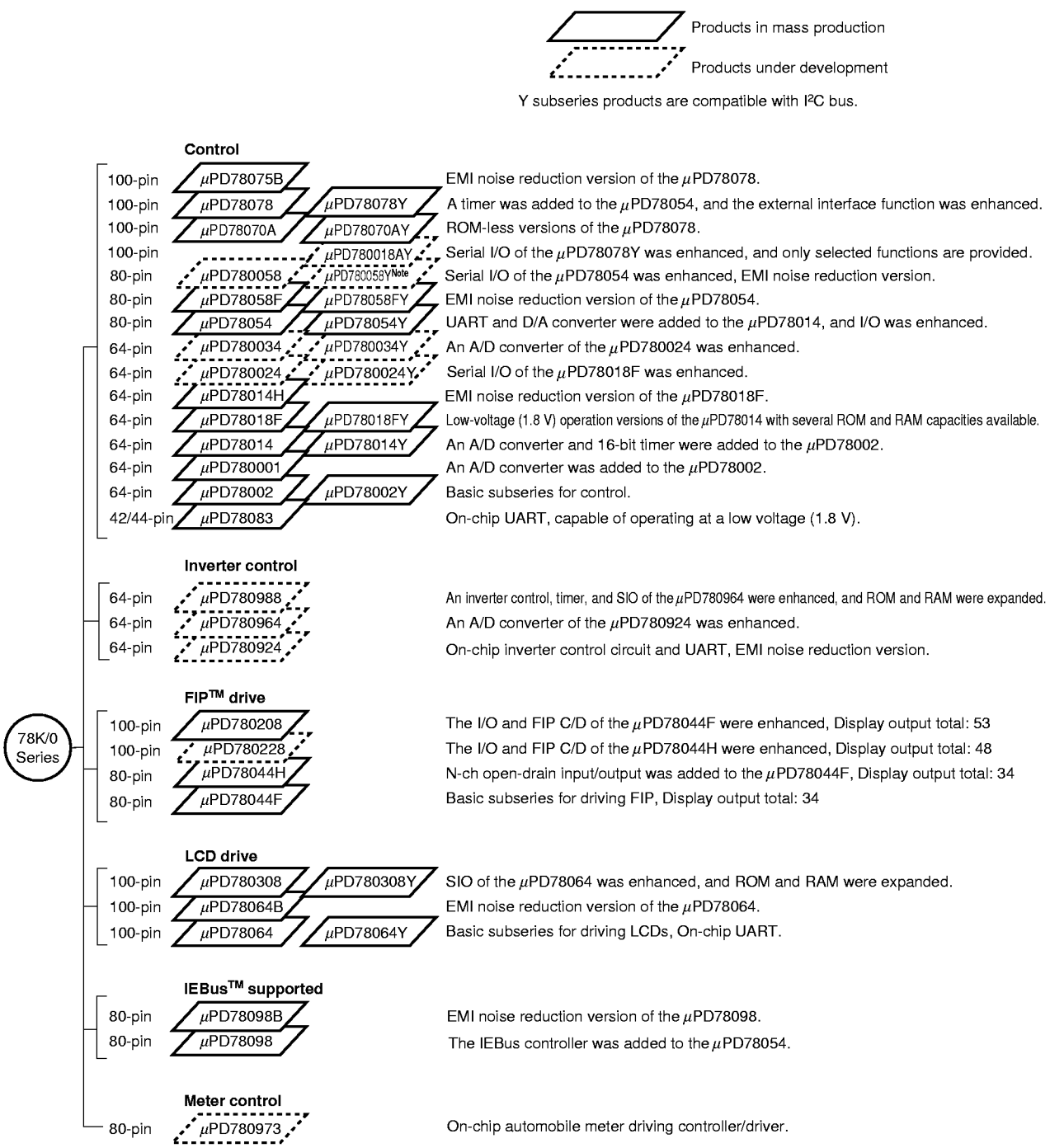
Note Under development

Caution The μPD78P054GC contains two types of packages (refer to 11. PACKAGE DRAWINGS). For the packages which can be supplied, consult your local NEC sales representative.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under planning

The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2ch							3ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780034	8 K to 32 K					–	8ch	–	3ch (UART: 1ch, time-division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K to 60 K											
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		–	–					1ch	39		–
	μPD78002	8 K to 16 K			1ch		–				53		Available
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780988	32 K to 60 K	3ch	Note 1	–	1ch	–	8ch	–	3ch (UART: 2ch)	47	4.0 V	Available
	μPD780964	8 K to 32 K		Note 2						2ch (UART: 2ch)		2.7 V	
	μPD780924						8ch	–					
FIP drive	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48 K to 60 K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32 K to 48 K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16 K to 40 K								2ch			
LCD drive	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time-division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2ch (UART: 1ch)			
	μPD78064	16 K to 32 K											
IEBus supported	μPD78098B	40 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	Available
	μPD78098	32 K to 60 K											
Meter control	μPD780973	24 K to 32 K	3ch	1ch	1ch	1ch	5ch	–	–	2ch (UART: 1ch)	56	4.5 V	–

Notes 1. 16-bit timer : 2 channels
10-bit timer : 1 channel

2. 10-bit timer : 1 channel

FUNCTION DESCRIPTION

Item \ Part Number		μPD78P054	μPD78P058
Internal memory	PROM	32 Kbytes[Note 1]	60 Kbytes[Note 1]
	High-speed RAM	1024 bytes[Note 1]	
	Buffer RAM	32 bytes	
	Expansion RAM	None	1024 bytes[Note 2]
Memory space		64 Kbytes	
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		Minimum instruction execution time is variable.	
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0-MHz operation)	
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8-bit × 8-bit, 16-bit ÷ 8-bit) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O port		Total : 69 • CMOS input : 2 • CMOS input/output : 63 • N-ch open-drain input/output : 4	
A/D converter		8-bit resolution × 8 ch	
D/A converter		8-bit resolution × 2 ch	
Serial interface		• 3-wire serial I/O, SBI, or 2-wire serial I/O mode selectable : 1 ch • 3-wire serial I/O mode (with on-chip max. 32-byte automatic transmit/receive function) : 1 ch • 3-wire serial I/O or UART mode selectable : 1 ch	
Timer		• 16-bit timer/event counter : 1 ch • 8-bit timer/event counter : 2 ch • Watch timer : 1 ch • Watchdog timer : 1 ch	
Timer output		3 pins (14-bit PWM output: 1 pin)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (@ 5.0-MHz operation with main system clock)	
Vectored interrupt source	Maskable	Internal: 13, external: 7	
	Non-maskable	Internal: 1	
	Software	1	
Test input		Internal: 1, external: 1	
Supply voltage		V_{DD} = 2.0 to 6.0 V	
Operating ambient temperature		T_A = −40 to +85°C	
Package		• 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) : μPD78P054 only • 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) : μPD78P054 is under development • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) : μPD78P054 only • 80-pin ceramic WQFN (14 × 14 mm)	

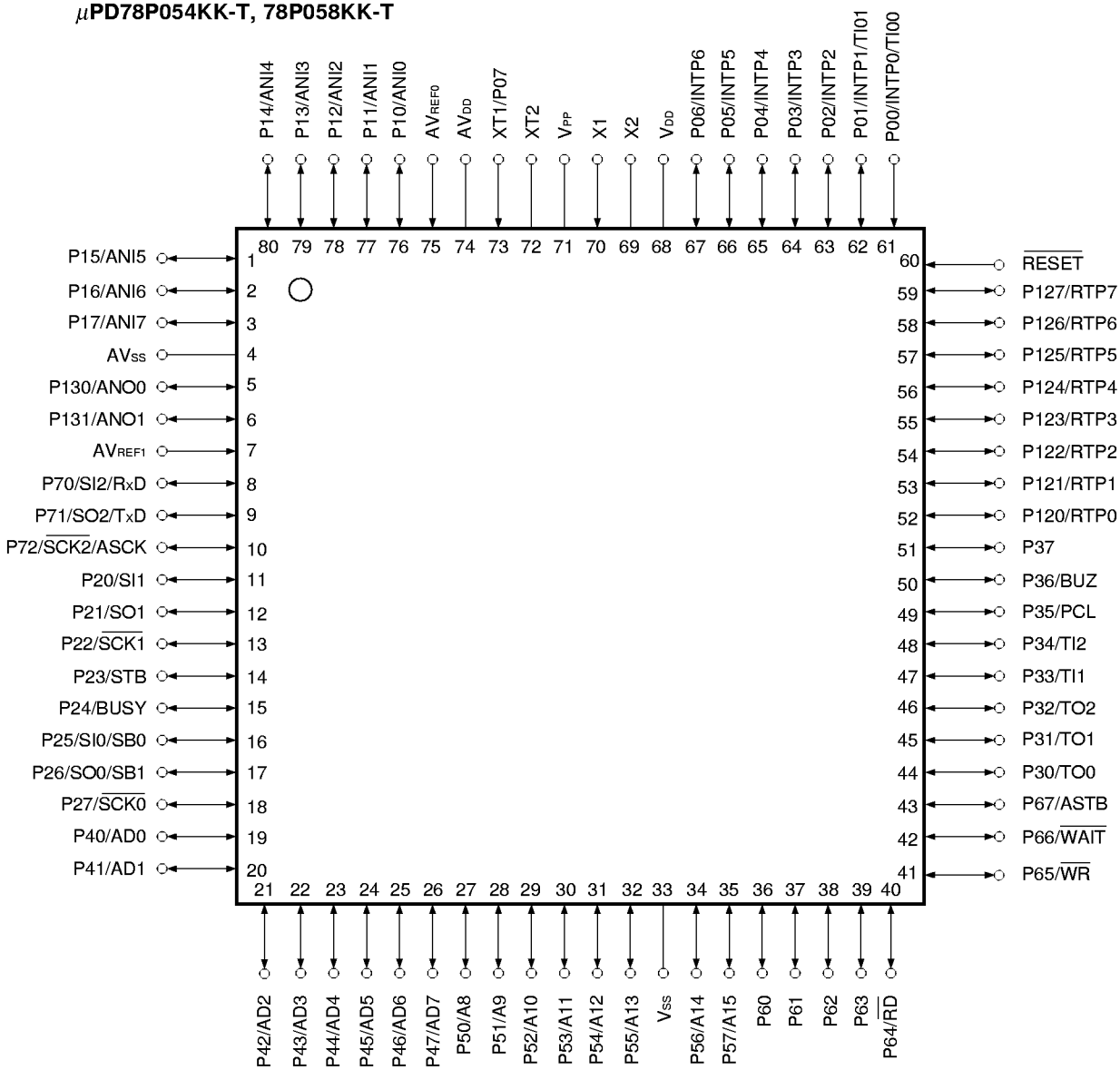
Notes 1. Internal PROM/internal high-speed RAM capacity can be changed by memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register(IXS).

PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

- **80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)**
  μPD78P054GC-3B9
- **80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**
  μPD78P054GC-8BT[Note], 78P058GC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD78P054GK-BE9
- **80-pin ceramic WQFN (14 × 14 mm)**
  μPD78P054KK-T, 78P058KK-T



Note Under development

★ **Cautions 1. Connect V_{PP} pin directly to V_{SS}.**

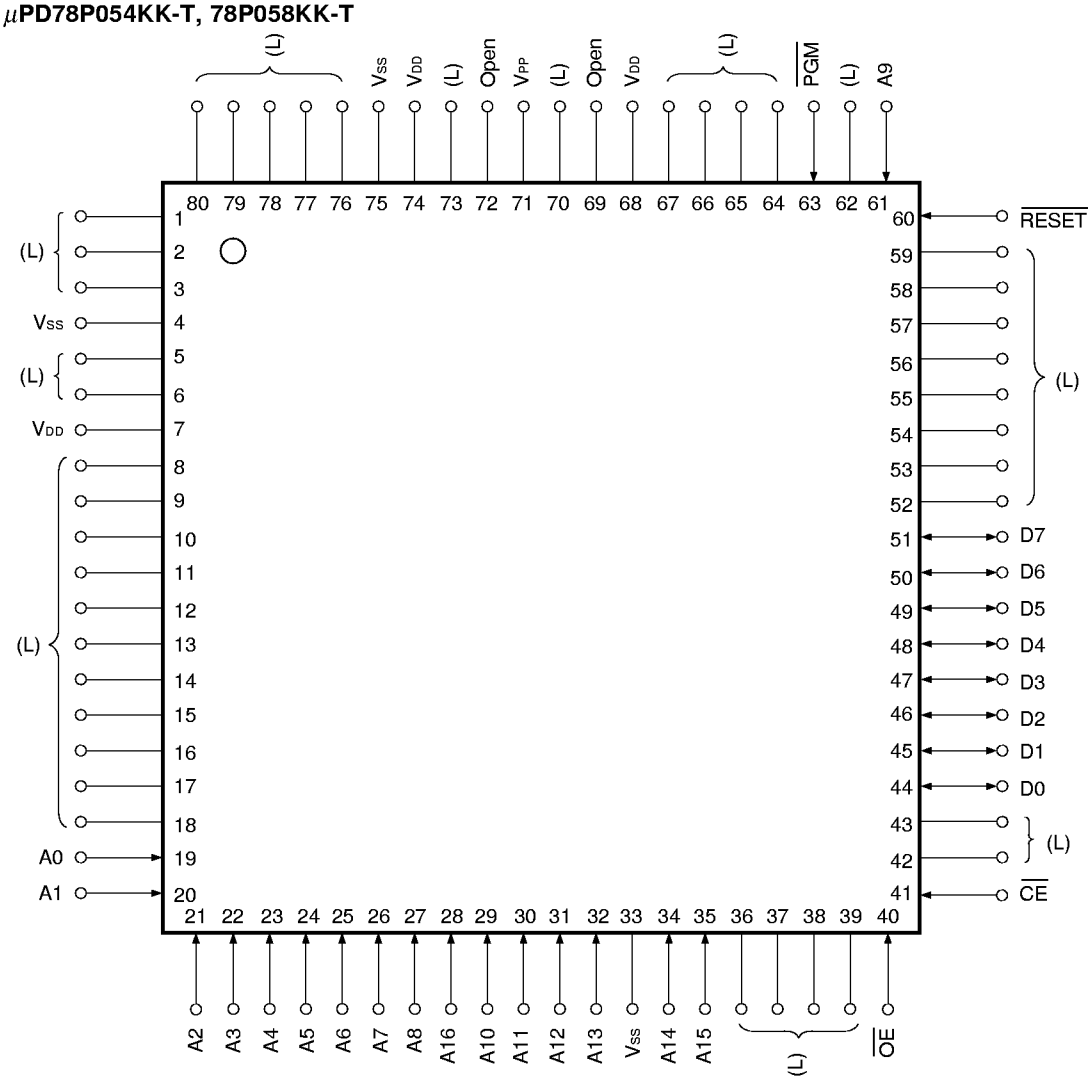
2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

A8 to A15	:	Address Bus
AD0 to AD7	:	Address/Data Bus
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
ASCK	:	Asynchronous Serial Clock
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF0}, AV_{REF1}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BUSY	:	Busy
BUZ	:	Buzzer Clock
INTP0 to INTP6	:	Interrupt from Peripherals
P00 to P07	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P72	:	Port 7
P120 to P127	:	Port 12
P130, P131	:	Port 13
PCL	:	Programmable Clock
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
RTP0 to RTP7	:	Real-Time Output Port
RxD	:	Receive Data
SB0, SB1	:	Serial Bus
$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
SI0 to SI2	:	Serial Input
SO0 to SO2	:	Serial Output
STB	:	Strobe
TI00, TI01	:	Timer Input
TI1, TI2	:	Timer Input
TO0 to TO2	:	Timer Output
TxD	:	Transmit Data
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

(2) PROM programming mode

- **80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)**
  μPD78P054GC-3B9
- **80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**
  μPD78P054GC-8BT[Note], 78P058GC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm)**
  μPD78P054GK-BE9
- **80-pin ceramic WQFN (14 × 14 mm)**
  μPD78P054KK-T, 78P058KK-T

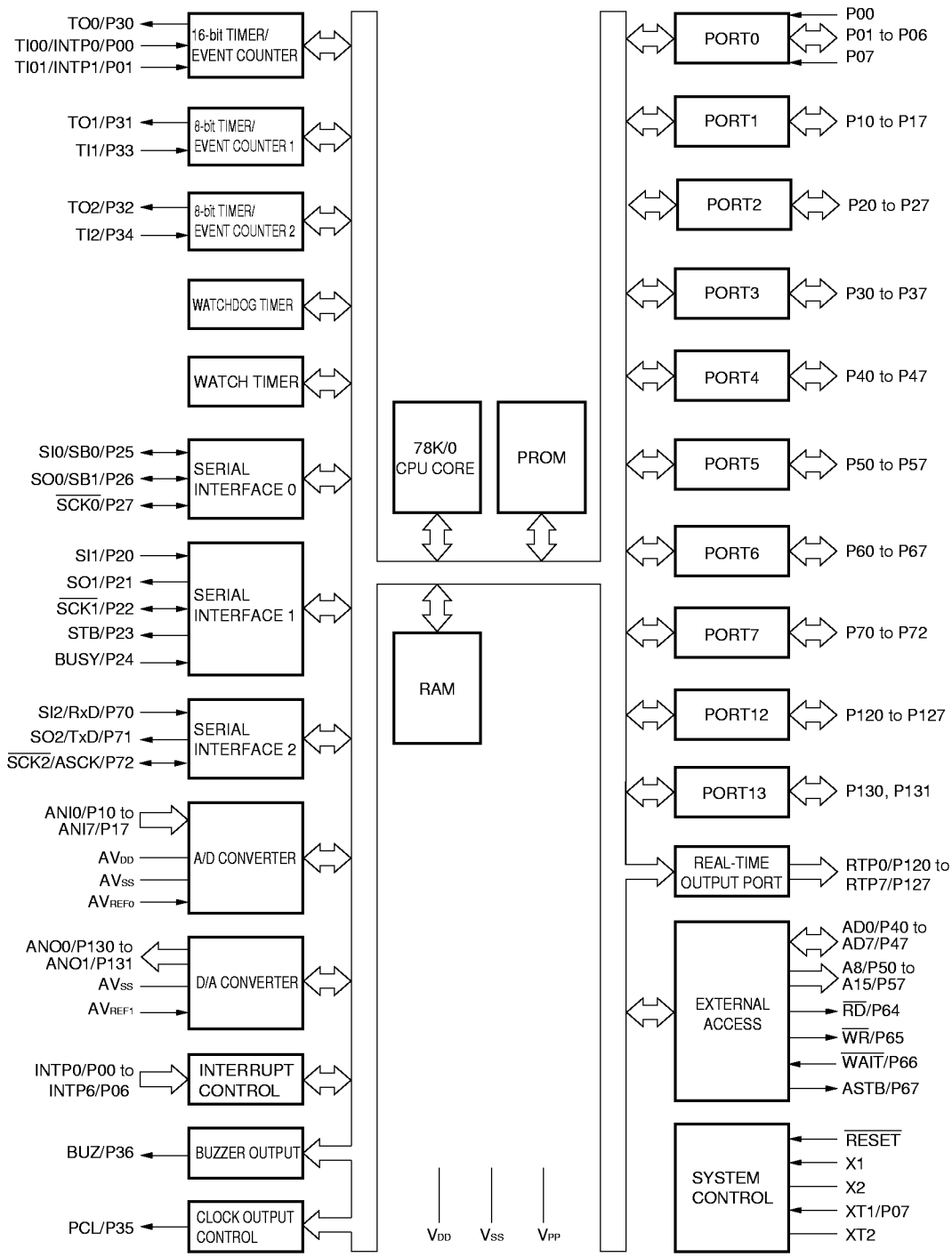


Note Under development

Cautions 1. (L) : Individually connect to VSS via a pull-down resistor.
2. VSS : Connect to GND.
3. RESET : Set to low level.
4. Open : No connection

A0 to A16	:	Address Bus	RESET	:	Reset
CE	:	Chip Enable	VDD	:	Power Supply
D0 to D7	:	Data Bus	VPP	:	Programming Power Supply
OE	:	Output Enable	VSS	:	Ground
PGM	:	Program			

BLOCK DIAGRAM



Remark The internal PROM and internal RAM capacity differ depending on the product.

CONTENTS

★ 1. DIFFERENCES BETWEEN μPD78P054, 78P058 AND MASK ROM VERSIONS

The μPD78P054 and 78P058 are single-chip microcontrollers with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure, and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option of P60 to P63 pins, to the same as those of mask ROM versions by setting the memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Differences between the PROM versions (μPD78P054 and 78P058) and mask ROM versions (μPD78052, 78053, 78054, 78055, 78056, and 78058) are shown in Table 1-1.

Table 1-1. Differences between μPD78P054, 78P058 and Mask ROM Versions

Item	μPD78P054, 78P058	Mask ROM Versions
Internal ROM structure	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	μPD78P054 : 32 Kbytes μPD78P058 : 60 Kbytes	μPD78052 : 16 Kbytes μPD78053 : 24 Kbytes μPD78054 : 32 Kbytes μPD78055 : 40 Kbytes μPD78056 : 48 Kbytes μPD78058 : 60 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD78052 : 512 bytes Other than μPD78052 : 1024 bytes
Internal expansion RAM capacity	μPD78P054 : None μPD78P058 : 1024 bytes	μPD78058 : 1024 bytes Other than μPD78058 : None
Change of internal ROM and internal high-speed RAM capacity by memory size switching register (IMS)	Can be changed[Note 1]	Cannot be changed
Change of internal expansion RAM capacity by internal expansion RAM size switching register (IXS)	Can be changed[Note 2]	Cannot be changed
IC pin	None	Provided
V_{PP} pin	Provided	None
Pull-up resistor on-chip mask option of P60 to P63 pins	None	Provided
Electrical specifications, recommended soldering conditions	Refer to Data Sheet for each product.	

Notes 1. The internal PROM capacity and internal high-speed RAM capacity become as follows by $\overline{\text{RESET}}$ input.
Internal PROM capacity : 32 Kbytes (μPD78P054), 60 Kbytes (μPD78P058)
Internal high-speed RAM capacity : 1024 bytes

2. The internal expansion RAM capacity becomes 1024 bytes by $\overline{\text{RESET}}$ input (μPD78P058 only).

Caution The PROM version and mask ROM version differ in noise tolerance and noise emission. When replacing a PROM version with a mask ROM version when switching from experimental production to mass production, make a thorough evaluation with a CS version (not ES version) of the mask ROM version.

Remarks 1. The μPD78P054 is a PROM version of the μPD78052, 78053, and 78054.
The μPD78P058 is a PROM version of the μPD78055, 78056, and 78058.

2. The internal expansion RAM size switching register (IXS) is included only in the μPD78058 and 78P058.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	INTP0/TI00
P01	Input/output	8-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software. [Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When P07/XT1 pins are used as the input ports, set the processor clock control register (PCC) bit 6 (FRC) to 1 (be sure not to use the feedback resistor of the subsystem clock oscillation circuit).

2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, set port 1 to input mode. The pull-up resistors are automatically disabled.

(1) Port pins (2/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output is specifiable as 8-bit unit. When used as the input port, it is possible to use an on-chip pull-up resistor by software. Set test input flag (KRIF) to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	Input/output	Port 5 8-bit input/output port It is possible to directly drive LEDs. Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port Input/output is specifiable bit-wise.	N-ch open-drain input/output port. It is possible to directly drive LEDs.	Input	—
P61					
P62					
P63					
P64			When used as the input port, it is possible to use an on-chip pull-up resistor by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor by software.		Input	ANO0, ANO1

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request inputs, with specifiable valid edges (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial data input of the serial interface	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial data output of the serial interface	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial clock input/output of the serial interface	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Automatic transmitting/receiving strobe output of the serial interface	Input	P23
BUSY	Input	Automatic transmitting/receiving busy input of the serial interface	Input	P24
RxD	Input	Serial data input for asynchronous serial interface	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (Can also be used as 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port which outputs data in synchronization with trigger	Input	P120 to P127
AD0 to AD7	Input/output	Low-order address/data bus when expanding memory to the outside	Input	P40 to P47
A8 to A15	Output	High-order address bus when expanding memory to the outside	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for the external memory read operation	Input	P64
$\overline{WR}$		Strobe signal output for the external memory write operation	Input	P65

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
$\overline{WAIT}$	Input	Wait insertion when accessing external memory	Input	P66
ASTB	Output	Strobe output to externally latches address information which is output to ports 4 and 5 for accessing external memory	Input	P67
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
ANO0, ANO1	Output	Analog output of D/A converter	Input	P130, P131
AV_{REF0}	Input	Reference voltage input of A/D converter	—	—
AV_{REF1}	Input	Reference voltage input of D/A converter	—	—
AV_{DD}	—	Analog power supply of A/D converter. Connect to V_{DD}.	—	—
AV_{SS}	—	Ground potential of A/D converter and D/A converter. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
★ V_{PP}	—	High-voltage applied during program write/verify. Connect directly to V_{SS} in normal operating mode.	—	—
V_{SS}	—	Ground potential	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Pin Input/Output Circuit Type (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Independently connect to V_{SS} through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Independently connect to V_{DD} or V_{SS} through resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Independently connect to V_{DD} through resistor.
P50/A8 to P57/A15	5-A		Independently connect to V_{DD} or V_{SS} through resistor.
P60 to P63	13-D		Independently connect to V_{DD} through resistor.
P64/$\overline{RD}$	5-A		Independently connect to V_{DD} or V_{SS} through resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A		Independently connect to V_{SS} through resistor.

Table 2-1. Pin Input/Output Circuit Type (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
$\overline{\text{RESET}}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
★ V_{PP}			Connect directly to V_{SS}.

Figure 2-1. Pin Input/Output Circuits (1/2)

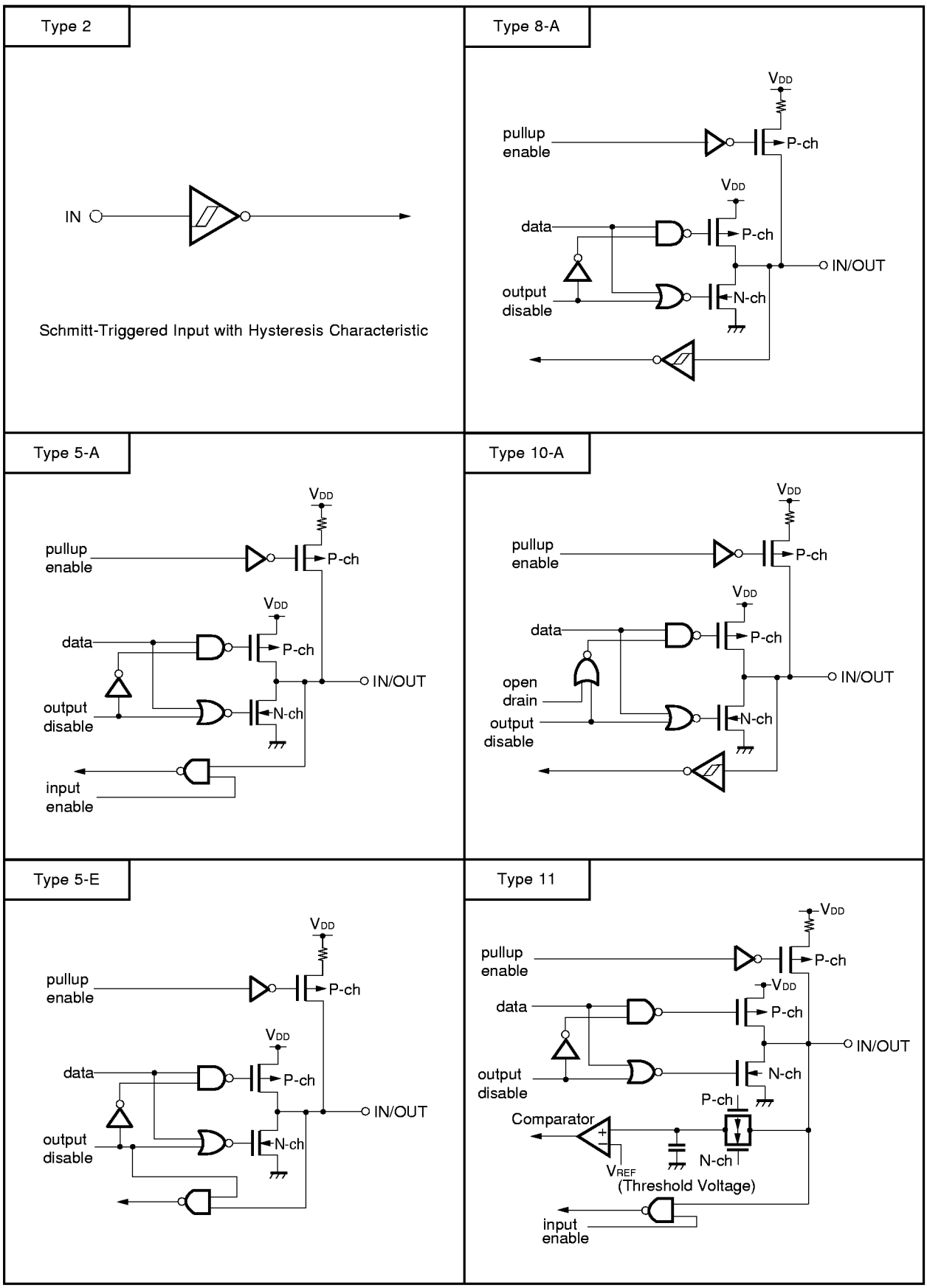
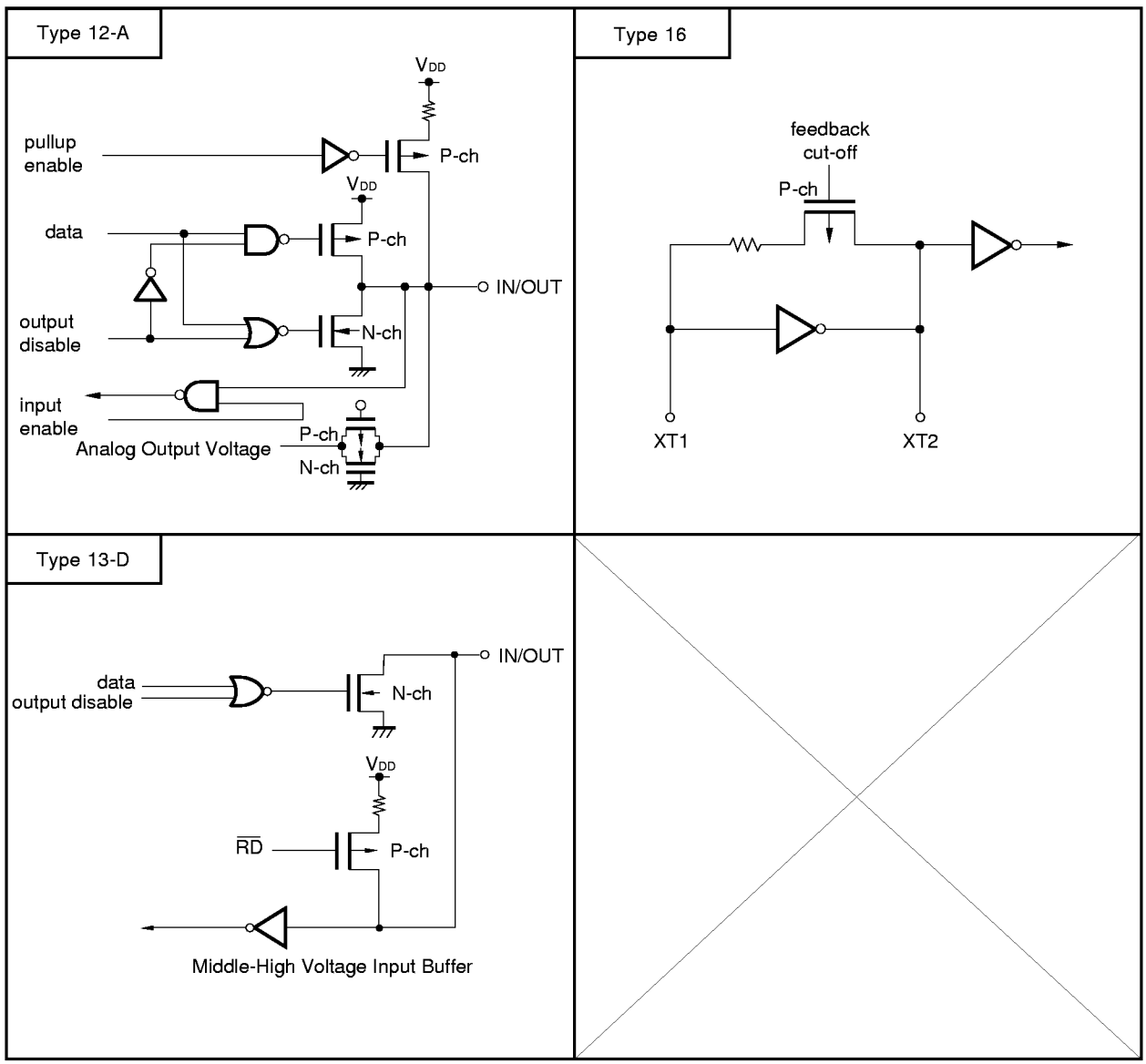


Figure 2-1. Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory map as that of mask ROM version having different internal memory (ROM, RAM) capacity.

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to C8H (μPD78P054)/CFH (μPD78P058).

Figure 3-1. Memory Size Switching Register Format (μPD78P054)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which makes the memory map the same as that of the various mask ROM versions.

Table 3-1. Memory Size Switching Register Setting Values (μPD78P054)

Target Mask ROM Version	IMS Setting Value
μPD78052	44H
μPD78053	C6H
μPD78054	C8H

Figure 3-2. Memory Size Switching Register Format (μPD78P058)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes Note
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Note Set the internal ROM capacity to 56 Kbytes or less when external device expansion function is used.

Table 3-2 shows the setting values of IMS which makes the memory map the same as that of the various mask ROM versions.

Table 3-2. Memory Size Switching Register Setting Values (μPD78P058)

Target Mask ROM Version	IMS Setting Value
μPD78052	44H
μPD78053	C6H
μPD78054	C8H
μPD78055	CAH
μPD78056	CCH
μPD78058	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS) (μPD78P058 ONLY)

This is a register to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size switching register (IXS), it is possible to get the same memory map as that of mask ROM version having different internal expansion RAM capacity.

The IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IXS to 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of Internal Expansion RAM Capacity
1	1	0	0	0 byte
1	0	1	0	1024 bytes
Other than above				Setting prohibited

Table 4-1 shows the setting values of IXS which makes the memory map the same as that of the various mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Version	IXS Setting Value
μPD78052	0CH
μPD78053	
μPD78054	
μPD78055	
μPD78056	
μPD78058	0AH

Remark Even if the μPD78P058 program that includes "MOV IXS, #0CH" is implemented on the μPD78052, 78053, 78054, 78055, or 78056, its operation will not be affected.

5. PROM PROGRAMMING

The μPD78P054 and 78P058 have an on-chip 32-Kbyte and 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For connecting unused pins, refer to **PIN CONFIGURATIONS (Top View) (2) PROM programming mode**.

Caution The program of the μPD78P054 should be written in the address range 0000H to 7FFFH (the last address, 7FFFH, should be specified). The program of the μPD78P058 should be written in the address range 0000H to EFFFH (the last address, EFFFH, should be specified). Writing cannot be performed with a PROM programmer that cannot specify the write addresses.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remark × : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P054s or 78P058s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1-page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly, after the write.

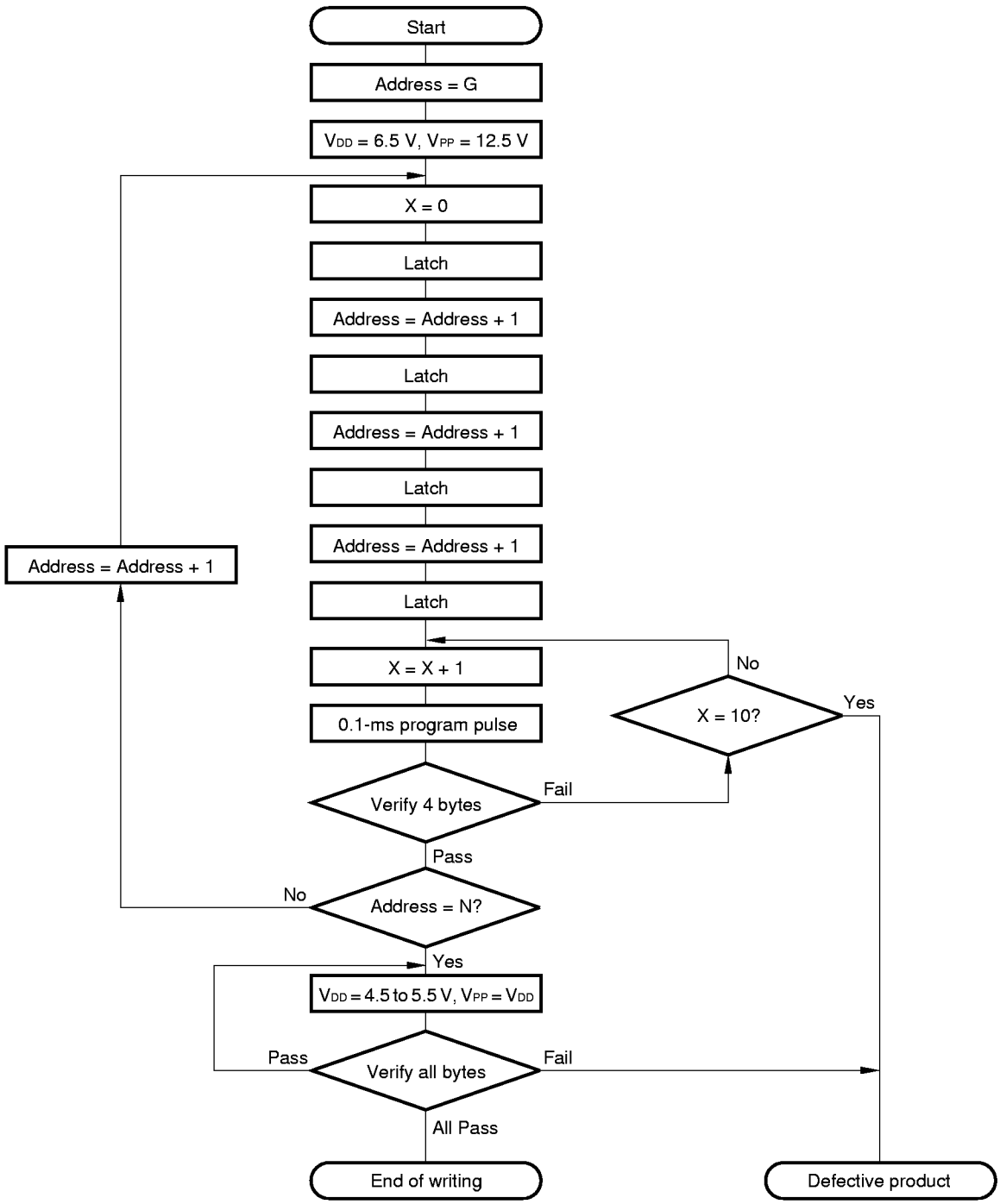
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin, and D0 to D7 pins of multiple μPD78P054s or 78P058s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flowchart



Remark G = Start address
N = Program last address

Figure 5-2. Page Program Mode Timing

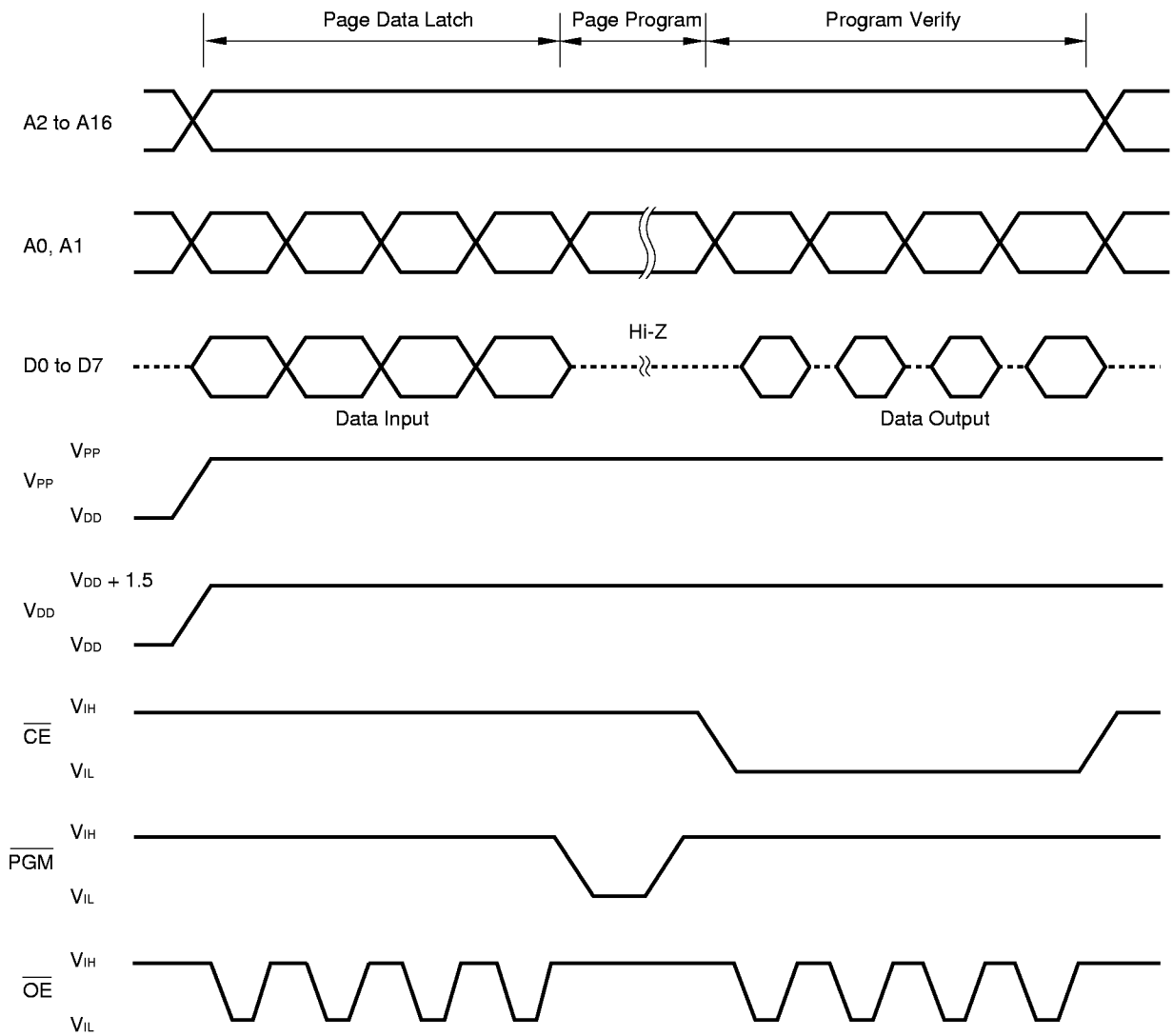
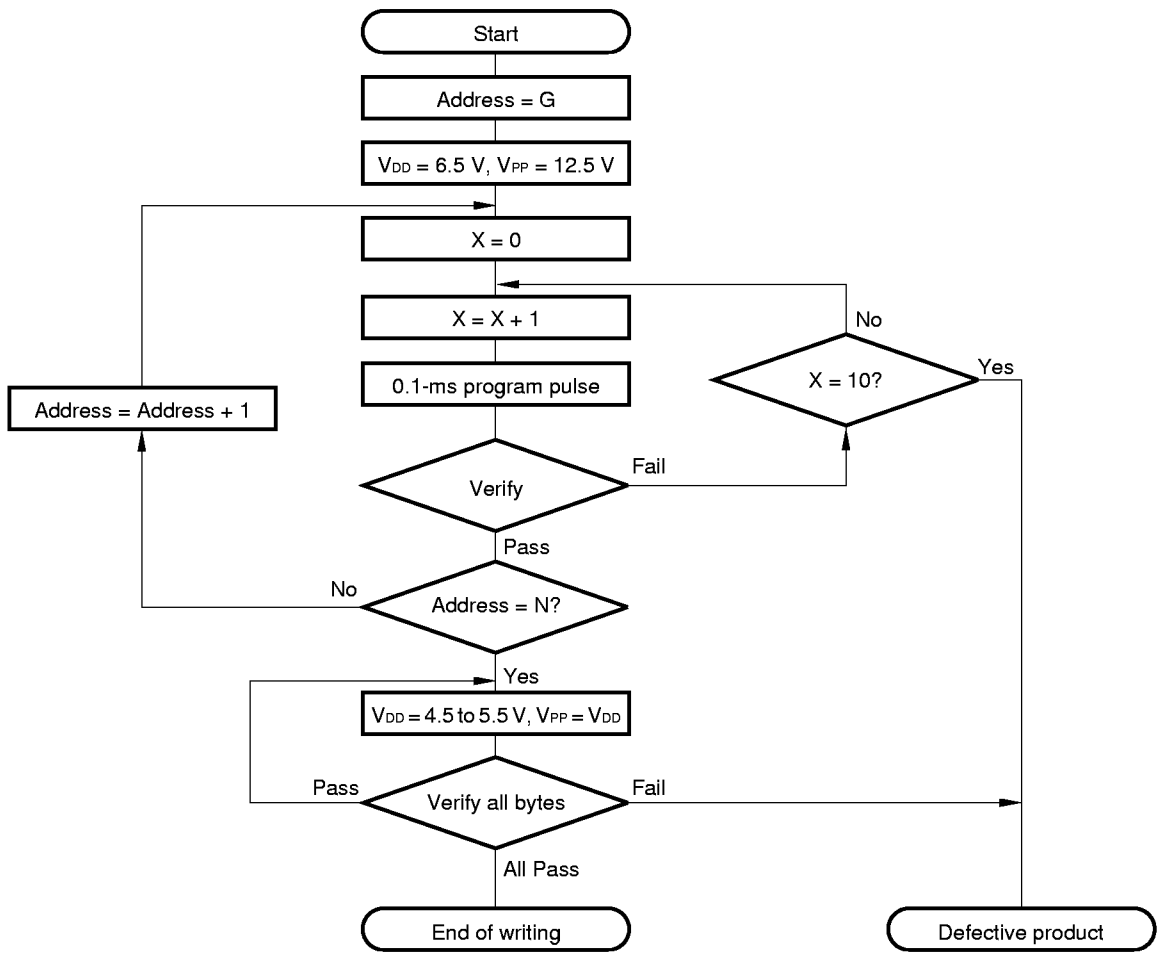
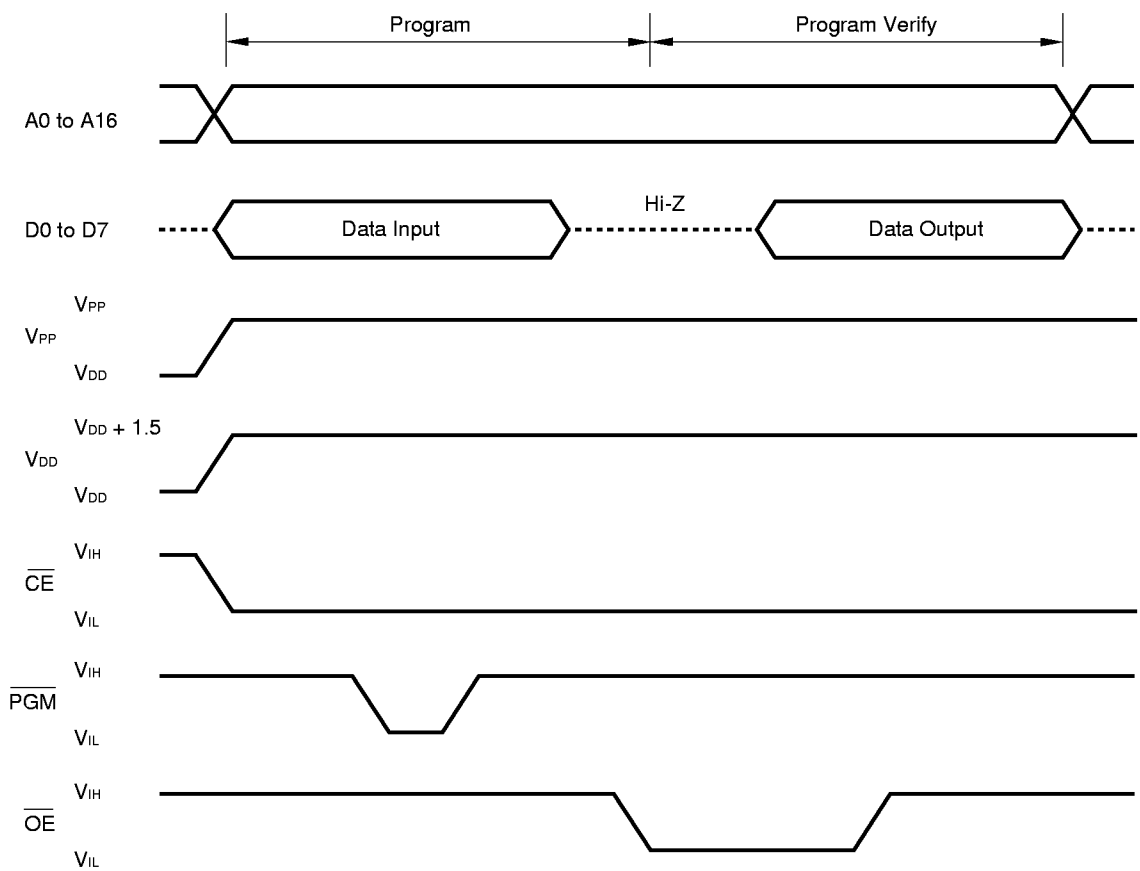


Figure 5-3. Byte Program Mode Flowchart



Remark G = Start address
N = Program last address

Figure 5-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **PIN CONFIGURATIONS (Top View) (2) PROM programming mode**.

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

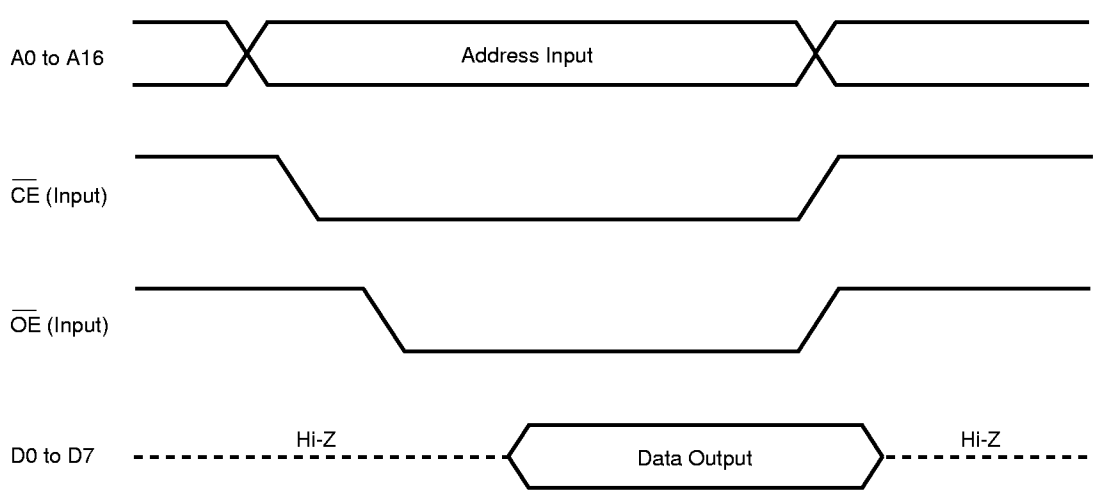
(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings



6. ERASURE METHOD (μPD78P054KK-T, 78P058KK-T ONLY)

The μPD78P054KK-T and 78P058KK-T are capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the data, irradiate light having a wavelength of less than about 400 nm to the window on the top of the package. Normally, ultraviolet rays of 254-nm wavelength should be used. Volume of irradiation required to completely erase the data is as follows:

★ • UV intensity × erasing time : 30 W•s/cm² or more

★ • Erasing time : 40 minutes or more (When a UV lamp of 12 mW/cm² is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided on the UV lamp, remove the filter during the erasure process.

7. ERASURE WINDOW OPAQUE FILM (μPD78P054KK-T, 78P058KK-T ONLY)

To protect from unintentional erasure by other than EPROM erasure lamp light, or to protect internal circuits other than EPROM from malfunction due to light coming in through the window, mask the window with the attached opaque film except when EPROM erasure is performed.

8. SCREENING OF ONE-TIME PROM VERSIONS

The one-time PROM versions (μPD78P054GC-3B9, 78P054GC-8BT, 78P054GK-BE9, and 78P058GC-8BT) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the conditions below.

Storage Temperature	Storage Time
125°C	24 hours

At present, a fee is charged by NEC for one-time PROM writing, marking, screening, and verify service for the QTOP Microcontroller. For details, contact your sales representative.

9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

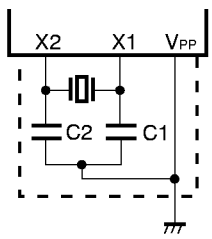
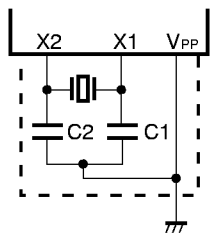
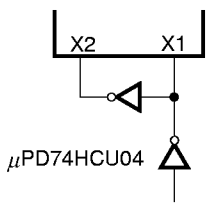
Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch open-drain	–0.3 to +16	V
	V_{I3}	A9	PROM programming mode	–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		–15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		–15	mA
Output current, low	I_{OL}[Note]	Per pin	peak value	30	mA
			r.m.s. value	15	mA
		Total for P50 to P55	peak value	100	mA
			r.m.s. value	70	mA
		Total for P56, P57, P60 to P63	peak value	100	mA
			r.m.s. value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	peak value	50	mA
			r.m.s. value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	peak value	50	mA
			r.m.s value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note r.m.s. values should be calculated as follows: [r.m.s. value] = [peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

s specified otherwise, alternate-function pin characteristics are the same as port pin characteris-

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.

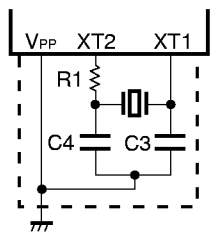
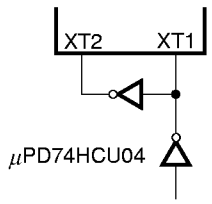
2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by broken lines to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.

★ **2.** This is the time required for oscillation to stabilize after V_{DD} has reached the MIN. of oscillation voltage range.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by broken lines to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANT

(1) μPD78P054

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.0MC3	4.0	Built-in	Built-in	2.0	6.0
	CCR5.0MC3	5.0	Built-in	Built-in	2.0	6.0

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (kHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku Corp.	DT-38 (1TA252E00, load capacitance 12.5 pF)	32.768	22	22	330	2.0	6.0

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

(2) μPD78P058

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –20 to +80°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	KBR-4.19MKS	4.19	Built-in	Built-in	2.0	6.0

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CST5.00MGW	5.0	Built-in	Built-in	2.7	6.0
	CSA5.00MG	5.0	30	30	2.7	6.0

★ **Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.**

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open-drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V[Note]	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V[Note]	0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, N-ch open-drain, with pull-up resistor (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When XT1/P07 pin is used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

cified otherwise, alternate-function pin characteristics are the same as port pin characteris-

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3[Note 1]	μA
Output leakage current, high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor[Note 2]	R_2	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. In P60 to P63, a low-level input leakage current of –200 μA (MAX.) flows only during the 1.5-clock interval (no wait) when the read instruction is executed for port 6 (P6) or port mode register 6 (PM6). Other than the 1.5-clock interval when the read instruction is executed, the current is –3 μA (MAX.).

2. A software pull-up resistor can only be used in the range V_{DD} = 2.7 to 6.0 V.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

	Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
	Supply current[Note 5]	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 1]		5	15	mA
				V_{DD} = 3.0 V ±10%[Note 2]		0.7	2.1	mA
				V_{DD} = 2.2 V ±10%[Note 2]		0.4	1.2	mA
			5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%[Note 1]		9.0	27.0	mA
				V_{DD} = 3.0 V ±10%[Note 2]		1.0	3.0	mA
		I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%		1.4	4.2	mA
				V_{DD} = 3.0 V ±10%		0.5	1.5	mA
				V_{DD} = 2.2 V ±10%		280	840	μA
			5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%		1.6	4.8	mA
				V_{DD} = 3.0 V ±10%		0.65	1.95	mA
		I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 6]	V_{DD} = 5.0 V ±10%		135	270	μA
				V_{DD} = 3.0 V ±10%		95	190	μA
				V_{DD} = 2.2 V ±10%		70	140	μA
		I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 6]	V_{DD} = 5.0 V ±10%		25	55	μA
				V_{DD} = 3.0 V ±10%		5	15	μA
				V_{DD} = 2.2 V ±10%		2.5	12.5	μA
★		I_{DD5}	XT1 = V_{DD} STOP mode Feedback resistor used	V_{DD} = 5.0 V ±10%		1	30	μA
				V_{DD} = 3.0 V ±10%		0.5	10	μA
				V_{DD} = 2.2 V ±10%		0.3	10	μA
★		I_{DD6}	XT1 = V_{DD} STOP mode Feedback resistor not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
				V_{DD} = 3.0 V ±10%		0.05	10	μA
				V_{DD} = 2.2 V ±10%		0.05	10	μA

Notes 1. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

2. Low-speed mode operation (when PCC is set to 04H).

3. Main system clock $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H).

4. Main system clock $f_{XX} = f_X$ operation (when OSMS is set to 01H).

5. A current flowing in V_{DD} and AV_{DD} pins. Not including the current flowing in A/D converter, D/A converter, and on-chip pull-up resistor.

6. When the main system clock operation is stopped.

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating on main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
				2.2		64	μs
		Operating on main system clock (f_{XX} = 5.0 MHz)Note 2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.4		32	μs
			2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
★		Operating on subsystem clock		40Note 3	122	125	μs
TI01, TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
				0		275	kHz
TI00 input high-/low-level width	t_{TIH}, t_{TIL}			$8/f_{sam}$Note 4			μs
TI01, TI1, TI2, input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		100			ns
				1.8			μs
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0		$8/f_{sam}$Note 4			μs
		INTP1 to INTP6, KR0 to KR7	V_{DD} = 2.7 to 6.0 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V		10			μs
				20			μs

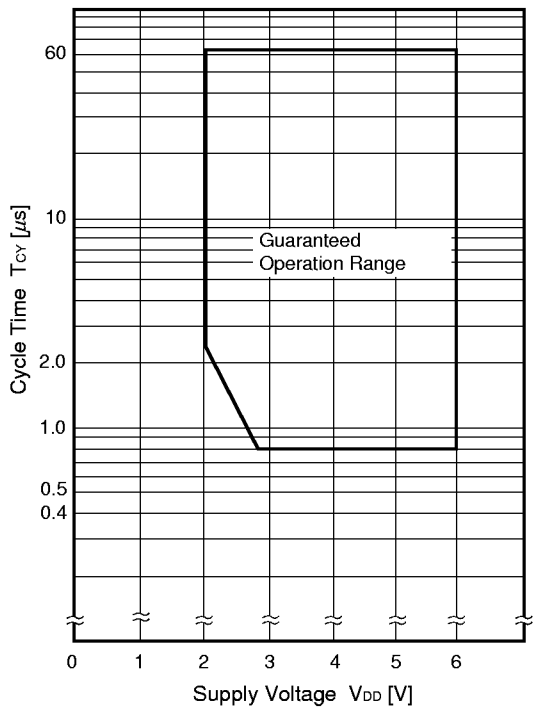
Notes 1. Main system clock f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

2. Main system clock f_{XX} = f_X operation (when OSMS is set to 01H).

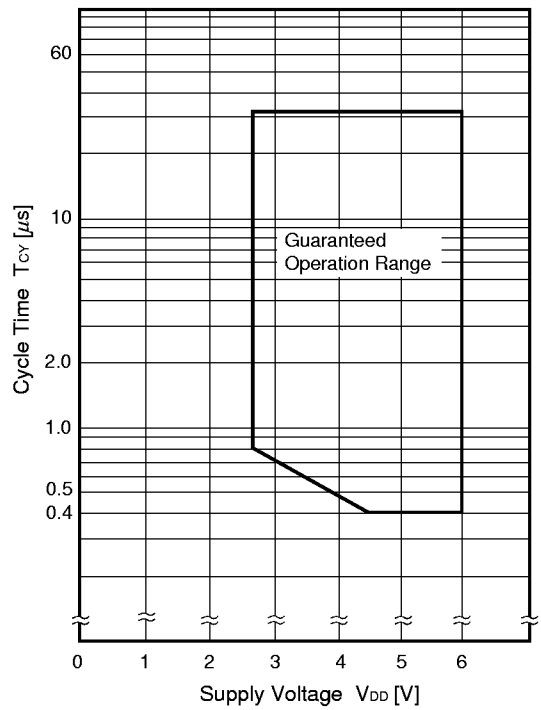
★ **3.** The value when the external clock is used. When the crystal resonator is used, the value is 114 μs (MIN.).

4. f_{sam} can be selected as $f_{XX}/2^N$, f_{XX}/32, f_{XX}/64, or f_{XX}/128 (N = 0 to 4) by bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (SCS).

T_{CY} vs V_{DD} (Main System Clock f_{XX} = f_X/2 Operation)



T_{CY} vs V_{DD} (Main System Clock f_{XX} = f_X Operation)



(2) Read/Write Operations

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY} - 50$		ns
Address setup time	t_{ADS}		$0.85t_{CY} - 50$		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY} - 80$	ns
	t_{ADD2}			$(4 + 2n)t_{CY} - 100$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY} - 100$	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY} - 100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY} - 60$		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY} - 50$	ns
	t_{RDWT2}			$2t_{CY} - 60$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY} - 60$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY} - 100$		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY} + 20$		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.85t_{CY} - 10$	$1.15t_{CY} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.85t_{CY} - 50$	$1.15t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY} + 40$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY} + 40$	$3.15t_{CY} + 40$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY} + 30$	$3.15t_{CY} + 30$	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0 V	t_{CY} – 80		ns
			t_{CY} – 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} – 10		ns
			0.37t_{CY} – 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0 V		(3 + 2n)t_{CY} – 160	ns
				(3 + 2n)t_{CY} – 320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0 V		(4 + 2n)t_{CY} – 200	ns
				(4 + 2n)t_{CY} – 300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0 V		(1.4 + 2n)t_{CY} – 70	ns
				(1.37 + 2n)t_{CY} – 120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0 V		(2.4 + 2n)t_{CY} – 70	ns
				(2.37 + 2n)t_{CY} – 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0 V	(1.4 + 2n)t_{CY} – 20		ns
			(1.37 + 2n)t_{CY} – 20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0 V		t_{CY} – 100	ns
				t_{CY} – 200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0 V		2t_{CY} – 100	ns
				2t_{CY} – 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 60		ns
			(2.37 + 2n)t_{CY} – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} – 20		ns
			(2.37 + 2n)t_{CY} – 20		ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(2/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0 V	$0.4t_{CY}$ – 30		ns
			$0.37t_{CY}$ – 50		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0 V	$1.4t_{CY}$ – 30		ns
			$1.37t_{CY}$ – 50		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 6.0 V	$0.4t_{CY}$ – 20		ns
			$0.37t_{CY}$ – 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 6.0 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}	V_{DD} = 2.7 to 6.0 V	$0.6t_{CY}$ + 180	$2.6t_{CY}$ + 180	ns
			$0.63t_{CY}$ + 350	$2.63t_{CY}$ + 350	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}	V_{DD} = 2.7 to 6.0 V	$0.6t_{CY}$ + 120	$2.6t_{CY}$ + 120	ns
			$0.63t_{CY}$ + 240	$2.63t_{CY}$ + 240	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 6.0 V	$t_{KCY1}/2 - 50$			ns
			$t_{KCY1}/2 - 100$			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100pF[Note]			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	$t_{KCY5}/2 - 160$			ns
				$t_{KCY5}/2 - 190$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 6.0 V	$t_{KCY7}/2 - 50$			ns
			$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 6.0 V	$t_{KCY9}/2 - 50$			ns
			$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF[Note]			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	V_{DD} = 2.7 to 6.0 V	$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
			$t_{KCY9} - 60$		$t_{KCY9} + 60$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			200			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

★ **(c) Serial interface channel 2**

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 6.0 V	$t_{KCY11}/2 - 50$			ns
			$t_{KCY11}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF[Note]			300	ns

Note C is the SO2 output line load capacitance.

(ii) UART mode (Dedicated baud rate generator output)

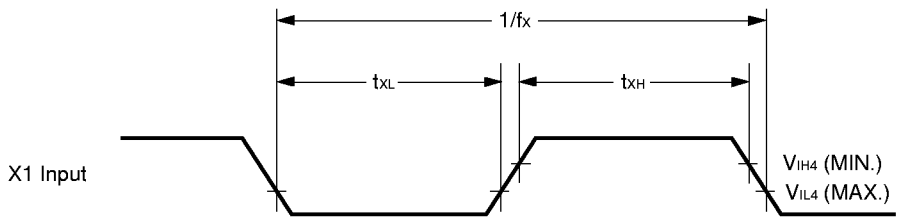
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

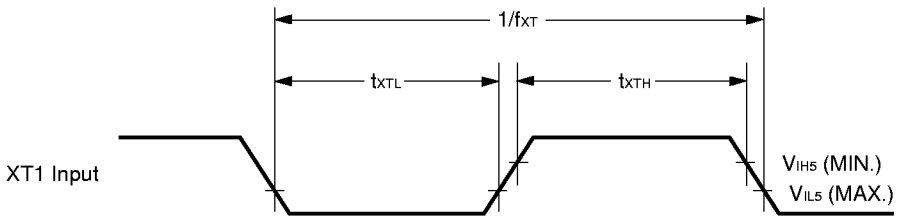
(iii) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R12}, t_{F12}	V_{DD} = 4.5 to 6.0 V, when not using external device expansion function			1000	ns
					160	ns

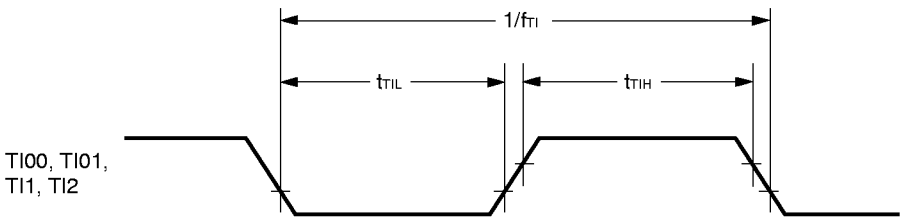
AC Timing Test Point (Excluding X1, XT1 Inputs)

Clock Timing



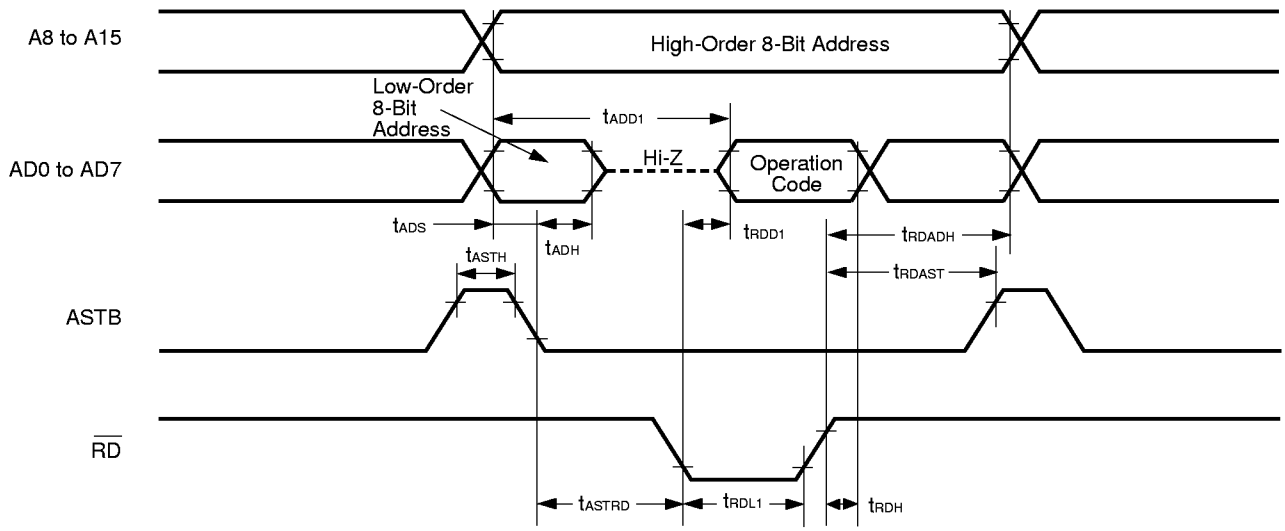


TI Timing

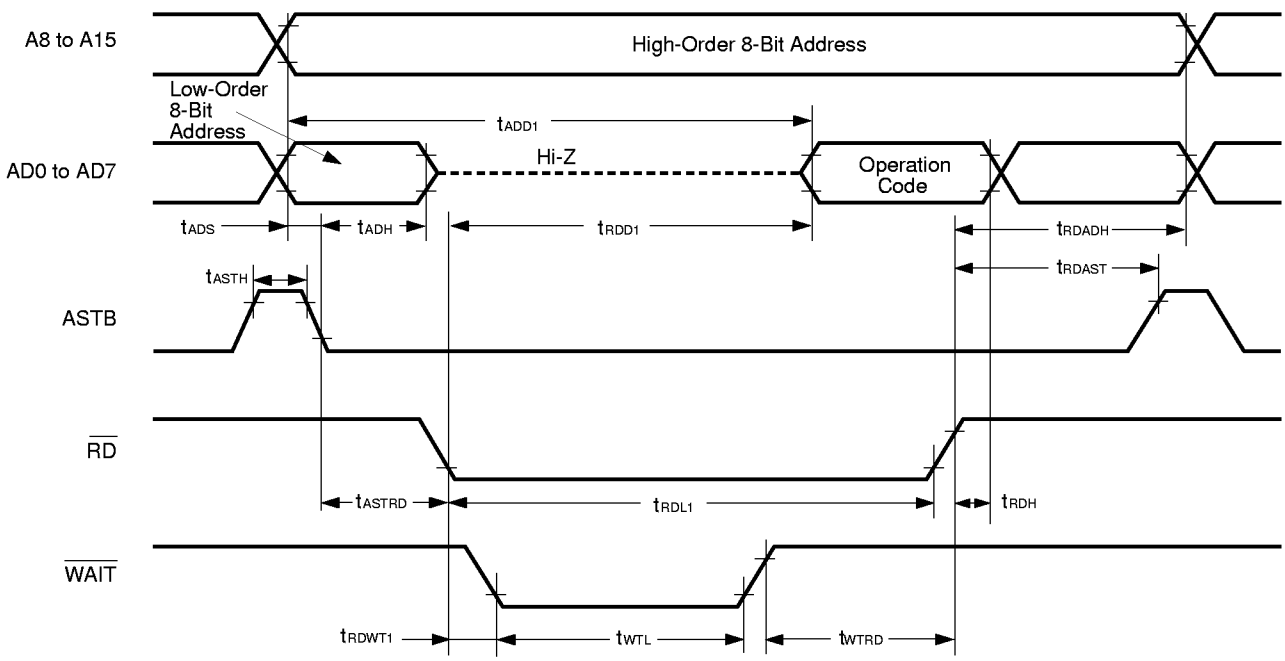


Read/Write Operations

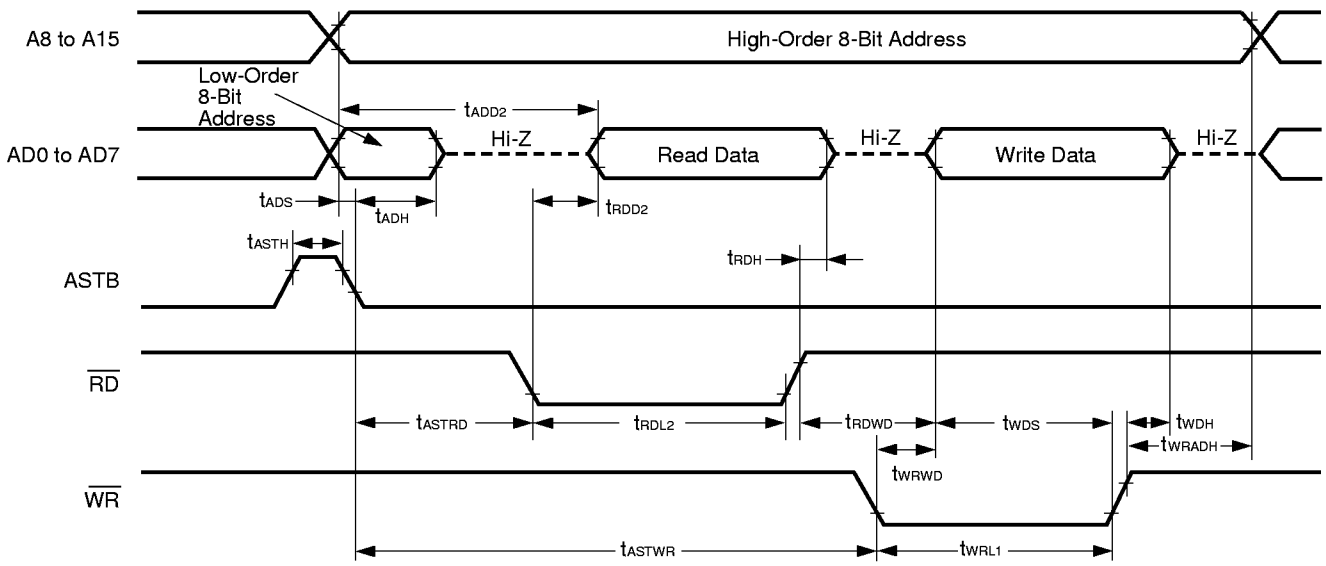
External fetch (no wait):



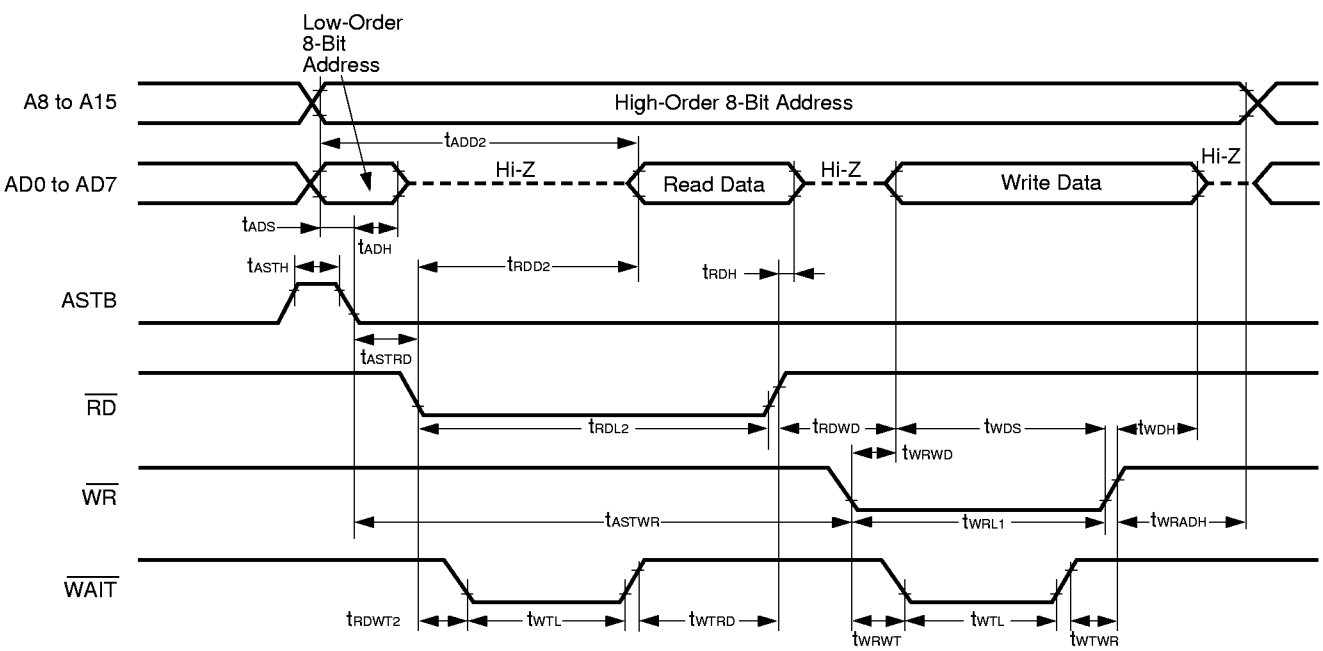
External fetch (wait insertion):



External data access (no wait):

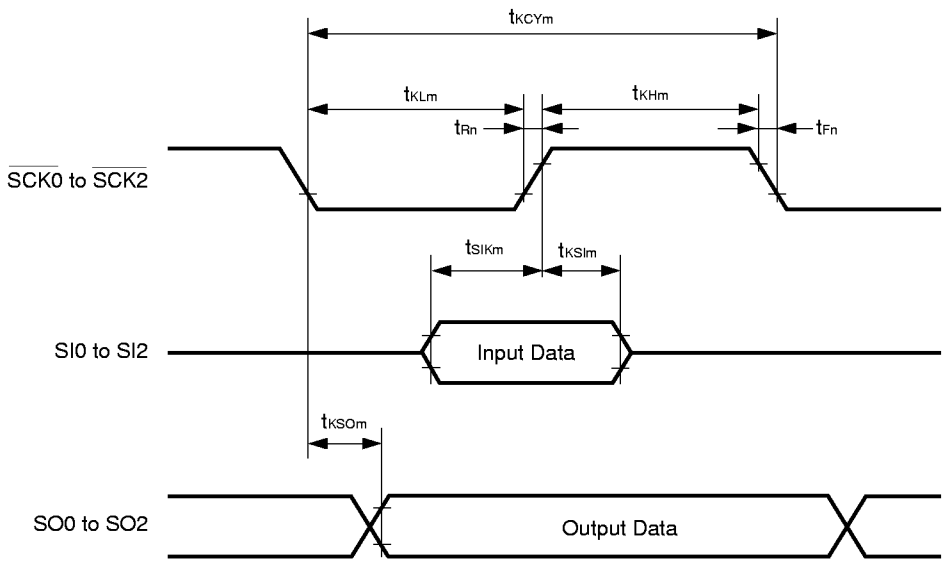


External data access (wait insertion):



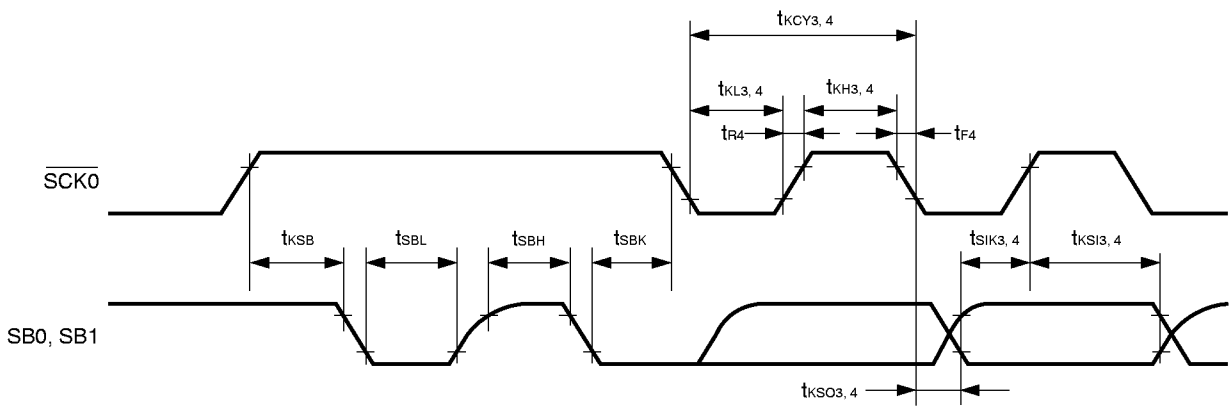
Serial Transfer Timing

3-wire serial I/O mode:

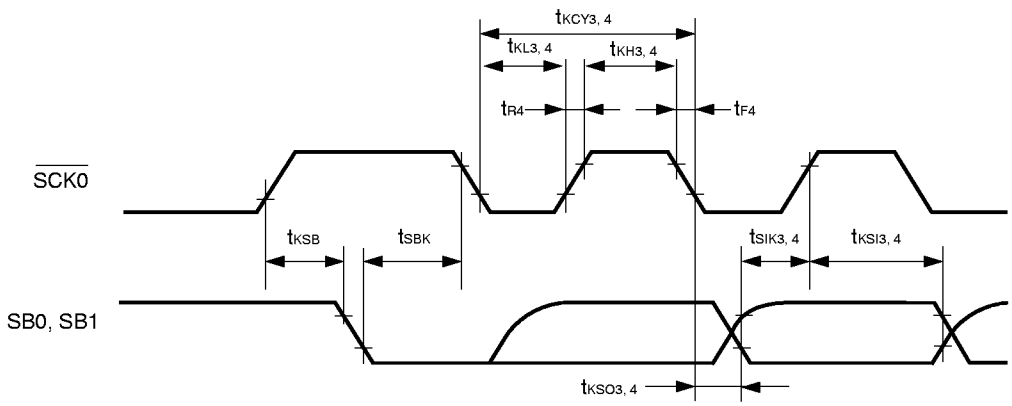


Remark m = 1, 2, 7, 8, 11
n = 2, 8

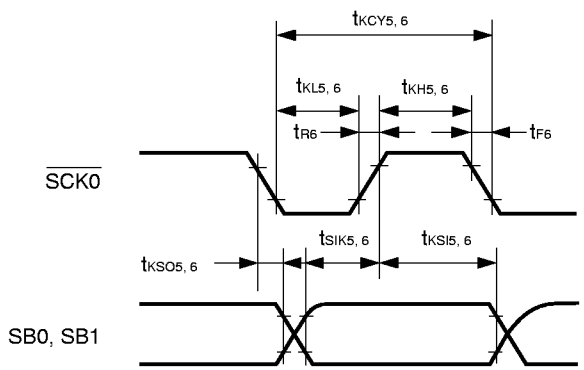
SBI mode (bus release signal transfer):



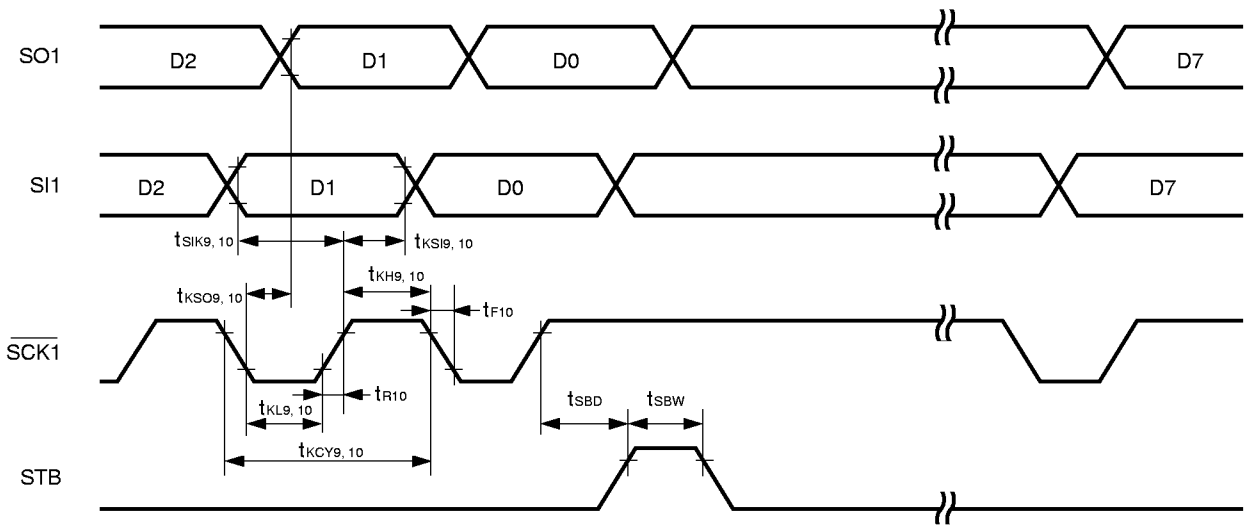
SBI mode (command signal transfer):



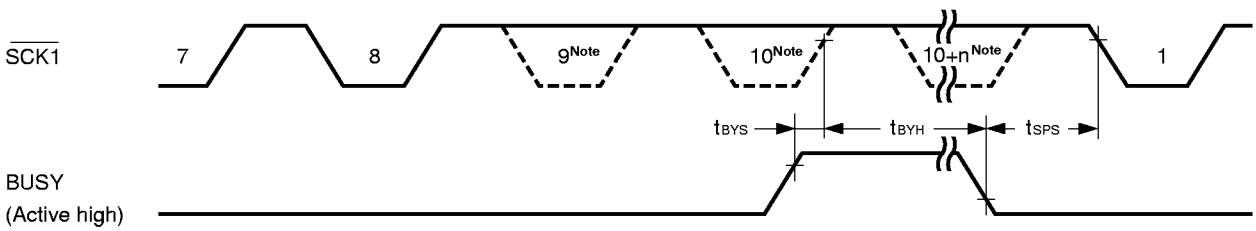
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

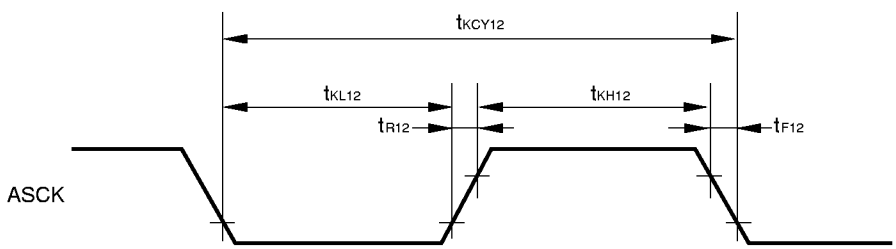


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external clock input):



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}	μPD78P054			1.0	%
			μPD78P058			1.4	%
Conversion time	t_{CONV}			19.1		200	μs
Sampling time	t_{SAMP}			12/f_{XX}			μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}			2.7		AV_{DD}	V
AV_{REF0}-AV_{SS} resistance	R_{AIREF0}			4			kΩ

Note Excluding quantization error (±1/2LSB). Shown as a percentage of the full scale value.

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ[Note 1]				1.2	%
		R = 4 MΩ[Note 1]				0.8	%
		R = 10 MΩ[Note 1]				0.6	%
Settling time		C = 30 pF[Note 1]	4.5 V ≤ AV_{REF1} ≤ 6.0 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.0 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_{O0}	DACS0 = 55H			10		kΩ
	R_{O1}	DACS1 = 55H			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
AV_{REF1} current	AI_{REF1}	**Note 2**				1.5	mA

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

Remark DACS0, DACS1 : D/A conversion value setting register 0, 1

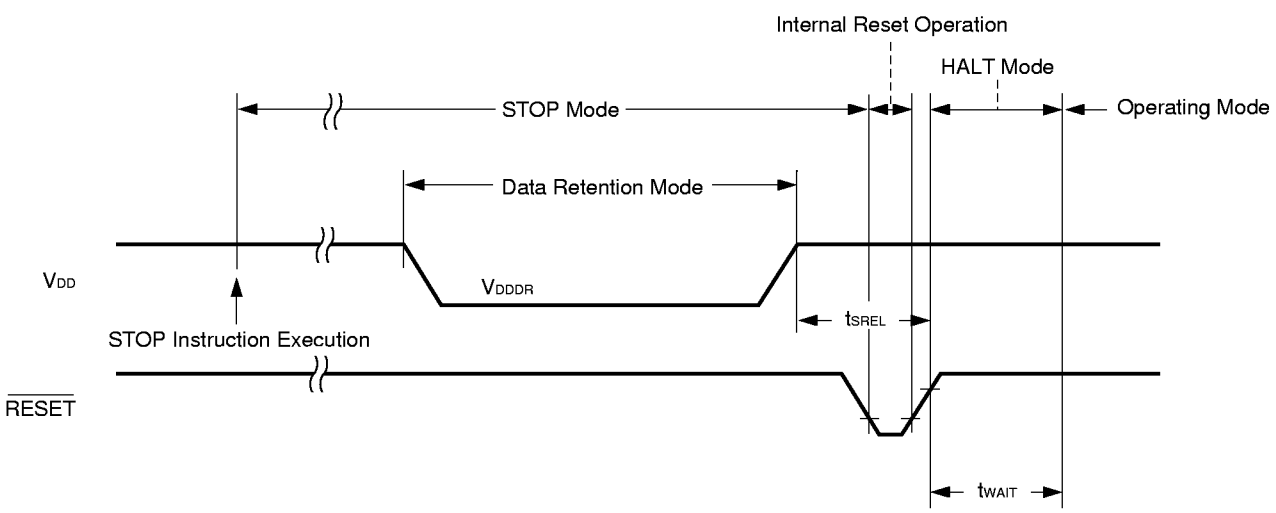
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stopped, feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt request		**Note**		ms

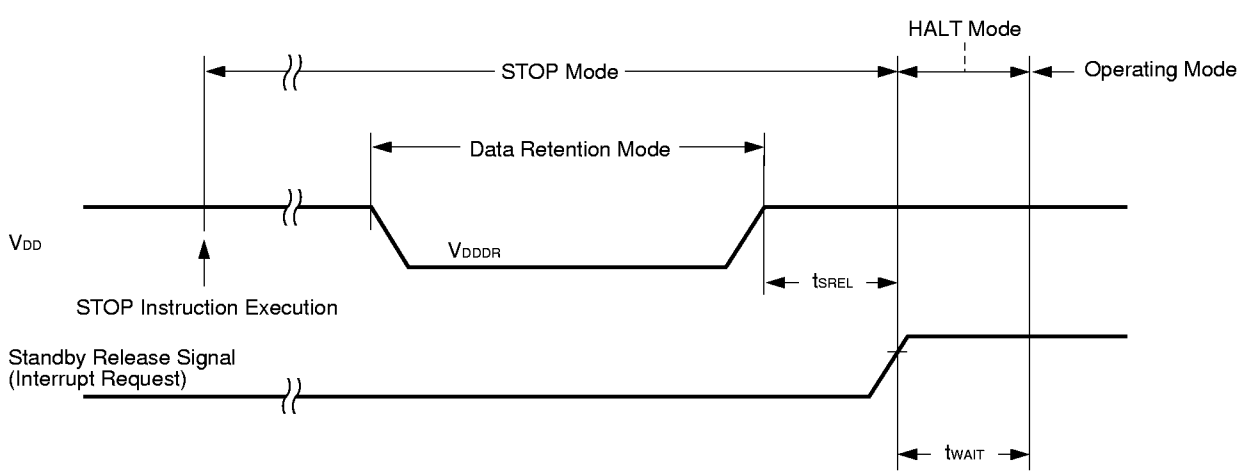
Note $2^{12}/fxx$, or $2^{14}/fxx$ through $2^{17}/fxx$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark fxx : Main system clock frequency (fx or fx/2)
fx : Main system clock oscillation frequency

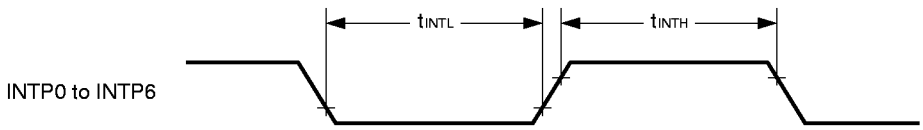
Data Retention Timing (STOP mode release by $\overline{RESET}$)



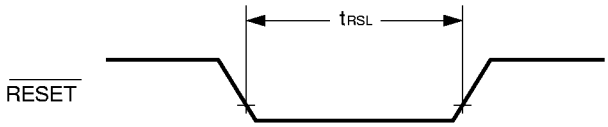
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding symbols for the μPD27C1001A.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$↑)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}$↓	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ set time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$↑)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}$↓	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding symbols for the μPD27C1001A.

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

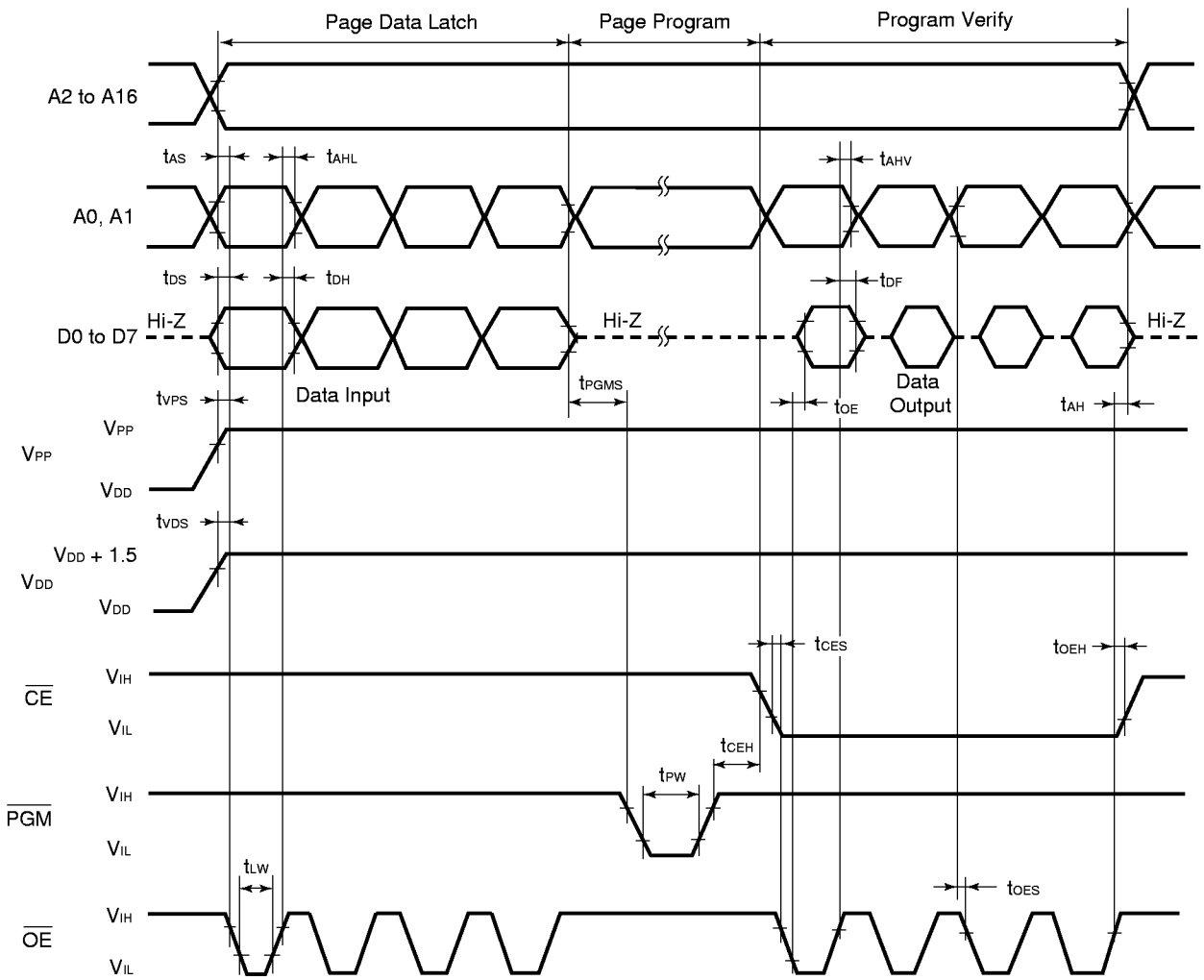
Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding symbols for the μPD27C1001A.

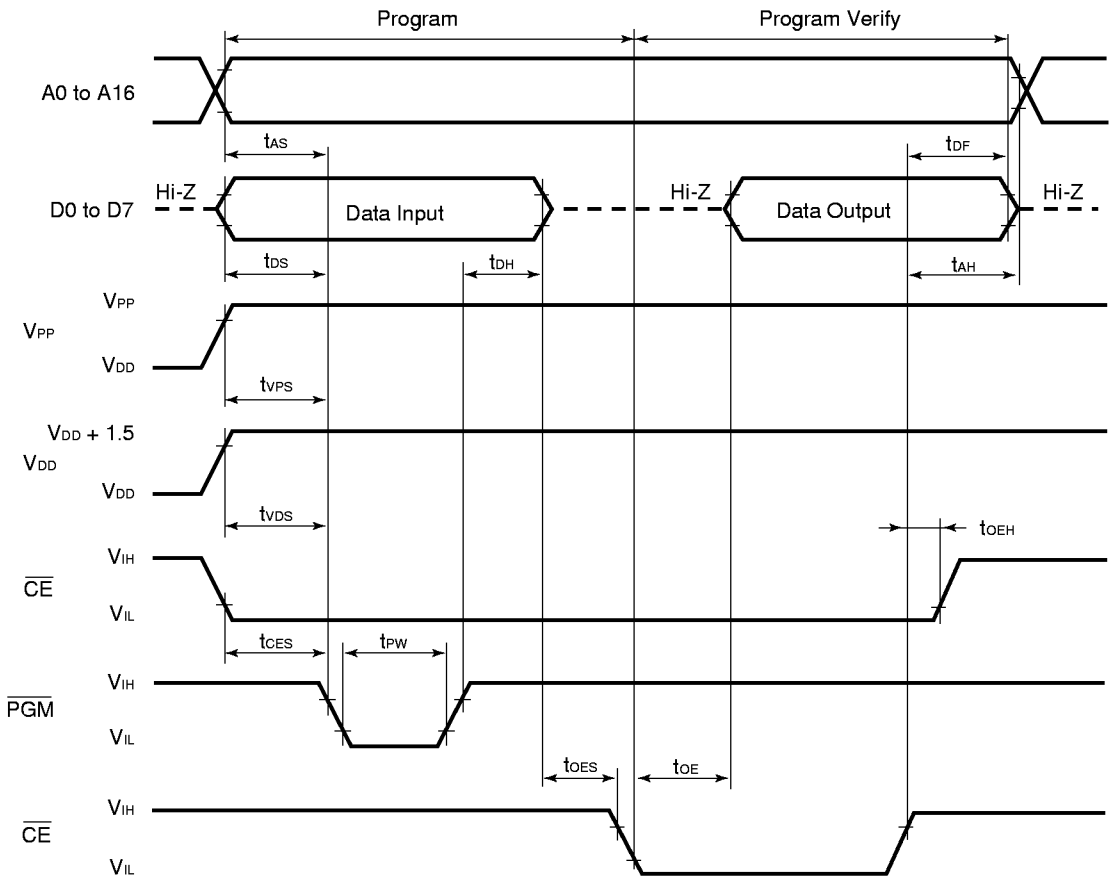
(3) PROM Programming Mode Setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

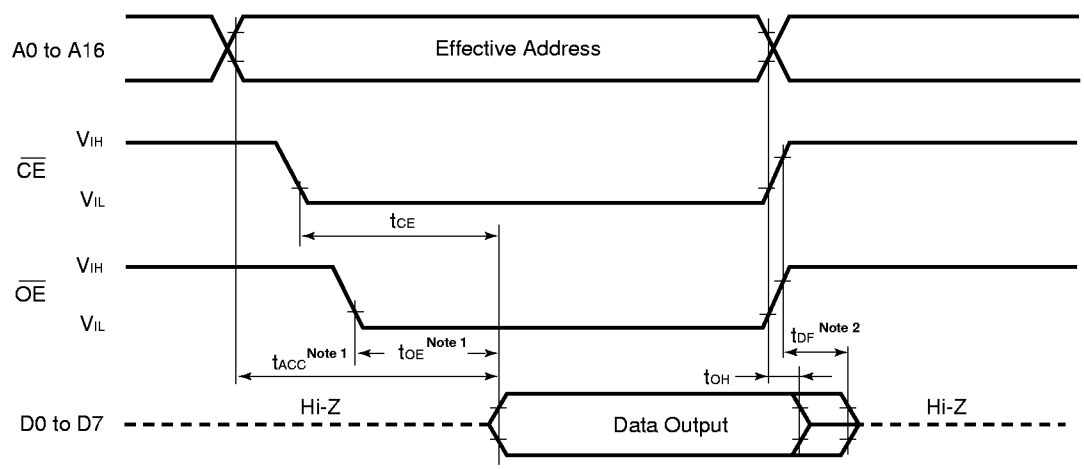


Cautions 1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

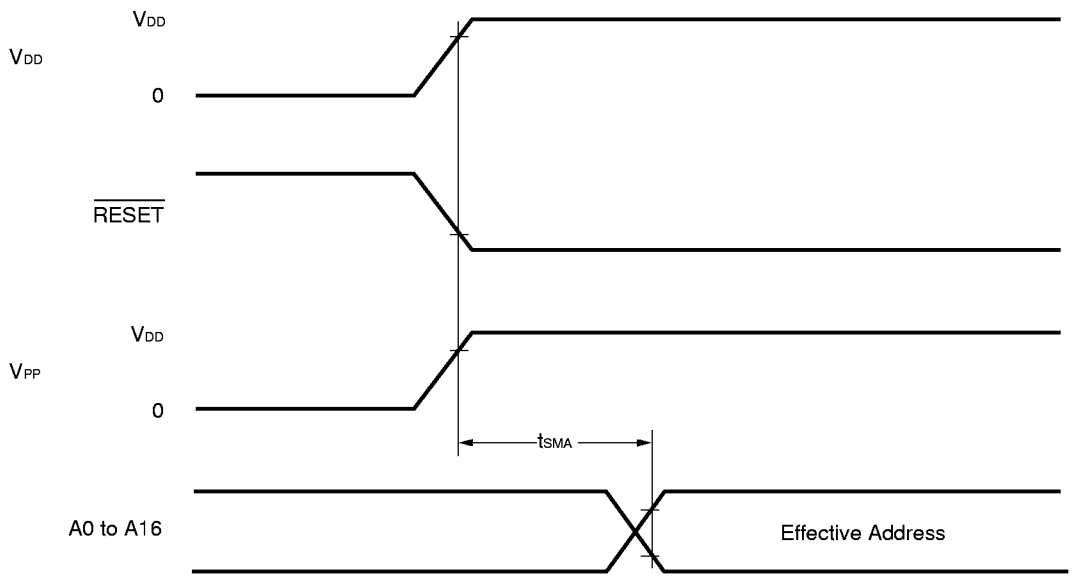
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC} - t_{OE}$.

: the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

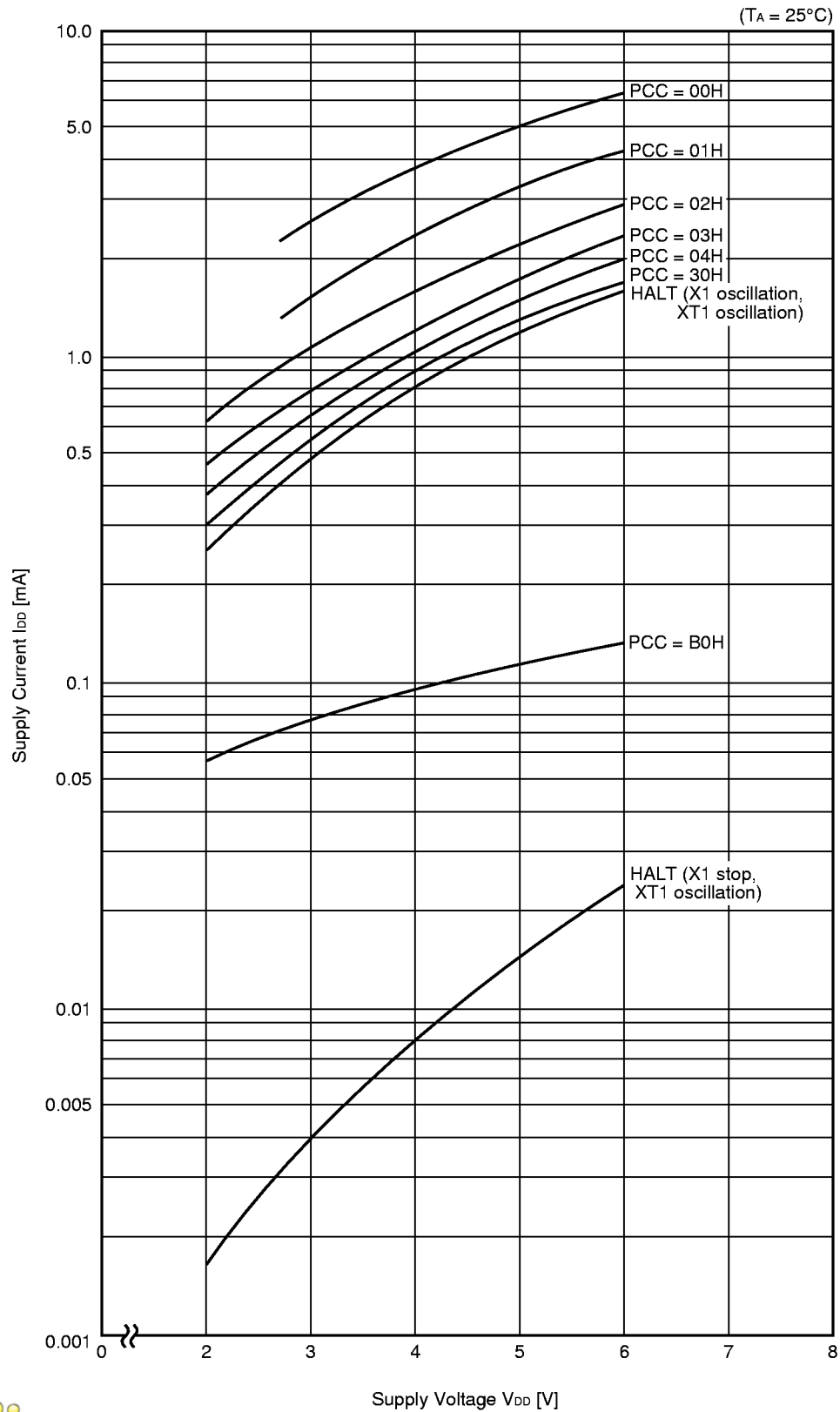
PROM Programming Mode Setting Timing



10. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

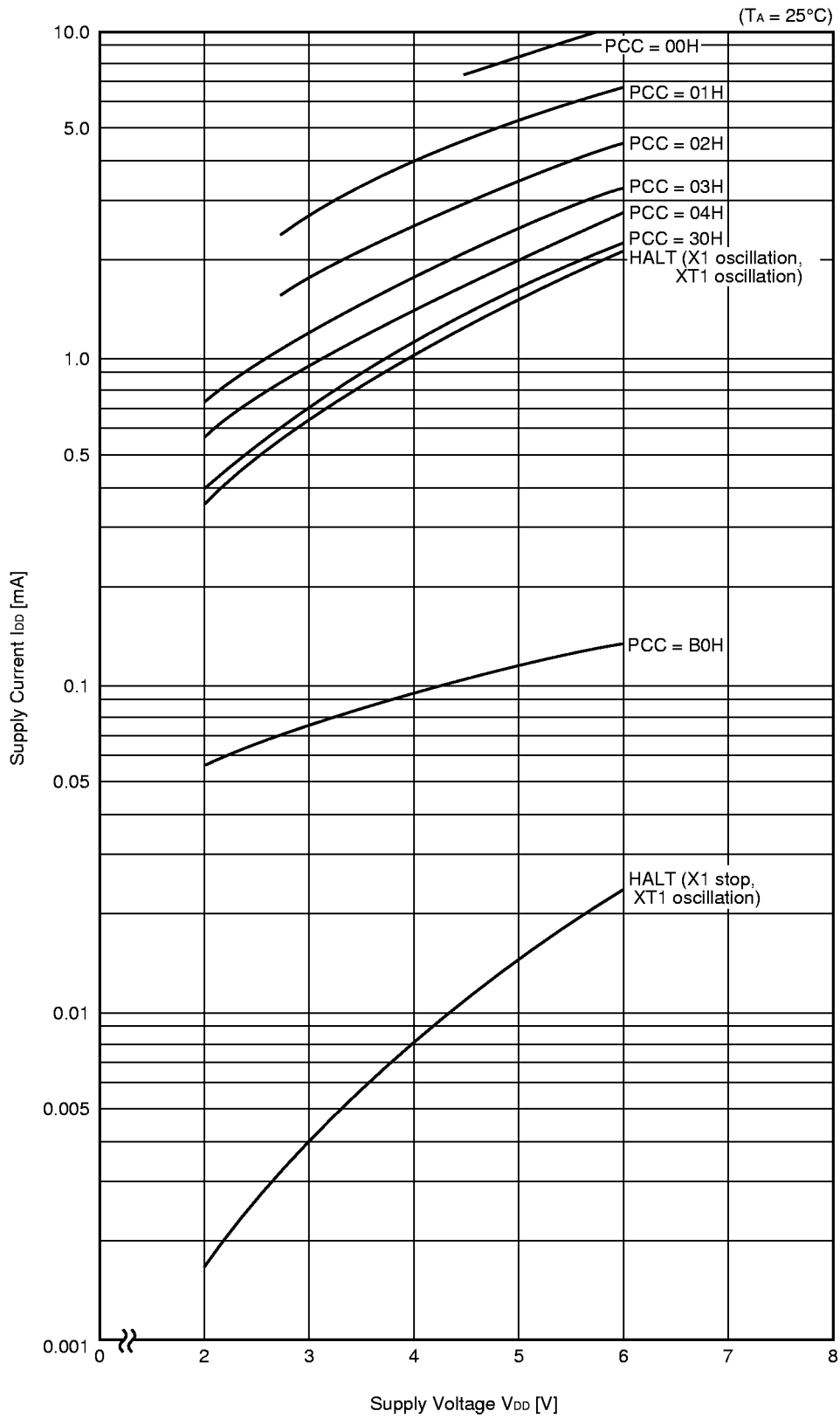
(1) Characteristic curves of μPD78P054 (1/2)

I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



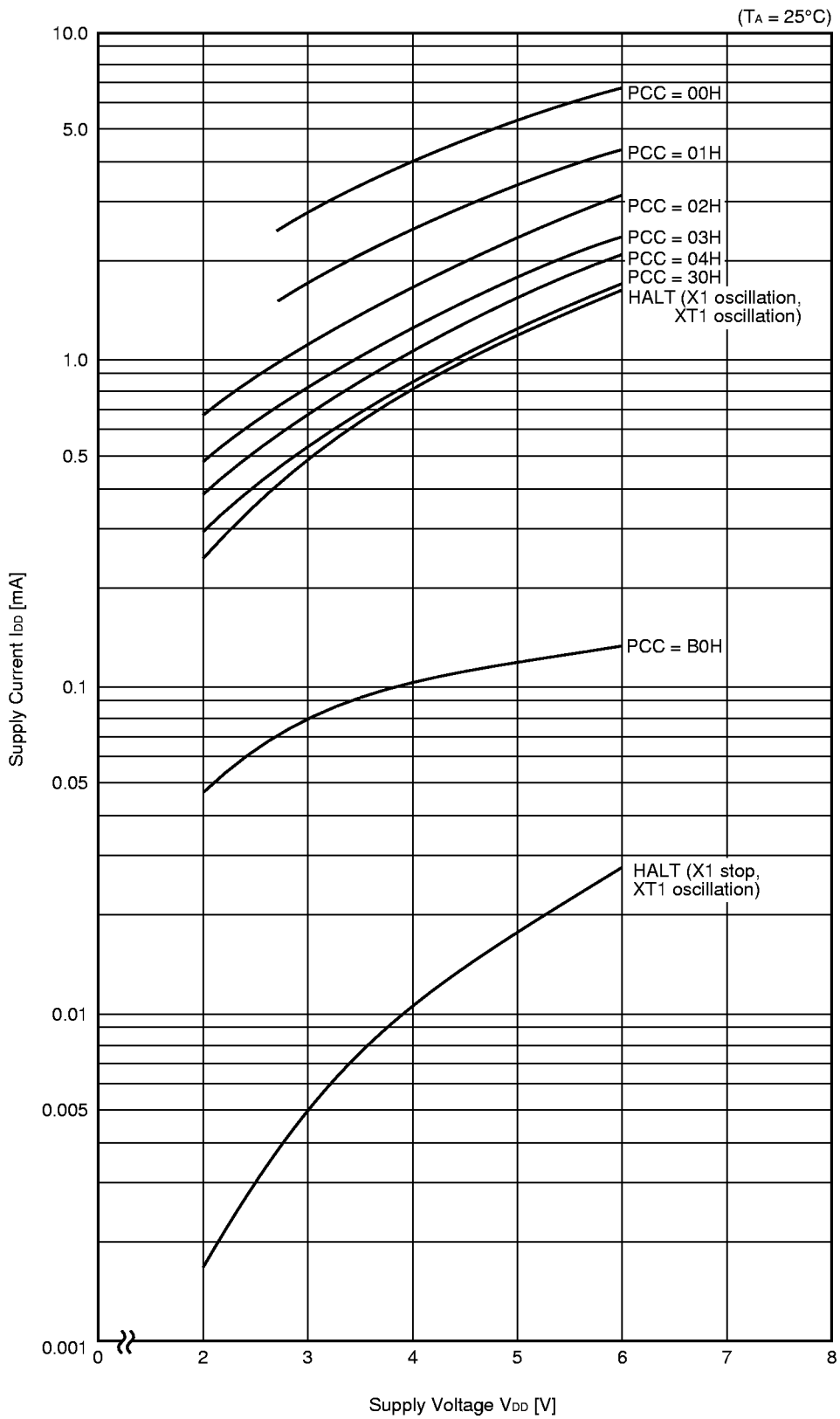
(1) Characteristic curves of μPD78P054 (2/2)

I_{DD} vs V_{DD} (f_X = f_{XX} = 5.0 MHz)



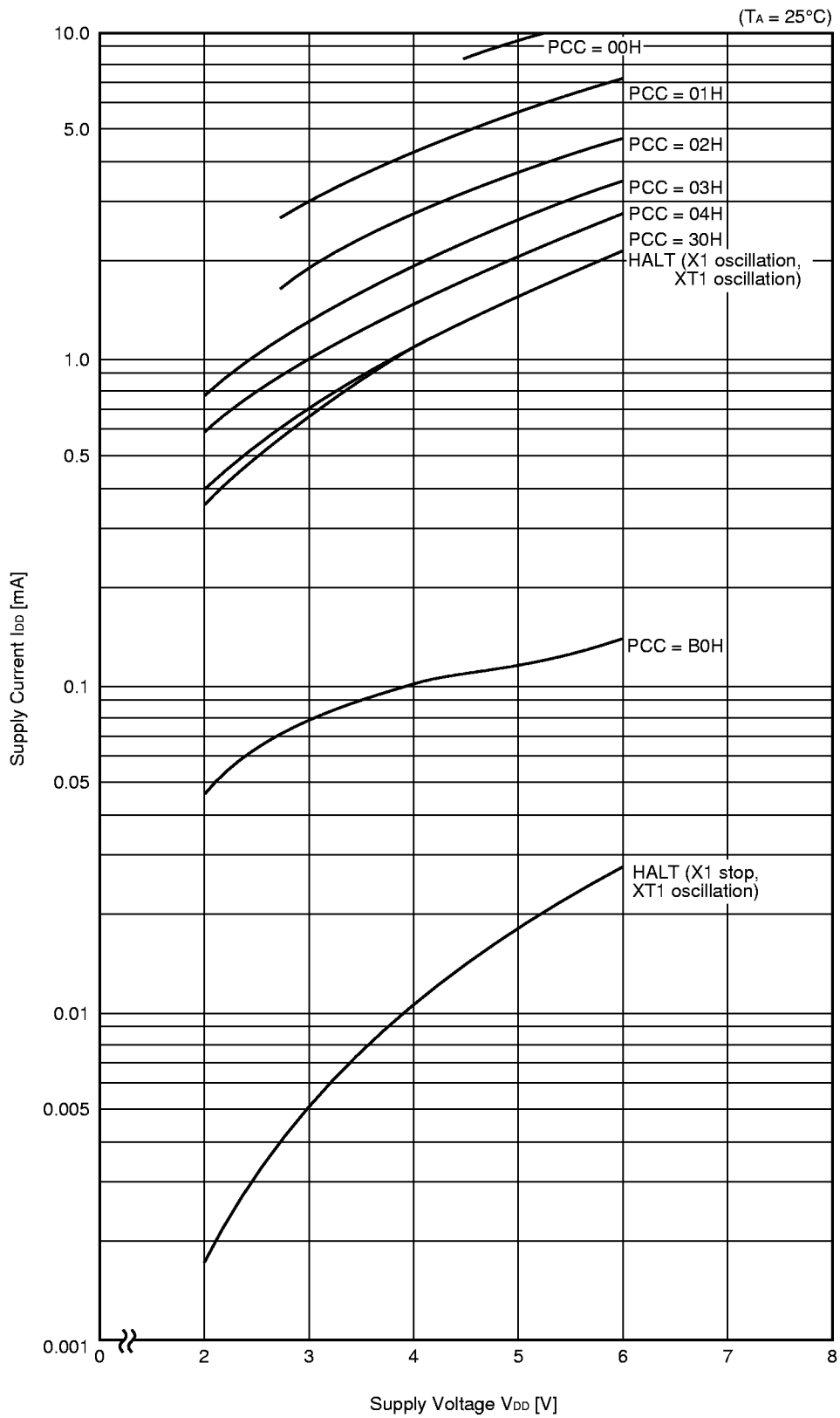
(2) Characteristic curves of μPD78P058 (1/2)

I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



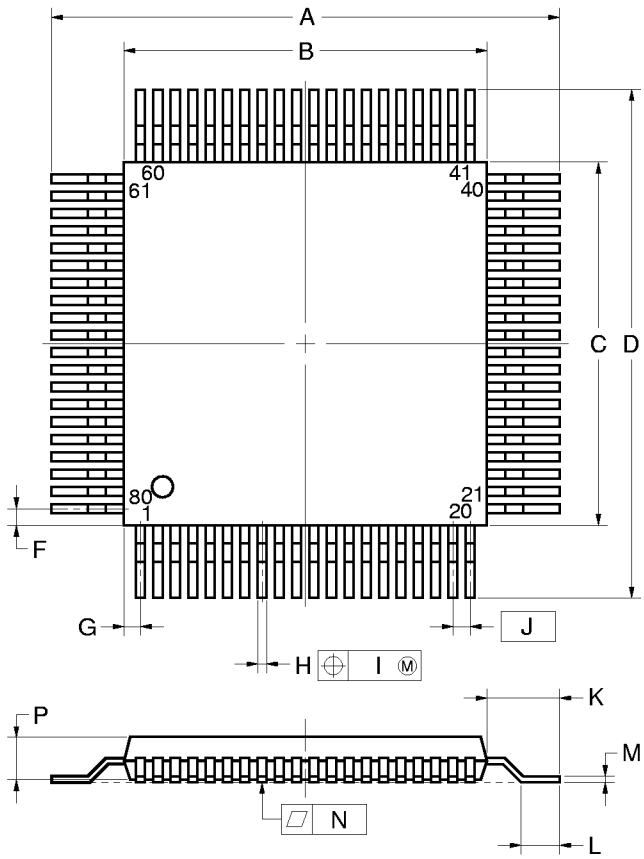
(2) Characteristic curves of μPD78P058 (2/2)

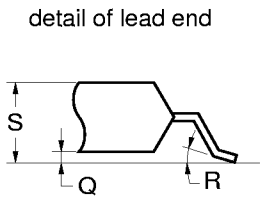
I_{DD} vs V_{DD} (f_X = f_{XX} = 5.0 MHz)



11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14x14)





NOTE

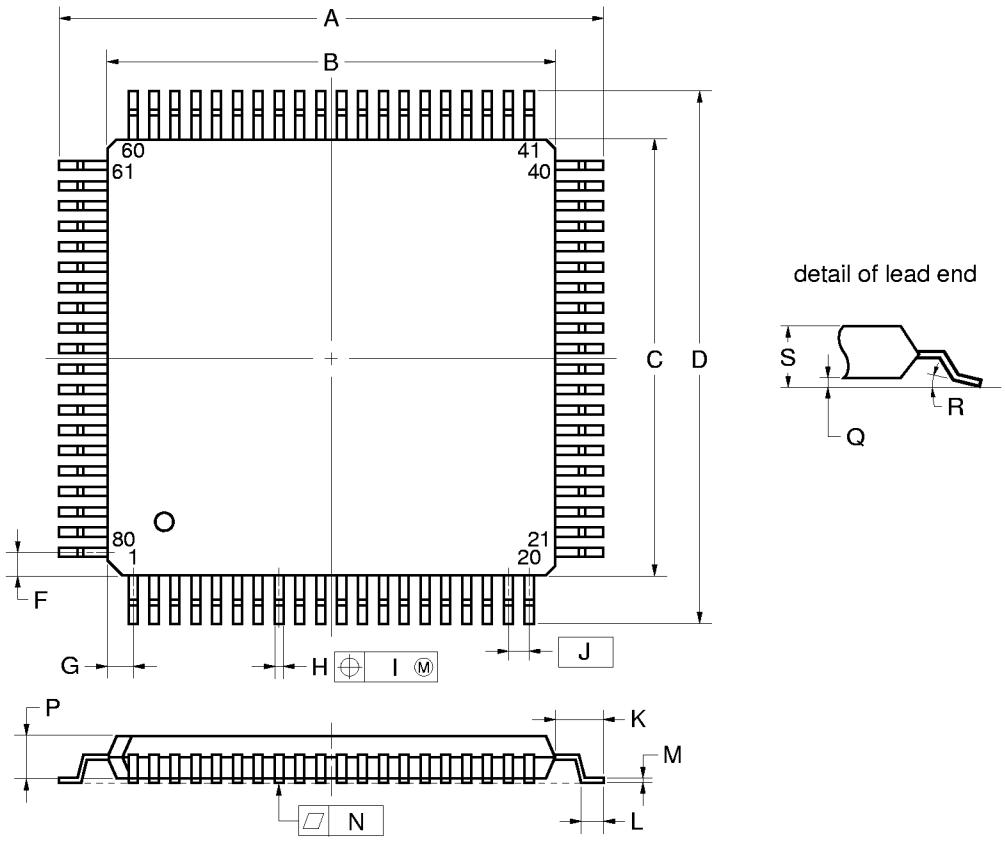
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-5

Remark The dimensions and materials of ES product are the same as those of mass-production products.

80 PIN PLASTIC QFP (14×14)



NOTE

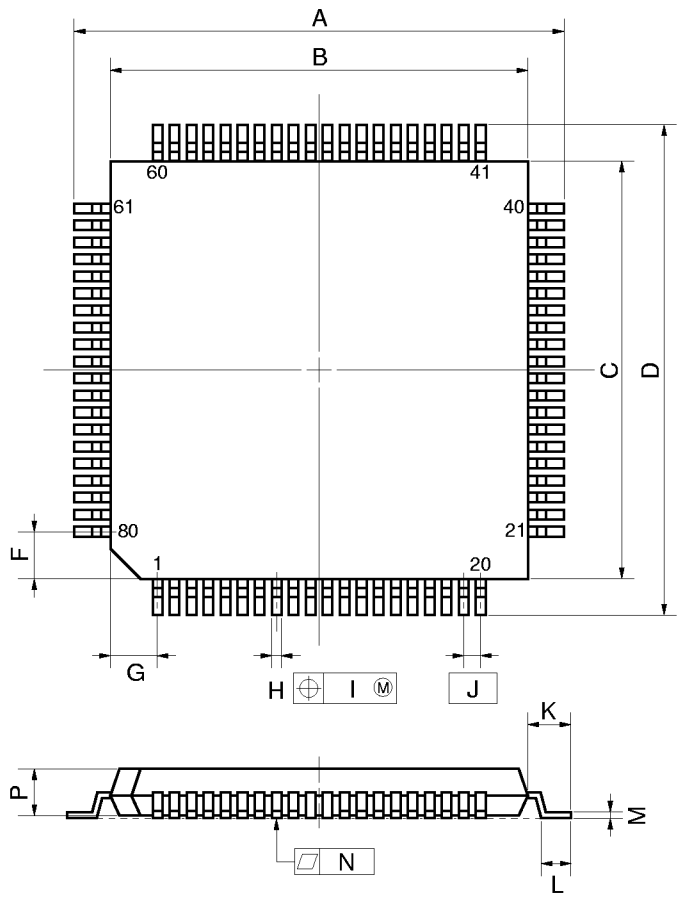
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.70 MAX.	0.067 MAX.

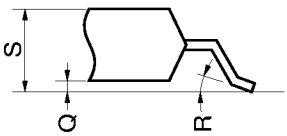
P80GC-65-8BT

Remark The dimensions and materials of ES product are the same as those of mass-production products.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



detail of lead end



NOTE

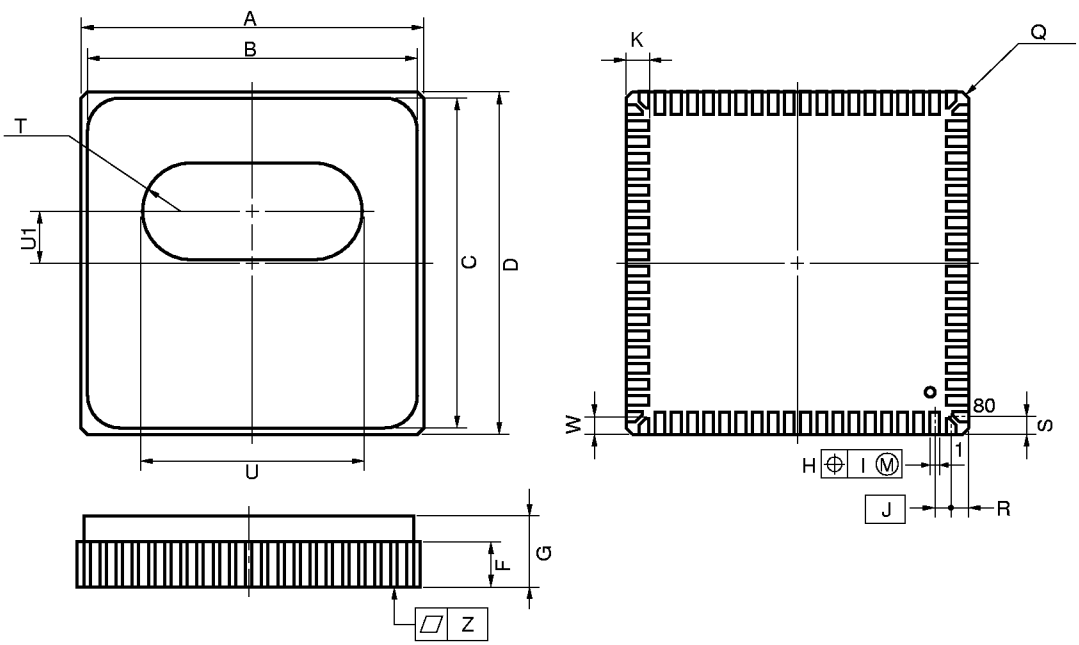
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

Remark The dimensions and materials of ES product are the same as those of mass-production products.

80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.006}_{-0.007}$
Z	0.10	0.004

★ 12. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 12-1. Surface Mount Type Soldering Conditions (1/2)

(1) μPD78P054GC-3B9 : 80-pin plastic QFP (14 × 14 mm, resin thickness: 2.7 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max.	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: 1, Preheating temperature: 120°C or below (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

(2) μPD78P054GK-BE9 : 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-3
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

Cautions 1. Use of more than one soldering method should be avoided (except in the case of pin partial heating method).

2. Because the μPD78P054GC-8BT is under development, soldering conditions are not determined.

Table 12-1. Surface Mount Type Soldering Conditions (2/2)

(3) μPD78P058GC-8BT : 80-pin plastic QFP (14 × 14 mm, resin thickness: 1.4 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or below, Number of flow processes: 1, Preheating temperature: 120°C or below (package surface temperature), Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	WS60-107-1
Pin partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note The number of days for storage after the dry pack has been opened. Storage conditions are 25°C and 65% RH max.

Caution Use of more than one soldering method should be avoided (except in the case of pin partial heating method).

★ APPENDIX A. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD78P054 and 78P058.
Refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	78K/0 Series common assembler package
CC78K/0	78K/0 Series common C compiler package
DF78054	μPD78054 Subseries device file
CC78K/0-L	78K/0 Series common C compiler library source file

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	Programmer adapter connected to a PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tools

• When using in-circuit emulator IE-78K0-NS

IE-78K0-NS[Note]	78K/0 Series common in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C[Note]	Interface adapter when using PC-9800 Series (except notebook type computer) as a host machine
IE-70000-CD-IF[Note]	PC card and interface cable when using PC-9800 Series notebook type computer as a host machine
IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT™ and its compatibles as a host machine
IE-780308-NS-EM1[Note]	Emulation board common to μPD780308 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-3B9, GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket for connecting target system board that is created for mounting 80-pin plastic QFP (GC-3B9, GC-8BT type) and NP-80GC
TGK-080SDW	Conversion adapter for connecting target system board that is created for mounting 80-pin plastic TQFP (GK-BE9 type) and NP-80GK
ID78K0-NS[Note]	Integrated debugger for IE-78K0-NS
SM78K0	78K/0 Series common system simulator
DF78054	Device file for μPD78054 Subseries

Note Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A[Note]	78K/0 Series common in-circuit emulator
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter when using PC-9800 Series (except notebook type computer) as a host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT and its compatibles as a host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as a host machine
IE-780308-NS-EM1[Note] IE-780308-R-EM	Emulation board common to μPD780308 Subseries
IE-78K0-R-EX1[Note]	Emulation probe conversion board necessary when using IE-780308-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9, GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket for connecting target system board that is created for mounting 80-pin plastic QFP (GC-3B9, GC-8BT type) and EP-78230GC-R
TGK-080SDW	Conversion adapter for connecting target system board that is created for mounting 80-pin plastic TQFP (GK-BE9 type) and EP-78054GK-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	78K/0 Series common system simulator
DF78054	Device file for μPD78054 Subseries

Note Under development

(4) Real-Time OS

RX78K/0	78K/0 Series real-time OS
MX78K0	78K/0 Series OS

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78054.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF78054.
- The NP-80GC and NP-80GK are the products of Naitou Densei Machidaseisakusho Co., Ltd. (TEL 044-822-3813). Consult NEC sales representative for purchasing these products.
- The TGK-080SDW is a product of TOKYO ELETECH CORPORATION.

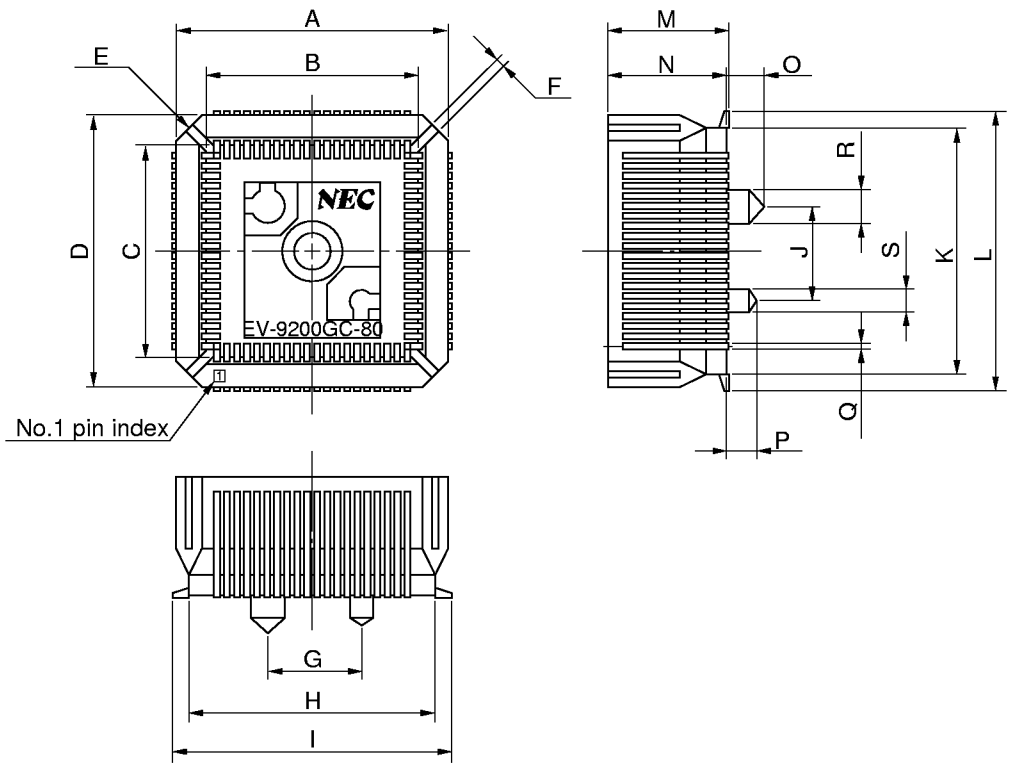
  Reference : Daimaru Kogyo Corporation Tokyo electronic components (TEL 03-3820-7112)
  Osaka electronic components (TEL 06-244-6672)
- For third party development tools, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machines and operating systems corresponding to each software are as follows.

Host Machine [OS] / Software	PC	EWS
	PC-9800 Series [Windows™] IBM PC/AT and its compatibles [Japanese/English Windows]	HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
PG-1500 controller	√Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

CONVERSION SOCKET (EV-9200GC-80) DRAWING AND FOOTPRINT

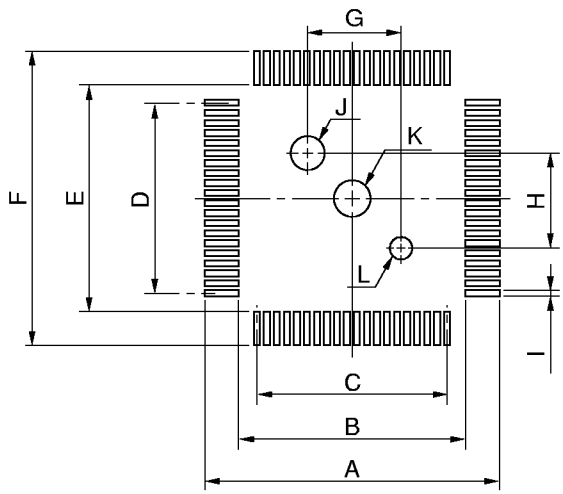
Figure A-1. EV-9200GC-80 Drawing (for reference only)



EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. EV-9200GC-80 Footprint (for reference only)



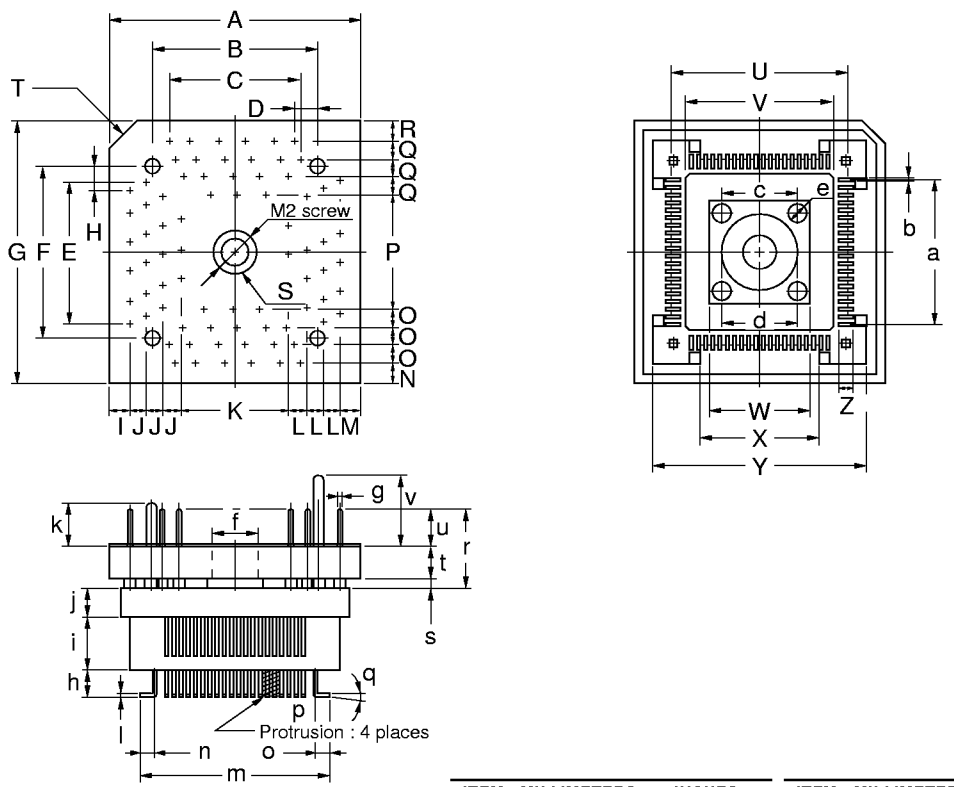
EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

CONVERSION ADAPTER (TGK-080SDW) DRAWING

Figure A-3. TGK-080SDW Drawing (for reference only)



ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	11.77	0.463
C	0.5x19=9.5	0.020x0.748=0.374
D	0.5	0.020
E	0.5x19=9.5	0.020x0.748=0.374
F	11.77	0.463
G	18.0	0.709
H	0.5	0.020
I	1.58	0.062
J	1.2	0.047
K	7.64	0.301
L	1.2	0.047
M	1.58	0.062
N	1.58	0.062
O	1.2	0.047
P	7.64	0.301
Q	1.2	0.047
R	1.58	0.062
S	ϕ3.55	ϕ0.140
T	C 2.0	C 0.079
U	12.31	0.485
V	10.17	0.400
W	6.8	0.268
X	8.24	0.324
Y	14.8	0.583
Z	1.4±0.2	0.055±0.008

ITEM	MILLIMETERS	INCHES
a	0.5x19=9.5±0.10	0.020x0.748=0.374±0.004
b	0.25	0.010
c	ϕ5.3	ϕ0.209
d	ϕ5.3	ϕ0.209
e	ϕ1.3	ϕ0.051
f	ϕ3.55	ϕ0.140
g	ϕ0.3	ϕ0.012
h	1.85±0.2	0.073±0.008
i	3.5	0.138
j	2.0	0.079
k	3.0	0.118
l	0.25	0.010
m	14.0	0.551
n	1.4±0.2	0.055±0.008
o	1.4±0.2	0.055±0.008
p	h=1.8 ϕ1.3	h=0.071 ϕ0.051
q	0~5°	0.000~0.197°
r	5.9	0.232
s	0.8	0.031
t	2.4	0.094
u	2.7	0.106
v	3.9	0.154

TGK-080SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Device Documents

Document Name		Document No. (English)	Document No. (Japanese)
μPD78054, 78054Y Subseries User's Manual		U11747E	U11747J
μPD78052, 78053, 78054, 78055, 78056, 78058 Data Sheet		U12327E	U12327J
μPD78P054, 78P058 Data Sheet		This document	U10417J
78K/0 Series User's Manual Instructions		U12326E	U12326J
78K/0 Series Instruction Set		—	U10904J
78K/0 Series Instruction Table		—	U10903J
μPD78054 Subseries Special Function Register Table		—	U10102J
78K/0 Series Application Note	Basic (III)	U10182E	U10182J
	Floating Point Arithmetic Programs	IEA-1289	IEA-718

Development Tool Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
PG-1500 PROM Programmer		U11940E	U11940J
PG-1500 Controller PC-9800 Series (MS-DOS™) based		EEU-1291	EEU-704
PG-1500 Controller IBM PC Series (PC DOS™) based		U10540E	EEU-5008
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-EM		To be prepared	To be prepared
IE-780308-NS-EM1		To be prepared	To be prepared
IE-780308-R-EM		U11362E	U11362J
EP-78230		EEU-1515	EEU-985
EP-78054GK-R		EEU-1468	EEU-932
SM78K0 System Simulator Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared	U12900J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows based	Guide	U11649E	U11649J

contents of the above documents are subject to change without notice. Please ensure that

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.