ATJ2091N Datasheet

Version 1.1

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Revision History

Version	Date	Description
Ver1.0	Nov. 2006	1st version created for ATJ2091N
Ver1.1	Mar. 2007	2nd version modified for ATJ2091N, electrical characteristics added.

1 .Introduction

ATJ2091N is a third generation single-chip highly-integrated digital music system solution for devices such as dedicated audio players, PDAs, and cell phones. It includes an audio decoder with a high performance DSP with embedded RAM and ROM, ADPCM record capabilities and USB interface for downloading music and uploading voice recordings. ATJ2091N also provides an interface flash memory, LED/LCD, button and switch inputs, headphones, microphone and FM radio input and control. ATJ2091N contains a high performance DSP, which can easily be programmed to support many kinds of digital audio standards such as WMA, etc. For devices like USB-Disk, ATJ2091N can act as a USB mass storage slave device to personal computer system. ATJ2091N has low power consumption to allow long battery life and an efficient flexible on-chip DC-DC converter that allows many different battery configurations, including 1xAA and 1xAAA. The built-in Sigma-Delta DAC includes a headphone driver to directly drive low impedance headphones. The ADC includes inputs for both Microphone and Analog Audio in to support voice recording and FM radio integration features. ATJ2091N provides a true “ALL-IN-ONE” solution that is ideally suited for highly optimized digital audio players.

Features:

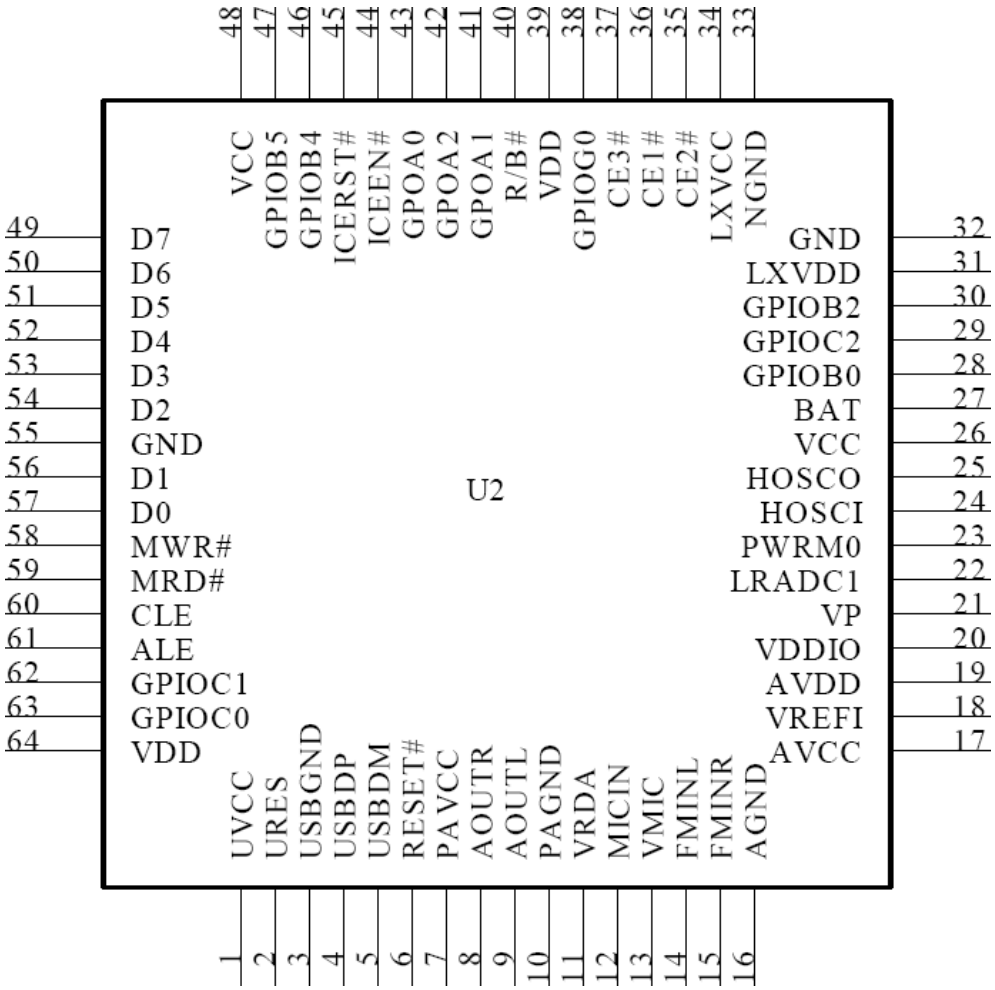
- MPEG1/2/2.5 Audio Layer 1,2,3 decoder, bit rate 8-448Kbps, 8-48KHz, CBR/VBR
- Support WMA Decoder, bit rate 32-384Kbps, 8-48KHz
- Digital Voice Recording at ultra low 4.4 or 8Kbps w/ Actions Speech Algorithm
- 24 bits DSP Core with on-chip Debug Support Unit (DSU)

- On-chip DSP PM with SRAM(16K*24) ,can be switched to be MCU memory space
- On-chip DSP DM with SRAM(16K*24), can be switched to be MCU memory space
- Integrated MCU with DSU, the instruction set is compatible with Z80
- Internal (16K-64)x8(ZRAM1),(3K+3K)(ZRAM2) and 6k ZRAM3 accessed by MCU
- Internal 12Kx8 BROM build in Boot up and USB Upgrade firmware
- Internal (21K+17K)x8 TROM
- Internal SRAM access time<7ns, MROM access time<16ns
- External up to 3(pcs)x 32M/64M/128M/256M/512M/1G/2G/4G bytes Nand type Flash accessed by MCU or DMA
- Support 24MHz OSC with on-chip PLL for DSP and about 32KHz RC oscillator
- 2-channel DMA , 1-channel CTC(Counter/Timer Controller) and interrupt controller for MCU
- Energy saving dynamic power management (PMU), supporting 1xAA and 1xAAA.
- Support USB 2.0 Compliance PHY+SIE, Read :7MB/S, Write: 6MB/S(Nand Flash Base)
- Build in Stereo 18-bit Sigma-Delta D/A
- Build in Key Scan Circuit and GPIO
- Support external 8080 Series LCM driver interface
- Support FM Radio input and 32 levels volume control
- Support Stereo 18-bit Sigma-Delta A/D for Microphone/FM Input/Line Input, sample rate at 8/12/16/22/24/32/48KHz
- MCU run at 48MHz(typ),F/W can program from DC up to 60MHz transparently
- DSP+PM/DM Speed up to 72MIPS,while 48mips@1.4v
- D/A+PA SNR :with A weight>92dB,without A weight>=88dB
- A/D SNR >79dB

- Headphone driver output 2x11Mw @16ohm
- Operating Voltage: IO: 3.0v, Core: 1.8v
- Standby Leakage Current: VCC:50uA@3.0V(MAX), VDD: 350uA@1.6V(MAX)
- Low Power Consumption : <80mW@1.5V at typical WMA decoder solution

2. Pin Description

2.1 Pin Out



2.2 Pin Definition

NOTE:

1： PWR---Power Supply

2： AI----Analog Input

3： AO----Analog Output
4： O-----Output
5： I-----Input
6： BI----Bidirection
7： TBD2C, BD2C, BD2XU, SBD2X, BD2XM5----2 miliampere driver
8： BD4CM2, BD4C, BD4CU----4 miliampere driver
9: BD1XM2----1 miliampere driver
10：USCU----USCHIMITCU

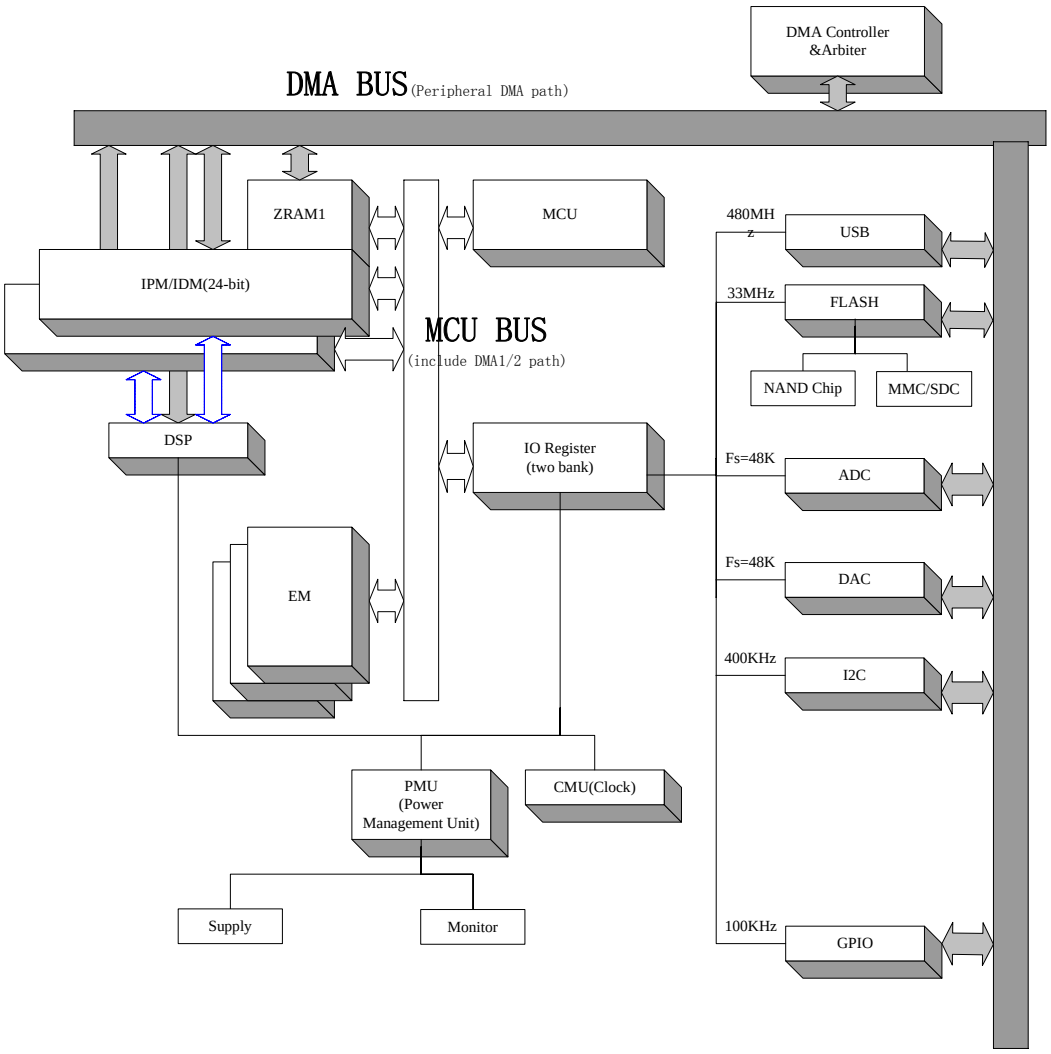
Pin No.	Pin Name	I/O Type	Driver	Reset Default	Description
1	VCC	PWR	/	/	Power supply for USB
2	UREG	AO	/	/	USB precision Resistor
3	GND	PWR	/	/	USB ground
4	USBDP	A	/	H	USB data plus
5	USBDM	A	/	H	USB data minus
6	RESET-	I	USCU	H	System reset input (active low)
7	PAVCC	PWR	/	/	Power supply for power amplifier
8	AOUTR	AO	/	/	Int. PA right channel analog output
9	AOUTL	AO	/	/	Int. PA left channel analog output
10	PAGND	PWR	/	/	Power amplifier ground
11	VRDA	AO	/	/	Bypass capacitor connect pin for Int. D/A Reference voltage
12	MICIN	AI	/	/	Microphone pre-amplifier input
13	VMIC	PWR	/	/	Power supply for Microphone
14	FMINL	AI	/	/	Left channel of FM line input
15	FMINR	AI	/	/	Right channel of FM line input
16	AGND	PWR	/	/	Analog ground
17	AVCC	PWR	/	/	power supply of Analog
18	VREFI	AI	/	/	Voltage reference input
19	AVDD	PWR	/	/	Analog Core power pin
20	VDDIO	PWR	/	Z	Core power input/output

21	VP	PWR	/	/	Power pin
22	LRADC1	AI	/	/	Low resolution A/D input 1
23	PWRMode0	AI	/	/	POWER mode select 0
24	HOSCI	AI	/	/	High frequency crystal OSC input
25	HOSCO	AO	/	/	High frequency crystal OSC output
26	VCC	PWR	/	/	PAD power pin
27	BAT	I	/	/	Battery Voltage input.
28	GPIO_B0	BI	BD2C	Z	Bit0 of General purpose I/O port B
	KEYI0	I		H	Bit0 of key scan circuit input
29	GPIO_C2	BI	BD4CM2	/	Bit2 of General purpose I/O port C
30	GPIO_B2	BI	BD2XUM5	Z	Bit2 of General purpose I/O port B
	KEYI12	I		H	Bit1 of key scan circuit input
31	LXVDD	PWR	/	/	VDD DC-DC pin
32	GND	PWR	/	/	Ground
33	GND	PWR	/	/	NMOS Ground
34	LXVCC	PWR	/	/	VCC DC-DC pin
35	CE2-	O	NF_PAD	H	Ext. memory chip enable 2
36	CE1-	O	NF_PAD	H	Ext. memory chip enable 1
37	CE3-	O	BD4CU	H	Ext. memory chip enable 3
	GPO_A3	O		/	Bit3 of General purpose Output port A
38	GPIO_G0	BI	TBD2C	Z	Bit0 of General purpose I/O port G
	CE4-	O		/	Ext. memory chip enable 4
39	VDD	PWR	/	/	Digital Core power
40	RB-	I	BD4C	H	Nand Type flash Ready/Busy status input.
41	GPO_A1	O	BD4C	L	Bit1 of General purpose Output port A
	ICECK	I		/	Clock input of DSU
42	GPO_A2	O	BD4C	L	Bit2 of General purpose Output port A
	ICEDO	O		/	Data output of DSU
	GPO_A0	O	BD4CM2	0	Bit0 of General purpose Output port A

43	ICEDI	I		/	Data input of DSU
44	ICEEN-	I	BD4C	/	DSU enable (active low)
45	ICERST-	I	BD4C	/	DSU reset (active low)
46	GPIO_B4	BI	BD2XM5	Z	Bit4 of General purpose I/O port B
	KEYO0	O		/	Bit0 of key scan circuit output
47	GPIO_B5	BI	BD2XM5	Z	Bit5 of General purpose I/O port B
	KEYO1	O		/	Bit1 of key scan circuit output
48	VCC	PWR	/	/	Digital power pad
49	D7	BI	NF_PAD	L	Bit7 of ext. memory data bus
50	D6	BI	NF_PAD	L	Bit6 of ext. memory data bus
51	D5	BI	NF_PAD	L	Bit5 of ext. memory data bus
52	D4	BI	NF_PAD	L	Bit4 of ext. memory data bus
53	D3	BI	NF_PAD	L	Bit3 of ext. memory data bus
54	D2	BI	NF_PAD	L	Bit2 of ext. memory data bus
55	GND	PWR	/	/	Ground
56	D1	BI	NF_PAD	L	Bit1 of ext. memory data bus
57	D0	BI	NF_PAD	L	Bit0 of ext. memory data bus
58	MWR-	O	NF_PAD	H	Ext. memory write strobe
59	MRD-	O	NF_PAD	H	Ext. memory read strobe
60	CLE	O	NF_PAD	L	Command latch enable for NAND flash
61	ALE	O	NF_PAD	L	Address latch enable for NAND flash
62	GPIO_C1	BI	SBD2X	OD	Bit1 of General purpose I/O port C
	I2C_SDA	O		/	I2C Serial data (Open drain)
	SIRQ-	I		/	Ext. interrupt request input
63	GPIO_C0	BI	SBD2X	OD	Bit0 of General purpose I/O port C
	I2C_SCL	O		/	I2C serial clock (Open drain)
64	VDD	PWR	/	/	Digital Core power

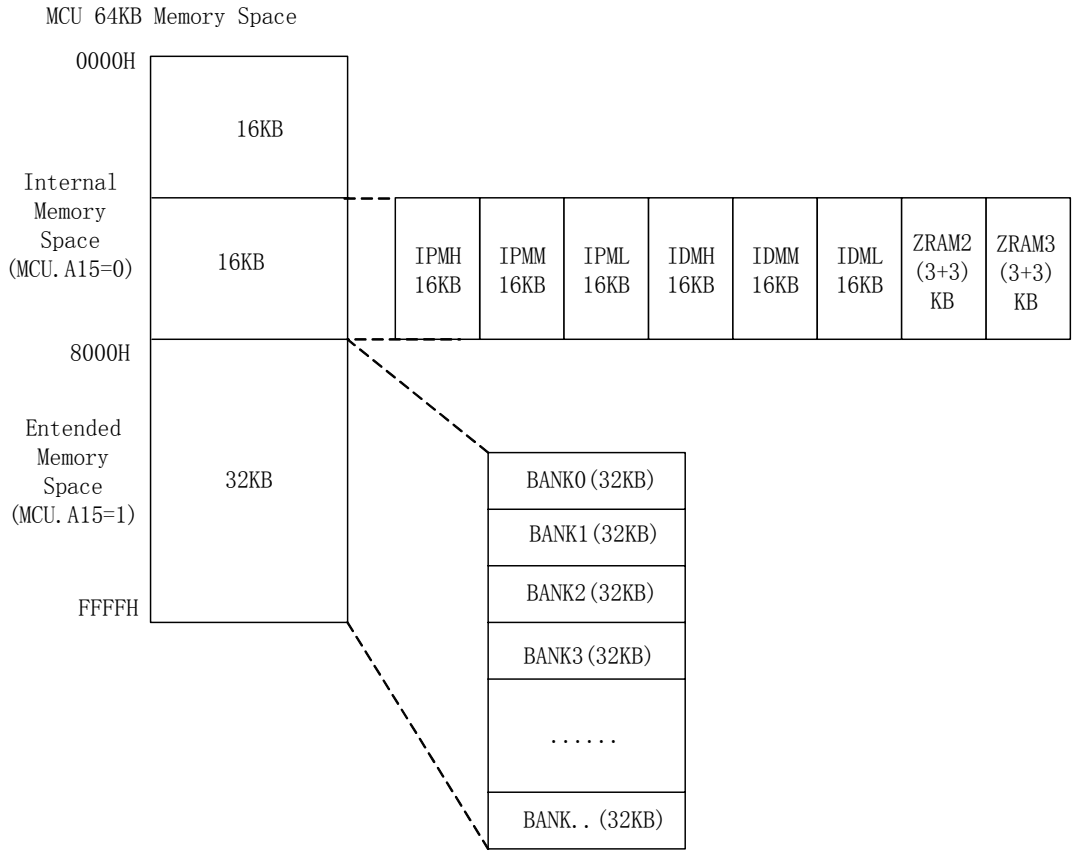
3. Function Description

3.1 Functional Block Diagram



3.2 MCU Core

3.2.1 MCU System Memory Mapping



If IA15=0 -> mapped to internal Memory

If IA14=0, mapped to internal ZRAM（16K-64 ZRAM1）

If IA14=1, mapped to internal DSP IPM/IDM when they are mapped into MCU memory space 3 extended address bits of a IO mapped register (Mapped at registered are used to decode the access to one of these memory blocks

Bit 2 1 0	Accessed Block
0 0 0	IPM low byte

0 0 1	IPM middle byte
0 1 0	IPM high byte
0 1 1	ZRAM3
1 0 0	IDM low byte
1 0 1	IDM middle byte
1 1 0	IDM high byte
1 1 1	ZRAM2 （B1+B2）

Since IPM/IDM is mapped to MCU memory space per 8K block, IA13 is used to select low/high block of 8K bytes in each 16K byte block.

If IA15=1 -> Extended address bits are IO mapped at 01h and 02h for EMA15-28. EMA15-25 are output as address bus, while the EMA26-28 are used to decode CE0- ~ CE3-.

CE0- is used to access boot code from ROM/MASK/NOR- type Flash.

CE1- to CE3- can be configured to access ROM, or RAM or NAND-type Flash.

ATJ2091N's internal MCU MROM/SRAM memory mapping:

1) (16K-64) byte ZRAM1(IA15=0,IA14=0): 0000H-3FBFH
2) 6Kbyte ZRAM2 (IA15=0, IA14=1, IOReg05.[2:0]=111): 4000H-57FFH
3) (2K+256) byte URAM: 5800H-60FFH it has synchronization and asynchronism accessing mode.
4) 12Kbyte BROM (IA15=1,Reg02=00h, Reg01=00h): 8000h-AFFFh
5) 21Kbyte TROM1 (IA15=1,Reg02=00h,Reg01=02h): 8000h-D3FFh
6) 17Kbyte TROM2 (IA15=1,Reg02=00h,Reg01=03h): 8000h-C400h
7) 6Kbyte ZRAM3 (IA15=0,IA14=1,IOReg05.[2:0]=011): 4000H-57FFH

ATJ2091N's internal DSP IPM/IDM memory mapping:

1) 16K x24bit IPM SRAM: 0000H-3FFFH
2) 16K x24bit IDM SRAM : 0000H-3FFFH

ATJ2091N's internal DSP IPM/IDM memory mapping accessed by MCU:

1) 16K x3 byte IPM SRAM: 4000H-7FFFH
2) 16K x3 byte IDM SRAM : 4000H-7FFFH

(Hi/Mid/Low Byte Select and Mapping Mode controlled by IOReg05)

DMA Mode Notes:

1: When DMA1 and DMA2 are active, MCU will halt, and DMA1 and DMA2 have priority.

2: FLASHDMA or USB DMA is active, MCU will not halt.

3.3 DSP24 Core

This Core is a high performance, programmable Digital Signal Processor (DSP) suitable for a variety of digital audio compounding functions, such as Dolby AC-3 Surround, MPEG1 Layer3 which require large memory provided and the higher accuracy. RDSP24 is a general purpose DSP which can be appended various peripherals circuitry to implement some advanced signal processing algorithms for audio application.

3.4 ZRAM1 and ZRAM2

Input: A[13:0], ID[7:0], ZRAMRD-, ZRAMWR-

Output: RD[7:0] (Tri-state)

Speed: max read time 30 ns from ZRAMRD- going low

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

ZRAM2 is composed of B1 and B2, and each of them is 2k*8 byte SRAM. B1, B2 and ZRAM1(B0) can be operated independently. It has the following modes:

1) MCU running at B0, while DMA[M] read B1 and DMA[N] write B2.B1 and B2 are vise versa. M=1, 2, 3, 4, 5, 6; N=1, 2, 3, 4, 5, 6; M!=N.
2) MCU running at B0+B1+B2 or B0+B1 or B0+B2.

IPM and IDM Notes:

Power consumption: stand by when both WR- and RD- are inactive, access current is as low as possible. PM/DM can be visited by MCU, DSP, DMA1, DMA2 and DMA5. When DSP visits low(high) bytes of 8Kbytes, MCU/DMA1,2,5 can visit high(low) bytes of 8Kbytes at the same time.

3.5 USB2.0 SIE

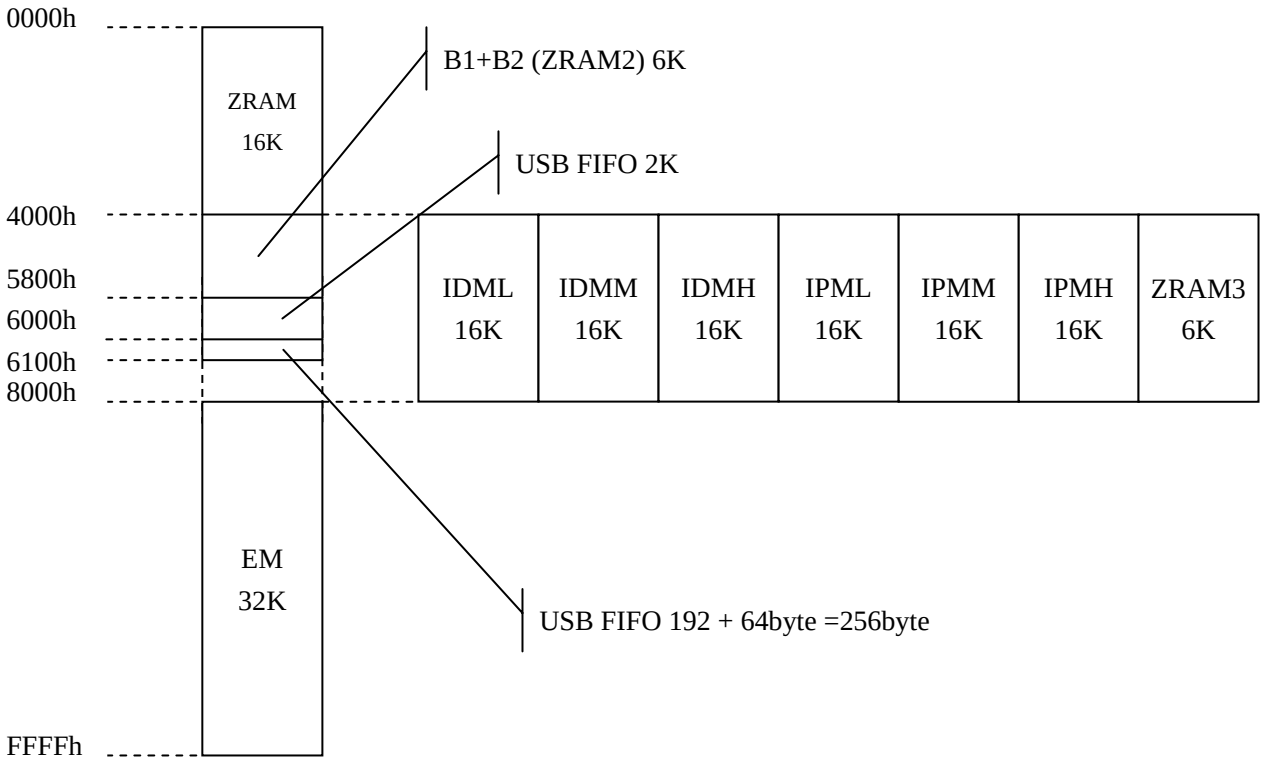
3.5.1 General Description

The Actions USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. In high-speed mode this device is capable of transmitting or receiving data up to 480Mbps.This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

3.5.2 Features

- Fully compliant with USB Specification 2.0
- Supports USB High Speed (480Mb/s) and Full Speed (12Mb/s)
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Inter UTMI
- Supports DMA interface (16-bit)
- 2K bytes configurable FIFO for endpoints and provides double buffer to increase throughput.
- Supports USB remote wake-up feature
- Software controlled connection to USB bus for re-enumeration

3.5.3 USB Using Memory

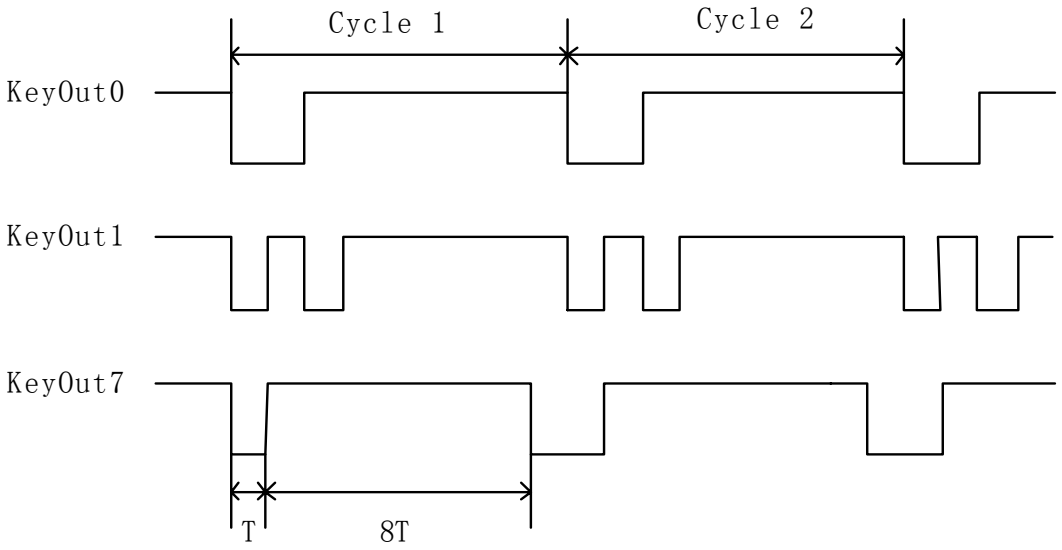


3.6 NAND Flash Interface

ATJ2091N can support NAND type flash from 32M to 4G bytes.

3.7 Key Scan Interface

KEY Scan Timing：



Key Scan Timing

When key scan circuit is enabled, ATJ2091N will scan the keyboard periodically. It drives pin KEYOUTn [n=2…7] scan pulse in turn. When any key is pressed, the corresponding Keyout N will send out the scan pulse. When a key is pressed, pin Keyin N connecting the key will be found low level.

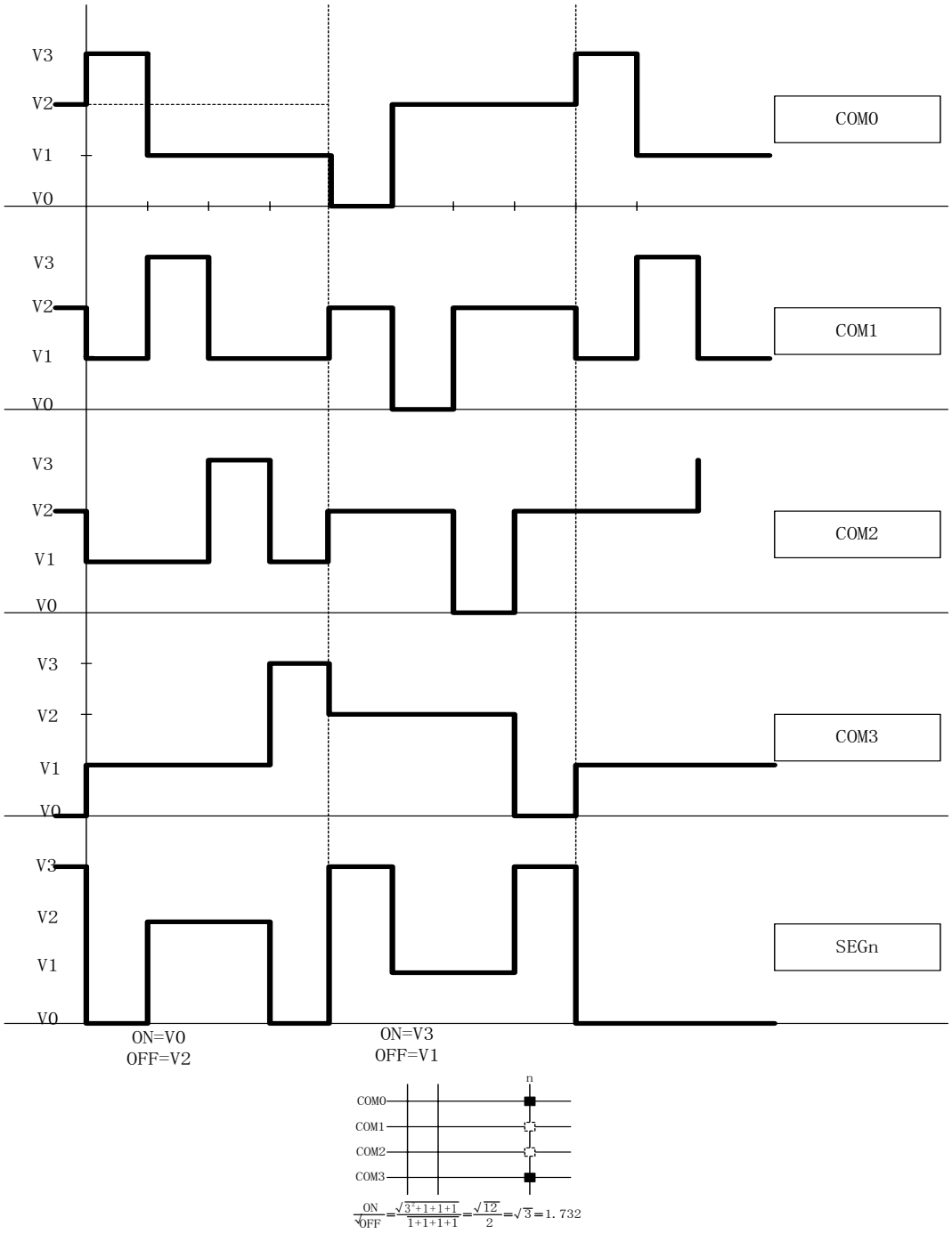
There are 12 internal 8-bit registers for key value latch per scan. But only another one register (Key Scan Data Register) for MCU may access key value. Those 12 internal registers are mapped into this register, and an internal pointer is used to point to the current register to return scan data when read. Any IO write to this register will clear the internal register, and the pointer will increase by 1 and point to the next register after read is performed.

3.8 LCD Interface

It is an ICON LCD control interface. We can operate 4*19 icons using the 10 registers

from 0xc2 to 0xcb.

ICON LCD 4*19



3.9 General Purpose IO Ports

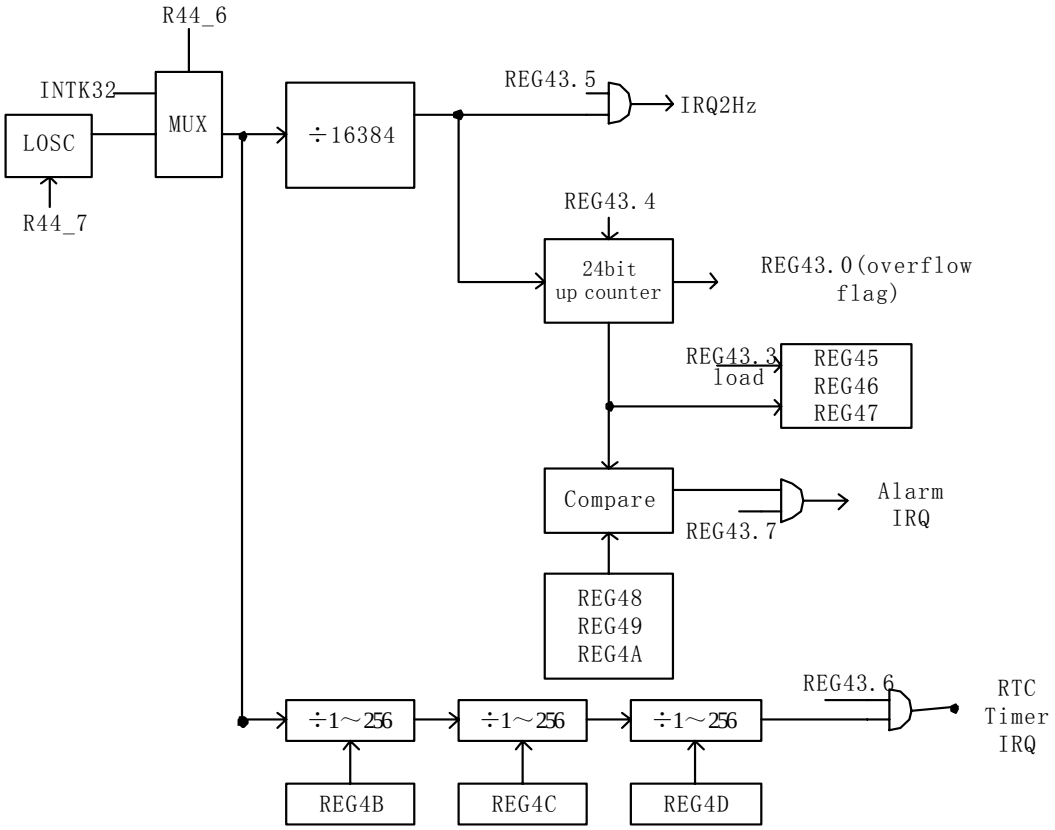
ATJ2091N has GPOA, GPIOB, GPIOC and GPIOG. They have different functions in different modes.

GPIO	F1(CE0S=H default)	F2(key8*12)	F3(ILCD)	F4(CE0S=L default)MROM)
GPO_A0	GPO_A0/ICEDI			
GPO_A1	GPO_A1/ICECK			
GPO_A2	GPO_A2/ICEDO			
GPO_A3	CE3-/GPOA3/MMC_CMD	CE3-/GPOA3		
GPIO_B0	KEYI0/GPIO_B0			
GPIO_B2	KEYI2/GPIO_B2	KEYI2/GPIO_B2/SPI_SCK		
GPIO_B4	KEYO0/GPIO_B4			
GPIO_B5	KEYO1/GPIO_B5	KEYO1/GPIO_B5/SPI_MOSI		
GPIO_C0	GPIO_C0	GPIO_C0/I2C_SCL		
GPIO_C1	GPIO_C1	GPIO_C1/I2C_SDA/SIRQ-		
GPIO_C2	GPIO_C2 /MMC_SCLK	GPIO_C2	GPIO_C2	
GPIO_G0	GPIO_G0	GPIO_G0	GPIO_G0/SEG16	GPIO_G0

3.10 LOSC/RTC

RTC is a 24-bits counter with the following functions; the clock source is LOSC/INTK32.

- Time
- Alarm
- Timer



3.11 HOSC/PLL

Input: A[7:0], DI[7:0], IOW-, IOR-, RESET-

Output: HCK, PLLCK, CK48MHZ

ATJ2091N supports 24Mhz crystal, and it is the system clock source.

A low jitter PLL referenced to 24MHz is used to generate clock for DSP and for serial communication protocols such as USB, UART, etc. The clock used in serial communications is 48MHz. Another PLL referenced to 24MHz is used to generate

22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz and 24.576MHz for audio sequence of 48khz.

3.12 PMU/DC-DC

The power management unit, PMU, includes:

1. VDD (for core), VCC (for I/O) DC-DC PFM converter
2. VDD regulator
3. RC oscillator for one battery DC-DC startup
4. IC oscillator for DC-DC controller
5. Control management
6. Voltage monitor
7. External L & C

Particular Suggestion: Both DCOP1/2 and internal NMOS are working at the beginning of power up. The unused line should be turned off after level off to reduce power consumption and interference.

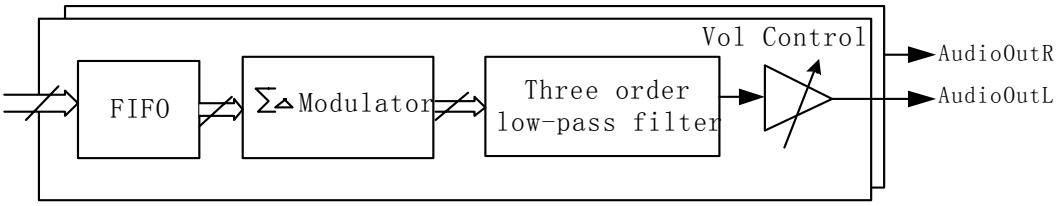
3.13 A/D, D/A and Headphone Driver

3.13.1 D/A Interface

ATJ2091N's internal D/A is an on-chip Sigma-Delta Modulator, a high performance D/A is composed of it and the D/A analog block referenced to 17.2. The D/A interface support 4-level play back FIFO (8 X 20-bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256XFS clock for over-sampling, while 24.576MHz supports 48K/32K/24K/16K/12K/8KHz

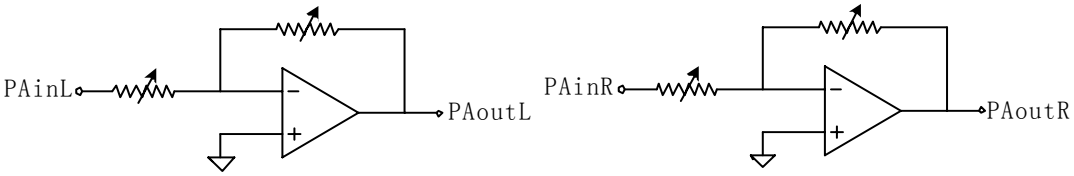
with 256XFS for over-sampling.

D/A Block Diagram



Internal D/A can drive earphone directly and the pin PAVCC need a bypass capacitor about 100uF to eliminate the “PENG” when D/A is powered on or off. D/A includes an analog mixer, reference to the ADDA block diagram.

Power Amplifier Diagram



3.13.2 A/D Interface

The internal microphone amplifier has gain for recording. The VMIC pin is the power supply (2.2V) for microphone.

The audio A/D is a 18 bits sigma delta Analog-to-Digital Converter. Its input source can be selected from MIC amplifier or external FM or line-in, and it has two FIFO.

BATTERY A/D is used for battery voltage monitoring, and the voltage range is 0.7~2.2V.

LRADC1 works as line controller, and the voltage range is 0.7~2.2V. When LRADC1 PAD voltage<2.0V, it will send an interrupt request to MCU to reduce MCU’s dealing time to line controller.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.6	-0.3~2.0	V
	VCC	3.0	-0.3~3.6	V
Input voltage	V_I		-0.3~3.6	V
Storage temperature	T_{stg}	25	-65~150	℃

Note:

1. T_O = 25℃（Operating Temperature）
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

4.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T_O = 25℃, VCC = 0 V.

4.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.6*VCC		VCC+0.6	V
Low-level input voltage	V_{IL}		-0.3		0.4*VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			±5	uA
Tri-State leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			±3	uA
GPIO Drive	I_{drive1}	GPOA0,GPOA1,GPOA2		4		mA
	I_{drive2}	GPIO_B2, GPIO_B4, GPIO_B5		10		mA
	I_{drive3}	Other GPIO		2		mA
Supply Current （One battery mode）	I_{VDD}	In Full speed mode (MCU run 24MHz in internal SRAM, DSP run 36MIPS)	13.5	14.5	18	mA

		In Standby mode	30	45	60	uA
	I_{VCC}	In Full speed mode (MCU run 24MHz in internal SRAM, DSP run 36MIPS)	0.15	0.2	1	mA
		In Standby mode	50	60	70	uA

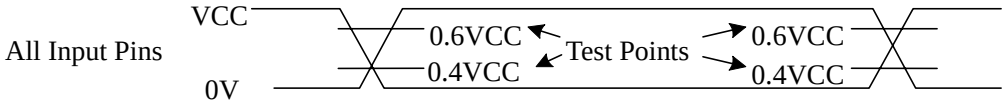
NOTES:

1. T_o = -10 to +70℃, VDD = 1.6 V, VCC = 3.0 V
2. I_{VDD} is a total power supply current for the 1.6 V power supply. I_{VDD} is applied to the LOGIC and PLL and OSC block.
3. I_{VCC} is a total power supply current for the 3.0 V power supply. I_{VCC} is applied to the USB, IO and AD block.

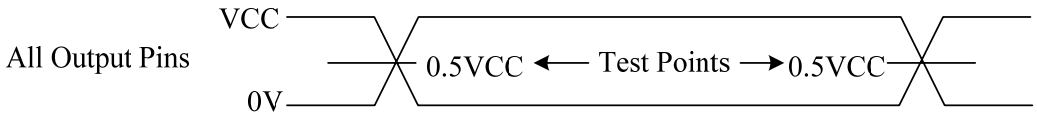
4.4 AC Characteristics

T_o = -10 to +70℃

4.4.1 AC Test Input Waveform

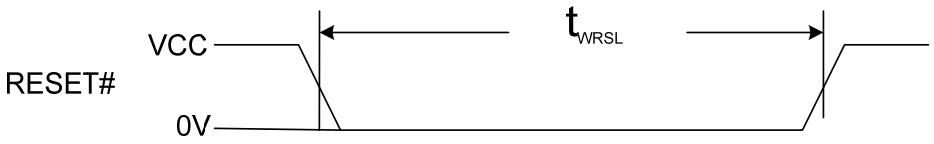


4.4.2 AC Test Output Measuring Points



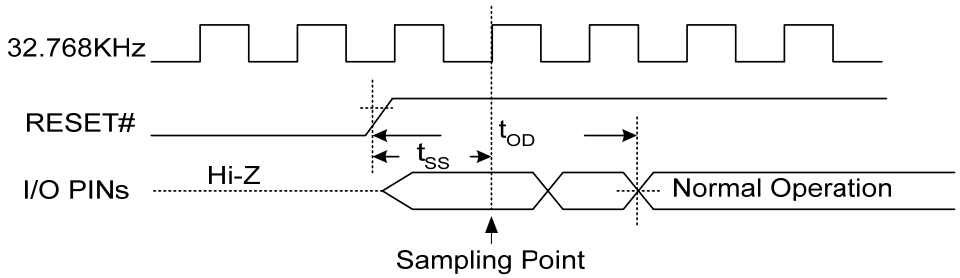
4.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us



4.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}		—	61.04	us
Output delay time (from RESET#)	t_{OD}		61.04	—	us

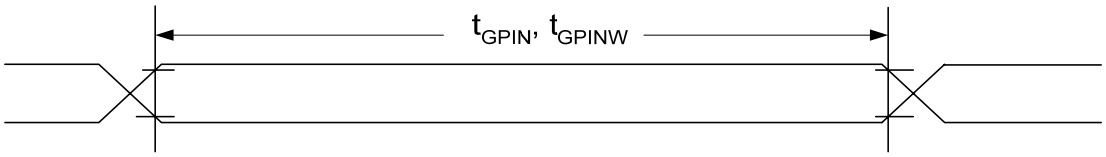


4.4.5 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$11/f_{mcuclk}$		s
GPIO output rise time	t_{GPRISE}		5	50	ns
GPIO output fall time	t_{GPFALL}		5	50	ns
Output level width	t_{GPOUT}		$11/f_{mcuclk}$		s

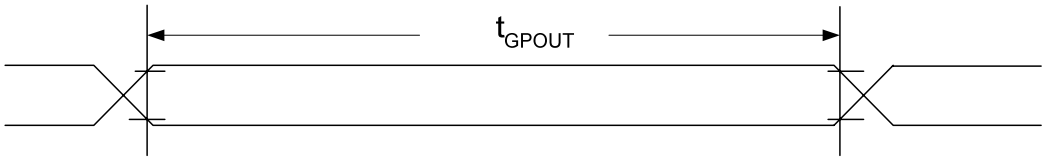
Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.

Input level width



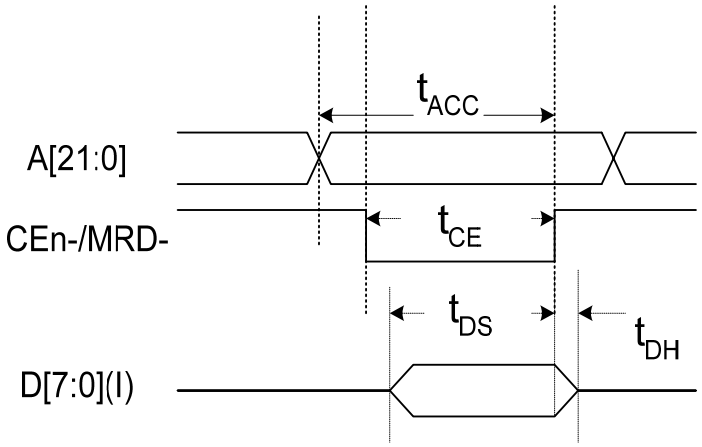
Output rise/fall time

Output level width

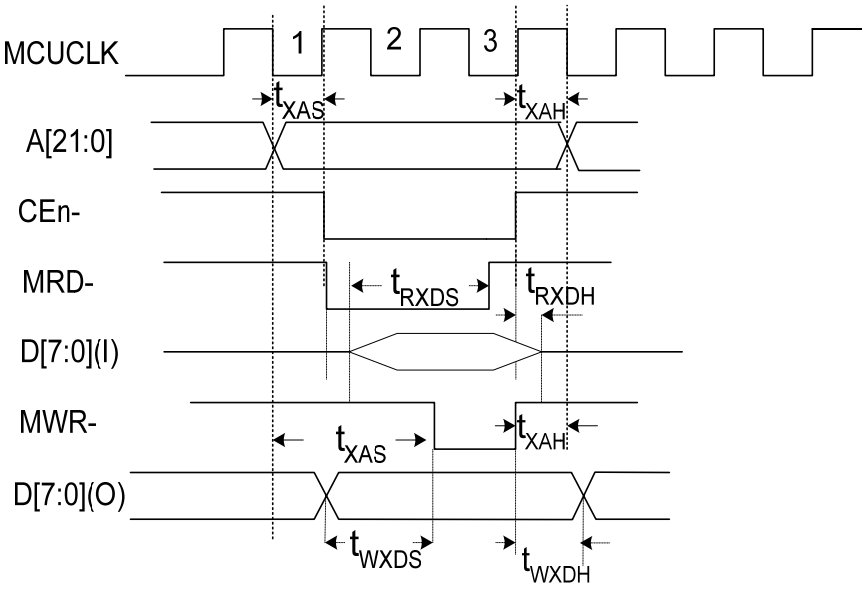


4.4.6 Ordinary ROM Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	90		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	90		ns
Data input setup time	t_{DS}	HOSC=24MHz	40		ns
Data input hold time	t_{DH}	HOSC=24MHz	15		ns



4.4.7 External System Bus Parameter



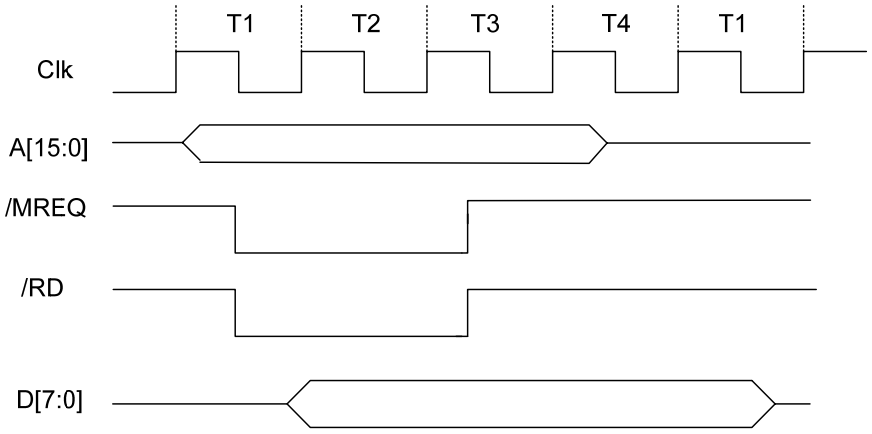
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	10		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns
Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1/ f_{MCUCLK}

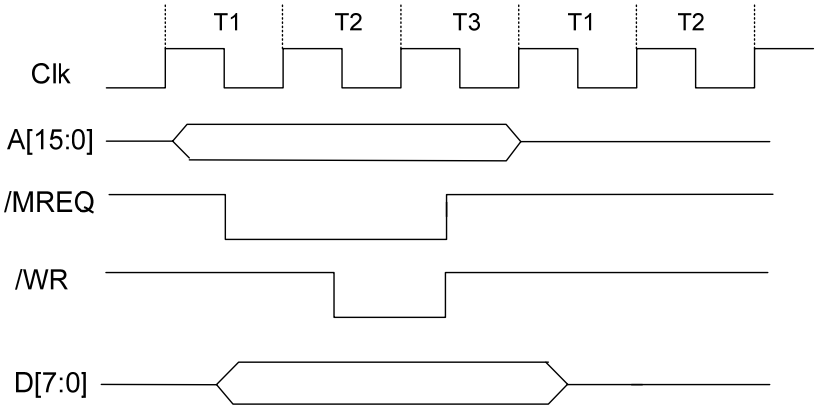
4.4.8 Bus Operation

Memory Read Timing



Memory Read Timing

Memory Write Timing



Memory Write Timing

4.4.9 Serial Interface Parameter

Pre-scale Value	13		1.625		1	
Baud Rate	Divisor	%Error	Divisor	Baud Rate	Divisor	%Error
600	192	0.16%	-	600	192	0.16%
1200	96	0.16%	-	1200	96	0.16%
1800	64	0.16%	-	1800	64	0.16%
2000	58	0.53%	-	2000	58	0.53%
2400	48	0.16%	-	2400	48	0.16%
3600	32	0.16%	256	3600	32	0.16%
4800	24	0.16%	192	4800	24	0.16%
7200	16	0.16%	128	7200	16	0.16%
9600	12	0.16%	96	9600	12	0.16%
14400	8	0.16%	64	14400	8	0.16%
19200	6	0.16%	48	19200	6	0.16%
28800	4	0.16%	32	28800	4	0.16%
38400	3	0.16%	24	38400	3	0.16%
57600	2	0.16%	16	57600	2	0.16%
115200	1	0.16%	8	115200	1	0.16%
230400	-	-	4	230400	-	-
460800	-	-	2	460800	-	-
750000	-	-	-	750000	-	-
921600	-	-	1	921600	-	-
1500000	-	-	-	1500000	-	-

Note: Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with UART Baud Rate Registers and clock pre scale that is set

4.4.10 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.6 V, VCC = 3.0V, Sample Rate=32KHz)

Characteristics	Min	Typ.	Max	Unit
Dynamic range		80		dB
Total Harmonic Distortion + Noise		-75		dB
Frequency Response (20-13KHz)	-0.55	0.2	0.25	dB
Full Scale Input Voltage(Gain=0dB)		2		Vpp

4.4.11 I2S Interface Parameter

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	Clock Output Frequency	BCKIN		330		ns	48 kHz/s Stereo 16 bit/s
t_{SOISS}	Word strobe Hold Time after falling edge of clock	BCKIN, LRCIN		320		ns	
t_{SOODC}	Data Hold Time after falling edge of clock	BCKIN, DIN		320		ns	

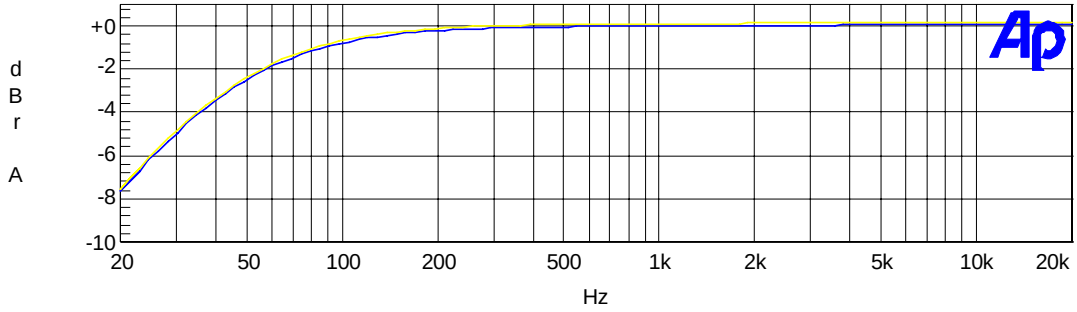
4.4.12 Headphone Driver Characteristics Table

(T_o =-10 - +70℃, VDD = 1.6 V, VCC = 3.0 V, Sample Rate=32KHz, Volume Level=0x1F)

Characteristics	Min	Typ	Max	Unit
Dynamic Range –60 dBFS Input		-87		dB

Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		Vpp
Inter channel Gain Mismatch(1KHz)		-66		dB

Frequency Response Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

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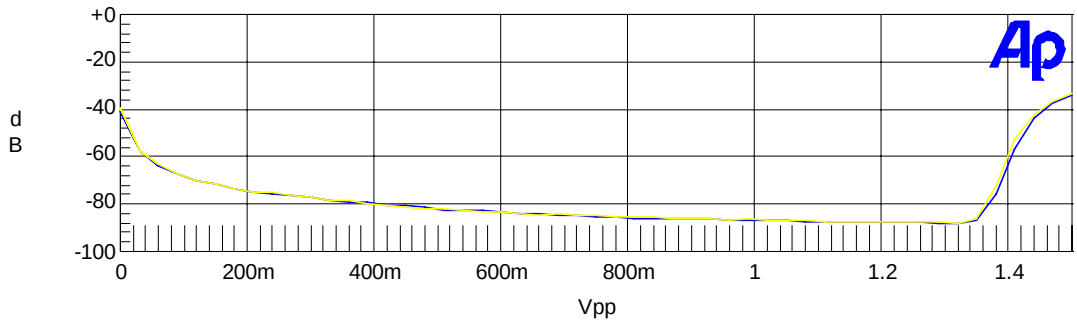
THD + N Amplitude Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THD+N Ratio	Left	

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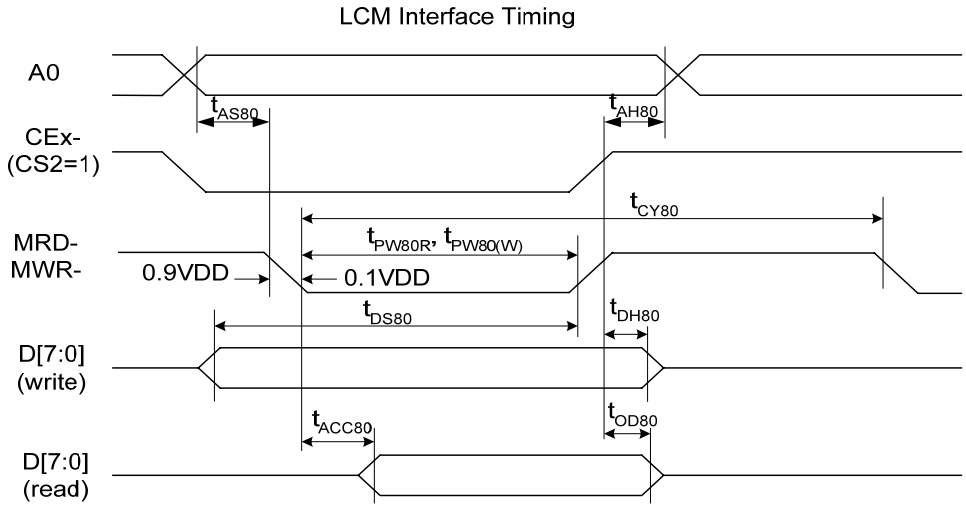
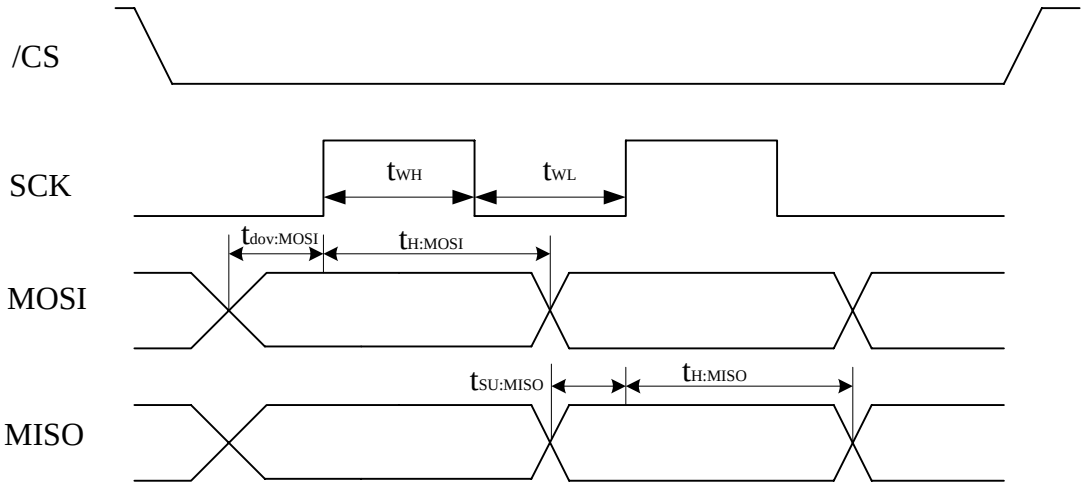
4.4.13 LCM Driver Parameter



Parameter	Symbol	Condition	Typ	Unit
Data access time(write)	$t_{PW80(W)}$	HOSC=24MHZ	42	ns
Data access time (Read)	$t_{PW80(R)}$	HOSC=24MHZ	62	ns

Write cycle time	$t_{CY80(W)}$	HOSC=24MHZ	84	ns
Read cycle time	$t_{CY80(R)}$	HOSC=24MHZ	544	ns
Data setup time	t_{DS80}	HOSC=24MHZ	16	ns
Data hold time	t_{DH80}	HOSC=24MHZ	36	ns
Address setup time	t_{AS80}	HOSC=24MHZ	11	ns
Address hold time	t_{AH80}	HOSC=24MHZ	11	ns
Read access time	t_{ACC80}	HOSC=24MHZ	11	ns
Data input hold time	t_{OD80}	HOSC=24MHZ	9	ns

4.4.14 SPI Parameter



SPI timing

Parameter	Symbol	Typical	Unit
SCLK period	t_{CP}	250	us
Clock low time	t_{CL}	125	ns

Clock high time	t_{CH}	125	ns
Clock rise time	t_{TLH}	22	ns
Clock fall time	t_{THL}	22	ns
Input setup time	t_{ISU}	115	ns
Input hold time	t_{IH}	130	ns
Output delay time	t_{ODLY}	110	ns

5. Ordering Information

5.1 Soldering Conditions

Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 235℃(Lead) or 260℃(Lead Free)
	Reflow time: 30 seconds or less (210℃or more)----(Lead) or 60 seconds or less (217℃or more)---- (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%,Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note: Maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution: Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

5.2 Precaution against ESD for Semiconductors

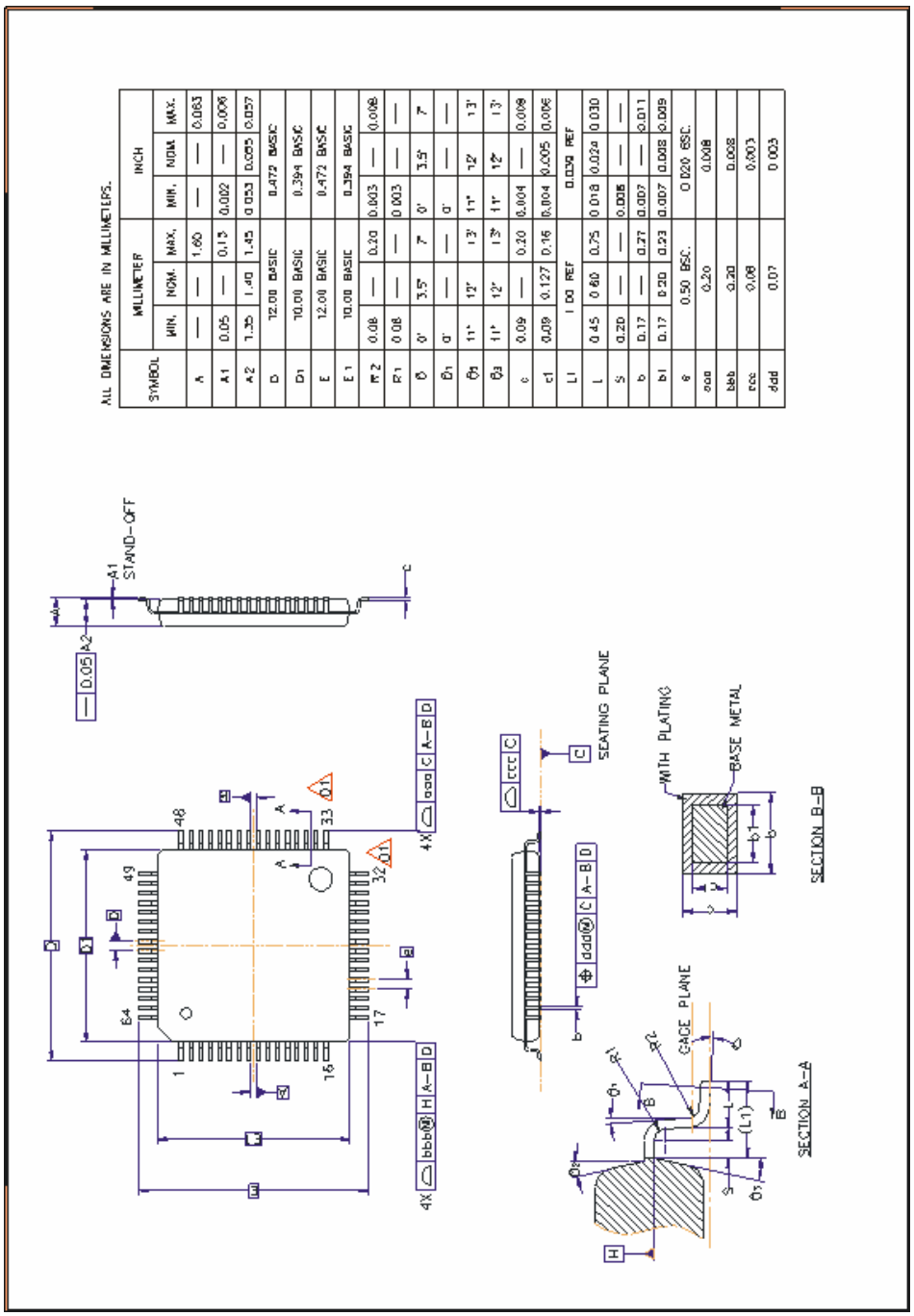
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should

be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

5.3 Status before Initialization of MOS Devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on.

6. ATJ 2091N Package Drawing



7. Appendix

Acronym and Abbreviations

ACK—Acknowledgement

ADC—Analog Digital Convert

ATAIRQ—Advanced Technology Attachment Interrupt Request

CTC—Clock/Timer/Counter

DAC—Digital Analog Convert

DMA—Direct Memory Address

DRQ—Data Request

DST—Destination

DST—Destination

ECC—Error Correction Code

EM—External Memory

FIFO—First In First Out

HIP—Host Interface Port

HOSC—High Frequency Oscillator

IDM—Internal Data Memory

IPM—Internal Program Memory

IRQ—Interrupt Request

IR—Infra-red

LOSC—Low Frequency Oscillator

MIC—Microphone

NAK—Negative Acknowledgement

PLL—Phase Locked Loop

RTC—Real Time Clock

RB—Ready/Busy

SIRQ—System Interrupt Request

SPDIF—Sony/Philips Digital Interface

SPI—Serial Port Interface

SRC—Source

TC—Transmit Complete

UART—Universal Asynchronous Receiver/Transmitter

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