DATA SHEET

SUNPLUS

SPHE8200A

DVD Single Chip MPEG A/V Processor

Preliminary

OCT. 07, 2003

Version 0.2

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DVD SINGLE CHIP MPEG A/V PROCESSOR

1.GENERAL DESCRIPTION

SPHE8200A A/V decoder is a single-chip integrated DVD A/V decoder. It performs real-time decoding and playback of ISO/IEC 11172 MPEG1 and 13818 MPEG2 stream for multiple bitstream sources.

SPHE8200A supports DVD-Video, DVD-Audio, Super Video CD, Video CD, CD-DA, HDCD, OKO, CD-ROM different disc formats.

SPHE8200A is designed to maximize system performance with minimum cost. For typical DVD application it integrates DVD/CD servo controller, multi-channel multi-format TV-encoder and audio quality ADC, with high quality 5.1ch Audio, or low cost 2-ch AC3 system.

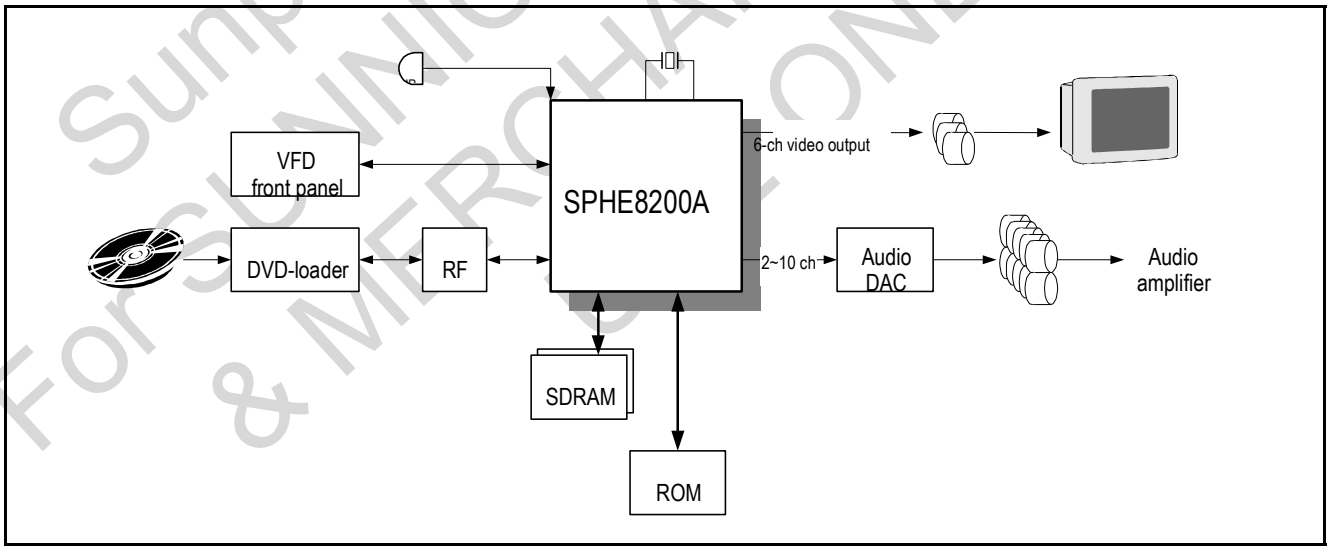
SPHE8200A supports Dolby Digital, DTS, MPEGI/II Layer1/2 , PCM, LPCM, WMA audio playback.

SPHE8200A also combines all the functions required for a high-performance progressive-scan DVD system. Built-in de-interlacing hardware allows high quality DVD playback. The embedded digital audio decoder is able to support key control and audio sound effects for Karaoke.

In additional to that SPHE8200A includes a flexible 2D graphics engine for high quality user interface and other applications. Complex application could be built using this platform easily.

Development tools of SPHE8200A include complete compiler tools, programming guide and system application libraries.

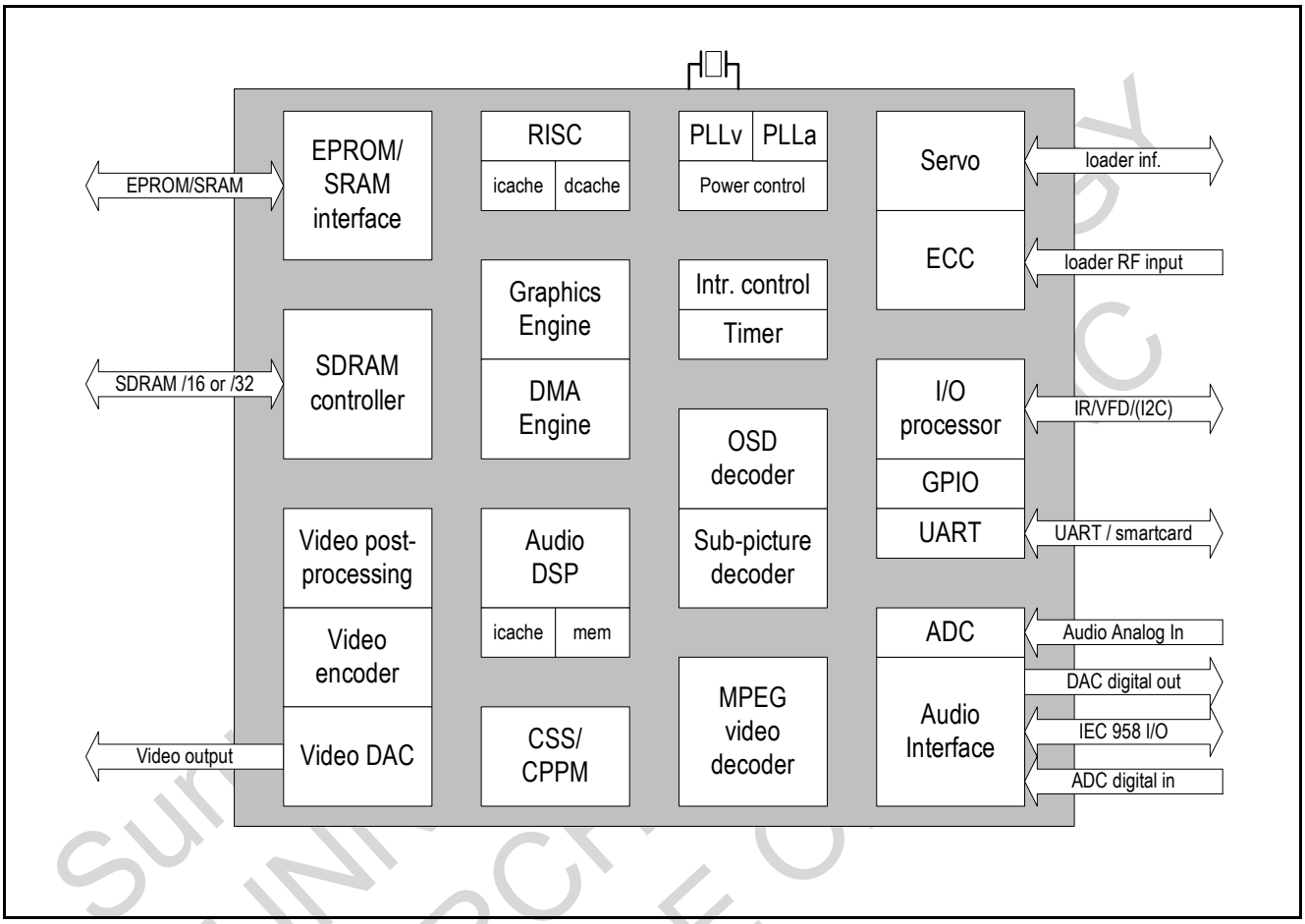
Application utilizing the SPHE8200A is presented below:



2.FEATURE

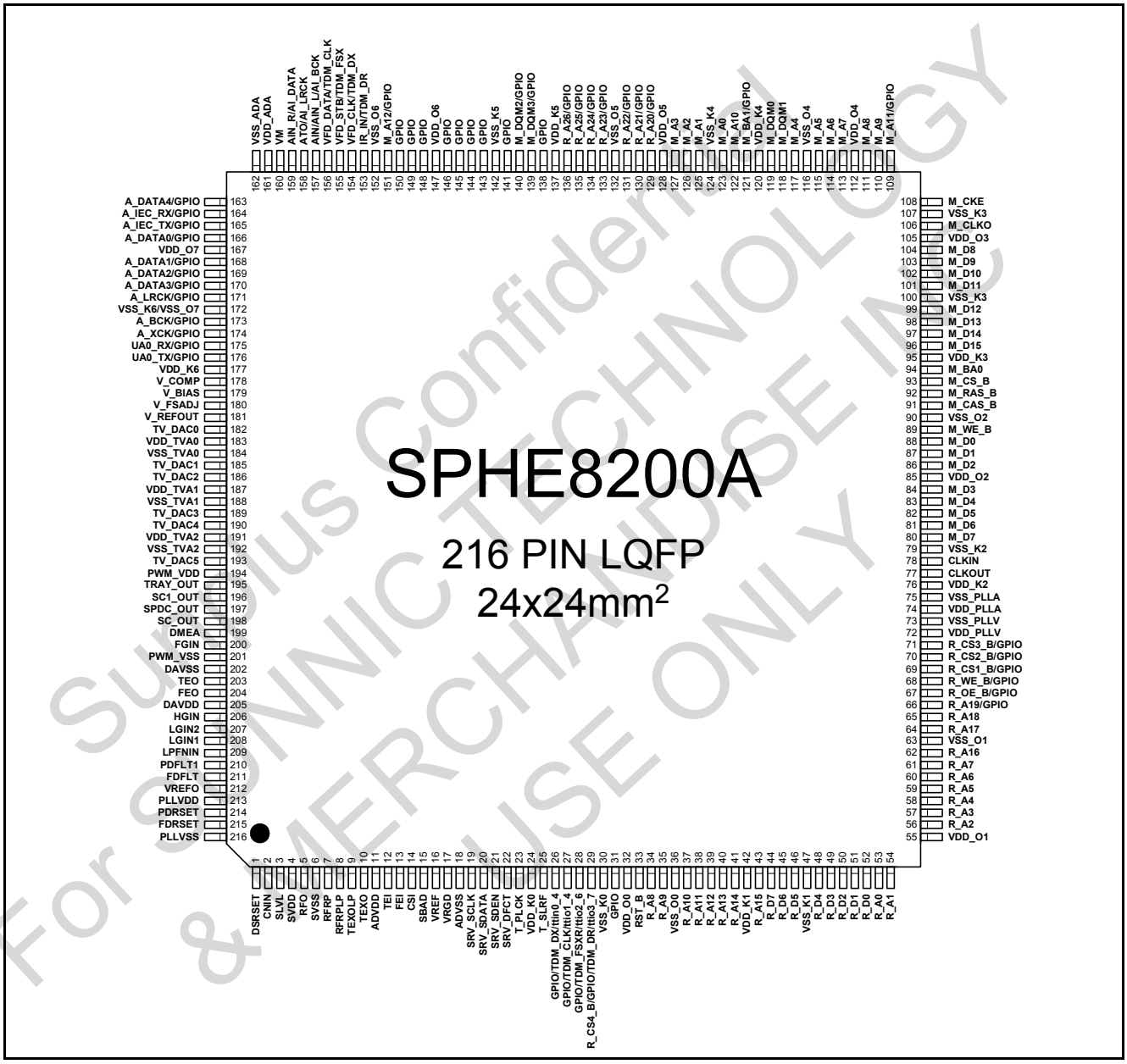
- Single Chip Integrated DVD Servo and A/V Decoder
- Integrated DVD/CD Servo Controller
  - Support 1x ~ 2x DVD format reading
  - Support 1x ~ 16x CD format reading
- Embedded 32-bit RISC Processor without external host controller
- Embedded Audio Processor supports multiple audio standards
- Embedded I/O processor supports programmable interface control
- Embedded TV encoder with multi-channel built-in high-speed video DAC supports various display standards
- Embedded audio ADC supports stereo analog audio input
- Built-in system PLL and audio PLL generate all clock sources required from single 27MHz input
- Support following disc format:
  - DVD Navigation 1.0
  - DVD audio
  - SVCD (Chaoji VCD)
  - OKO disc
  - VCD 2.0/1.1/1.0
  - CDDA / HDCD
  - CDROM (game, WMA and JPEG disc)
- CSS/CPPM hardware
  - Built-in CSS hardware
  - Built-in CPPM C2_DCBC and C2_D/C2_D function
- Video Decoder
  - Real time MPEG2 MP@ML decoding
  - Real time MPEG1 D1 (720x480x30 /720x576x25) decoding
  - Hardware accelerated JPEG decoding
  - Advanced decoding and display control
- Sub-picture Decoder
  - Advanced Sub-Picture Decoder for DVD SVCD and OKO
  - Support hardware vertical scaling
- Audio Decoder
  - Flexible Programmable DSP Architecture
  - Embedded high resolution audio quality ADC
  - Support CDDA, HDCD, and DVD-Audio
  - Support LPCM, PCM, and WMA playback
  - Support MPEGI/II layer 1/2 and MPEG 2.5 playback (with optional down-mixing)
  - Support Dolby Digital AC3 5.1ch / DTS 5.1ch playback (with optional down-mixing)
  - Support Key Shift of 2 channels
  - Support equalization, reverb and special sound field
- SDRAM controller
  - High Performance SDRAM controller
  - Support 16 or 32 bit operation
  - Support up to 4 SDRAM devices
  - Support 16M/64M/128M/256M SDRAM devices
- Graphics
  - Embedded 2D Graphics Accelerator
  - BitBlt, line, triangle drawing support
- Display
  - De-interlacing of interlaced video source
  - Flexible vertical interpolation
  - Flexible horizontal interpolation with optional CIF filter
  - Powerful cropping and panning effect
  - Support YUV422, 8-bit indexed color or 16-bit direct color format
- OSD
  - Multiple OSD regions with different formats
  - Support 4/16/256 indexed color
  - Support 16/24-bit direct color
  - Support x2/x3/x4 horizontal scaling
- Embedded TV encoder
  - Simultaneous multi-channel output
  - Support 480i/480p/576i/576p format
  - Support 640x480 VGA / 800x600 SVGA format
  - Support CVBS output
  - Support SVideo, Component (YUV / YPbPr) or RGB output
  - Macrovision 7.01 and Macrovision AGC v1.03 copy protection
- Interface
  - 27MHz crystal driver
  - 16/32-bit SDRAM interface
  - 8/16-bit ROM/FLASH/SRAM interface
  - UART ports
  - IR and VFD support
  - Video DAC analog output
  - Simultaneous 10-channel audio DAC output
  - IEC958/SPDIF digital input / output
  - Analog audio input
  - External ADC digital input interface (optional)
  - Optional ATAPI and I2S interface support
  - Optional Parallel Port interface support
- Low power
  - Advanced low power design
  - Selective standby mode
  - Programmable low speed operation
- Technology
  - Advanced CMOS technology
  - 216pin LQFP package
  - 3v (I/O) and 1.8v (kernel) power supplies
  - 5v I/O tolerance

3.BLOCK DIAGRAM

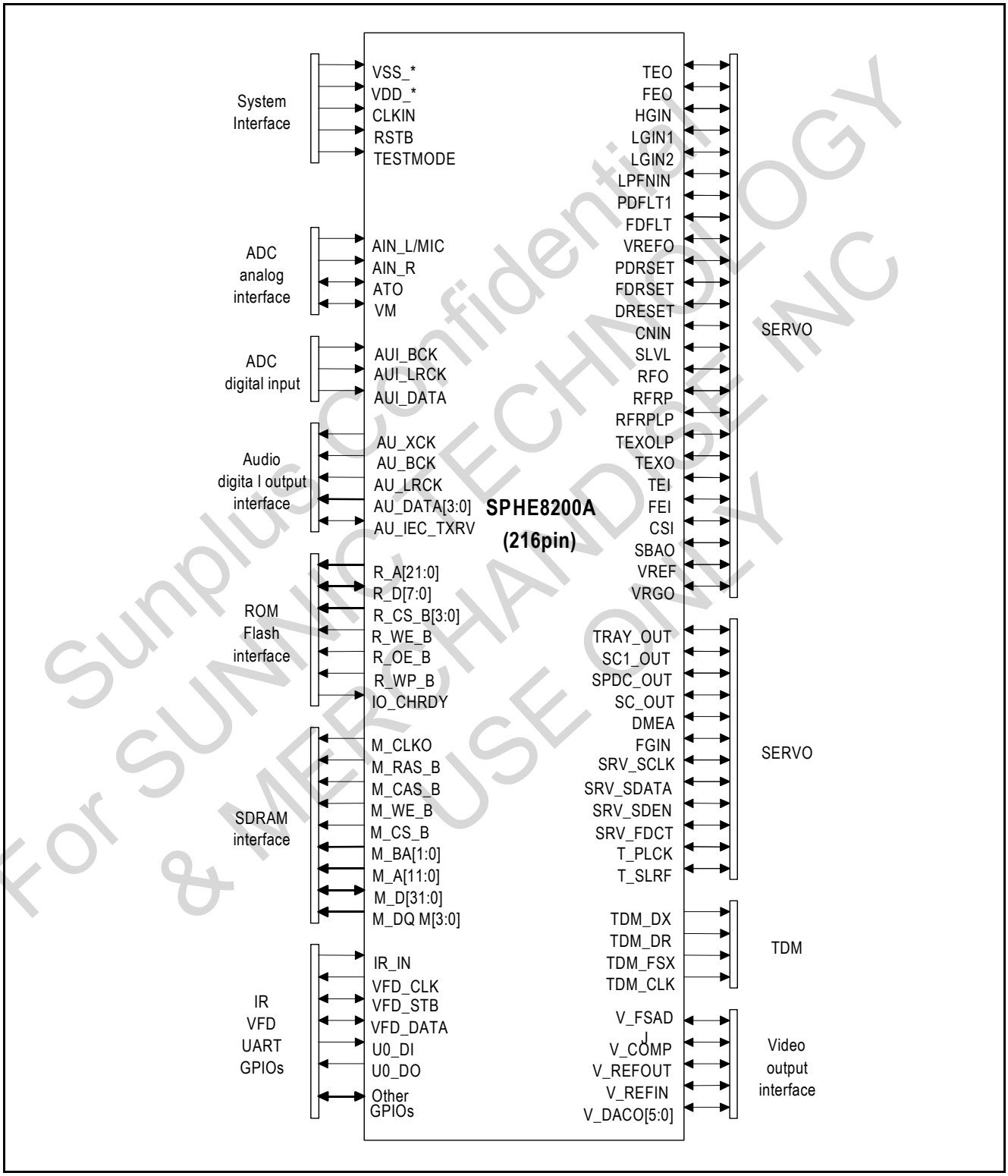


4.SIGNAL DESCRIPTION

4.1. Pin Map



4.2. Group Map



4.3. Pin Description

Signal	Pin	State	Description
Supply Pins (51)			
VSS_K*	30, 47, 79, 100, 124, 142	S	Ground pins for chip kernel logic
VSS_O*	36, 63, 90, 107, 116, 132, 152	S	Ground pins for chip output
VSS_K6/O7	172	S	Shared ground pin
VDD_K*	24, 42, 76, 95, 120, 137, 177	S	1.8V power supply pins for chip kernel logic and input pre-driver
VDD_O*	32, 55, 85, 105, 112, 128, 147, 167,	S	3.3V power supply pins for output pins
VSS_PLLV	73	S	Ground pin for system PLL
VDD_PLLV	72	S	1.8V power supply pin for system PLL
VSS_PLLA	75	S	Ground pin for audio PLL
VDD_PLLA	74	S	3.3V power supply pin for audio PLL
VDD_TVA*	183, 187, 191	S	3.3V power supply pin for TV DAC
VSS_TVA*	184. 188. 192	S	Ground pin for TV DAC
VSS_ADA	162	S	Ground pin for on-chip audio ADC
VDD_ADA	161	S	3.3V power supply pin for on-chip audio ADC
PWM_VSS	201	S	Servo PWM ground (digital)
PWM_VDD	194	S	Servo PWM 3.3V power (digital)
DA_VSS	202	S	Servo DAC ground
DA_VDD	205	S	Servo DAC 3.3V power
PLLVDD	213	S	Servo PLL 3.3V power
PLLVSS	216	S	Servo PLL ground
SVSS	6	S	Servo analog ground
SVDD	4	S	Servo analog 3.3V power
ADVSS	18	S	Servo ADC ground
ADVDD	11	S	Servo ADC 3.3V power
System Control Pin			
RST_B	33	I	System reset (active low reset)
ROM / SRAM / Flash Interface (33)			
R_A[8]	34	O	ROM / SRAM / flash address bus bit [8]
R_A[9]	35	O	ROM / SRAM / flash address bus bit [9]
R_A[10]	37	O	ROM / SRAM / flash address bus bit [10]
R_A[11]	38	O	ROM / SRAM / flash address bus bit [11]
R_A[12]	39	O	ROM / SRAM / flash address bus bit [12]
R_A[13]	40	O	ROM / SRAM / flash address bus bit [13]
R_A[14]	41	O	ROM / SRAM / flash address bus bit [14]
R_A[15]	43	O	ROM / SRAM / flash address bus bit [15]
R_D[7]	44	I/O	ROM / SRAM / flash data bus [7]
R_D[6]	45	I/O	ROM / SRAM / flash data bus [6]

Signal	Pin	State	Description
R_D[5]	46	I/O	ROM / SRAM / flash data bus [5]
R_D[4]	48	I/O	ROM / SRAM / flash data bus [4]
R_D[3]	49	I/O	ROM / SRAM / flash data bus [3]
R_D[2]	50	I/O	ROM / SRAM / flash data bus [2]
R_D[1]	51	I/O	ROM / SRAM / flash data bus [1]
R_D[0]	52	I/O	ROM / SRAM / flash data bus [0]
R_A[0]	53	O	ROM / SRAM / flash address bus bit [0]
R_A[1]	54	O	ROM / SRAM / flash address bus bit [1]
R_A[2]	56	O	ROM / SRAM / flash address bus bit [2]
R_A[3]	57	O	ROM / SRAM / flash address bus bit [3]
R_A[4]	58	O	ROM / SRAM / flash address bus bit [4]
R_A[5]	59	O	ROM / SRAM / flash address bus bit [5]
R_A[6]	60	O	ROM / SRAM / flash address bus bit [6]
R_A[7]	61	O	ROM / SRAM / flash address bus bit [7]
R_A[16]	62	O	ROM / SRAM / flash address bus bit [16]
R_A[17]	64	O	ROM / SRAM / flash address bus bit [17]
R_A[18]	65	O	ROM / SRAM / flash address bus bit [18]
R_A19/GPIO	66	I/O	ROM / SRAM / flash address bus bit 19 or GPIO **Priority selection** / **Function** sft_cfg0[0]=1'b1 / R_A19 (default) sft_cfg2[4:2]=3'b010 / UART0 TX (other) / GPIO[32]
R_OE_B/GPIO	67	I/O	ROM / SRAM / flash output enable or GPIO **Priority selection** / **Function** sft_cfg1[4]=1'b1 / R_OE_B (default) sft_cfg4[2:0]=3'b100 / DSP FL0 (other) / GPIO[33]
R_WE_B/GPIO	68	I/O	ROM / SRAM / flash write strobe or GPIO **Priority selection** / **Function** sft_cfg1[5]=1'b1 / R_WE_B (default) sft_cfg4[5:3]=3'b100 / DSP FL1 (other) / GPIO[34]

<table>
<tr><th>Signal</th><th>Pin</th><th>State</th><th>Description</th></tr>
<tr><td>R_CS1_B/GPIO</td><td>69</td><td>I/O</td><td>ROM / SRAM / flash chip select #1 (first device) or GPIO

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg1[0]=1’b1</td><td>R_CS1_B (default)</td></tr><tr><td>(other)</td><td>GPIO[13]</td></tr></table></td></tr>
<tr><td>R_CS2_B/GPIO</td><td>70</td><td>I/O</td><td>ROM / SRAM / flash chip select #2 or GPIO

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg1[1]=1’b1</td><td>R_CS2_B (default)</td></tr><tr><td>sft_cfg4[8:6]=3’b100</td><td>DSP FL2</td></tr><tr><td>(other)</td><td>GPIO[35]</td></tr></table></td></tr>
<tr><td>R_CS3_B/GPIO</td><td>71</td><td>I/O</td><td>ROM / SRAM / flash chip select #3 or GPIO

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg1[2]=1’b1</td><td>R_CS3_B (default)</td></tr><tr><td>sft_cfg4[11:9]=3’b100</td><td>DSP FLAGOUT</td></tr><tr><td>(other)</td><td>GPIO[36]</td></tr></table></td></tr>
<tr><td colspan="4">Crystal / Clock Pins (2)</td></tr>
<tr><td>CLKIN</td><td>78</td><td>I</td><td>Clock input / crystal in (XTALI)</td></tr>
<tr><td>CLKOUT</td><td>77</td><td>O</td><td>Clock output / crystal out (XTALO)</td></tr>
<tr><td colspan="4">SDRAM Interface Pins (57)</td></tr>
<tr><td>M_DD[7]</td><td>80</td><td>I/O</td><td>SDRAM data bus [7]</td></tr>
<tr><td>M_DD[6]</td><td>81</td><td>I/O</td><td>SDRAM data bus [6]</td></tr>
<tr><td>M_DD[5]</td><td>82</td><td>I/O</td><td>SDRAM data bus [5]</td></tr>
<tr><td>M_DD[4]</td><td>83</td><td>I/O</td><td>SDRAM data bus [4]</td></tr>
<tr><td>M_DD[3]</td><td>84</td><td>I/O</td><td>SDRAM data bus [3]</td></tr>
<tr><td>M_DD[2]</td><td>86</td><td>I/O</td><td>SDRAM data bus [2]</td></tr>
<tr><td>M_DD[1]</td><td>87</td><td>I/O</td><td>SDRAM data bus [1]</td></tr>
<tr><td>M_DD[0]</td><td>88</td><td>I/O</td><td>SDRAM data bus [0]</td></tr>
<tr><td>M_WE_B</td><td>89</td><td>O</td><td>SDRAM write enable / row precharge</td></tr>
<tr><td>M_CAS_B</td><td>91</td><td>O</td><td>SDRAM column address strobe</td></tr>
<tr><td>M_RAS_B</td><td>92</td><td>O</td><td>SDRAM row address strobe / precharge</td></tr>
<tr><td>M_CS_B</td><td>93</td><td>O</td><td>SDRAM chip select</td></tr>
<tr><td>M_BA0</td><td>94</td><td>O</td><td>SDRAM bank select address [0]</td></tr>
<tr><td>M_DD[15]</td><td>96</td><td>I/O</td><td>SDRAM data bus [15]</td></tr>
<tr><td>M_DD[14]</td><td>97</td><td>I/O</td><td>SDRAM data bus [14]</td></tr>
<tr><td>M_DD[13]</td><td>98</td><td>I/O</td><td>SDRAM data bus [13]</td></tr>
<tr><td>M_DD[12]</td><td>99</td><td>I/O</td><td>SDRAM data bus [12]</td></tr>
<tr><td>M_DD[11]</td><td>101</td><td>I/O</td><td>SDRAM data bus [11]</td></tr>
</table>

Signal	Pin	State	Description
M_DD[10]	102	I/O	SDRAM data bus [10]
M_DD[9]	103	I/O	SDRAM data bus [9]
M_DD[8]	104	I/O	SDRAM data bus [8]
M_CLKO	106	O	SDRAM clock output
M_CKE	108	O	SDRAM clock enable
M_A[11]/GPIO	109	I/O	SDRAM address bus [11] or GPIO **Priority selection** / **Function** sft_cfg6[4]=1'b1 / M_A[11] (default) (other) / GPIO[14]
M_A[9]	110	O	SDRAM address bus [9]
M_A[8]	111	O	SDRAM address bus [8]
M_A[7]	113	O	SDRAM address bus [7]
M_A[6]	114	O	SDRAM address bus [6]
M_A[5]	115	O	SDRAM address bus [5]
M_A[4]	117	O	SDRAM address bus [4]
M_DQM1	118	O	SDRAM data input/output mask for M_DD[15:8]
M_DQM0	119	O	SDRAM data input/output mask for M_DD[7:0]
M_BA1	121	O	SDRAM bank select address [1] **Priority selection** / **Function** sft_cfg6[6]=1'b1 / M_BA1 (other) / GPIO[15]
M_A[10]	122	O	SDRAM address bus [10]
M_A[0]	123	O	SDRAM address bus [0]
M_A[1]	125	O	SDRAM address bus [1]
M_A[2]	126	O	SDRAM address bus [2]
M_A[3]	127	O	SDRAM address bus [3]
M_DD[31]	129	I/O	SDRAM data bus bit 31
M_DD[30]	130	I/O	SDRAM data bus bit 30
M_DD[29]	131	I/O	SDRAM data bus bit 29
M_DD[28]	133	I/O	SDRAM data bus bit 28
M_DD[27]	134	I/O	SDRAM data bus bit 27
M_DD[26]	135	I/O	SDRAM data bus bit 26
M_DD[25]	136	I/O	SDRAM data bus bit 25
M_DD[24]	138	I/O	SDRAM data bus bit 24
M_DQM3/GPIO	139	I/O	SDRAM data input/output mask for M_DD[31:24]
M_DQM2/GPIO	140	I/O	SDRAM data input/output mask for M_DD[23:16]
M_DD[23]	141	I/O	SDRAM data bus bit 23
M_DD[22]	143	I/O	SDRAM data bus bit 22

Signal	Pin	State	Description
M_DD[21]	144	I/O	SDRAM data bus bit 21
M_DD[20]	145	I/O	SDRAM data bus bit 20
M_DD[19]	146	I/O	SDRAM data bus bit 19
M_DD[18]	148	I/O	SDRAM data bus bit 18
M_DD[17]	149	I/O	SDRAM data bus bit 17
M_DD[16]	150	I/O	SDRAM data bus bit 16
M_A[12]/GPIO	151	I/O	SDRAM address bus [12] or GPIO **Priority selection** / **Function** sft_cfg6[5]=1'b1 / M_A[12] (default) (other) / GPIO[18]
Audio Interface (10)			
A_DATA[4] / GPIO	163	I/O	Serial audio data output for channel 9/8 or GPIO **Priority selection** / **Function** sft_cfg3[5]=1'b1 / A_DATA[4] (default) (other) / GPIO[57]
A_IEC_RX/GPIO	164	I/O	IEC-958 receive data **Priority selection** / **Function** sft_cfg3[7]=1'b1 / A_IEC_RX (default) (other) / GPIO[58]
A_IEC_TX/GPIO	165	I/O	IEC-958 transmit data **Priority selection** / **Function** sft_cfg3[7]=1'b1 / A_IEC_TX (default) (other) / GPIO[19]
A_DATA[0] / GPIO	166	I/O	Serial audio data output for channel 1/0 or GPIO **Priority selection** / **Function** sft_cfg3[7]=1'b1 / A_DATA[0] (default) (other) / GPIO[20]
A_DATA[1] / GPIO	168	I/O	Serial audio data output for channel 3/2 or GPIO **Priority selection** / **Function** sft_cfg3[7]=1'b1 / A_DATA[1] (default) (other) / GPIO[21]

<table>
<tr><th>Signal</th><th>Pin</th><th>State</th><th>Description</th></tr>
<tr><td>A_DATA[2] / GPIO</td><td>169</td><td>I/O</td><td>Serial audio data output for channel 5/4 or GPIO

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg3[3]=1’b1</td><td>A_DATA[2] (default)</td></tr><tr><td>(other)</td><td>GPIO[59]</td></tr></table></td></tr>
<tr><td>A_DATA[3] / GPIO</td><td>170</td><td>I/O</td><td>Serial audio data output for channel 7/6 or GPIO

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg3[4]=1’b1</td><td>A_DATA[3] (default)</td></tr><tr><td>(other)</td><td>GPIO[60]</td></tr></table></td></tr>
<tr><td>A_LRCK/GPIO</td><td>171</td><td>I/O</td><td>PCM data output L/R strobe

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg3[6]=1’b1</td><td>A_LRCK (default)</td></tr><tr><td>(other)</td><td>GPIO[61]</td></tr></table></td></tr>
<tr><td>A_BCK/GPIO</td><td>173</td><td>I/O</td><td>PCM bit clock

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg3[7]=1’b1</td><td>A_BCK (default)</td></tr><tr><td>(other)</td><td>GPIO[22]</td></tr></table></td></tr>
<tr><td>A_XCK/GPIO</td><td>174</td><td>I/O</td><td>Audio over-sampling clock

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg3[7]=1’b1</td><td>A_XCK (default)</td></tr><tr><td>(other)</td><td>GPIO[23]</td></tr></table></td></tr>
<tr><td colspan="4">GPIO (7)</td></tr>
<tr><td>GPIO</td><td>31</td><td>I/O</td><td>GPIO pin

<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg2[8:5]=4’b1110</td><td>UART1_TX</td></tr><tr><td>sft_cfg1[6]=1’b1</td><td>ISA_CH_RDY</td></tr><tr><td>sft_cfg5[2:0]=3’b011</td><td>DSP_IRQE</td></tr><tr><td>sft_cfg5[8:6]=3’b011</td><td>RI_INT[12]</td></tr><tr><td>sft_cfg5[11:9]=3’b011</td><td>RISC_INT[3]</td></tr><tr><td>sft_cfg5[14:12]=3’b011</td><td>RISC_INTE[1]</td></tr><tr><td>(other)</td><td>GPIO[4] (default)</td></tr></table></td></tr>
</table>

<table>
<tr><th>Signal</th><th>Pin</th><th>State</th><th>Description</th></tr>
<tr><td>IR_IN/TDM_DR</td><td>153</td><td>I/O</td><td>GPIO (for IR) or TDM data receive
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg4[14:13]=2’b10</td><td>TDM_DR</td></tr><tr><td>(other)</td><td>GPIO[53] (default)</td></tr></table></td></tr>
<tr><td>VFD_CLK/TDM_DX</td><td>154</td><td>I/O</td><td>GPIO (for VFD clock) or TDM data transmit
This pin must be pull-high to 3.3v.
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg4[14:13]=2’b10</td><td>TDM_DX</td></tr><tr><td>(other)</td><td>GPIO[54] (default)</td></tr></table></td></tr>
<tr><td>VFD_STB/TDM_FSX</td><td>155</td><td>I/O</td><td>GPIO (for VFD strobe) or TDM frame sync
This pin must be pull-high to 3.3v.
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg4[14:13]=2’b10</td><td>TDM_FSXR</td></tr><tr><td>(other)</td><td>GPIO[55] (default)</td></tr></table></td></tr>
<tr><td>VFD_DATA/TDM_CLK</td><td>156</td><td>I/O</td><td>GPIO (for VFD data) or TDM clock
This pin must be pull-high to 3.3v.
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg4[14:13]=2’b10</td><td>TDM_CLK</td></tr><tr><td>(other)</td><td>GPIO[56] (default)</td></tr></table></td></tr>
<tr><td>UA0_RX/GPIO</td><td>175</td><td>I/O</td><td>UART #0 data receive or GPIO
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg2[4:2]=3’b101</td><td>UART0_RX (default)</td></tr><tr><td>(other)</td><td>GPIO[62]</td></tr></table></td></tr>
<tr><td>UA0_TX/GPIO</td><td>176</td><td>I/O</td><td>UART #0 data transmit or GPIO
<table><tr><th>Priority selection</th><th>Function</th></tr><tr><td>sft_cfg2[4:2]=3’b101</td><td>UART0_TX (default)</td></tr><tr><td>(other)</td><td>GPIO[63]</td></tr></table></td></tr>
<tr><td colspan="4">Audio ADC pins (4)</td></tr>
<tr><td>AIN/AIN_L
AI_BCK</td><td>157</td><td>A</td><td>ADC input (left channel, with OP)
(bonding option) Digital audio input interface bit clock</td></tr>
</table>

Signal	Pin	State	Description
ATO AI_LRCK	158	A	ADC OP output. When not used, connect a 0.1uF to ground. (bonding option) Digital audio input interface L/R strobe
AIN_R AI_DATA	159	A	ADC input (right channel) (bonding option) Digital audio input interface data
VM	160	A	ADC input voltage reference. When not used, connect a 0.1uF to ground.
TV DAC (10)			
V_COMP	178	A	Compensation pin. A 0.1pF ceramic capacitor must be used to bypass this pin to VSSA. The lead length must be kept as short as possible to avoid noise.
V_BIAS	179		
V_FSADJ	180	A	Full-Scale adjustment control pin. The full-scale current of D/A converters can be adjusted by connecting a resistor (R_{SET}) between this pin and ground.
V_REFOUT	181	A	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive V_REFIN pin directly.
V_DAC[0]	182	A	Video DAC output #0. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[1]	185	A	Video DAC output #1. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[2]	186	A	Video DAC output #2. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[3]	189	A	Video DAC output #3. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[4]	190	A	Video DAC output #4. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
V_DAC[5]	193	A	Video DAC output #5. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.
Servo Digital Interface (16)			
TRAY_OUT	195		(Servo digital pins)
SC1_OUT	196		(Servo digital pins)
SPDC_OUT	197		(Servo digital pins)
SC_OUT	198		(Servo digital pins)
DMEA	199		(Servo digital pins)
FGIN	200		(Servo digital pins)
SRV_SCLK	19		(Servo digital pins)
SRV_SDATA	20		(Servo digital pins)
SRV_SDEN	21		(Servo digital pins)
SRV_DFCT	22		(Servo digital pins)
T_PLCK	23		(Servo digital pins)
T_SLRF	25		(Servo digital pins)
TDM_DX/ttin0_4/GPIO	26	I/O	TDM output data or GPIO
TDM_CLK/ttin1_5/GPIO	27	I/O	TDM master clock or GPIO

Signal	Pin	State	Description
TDM_FSXR/ttin2_6 /GPIO	28	I/O	TDM input/output frame signal or GPIO
TDM_DR/ttin3_7/G PIO/R_CS4_B	29	I/O	TDM input data or GPIO
Servo Analog Interface (25)			
TEO	203	A	(Servo analog pins)
FEO	204	A	(Servo analog pins)
HGIN	206	A	(Servo analog pins)
LGIN2	207	A	(Servo analog pins)
LGIN1	208	A	(Servo analog pins)
LPFNIN	209	A	(Servo analog pins)
PDFLT1	210	A	(Servo analog pins)
FDFLT	211	A	(Servo analog pins)
VREFO	212	A	(Servo analog pins)
PDRSET	214	A	(Servo analog pins)
FDRSET	215	A	(Servo analog pins)
DRESET	1	A	(Servo analog pins)
CNIN	2	A	(Servo analog pins)
SLVL	3	A	(Servo analog pins)
RFO	5	A	(Servo analog pins)
RFRP	7	A	(Servo analog pins)
RFRPLP	8	A	(Servo analog pins)
TEXOLP	9	A	(Servo analog pins)
TEXO	10	A	(Servo analog pins)
TEI	12	A	(Servo analog pins)
FEI	13	A	(Servo analog pins)
CSI	14	A	(Servo analog pins)
SBAD	15	A	(Servo analog pins)
VREF	16	A	(Servo analog pins)
VRGD	17	A	(Servo analog pins)

Note: Please reference SPHE8200 servo datasheet for servo related information.

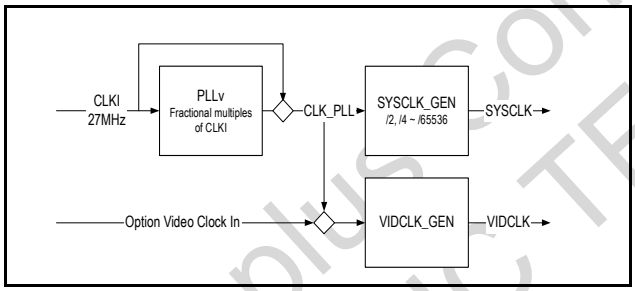
5.FUNCTIONAL DESCRIPTIONS

SPHE8200 is a highly integrated system-on-chip design. It includes DVD/CD servo controller, RISC processor, MPEG1/2 video decoder, programmable audio decoder, programmable peripheral controller, audio ADC and multi-format TV-encoder on a single chip.

5.1. PLL and ClockGen

SPHE8200 contains two PLLs to generate system clock (PLLv) and audio reference clocks (PLLa). Both the PLLs reference a single external 27MHz clock or crystal to generate all the required clocks.

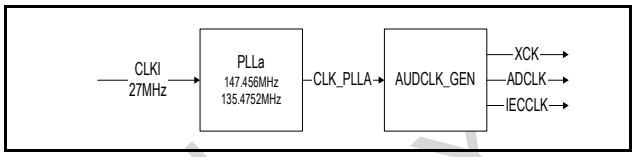
System clock is then derived from division of the PLLv output.



Some pre-defined PLLv/SYSCLK frequencies are listed below:

SYSCLK Frequency	PLLV Frequency
101.25MHz	405MHz
108MHz	216MHz
114.75MHz	459MHz
121.5MHz	486MHz
128.25MHz	256.5MHz
135MHz	270MHz
141.75MHz	283.5MHz
148.5MHz	297MHz
155.25MHz	310.5MHz
162MHz	324MHz
168.75MHz	337.5MHz
175.5MHz	351MHz
182.25MHz	364.5MHz
189MHz	378MHz

PLLa supports two center frequencies (for 48kHz family or 44.1kHz family) and generates required audio clocks from the audio system clock.



5.2. Power Control

SPHE8200 provides various levels of power-control mechanism in order to achieve minimum power consumption.

- Automatic power-save:
  Most hardware modules are automatically power-saved when not operating.
- Module-level stop-operation:
  SPHE8200 provides a function to turn off specific module from operating. Without explicit wake-up, the hardware module will remain static and consume very little power.
- System-level doze:
  For maximum power-saving, firmware could fine-tune system performance according to system task.

5.3. Embedded 32-bit RISC Controller

SPHE8200 includes a powerful 32-bit RISC processor. This RISC processor is utilized to manage decoding tasks as well as UI tasks. It can access to all the memory and devices, cooperate between processor systems. Audio decoder and I/O processor handshake with RISC processor through the mailbox registers.

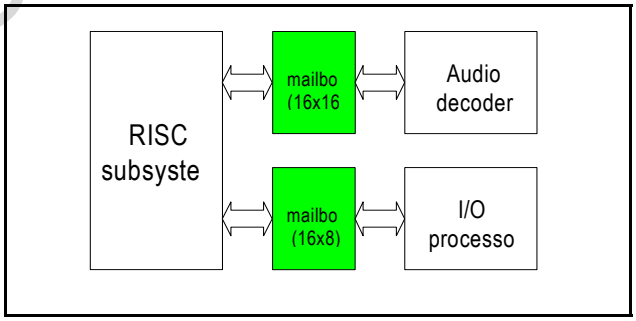


Figure 5-1: Communication between processors

The RISC processor is equipped with instruction and data caches. These caches can accelerate accesses to the SDRAM or ROM cacheable regions.

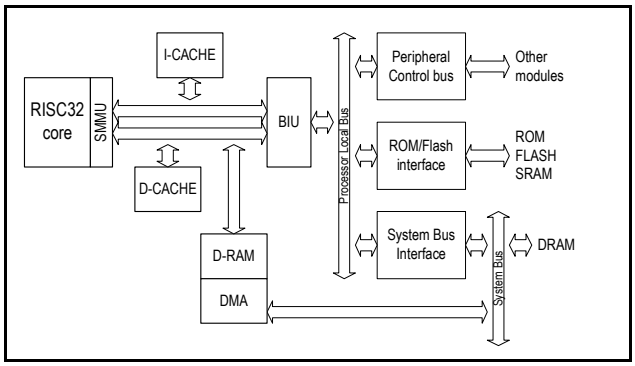


Figure 5-2: RISC subsystem

Table: RISC processor configuration

	Specification
I-Cache	8kbyte (2-way set associated)
D-Cache	4kbyte (direct-mapped)
D-RAM/DMA	1kbyte scratch buffer

The RISC sub-system is able to bootstrap from multiple sources. In typical application the RISC processor boots from external ROM device #1. Besides that, it also supports standalone booting without pre-loaded firmware.

5.4. RISC interface

RISC controllers interface to system via various interface control modules. These interface modules are mapped to the processor memory map and firmware could operate on them via typical memory accesses. These controllers include:

- ROM/FLASH/SRAM (RFS) controller
- RISC Memory Interface controller (SDRAM)
- Peripheral control interface

The RISC memory mapping of these controllers is shown in following table:

Table: RISC memory mapping

Memory range	Description
8000_0000-87ff_ffff	SDRAM (cached)
a000_0000-a7ff_ffff	SDRAM (uncached)
8800_0000-8fbf_ffff	ROM/FLASH/SRAM (cached)
a800_0000-afbf_ffff	ROM/FLASH/SRAM (uncached)
affe_8000-affe_ffff	Peripheral control registers
afff_0000-afff_03ff	DMA buffer

In additional to that, SPHE8200 includes dedicated RISC peripherals to assist the system tasks:

- Device interrupt controller:

  Device interrupt controller takes care of interrupt sources from on-chip devices and off chip sources. For each interrupt source the firmware is able to configure the interrupt behavior between edge-trigger and level-sensitive mode.

- Watchdog:

  Watchdog keeps monitoring RISC behavior and whenever firmware is in a deadlock, it can try to reset the system and keep the application functioning continuously.

- Timers

  There are 4-channel timers and 2 cascade counters for timed tasks. During A/V decoding, counters are utilized to synchronize audio and video.

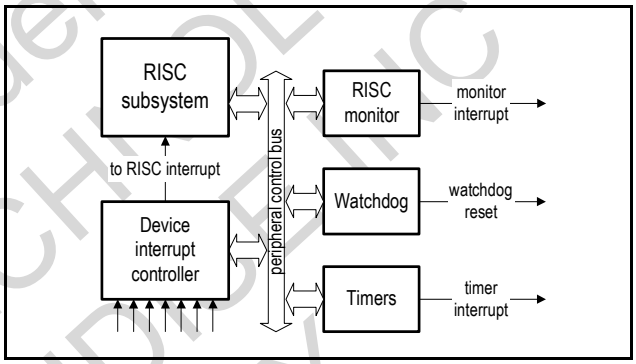


Figure 5-3: RISC dedicated hardware

Table: Device interrupt controller sources

Symbol	Description
INT_WDOG	Watchdog interrupt (if reset disabled)
INT_HSYNC	Interrupt when horizontal resync
INT_VSYNC	Interrupt when enter vertical resync
INT_FLD_ACT	Interrupt when enter active region
INT_FLD_SYNC	Interrupt when leave active region
INT_HOST	Host device interrupt
INT_TIMER0	Timer 0 interrupt
INT_TIMER1	Timer 1 interrupt
INT_TIMER2A	Timer 2 scale interrupt
INT_TIMER2B	Timer 2 count interrupt
INT_TIMER3A	Timer 3 scale interrupt
INT_TIMER3B	Timer 3 count interrupt
INT_TIMERW	Watchdog timer interrupt
INT_UART0	UART0 interrupt
INT_UART1	UART1 interrupt
INT_VDP0	Video decoder interrupt
INT_DSP	DSP interrupt
INT_EXT0	External interrupt #0
INT_EXT1	External interrupt #1
INT_EXT2	External interrupt #2
INT_EXT3	External interrupt #3
INT_IOP	IOP interrupt
INT_AUD	Audio hardware interrupt

5.5. ROM/Flash/SRAM controller

The SPHE8200 provides flexible connections to external ROM, Flash or SRAM (RFS). It can support up to 4 external RFS devices by using different chip-selects (R_CS_B[3:0]). The firmware can configure RFS memory anchor registers and map these devices into locations of memory space. For each memory space it can be in flash mode or in ISA mode. In FLASH mode the access timing is decided by wait-state setting, while in ISA mode the controller will reference external IO_CHRDY input.

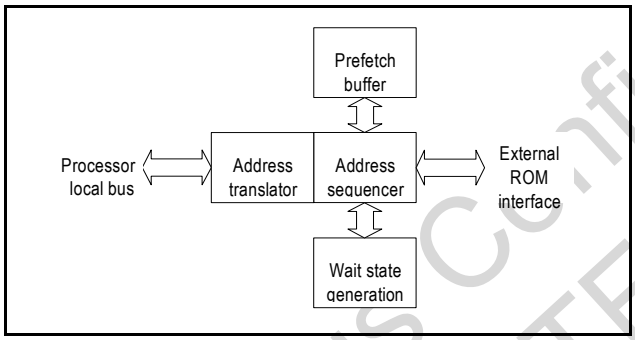


Figure 5-4: ROM/FLASH/SRAM controller

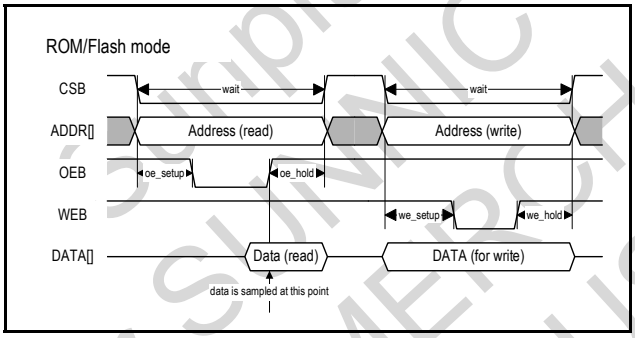


Figure 5-5: ROM/FLASH/SRAM mode timing

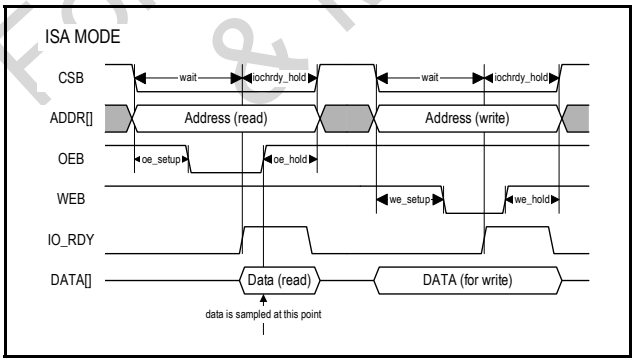


Figure 5-6: ISA mode timing

5.6. RISC Memory Interface

RISC memory interface provides a fast-path between processor local bus and system memory bus. Local bus transactions are mapped to system memory bus tasks.

5.7. Peripheral Control Interface

RISC firmware controls on-chip devices (such as video decoder, audio decoder..) by a dedicated peripheral control interface. Firmware controls the hardware behavior by writing to specific hardware registers with this interface.

5.8. CSS/CPPM support

SPHE8200 have built-in CSS and CPPM hardware support. For CSS the system supports accelerated DMA. For CPPM the system supports C2_D/C2_E and C2_DCBC functions.

5.9. MPEG Video Decoder

The system incorporates a powerful MPEG video decoding datapath and provides real-time video decoding of MPEGI/II bitstream. The bitstream can come from Servo hardware, ATAPI, TDM or UART. This enables various applications to be built over SPHE8200 such as real-time broadcasting over Ethernet.

The video decoder is a hardwired MPEG1/2 datapath. The system architecture is as in the figure. RISC subsystem is in charge of de-multiplexing the data and buffering formatted video data into video bitstream buffer resided in external SDRAM. Upon correct timing video decoder will decode the bitstream and write back reconstructed video frame for playback.

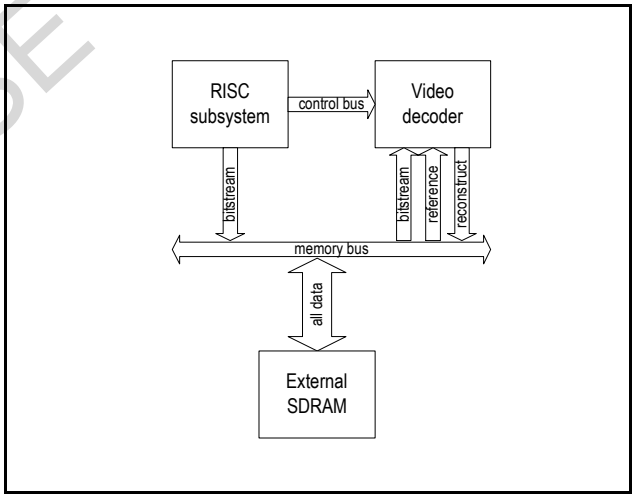


Figure 5-7: Interface between RISC and Video decoder

Advanced video decoding and display control mechanism is included to prevent tearing effect.

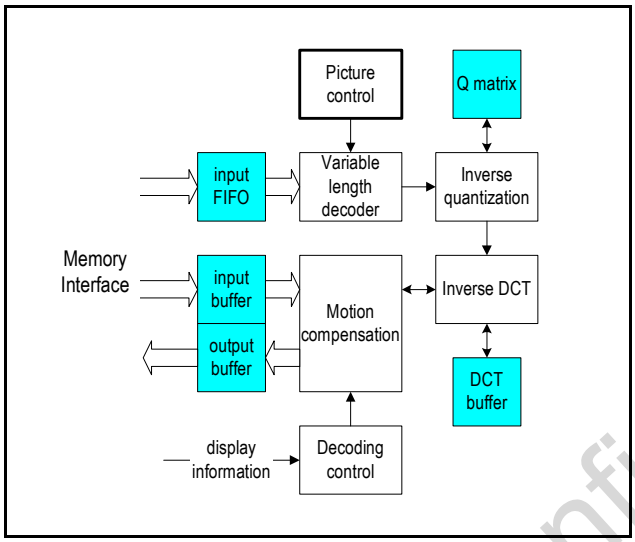


Figure 5-8: architecture of video decoding pipeline

5.10. Graphics Engine BondyPro®

For thin-client or set-top box applications, 2D graphics capabilities are key to system performance. This graphics engine is able to perform fast BitBlt and 2D drawing functions. The graphics engine is combined with 2 parts: graphics command interpreter and graphics datapath. Upon receiving command from RISC, interpreter will send micro-commands to graphics datapath, where raster operations are executed.

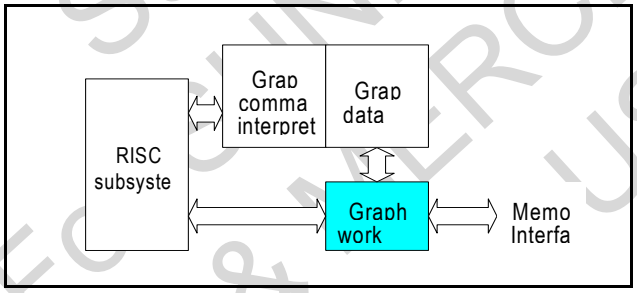


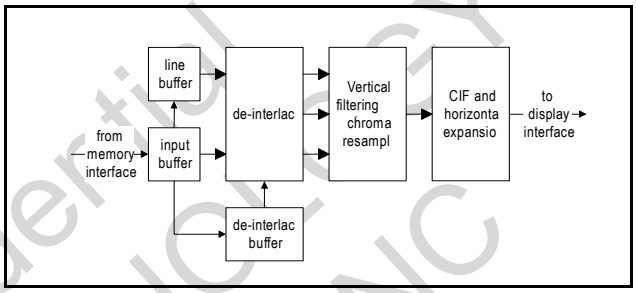
Figure 5-9: BondyPro® architecture

5.11. Video Post Processing

SPHE8200 includes powerful video-post-processing facilities to provide high video quality. It perform following functions:

- YUV411, YUV420, YUV422 and 8-bit indexed color
- SIF to CCIR601 interpolation
- MPEG1 CIF filter
- MPEG1/2 chroma vertical interpolation
- Up to 1/2x horizontal decimation
- Up to 1/512x vertical decimation
- Up to 1024x horizontal expansion
- Up to 1024x vertical expansion
- Powerful de-interlacing hardware
- Pan and scan function
- De-flicker during interlaced display
- Video contrast/bright/color enhancement

During runtime video post-processing hardware will fetch video sources from framebuffer and process the data as in the following figure.



5.12. Audio DSP

The SPHE8200 contains a high-performance 24-bit audio DSP optimized for embedded systems. The DSP processor can fetch operands from memories and perform multiplication-and-accumulation (MAC) in one cycle. During execution the DSP fetches instruction from main-memory or IROM, at the same time the ICACHE will store the LRU instructions. Data are loaded from and to main-memory by using the cycle-stealing DMA channels. There are 3 independent cycle-stealing DMA channels that allow DSP run without stalled by memory access.

The DSP works closely with RISC processors by using mailbox registers or shared-memory protocol. When downloaded with different codec firmware the DSP could support multi-standard audio and act as an accelerator for RISC in some case.

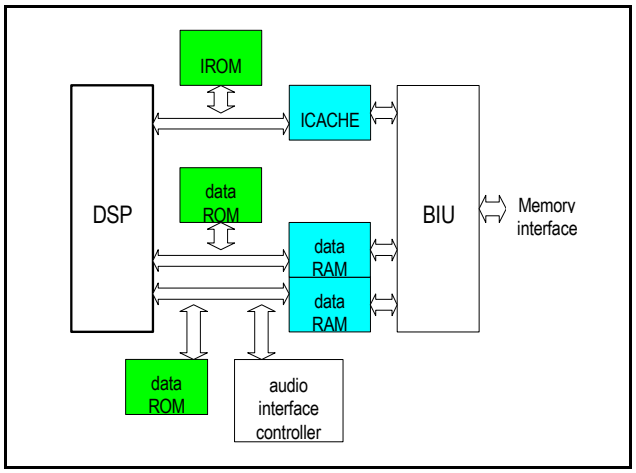


Figure 5-10: Audio DSP architecture

5.13. Audio Interface

The audio interface is in charge of servicing DSP and maintaining all audio-related tasks. It will buffer the DSP processed audio playback data and format them to audio DAC required format.

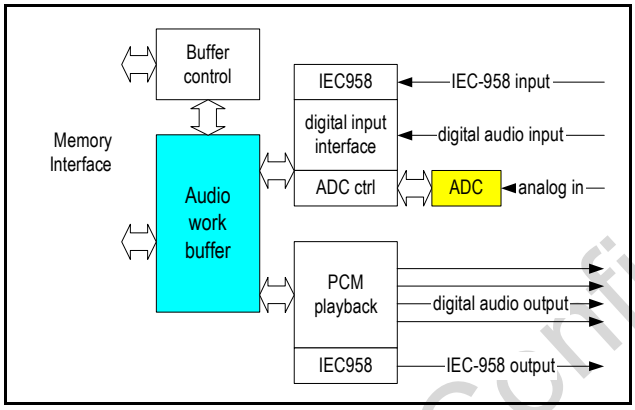


Figure 5-11: Audio Interface architecture

SPHE8200 support following audio DAC format combinations:

	32k	44.1k	48k	64k	88.2k	96k	192k
256fs	ok	ok	ok	ok	ok	ok	ok
384fs	ok	ok	ok	ok	ok	ok	ok

Data alignment	Left adjust, I2S, normal format
LRCK frame width	16b, 24b, 32b, 64b
Data bits	16b, 18b, 20b, 24b
Data sign extension	zero-extended, sign-extended

5.14. Integrated Audio Quality ADC

The embedded ADC is a 2-channel 64fs over-sampling ADC of12-bit quality. If required it could operate under 128fs over-sampling.

5.15. I/O Processor

The SPHE8200 includes an 8-bit micro-controller to handle most I/O jobs. IR, VFD and other slow devices can be interfaced using this I/O processor.

5.16. SDRAM Controller

SDRAM controller in SPHE8200 is very flexible and powerful. It was designed to meet different SDRAM timing requirement while achieving maximum performance. SDRAM tasks are optimized for maximum system performance. DRAM refreshing is issued automatically whenever required or SDRAM interface is idle for a given time.

For power-constrained applications SPHE8200 also implements SDRAM power-down modes to save dynamic operating power.

5.17. Sub-picture Decoder

For DVD and SVCD sub-picture content SPHE8200 includes an advanced multi-format sub-picture decoder. It could support real-time decode and display from raw sub-picture bitstream. Vertical interpolation is supported for PAL/NTSC translation or special effect.

5.18. On Screen Display

The on screen display (OSD) function of the SPHE8200 provides an overlay bitmap graphics on the final TV display. Applications can use this function to display specific information over the video display plane without operating on the video source.

The SPHE8200 can display multiple OSD regions on a single display frame, where every OSD regions can be in different size, location and color format. The OSD hardware supports 4, 16, 256 indexed color or 16-bit direct color. OSD regions are stored in main memory before display. During display, OSD decoder would read these header and data and interpret to be a graphic data that overlay with video to be output to the display interface.

5.19. Display Interface

The display interface of SPHE8200 integrates the video content generated from video-post-processing, sub-picture-decoder and on-screen-display modules. It also performs content cropping, underflow and overflow detection, and overall bright/contrast adjustment.

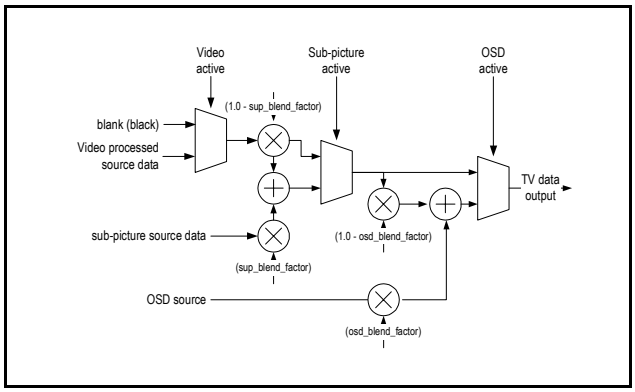


Figure 5-12: Display pipeline

The video enhancement process is show in following figure:

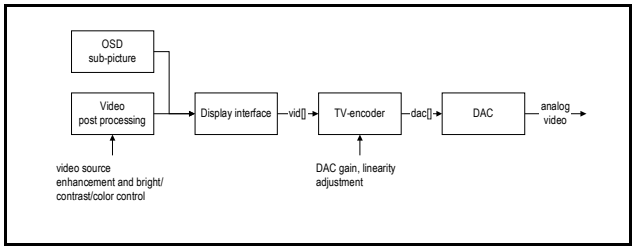


Figure 5-13: Display pipeline

5.20. Video DAC

SPHE8200 contains 6-channel 10-bit high-speed current-source DACs operating from 27MHz to 60MHz (for 480p/576p or SVGA display). The DAC outputs can drive a 37.5Ohm load directly.

5.21. ATAPI interface

SPHE8200 also supports ATAPI interface directly without glue logic. Although the SPHE8200 has integrated DVD/CD servo logics, with this interface the application could support other ATA/ATAPI compliant devices directly. The ATAPI/IDE interface is a standard ATA-5 host interface capable of PIO mode 2 to PIO mode 4 to external devices. By implementing this interface system could support IDE hard-disk drives, compact flash cards, ATAPI based DVDROM loaders or other ATA compliant devices.

5.22. GPIO

In SPHE8200 almost every pin that related to selectable features can serve as general-purpose input-output control function. When a pin is programmed to this mode, the RISC can take full control over the direction and output level.

5.23. UART

Two UART channels are provided for debugging or communication purpose. The UART can support standard serial port baud-rate and formats. It also supports auto baud-rate detection and hardware flow-control (CTS/RTS pair).

6.ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}	-0.3 to 5.5	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	-0.3 to 3.6	V
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	-0.3 to 1.98	V
Storage Temperature	T_{STG}	-55 to 150	°C
Soldering Temp. (Max. Time)	T_{SOLDER}	240 (for 5 Sec. Max.)	°C
Short circuit current	I_{OS}	50	mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. DC Operating Conditions

Recommended Operating Conditions (Voltage referenced to VSS=0V, TA=-0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	1.62	1.8	1.98	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	3.0	3.30	3.6	V
Input logic high voltage	V_{IH}	2.0	-	5.5	V
Input logic low voltage	V_{IL}	-0.3	-	0.8	V
Output logic high voltage	V_{OH}	2.4	-	-	V
Output logic low voltage	V_{OL}	-	-	0.4	V
Input leakage current	I_L	-10	-	10	uA

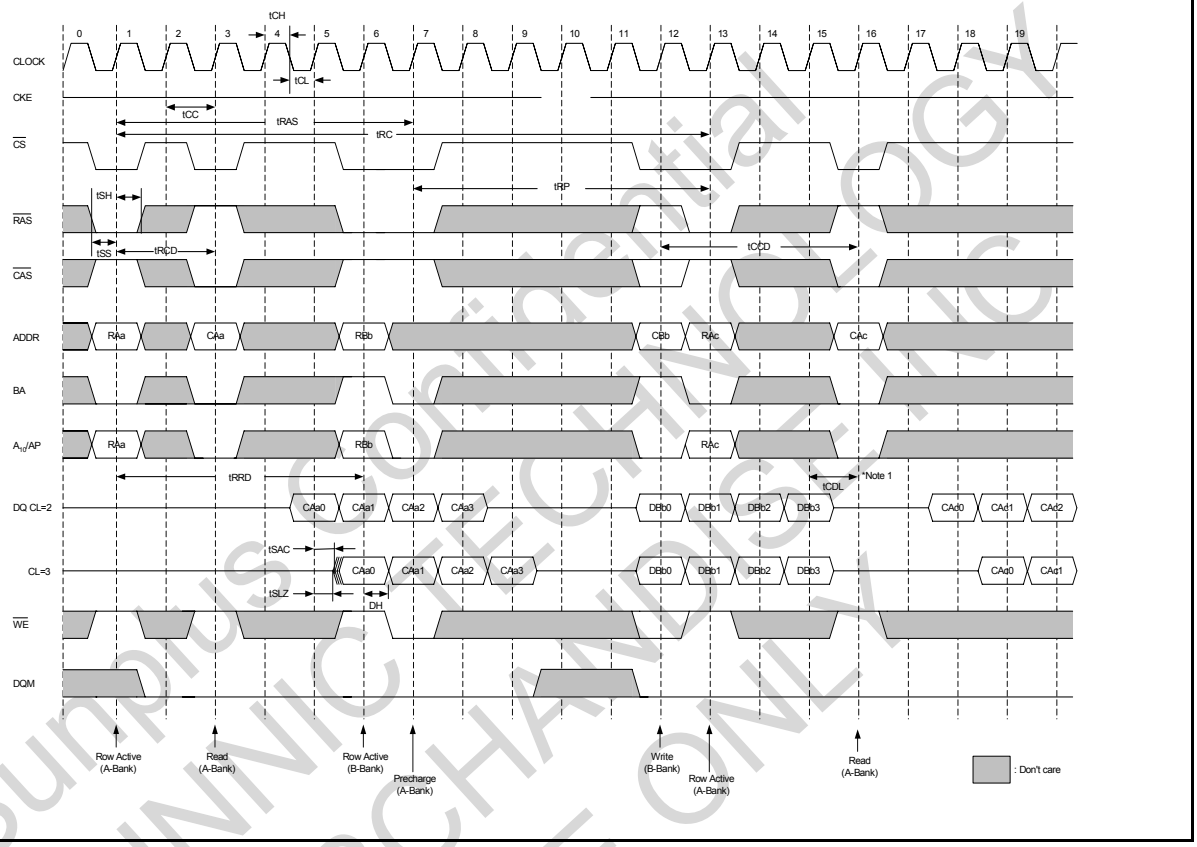
6.3. Capacitance

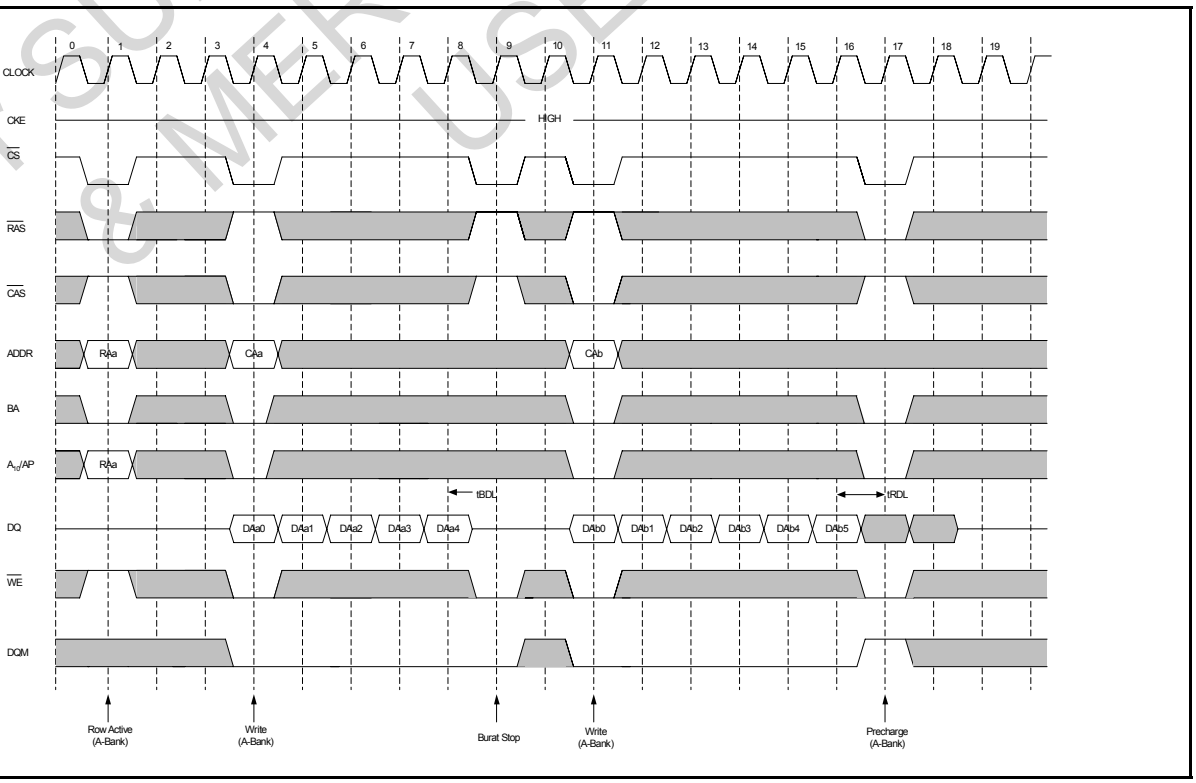
(V_{DDIO}=3.3V, TA=24°C, f=108MHz, V_{REF}=1.4V+-200mV)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input pin capacitance	C_{IN}	-	3.5	-	pF
Input pin capacitance	C_{OUT}	-	3.5	-	pF
Bidirectional pin capacitance	C_{BIDIR}	-	3.5	-	pF

6.4. AC Characteristics

6.4.1. SDRAM interface timing diagrams





(Recommended condition for DVD playback is listed in typical condition with f=121.5MHz)

Parameter	Symbol	Min	Typ	Max	Units
Row active to row active delay	t_{RRD}	1	2	4 *1	System clock cycle
RAS to CAS delay	t_{RCD}	1	2	4 *1	System clock cycle
Row precharge time	t_{RP}	1	2	4 *1	System clock cycle
Row active time	t_{RAS}	1	5	8 *1	System clock cycle
Row cycle time	t_{RC}	1	8	32 *1	System clock cycle
Last data in to new column address delay	t_{CDL}	1	1	4 *1	System clock cycle
Column address to column address delay	t_{CCD}	1	1	1	System clock cycle
CLK cycle time *2	t_{CC}	6	8.2	1000	ns
CLK to valid SDRAM output delay *2	t_{SAC}	-	6.0	6.5	ns
SDRAM output data hold time *2	t_{OH}	1	2	-	ns
CLK high pulse width *3	t_{CH}	-	3	-	ns
CLK low pulse width *3	t_{CL}	-	3	-	ns
CLK to SDRAM output Low-Z	t_{SLZ}	-	1.0	(t_{CC})	ns
CLK to SDRAM output High-Z	t_{SHZ}	-	6.0	(t_{SAC})	ns

*1 Using maximum values may limit system performance.

*2 Width of data window can be estimated from (t_{CC}-t_{SAC}+t_{OH}).

*3 Width of clock pulse depends on system clock cycle.

6.4.2. ROM / flash interface timing diagrams

ROM Compatible Mode

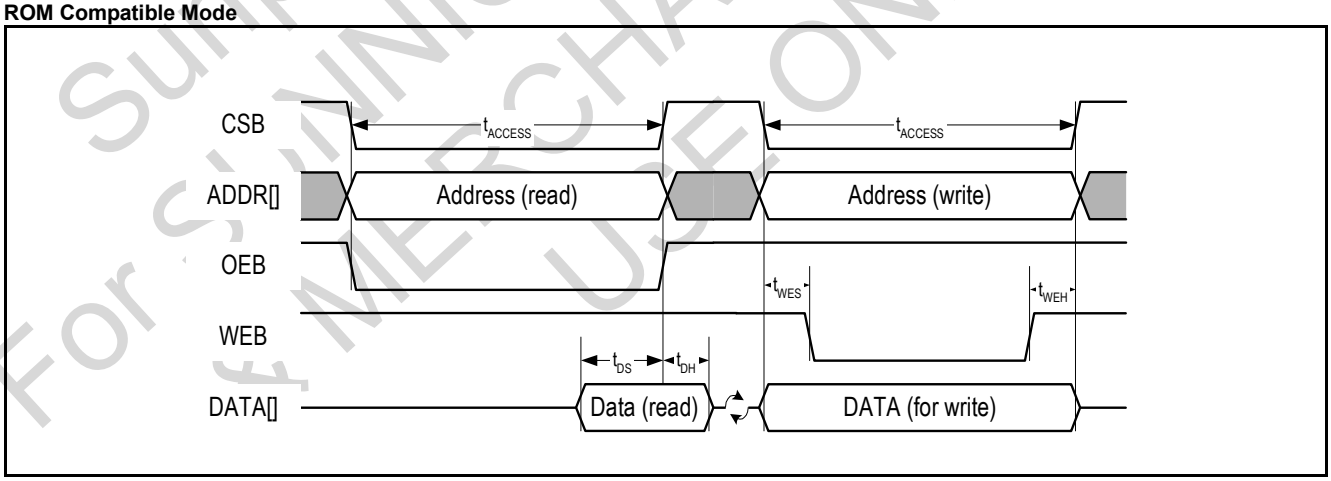


Figure 6-1: ROM / flash interface ROM mode access timing

Parameter	Symbol	Min	Typ	Max	Units
ROM / SRAM / flash access time	t_{ACCESS}	2	8 *1	31	System clock cycle
Data setup time for read	t_{DS}	5	-	-	ns
Data hold time for read	t_{DH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

*1 Recommended value when f=121.5MHz

ISA Compatible Mode

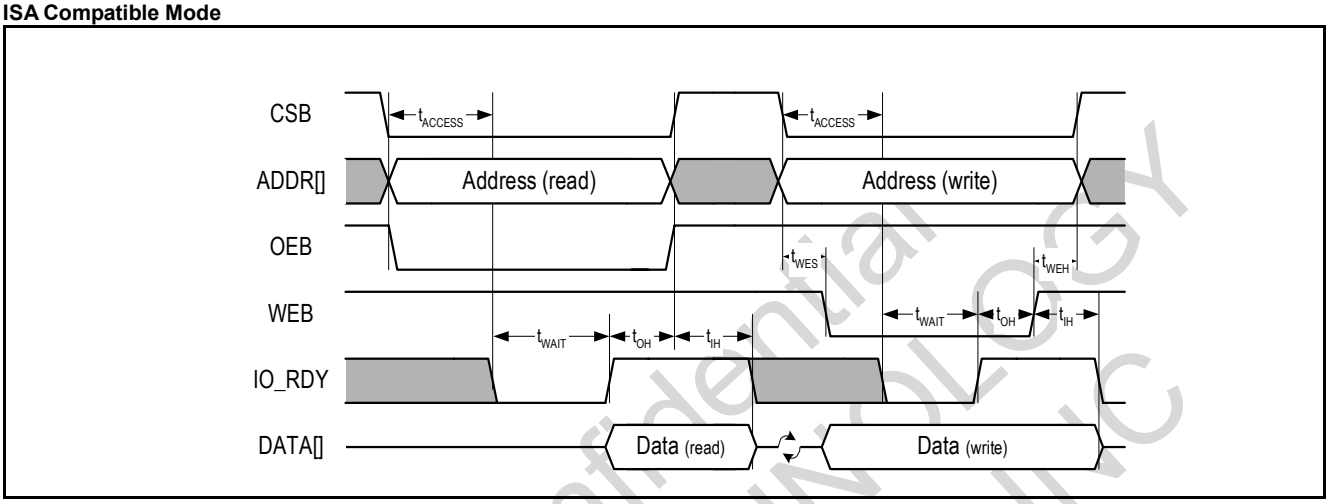


Figure 6-2: ROM / flash interface ISA mode access timing

Parameter	Symbol	Min	Typ	Max	Units
ISA access time *1	t_{ACCESS}	2	-	31	System clock cycle
IO_RDY wait time	t_{WAIT}	0	-	1000	ns
Output hold time	t_{OH}	1	-	-	System clock cycle
Input hold time	t_{IH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

*1 After this period of time IO_RDY_B must be stable and indicates correct status of target device.

6.4.3. Audio interface timing diagrams

Some audio interface configuration timing diagrams are shown below.

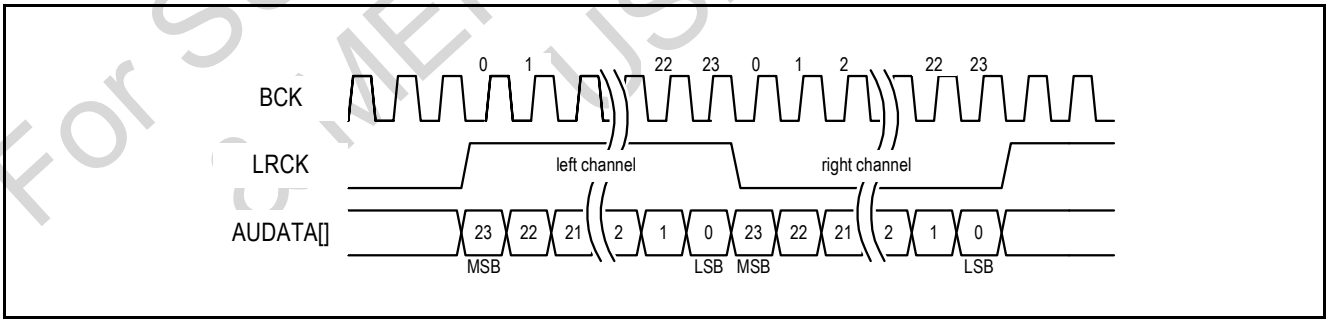


Figure 6-3: Normal mode / 24bit data / 24bit frame / MSB first

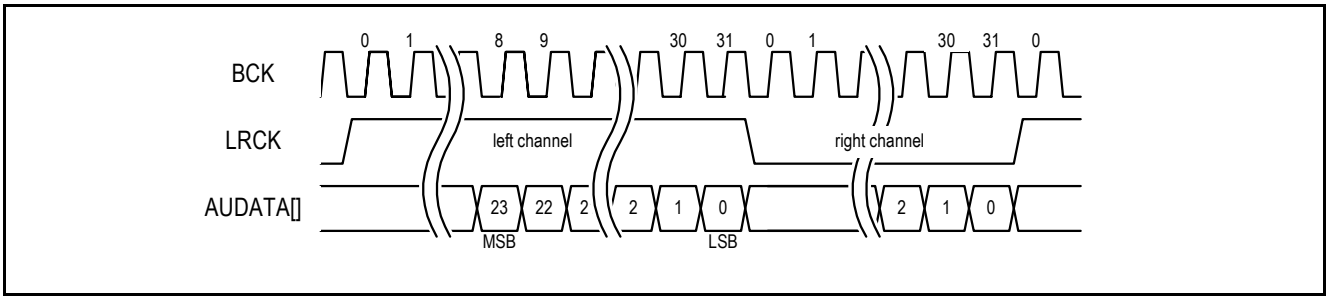


Figure 6-4: Right justified (normal) mode / 24bit data / 32bit frame / MSB first

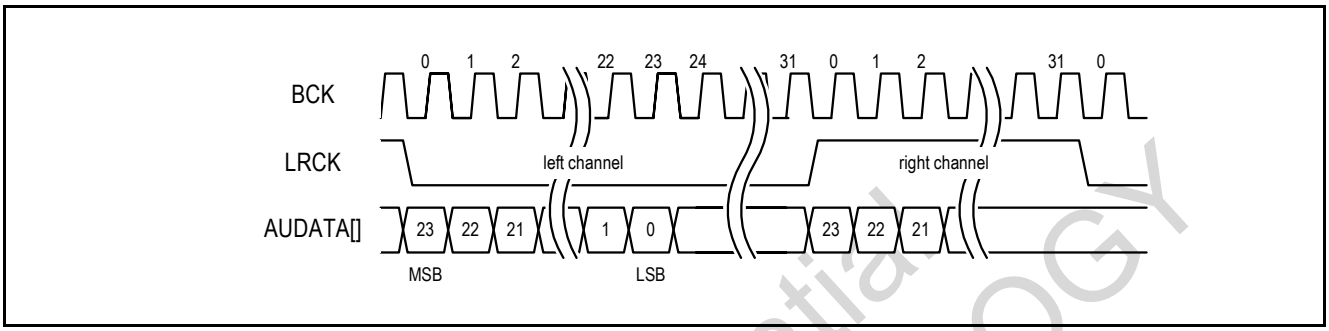


Figure 6-5: Left justified mode / 24bit data / 32bit frame / MSB first

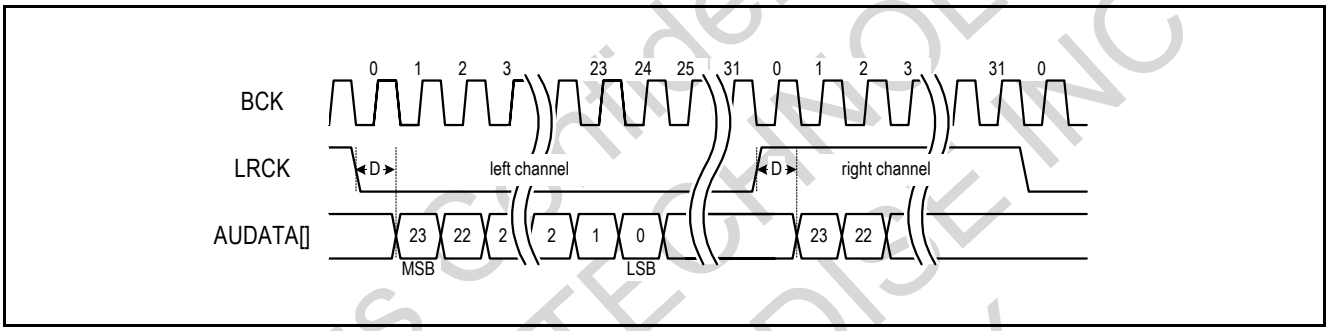


Figure 6-6: I²S mode / 24bit data / 32bit frame

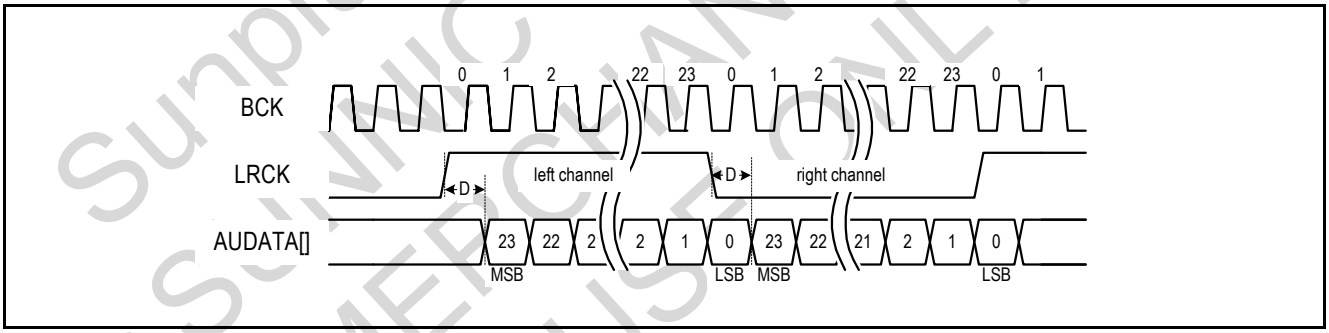


Figure 6-7: I²S mode / 24bit data / 24bit frame

Parameter	Symbol	Min	Typ	Max	Units
BCK rising to LRCK / AUDATA transition	t_S	-	0.5	-	System clock cycle

6.4.4. Video timing diagrams

Interlaced Modes

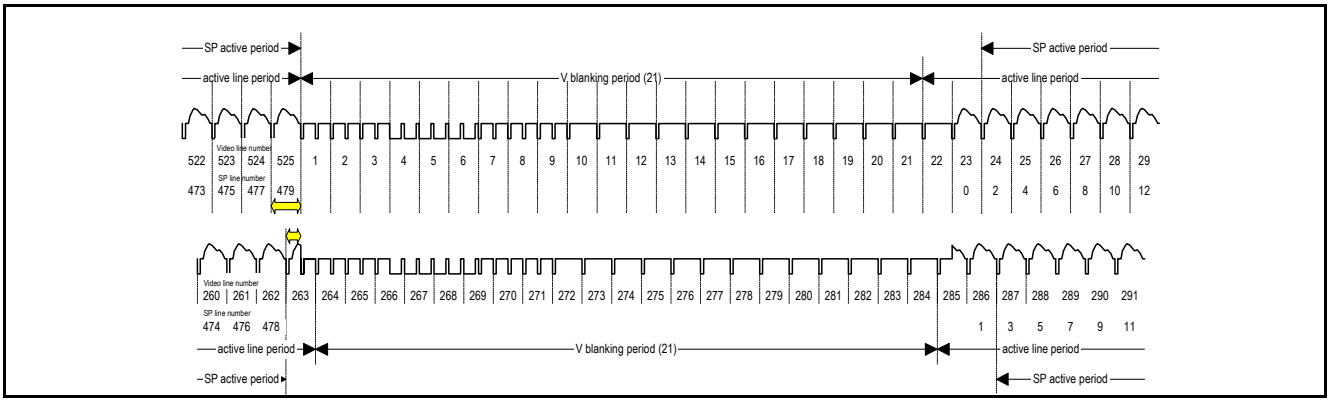


Figure 6-8: NTSC (480i) timing diagram

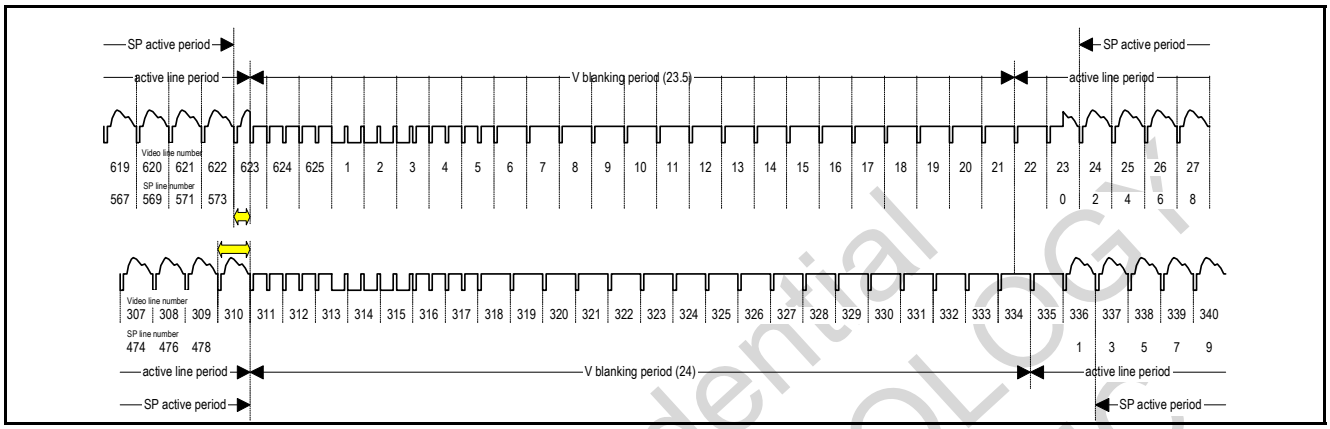


Figure 6-9: PAL (576i) timing diagram

Progressive Modes

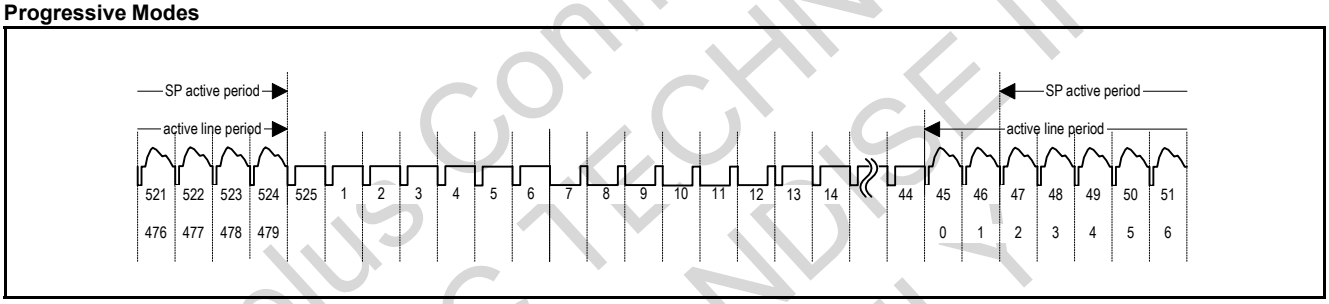


Figure 6-10: NTSC (480p) timing diagram

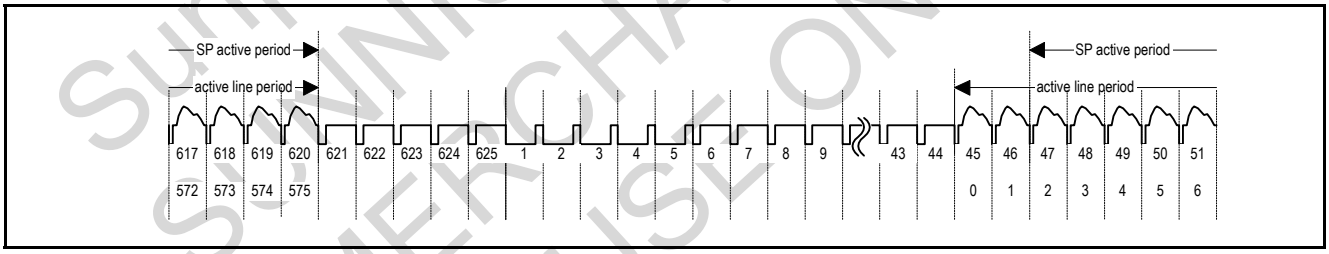


Figure 6-11: PAL (576p) timing diagram

7.REGISTER LIST

Name	Address	Description
GROUP 0		System Control Registers
sft_cfg0	0xbffe8044	Configure pin-mux 0
sft_cfg1	0xbffe8048	Configure pin-mux 1
sft_cfg2	0xbffe804c	Configure pin-mux 2
sft_cfg3	0xbffe8050	Configure pin-mux 3
sft_cfg5	0xbffe8058	Configure pin-mux 5
sft_cfg6	0xbffe805c	Configure pin-mux 6

0xbffe8044 sft_cfg0

Description

Pin MUX control register #0 (General)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field		RA26		RA25		RA24		RA23		RA22		RA21		RA20		RA19
Reset_2		1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Reset_3		0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Reset_*		1	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Reset_2: reset default when hardware-configuration is set to 2

Reset_3: reset default when hardware-configuration is set to 3

Reset_*: reset default for other hardware-configuration

RA19 ROM address bus bit 19 (R_A19) select

0: R_A19 is not available and ignored

1: Enable (default)

RA20 ROM address bus bit 20 (R_A20) select

00: R_A20 is not available and ignored

01: R_A20 is available at pin 19

10: R_A20 is available at pin 129

11: Reserved

RA21 ROM address bus bit 21 (R_A21) select

00: R_A21 is not available and ignored

01: R_A21 is available at pin 20

10: R_A21 is available at pin 130

11: Reserved

RA22 ROM address bus bit 22 (R_A22) select

00: R_A22 is not available and ignored

01: R_A22 is available at pin 21

10: R_A22 is available at pin 131

11: reserved

RA23 ROM address bus bit 23 (R_A23) select

00: R_A23 is not available and ignored

01: R_A23 is available only at 256 pin package

10: R_A23 is available at pin 133

11: reserved

RA24 ROM address bus bit 24 (R_A24) select

00: R_A24 is not available and ignored

01: R_A24 is available only at 256 pin package

10: R_A24 is available at pin 134

11: reserved

RA25 ROM address bus bit 25 (R_A25) select

00: R_A25 is not available and ignored

01: R_A25 is available only at 256 pin package

10: R_A25 is available at pin 135

11: reserved

RA26 ROM address bus bit 26 (R_A26) select

00: R_A26 is not available and ignored

01: R_A26 is available only at 256 pin package

10: R_A26 is available at pin 136

11: reserved

0xbffe8048 sft_cfg1

Description

Pin MUX control register #1 (General)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field	LPT		BOOT	pcmcia_WAIT			pcmcia_IORW			CHRDY	WE	OE	CS4	CS3	CS2	CS1
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

CS1 CS1 (ROM/FLASH chip select 1) function control

1: Enable Chip Select 1 (default)

0: Disable (CS1 becomes GPIO)

CS2 CS2 (ROM/FLASH chip select 2) function control

1: Enable Chip Select 2 (default)

0: Disabled (CS2 becomes GPIO)

CS3 CS3 (ROM/FLASH chip select 3) function control

1: Enable Chip Select 3 (default)

0: Disabled (CS3 becomes GPIO)

CS4 CS4 (ROM/FLASH chip select 4) function control

	1: Enable Chip Select 4 (default)
	0: Disabled (CS4 becomes GPIO)
OE	OEB (ROM/FLASH output enable) function control
	1: Enable OE function (default)
	0: Disabled (OEB becomes GPIO)
WE	WEB (FLASH/SRAM write enable) function control
	1: Enable WEB function (default)
	0: Disabled (WEB becomes GPIO)
CHRDY	IOCHRDY (ISA_IOCHRDY) function control
	1: Enable IOCHRDY input (i.e. output always tri-stated)
	0: Disabled (default)
pcmcia_IORW	PCMCIA IOR/IOW select
	000: Disabled (default)
	001: IOR from pin 19, IOW from pin 20
	010: IOR from pin 135, IOW from pin 136
	011: IOR from pin 58, IOW from pin 59
	100: Available only at 256 pin package
	101 to 111: Reserved
pcmcia_WAIT	bit 12-10 : PCMCIA_WAIT_B select
	000: Disabled (default)
	001: PCMCIA_WAIT_B is from pin 21
	010: PCMCIA_WAIT_B is from pin 61
	011: PCMCIA_WAIT_B is from pin 129
	100: PCMCIA_WAIT_B is from pin 138
	101: Available only at 256 pin package
	011 to 111: reserved
BOOT	RISC32 reset boot address
	0: RISC32 boots from bfc0_0000 (internal ROM) (default)
	1: RISC32 boots from 8000_0000 (SDRAM region)
LPT	LPT handshake signals (STROBE, ACK) select
	00: Disabled (default)
	01: LPT STROBE is from pin 62, LPT ACK is from pin 64
	10: LPT STROBE is from pin 135, LPT ACK is from pin 136
	11: Available only at 256 pin package

0xbffe804c sft_cfg2

Description

Pin MUX control register #2 (General)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field	SWAP	BRS	BRP	BRE	TV_LCD			UART1				UART0			IOP	ATAPI
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

ATAPI ATAPI interface

0: Disable (default)

1: Enabled

IOP IOP reset system

0: Disable (default)

1: Enabled

UART0 UART0 select

000: Disabled

001: UA0_RX is from pin 19, UA0_TXD is from pin 20

010: UA0_RX is from pin 65, UA0_TXD is from pin 66

011: UA0_RX is from pin 130, UA0_TXD is from pin 131

100: UA0_RX is from pin 144, UA0_TXD is from pin 145

101: UA0_RX is from pin 175, UA0_TXD is from pin 176 (default)

011,111: available only at 256 pin package

UART1 UART1 function selection

0000: Disable (default)

0001-1111: Please refer to pin-description

TV_LCD TV LCD function selection

000: Disable (default)

001-111: please refer to pin-description

BRE Bootstrap enable bit

0: Disable (default)

1: Enable

BRP Bootstrap RXD pull up enable (pin 175)

0: Internal pull up disable (default)

1: Internal pull up enable

BRS Bootstrap UART select

0: Bootstrap from UART0 (default)

1: Bootstrap from UART1

SWAP SWAP UART0 and UART1

0: No swap (default)

1: Swap UART0 and UART1 signals

0xbffe8050 sft_cfg3 (Audio interface and TV interface control)

Description

Pin MUX control register #3 (reference pin multiplex table for detailed information)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field	pc_SYNC		TELETEXT		SYNC				AUD	LRCK	AU4	AU3	AU2	EADC		
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0

EDAC External ADC select

000: Disabled (default)

001: BCK is from pin 19, LRCK is from pin 20, DATA is from pin 21

010: BCK is from pin 58, LRCK is from pin 59, DATA is from pin 60

011: BCK is from pin 34, LRCK is from pin 35, DATA is from pin 37

100: BCK is from pin 130, LRCK is from pin 131, DATA is from pin 133

101: BCK is from pin 141, LRCK is from pin 143, DATA is from pin 144

110: Available only at 256 pin package

111: reserved

AU2 Audio DAC interface data #2 (AU_DATA[2]) function control

0: Disabled (AU_DATA[2] becomes GPIO)

1: Enable (default)

AU3 Audio DAC interface data #3 (AU_DATA[3]) function control

0: Disabled (AU_DATA[3] becomes GPIO)

1: Enable (default)

AU4 Audio DAC interface data #4 (AU_DATA[4]) function control

0: Disabled (AU_DATA[4] becomes GPIO)

1: Enable (default)

LRCK Audio DAC interface LRCK function control

0: Disable

1: Enable (default)

AUD Audio function

0: Disable

1: enable (default)

SYNC H/V SYNC select

000: Disabled (default)

001: Reserved

010: Slave mode: HSYNC is from pin 146, VSYNC is from pin 148

011: Master mode: HSYNC is on pin 146, VSYNC is on pin 148

100: Slave mode: HSYNC is from pin 34, VSYNC is from pin 35

101: Master mode: HSYNC is on pin 34, VSYNC is on pin 35

110, 111: available only at 256 pin package

TELETEXT TELETEXT select

00: Disable (default)

01: Teletext BIT is from pin 149, teletext REQ is from pin 150

10: Teletext BIT is from pin 37, teletext REQ is from pin 38

11: available only at 256 pin package

pc_SYNC H/VSYNC PC select

00: Disabled (default)

01: HSYNC_PC is on pin 175, VSYNC_PC is on pin 176

10: HSYNC_PC is on pin 146, VSYNC_PC is on pin 148

11: HSYNC_PC is on pin 144, VSYNC_PC is on pin 145

0xbffe8058 sft_cfg5

Description

Pin MUX control register #5 (RISC interrupt control)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field		RISC_INTEXT			RISC_INT5_2			RISC_INT1								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RISC_INT1 RID INT1 bit 15 to bit 11 interrupt select

000: Disable (default)

001: INT1[11] is from pin 141,

INT1[12] is from pin 143,

INT1[13] is from pin 144,

INT1[14] is from pin 145,

INT1[15] is from pin 146

010: INT1[11] is from pin 129,

INT1[12] is from pin 130,

INT1[13] is from pin 131,

INT1[14] is from pin 133,

INT1[15] is from pin 134

011: INT1[11] is from pin 29,

INT1[12] is from pin 31,

INT1[13] is from pin 34,

INT1[14] is from pin 35,

INT1[15] is from pin 37

100-110 : Available only at 256 pin package

111: Reserved

RISC_INT5_2 RISC INT bit 5 to bit 2 interrupt select (level, active low)

000: Disable (default)

001: INTRQ_N[2] is from pin 141,

INTRQ_N[3] is from pin 143,

INTRQ_N[4] is from pin 144,

INTRQ_N[5] is from pin 145

010: INTRQ_N[2] is from pin 129,

INTRQ_N[3] is from pin 130,

INTRQ_N[4] is from pin 131,

INTRQ_N[5] is from pin 133

011: INTRQ_N[2] is from pin 29,

INTRQ_N[3] is from pin 31,

INTRQ_N[4] is from pin 34,

INTRQ_N[5] is from pin 35

100-110: Available only at 256 pin package

111: Reserved

RISC_INTEXT RISC INTEXT_N bit 5 to bit 0 interrupt select (level, active low)

000: Disable (default)

001: INTRQ_N[0] is from pin 141,

INTRQ_N[1] is from pin 143,

INTRQ_N[2] is from pin 144,

INTRQ_N[3] is from pin 145,

INTRQ_N[4] is from pin 146

INTRQ_N[5] is from pin 148

010: INTRQ_N[0] is from pin 129,

INTRQ_N[1] is from pin 130,

INTRQ_N[2] is from pin 131,

INTRQ_N[3] is from pin 133,

INTRQ_N[4] is from pin 134,

INTRQ_N[5] is from pin 135

011: INTRQ_N[0] is from pin 29,

INTRQ_N[1] is from pin 31,

INTRQ_N[2] is from pin 34,

INTRQ_N[3] is from pin 35,

INTRQ_N[4] is from pin 37,

INTRQ_N[5] is from pin 38

100-110: Available only at 256 pin package

111: Reserved

0xbffe805c sft_cfg6

Description

Pin MUX control register #6 (SDRAM interface control)

Attribute: RW

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit-field								SDQM3	SDQM2	SBA1	SA12	SA11				
Reset	0	0	0	0	1	1	0	1	1	1	1	1	0	1	1	1

SA11 SDRAM address 11 enable

0: SDRAM address 11 is disabled

1: SDRAM address 11 is enabled (default)

SA12 SDRAM address 12 enable

0: SDRAM address 12 is disabled

1: SDRAM address 12 is enabled (default)

SBA1 SDRAM BA1 enable

0: SDRAM BA1 is disabled

1: SDRAM BA1 is enabled (default)

SDQM2 SDRAM DQM2 enable

0: SDRAM DQM2 is disabled

1: SDRAM DQM2 is enabled (default)

SDQM3 SDRAM DQM3 enable

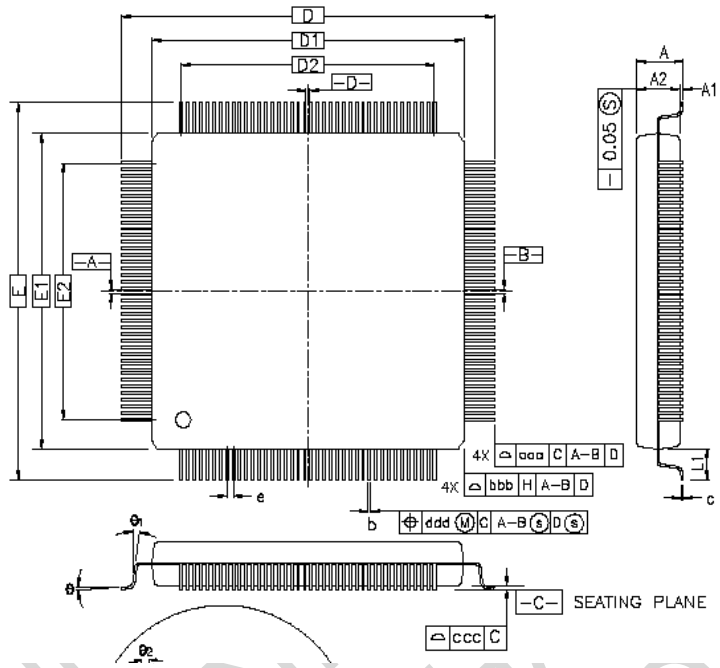
0: SDRAM DQM3 is disabled

1: SDRAM DQM3 is enabled (default)

8.PACKAGE/PAD LOCATION

8.1. Outline Dimensions

216-pin LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00 BSC.			1.024 BSC.		
D_1	24.00 BSC.			0.945 BSC.		
E	26.00 BSC.			1.024 BSC.		
E_1	24.00 BSC.			0.945 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

9.DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUN. 10, 2003	0.1	Original	14
OCT. 07, 2003	0.2	Add Functional Description and Electrical Specification and Register List	18-37