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ALS300 Media Audio Controller SPEC

Product Number : RL5305
Date: Mar, 26,1999
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Designer : Davis Kung

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Features :

- High performance PCI Digital Audio Subsystem Controller.
- Sound Blaster Pro/16 Emulation
- Support Audio CODEC 97 Specifications.
- Wave engine with wave sample downloadable.
- Support 1M X 4 ,4M X 4 DRAM.
- Normal and enhanced game Port
- 16 bit full-duplex playback/recording
- Full-duplex digital MODEM line IO from AC97 interface.
- Power down mode for notebook application.
- Build-In FM compatible synthesizer.
- Optional external E^2PROM support.

Applications :

- Windows and MPC level 2 compatible audio subsystem.
- PC games.
- Computer based audio reproduction
- Audio on-line tutorial
- Voice annotation or voice E-mail interface.
- Voice recognition or voice command controller.
- Text to speech.
- Karaoke/music sound box.
- MIDI controller.
- Software MODEM.

ALS300 Pin Descriptions:

128/160 pin QFP package

PCI Bus Interface Signal : 48 pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
AD0	I/O	59	50	PCI Address/Data bit 0	6mA TTL compatible CMOS IO (Vt=1.7V)
AD1	I/O	57	49	PCI Address/Data bit 1	6mA TTL compatible CMOS IO (Vt=1.7V)
AD2	I/O	56	48	PCI Address/Data bit 2	6mA TTL compatible CMOS IO (Vt=1.7V)
AD3	I/O	55	47	PCI Address/Data bit 3	6mA TTL compatible CMOS IO (Vt=1.7V)
AD4	I/O	53	46	PCI Address/Data bit 4	6mA TTL compatible CMOS IO (Vt=1.7V)
AD5	I/O	52	45	PCI Address/Data bit 5	6mA TTL compatible CMOS IO (Vt=1.7V)
AD6	I/O	51	44	PCI Address/Data bit 6	6mA TTL compatible CMOS IO (Vt=1.7V)
AD7	I/O	49	43	PCI Address/Data bit 7	6mA TTL compatible CMOS IO (Vt=1.7V)
AD8	I/O	46	41	PCI Address/Data bit 8	6mA TTL compatible CMOS IO (Vt=1.7V)
AD9	I/O	45	40	PCI Address/Data bit 9	6mA TTL compatible CMOS IO (Vt=1.7V)
AD10	I/O	43	39	PCI Address/Data bit 10	6mA TTL compatible CMOS IO (Vt=1.7V)
AD11	I/O	38	33	PCI Address/Data bit 11	6mA TTL compatible CMOS IO (Vt=1.7V)
AD12	I/O	36	32	PCI Address/Data bit 12	6mA TTL compatible CMOS IO (Vt=1.7V)
AD13	I/O	35	31	PCI Address/Data bit 13	6mA TTL compatible CMOS IO (Vt=1.7V)
AD14	I/O	34	30	PCI Address/Data bit 14	6mA TTL compatible CMOS IO (Vt=1.7V)
AD15	I/O	32	29	PCI Address/Data bit 15	6mA TTL compatible CMOS IO (Vt=1.7V)
AD16	I/O	17	17	PCI Address/Data bit 16	6mA TTL compatible CMOS IO (Vt=1.7V)
AD17	I/O	15	16	PCI Address/Data bit 17	6mA TTL compatible CMOS IO (Vt=1.7V)
AD18	I/O	14	15	PCI Address/Data bit 18	6mA TTL compatible CMOS IO (Vt=1.7V)
AD19	I/O	13	14	PCI Address/Data bit 19	6mA TTL compatible CMOS IO (Vt=1.7V)
AD20	I/O	11	12	PCI Address/Data bit 20	6mA TTL compatible CMOS IO (Vt=1.7V)
AD21	I/O	10	11	PCI Address/Data bit 21	6mA TTL compatible CMOS IO (Vt=1.7V)

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AD22	I/O	9	10	PCI Address/Data bit 22	6mA TTL compatible CMOS IO (Vt=1.7V)
AD23	I/O	7	9	PCI Address/Data bit 23	6mA TTL compatible CMOS IO (Vt=1.7V)
AD24	I/O	3	6	PCI Address/Data bit 24	6mA TTL compatible CMOS IO (Vt=1.7V)
AD25	I/O	158	128	PCI Address/Data bit 25	6mA TTL compatible CMOS IO (Vt=1.7V)
AD26	I/O	156	127	PCI Address/Data bit 26	6mA TTL compatible CMOS IO (Vt=1.7V)
AD27	I/O	155	126	PCI Address/Data bit 27	6mA TTL compatible CMOS IO (Vt=1.7V)
AD28	I/O	153	125	PCI Address/Data bit 28	6mA TTL compatible CMOS IO (Vt=1.7V)
AD29	I/O	152	124	PCI Address/Data bit 29	6mA TTL compatible CMOS IO (Vt=1.7V)
AD30	I/O	150	123	PCI Address/Data bit 30	6mA TTL compatible CMOS IO (Vt=1.7V)
AD31	I/O	149	122	PCI Address/Data bit 31	6mA TTL compatible CMOS IO (Vt=1.7V)
C/BE0	I/O	48	42	PCI Command/Byte enable bit 0	6mA TTL compatible CMOS IO (Vt=1.7V)
C/BE1	I/O	31	28	PCI Command/Byte enable bit 1	6mA TTL compatible CMOS IO (Vt=1.7V)
C/BE2	I/O	18	18	PCI Command/Byte enable bit 2	6mA TTL compatible CMOS IO (Vt=1.7V)
C/BE3	I/O	5	7	PCI Command/Byte enable bit 3	6mA TTL compatible CMOS IO (Vt=1.7V)
FRAME#	I/O	22	20	PCI Cycle Frame	8mA TTL compatible CMOS IO (Vt=1.7V)
IRDY#	I/O	23	21	PCI Initiator Ready	8mA TTL compatible CMOS IO (Vt=1.7V)
TRDY#	I/O	26	23	PCI Target Ready	8mA TTL compatible CMOS IO (Vt=1.7V)
STOP#	I/O	28	25	PCI Stop	8mA TTL compatible CMOS IO (Vt=1.7V)
IDSEL	I	6	8	PCI Initialization Device Select	TTL compatible CMOS input
DEVSEL#	I/O	27	24	PCI Device Select	8mA TTL compatible CMOS IO (Vt=1.7V)
CLK	I	143	117	PCI System Clock(33MHz)	TTL compatible CMOS input
RST#	I	141	115	PCI System Reset	Schmitt triggered CMOS input (1.4V-2.2V)
PAR	I/O	30	26	PCI Parity	6mA TTL compatible CMOS IO (Vt=1.7V)
REQ#	O	148	121	PCI Request	6mA TTL compatible CMOS output (Vt=1.7V)
GNT#	I	146	120	PCI Grant	TTL compatible CMOS input (Vt=1.7V)
INTA#	O	140	114	PCI Interrupt Request A	6mA TTL compatible CMOS output (Vt=1.7V)

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AC97 Interface Signal : 5 pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
SYNC	O	133	110	48Khz fixed rate sample sync	12mA TTL compatible CMOS output (Vt=1.7V)
BIT_CLK	I	136	112	12.288Mhz serial bit clock	TTL compatible CMOS input (Vt=1.7V)
SD_OUT	O	137	113	AC97 serial output stream	12mA TTL compatible CMOS output (Vt=1.7V)
SD_IN	I	135	111	AC97 serial input stream	TTL compatible CMOS input (Vt=1.7V)
RESET#	O	132	109	AC97 Reset	4mA TTL compatible CMOS output (Vt=1.7V)

ISA Interface : 38 pins (Enabled when BOND=0)

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
SA0	I	33	*	ISA system address bit 0	TTL input (Vt=1.7V)
SA1	I	37	*	ISA system address bit 1	TTL input (Vt=1.7V)
SA2	I	44	*	ISA system address bit 2	TTL input (Vt=1.7V)
SA3	I	47	*	ISA system address bit 3	TTL input (Vt=1.7V)
SA4	I	50	*	ISA system address bit 4	TTL input (Vt=1.7V)
SA5	I	54	*	ISA system address bit 5	TTL input (Vt=1.7V)
SA6	I	58	*	ISA system address bit 6	TTL input (Vt=1.7V)
SA7	I	63	*	ISA system address bit 7	TTL input (Vt=1.7V)
SA8	I	67	*	ISA system address bit 8	TTL input (Vt=1.7V)
SA9	I	71	*	ISA system address bit 9	TTL input (Vt=1.7V)
SA10	I	74	*	ISA system address bit 10	TTL input (Vt=1.7V)
SA11	I	77	*	ISA system address bit 11	TTL input (Vt=1.7V)
SA12	I	84	*	ISA system address bit 12	TTL input (Vt=1.7V)
SA13	I	87	*	ISA system address bit 13	TTL input (Vt=1.7V)
SA14	I	90	*	ISA system address bit 14	TTL input (Vt=1.7V)
SA15	I	94	*	ISA system address bit 15	TTL input (Vt=1.7V)
SAEN	I	110	*	ISA system address enable	TTL input (Vt=1.7V)
SD0	IO	126	*	ISA system data bus bit 0	4mA TTL compatible CMOS IO (Vt=1.7V)
SD1	IO	128	*	ISA system data bus bit 1	4mA TTL compatible CMOS IO (Vt=1.7V)
SD2	IO	130	*	ISA system data bus bit 2	4mA TTL compatible CMOS IO (Vt=1.7V)
SD3	IO	134	*	ISA system data bus bit 3	4mA TTL compatible CMOS IO (Vt=1.7V)
SD4	IO	138	*	ISA system data bus bit 4	4mA TTL compatible CMOS IO (Vt=1.7V)
SD5	IO	145	*	ISA system data bus bit 5	4mA TTL compatible CMOS IO (Vt=1.7V)
SD6	IO	147	*	ISA system data bus bit 6	4mA TTL compatible CMOS IO (Vt=1.7V)
SD7	IO	151	*	ISA system data bus bit 7	4mA TTL compatible CMOS IO (Vt=1.7V)
SIOW#	I	154	*	ISA IO write strobe	Schmitt triggered CMOS input (1.2V-2.6V)

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SIOR#	I	157	*	ISA IO read strobe	Schmitt triggered CMOS input (1.2V-2.6V)
DRQ0	O	25	*	ISA DMA request 0	4mA CMOS output with tri-state control
DRQ1	O	16	*	ISA DMA request 1	4mA CMOS output with tri-state control
DRQ3	O	8	*	ISA DMA request 3	4mA CMOS output with tri-state control
DACK0#	I	29	*	ISA DMA acknowledge 0	CMOS input (Vt=2.0V)
DACK1#	I	12	*	ISA DMA acknowledge 1	CMOS input (Vt=2.0V)
DACK3#	I	4	*	ISA DMA acknowledge 3	CMOS input (Vt=2.0V)
IRQ2/9	O	113	*	ISA interrupt request 2/9	4mA CMOS open drain output
IRQ5	O	101	*	ISA interrupt request 5	4mA CMOS open drain output
IRQ7	O	105	*	ISA interrupt request 7	4mA CMOS open drain output
IRQ10	O	20	*	ISA interrupt request 10	4mA CMOS open drain output
IRQ11	O	96	*	ISA interrupt request 11	4mA CMOS open drain output

Game Port/MIDI Interface Signal : 10 pins

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Pin Name	Type	P-160	P-128	Description	Characteristic Definition
MIDI_IN	I	131	108	MIDI serial input	Schmitt triggered CMOS input with 10KΩ pull up (1.7V-2.7V)
MIDI_OUT	O	129	107	MIDI serial output	8mA CMOS IO with 50KΩ pull up (Vt=1.7V)
GD0	I/O	107	88	Game Port A timer X	8mA Schmitt triggered CMOS IO (2.0V-3.0V)
GD1	I/O	106	87	Game Port A timer Y	8mA Schmitt triggered CMOS IO (2.0V-3.0V)
GD2	I/O	104	86	Game Port B timer X	8mA Schmitt triggered CMOS IO (2.0V-3.0V)
GD3	I/O	103	85	Game Port B timer Y	8mA Schmitt triggered CMOS IO (2.0V-3.0V)
GD4	I	102	84	Game Port A button A	Schmitt triggered CMOS input with 10KΩ pull up (2.0V-3.0V)
GD5	I	100	83	Game Port A button B	Schmitt triggered CMOS input with 10KΩ pull up (2.0V-3.0V)
GD6	I	99	82	Game Port B button A	Schmitt triggered CMOS input with 10KΩ pull up (2.0V-3.0V)
GD7	I	97	80	Game Port B button B	Schmitt triggered CMOS input with 10KΩ pull up (2.0V-3.0V)

DRAM Interface Signal : 20 pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
A0	O	92	77	DRAM address bit 0	4mA TTL compatible CMOS output (Vt=1.7V)
A1	O	91	76	DRAM address bit 1	4mA TTL compatible CMOS output (Vt=1.7V)
A2	O	89	75	DRAM address bit 2	4mA TTL compatible CMOS output (Vt=1.7V)
A3	O	88	74	DRAM address bit 3	4mA TTL compatible CMOS output (Vt=1.7V)
A4	O	86	72	DRAM address bit 4	4mA TTL compatible CMOS output (Vt=1.7V)
A5	O	85	71	DRAM address bit 5	4mA TTL compatible CMOS output (Vt=1.7V)
A6	O	83	70	DRAM address bit 6	4mA TTL compatible CMOS output (Vt=1.7V)
A7	O	81	69	DRAM address bit 7	4mA TTL compatible CMOS output (Vt=1.7V)
A8	O	78	64	DRAM address bit 8	4mA TTL compatible CMOS output (Vt=1.7V)
A9	O	76	63	DRAM address bit 9	4mA TTL compatible CMOS output (Vt=1.7V)
A10	O	75	62	DRAM address bit 10	4mA TTL compatible CMOS output (Vt=1.7V)
A11	O	73	61	DRAM address bit 11	4mA TTL compatible CMOS IO (Vt=1.7V)
DQ0	I/O	68	57	DRAM Data bit 0	4mA TTL compatible CMOS IO (Vt=1.7V)
DQ1	I/O	69	58	DRAM Data bit 1	4mA TTL compatible CMOS IO (Vt=1.7V)
DQ2	I/O	70	59	DRAM Data bit 2	4mA TTL compatible CMOS IO (Vt=1.7V)
DQ3	I/O	72	60	DRAM Data bit 3	4mA TTL compatible CMOS IO (Vt=1.7V)
RAS#	O	62	53	DRAM Row address strobe	4mA TTL compatible CMOS output (Vt=1.7V)
CAS0#	O	64	54	DRAM column address strobe 0	4mA TTL compatible CMOS output (Vt=1.7V)
CAS1#	O	65	55	DRAM column address strobe 1	4mA TTL compatible CMOS output (Vt=1.7V)
WE#	O	66	56	DRAM write enable	4mA TTL compatible CMOS output (Vt=1.7V)

Miscellaneous Signal : 6 pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
XTALI	I	118	97	Crystal or oscillator input (14.318M)	crystal / oscilator input pad
XTALO	O	117	96	Crystal output	crystal output pad
FILT	I/O	123	103	PLL filter IO	PLL filter IO
XCLK	O	120	98	Internal PLL clock output	2mA TTL compatible CMOS output
RING#	I	127	106	Ring detection input	Schmitt triggered CMOS input (1.4V-2.2V)
HOOK	O	125	105	Hook on output signal	2mA TTL compatible CMOS output with tri-stste control(Vt=1.7V)

E^2PROM Interface : 4 Pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
ROMCS	O	115	94	E^2PROM chip select	2mA TTL compatible CMOS output with 50KΩ pull low

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ROMCLK	O	111	91	E^2PROM clock	2mA TTL compatible CMOS output (Vt=1.7V)
ROMDOUT	I	114	93	E^2PROM serial data output	TTL compatible CMOS input (Vt=1.7V)
ROMDIN	O	112	92	E^2PROM serial data input	2mA TTL compatible CMOS output (Vt=1.7V)

Power/Ground : 17 pins

Pin Name	Type	P-160	P-128	Description	Characteristic Definition
VDD1	I	160	1	Digital power 5V	
VDD2	I	21	19	Digital power 5V	
VDD3	I	40	34	Digital power 5V	
VDD4	I	60	52	Digital power 5V	
VDD5	I	95	79	Digital power 5V	
VDD6	I	108	89	Digital power 5V	
VDD7	I	142	116	Digital power 5V	
VDD8	I	121	101	Digital power 5V	
AVDD	I	122	102	Analog power 5V	
GND1	I	1	5	Digital Ground	
GND2	I	24	22	Digital Ground	
GND3	I	41	38	Digital Ground	
GND4	I	80	65	Digital Ground	
GND5	I	98	81	Digital Ground	
GND6	I	116	95	Digital Ground	
GND7	I	144	118	Digital Ground	
AGND	I	124	104	Analog Ground	

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Bonding Option Pin : 1 pin

Pin Name	Type	Pin No	Description	Characteristic Definition
BOND	I	*	Bonding option pin	

BOND = 0 160 QFP
1 128 QFP

Part I : Specification for SB Core Logic

Spec modified from ALS120 :

1. Remove all recording command.
2. No support IDE CDROM and MODEM
3. Special MPU401 mode for internal Wave Engine.
4. Remove analog block. (Substitute analog block by AC97 CODEC)
5. All SB mixer write will generate an interrupt request via MXIRQ.
6. Disable hardware power down pin.
7. Add 128 bytes RAM for special MPU401 output.
8. Remove Enhanced Game-Port.

ALS300 Power-on latch :

On power up reset ,ALS300 latch the following pin state. Their default state are :

Pin Name	Default state
MIDIOUT	Internal 50KΩ pull high
ROMCS	Internal 50KΩ pull low

After reset, pull high resistors will be disconnected from VCC and pull low resistor will disconnect from GND. During the period of reset, the configuration register CR3 will latch those input pin state. Please refer to CR3 definition to get details.

I/O Register Address:

ESP (enhanced sound processor):

BASE+6h	W	ESP-RESET-PORT
BASE+Ah	R	ESP-READ-DATA
BASE+Ch	W	ESP-COMMAND/DATA
BASE+Ch	R	ESP-WR-STATUS
BASE+Eh	R	ESP-RD-STATUS8
BASE+Fh	R	ESP-RD-STATUS16

BASE = P 'N P logical device 0 port 60.1,0 and port 61.7-4;

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BASEENABLE = P 'N P logical device 0 port 30.0;

ESP-RD-STATUS = ESP-RD-STATUS8 or ESP-RD-STATUS16

Mixer & Control:

BASE+4h	R/W	MIXER-INDEX
BASE+5h	R/W	MIXER-DATA

FM (OPL3 compatible) synthesizer :

BASE+0-3h	R/W	OPL3/4 address:0-3
BASE+8,9h	R/W	OPL3/4 address:0,1
ADLIBBASE+0-3h	**R/W**	**OPL3/4 address:0-3**

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ADLIBBASE = 0388h (P 'N P logical device 1) ;
ADLIBENABLE = P 'N P logical device 1 port 30.0 (CR20.0);

Gameport :

GAMEBASE+0-7h	R	GAME-READ
GAMEBASE+0-7h	W	GAME-WRITE

GAMEBASE = 0200h (P 'N P logical device 2);
GAMEENABLE = P 'N P logical device 2 port 30.0 (CR21.0);

MPU401 And Wave-table Synthesizer:

MPU401BASE+0h	R	MIDI INPUT FIFO
MPU401BASE+0h	W	MIDI OUTPUT FIFO
MPU401BASE+1h	R	MIDI-STATUS
MPU401BASE+1h	W	MIDI-COMMAND
MPU401BASE+2h	R/W	RAM-CNT
MPU401BASE+3h	R	RAM-DATA

MPU401BASE = P 'N P logical device 3 port 60.1,0 (CR0C) and port 61.7-3 (CR0D);
MPU401ENABLE = P 'N P logical device 3 port 30.0 (CR0A);

CR3.5 = 1: Special MPU-401 or 0: Standard MPU-401
MPU401BASE+2~3h is effective only when CR3.5=1.

MIDIOUT : tri-state with internal pull up resisters when power up reset.

0	external 10K pull down
1	internal 50K pull up

Power up value
CR3.5 power up latch value of MIDIOUT

On power up reset , MIDIOUT will tri-state with 50K internal pull up resistors, after reset, these resistors will be disconnected from VCC.
Power Management Control Register

BASE+7h	R/W	POWER DOWN REGISTER
BASE+Bh	R/W	POWER MANAGEMENT REGISTER
BASE+Dh	R	ACTIVITY STATUS REGISTER

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POWER MANAGEMENT REGISTER:
8 bit read / write
Default FFh

Bit 7		FM clock select 1 : 14.318M or 14.318M/8 0 : 2M (from internal clock chip)
Bit 6	X	Reserved for future usage
Bit 5	0	power down OPL3
Bit 4	**0**	**power down wave engine**
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	0	power down MPU401 block
Bit 0	X	reserved for future usage

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Every bit of this register can read/write by PC and set to 1 by PC reset or by **activity register** specific bit is set to 1. Wave engine is waked up by bit 4 of **activity register** any time.

ACTIVITY STATUS REGISTER:
Read only
Default 00h

Bit 7,6	X	reserved, read as 0
Bit 5	1	OPL3 is active
Bit 4	**1**	**wave engine is active**
Bit 3	X	reserved, read as 0
Bit 2	X	reserved, read as 0
Bit 1	1	MPU401 block is active
Bit 0	X	reserved, read as 0

Any read of this register will clear all bits to zero. Each bit will be set when any of the following conditions happened:

Bit 5 = I/O access of OPL3 register (chip select active)
Bit 4 = CR3.5 & Bit 1
Bit 1 = I/O access of MPU401 port + MIDIIN input has ever been low

POWER DOWN REGISTER:
Read / write
Default A5h

Bit 7-0	software power down byte

When write 5Ah to this register, ALS300 will enter S/W power down mode until wake up by write with A5h. All other value will be ignored.

Game Port Definition:

When I/O write to gameport, ALS300 will drive GD3, GD2, and GD1 low with 3-5ns time delay from each other. After system IO write command goes inactive(SIOW_ goes high), ALS300 will sustain to drive low for extra **2us** time period. At this time period, any read to gameport will force ALS300 to drive SD0-3 with 1 and SD7-4 with input data form GD7-GD4. After this time period, ALS300 will drive SD0-7 with input data from those pins when I/O read to gameport.
ALS300 implement GD0 differently from GD1~3. It usually drive GD0 to low. When Game-port write command is active, GD0 is tri-state until level on GD0 is high again. This implementation work fine with analog joystick and digital game pad.

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SD7	GD7
SD6	GD6
SD5	GD5
SD4	GD4
SD3	invert of GD3
SD2	invert of GD2
SD1	invert of GD1
SD0	invert of GD0

GAMEPORT = GAMEBASE+0-7h

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MPU401 mode definition :

Standard-MPU401 Mode : (CR3.5=0)

Data access is identical to MPU401. Please refer to MIDI programming.

Special-MPU401 Mode : (CR3.5=1)

In this mode, any data write via MPU401 data port will store in RAM and will not send out via MIDIOUT. Read RAM-DATA will fetch data from RAM. When RAM is not empty, ALS300 will generate an IRQ via MPU401 IRQ line. **Note that the RAM is implemented as FIFO.** Writing RAM-CNT will acknowledge special MPU401 IRQ.

RAM-CNT **R/W**

Default : 80h

bit 7	RAM empty flag
0	Non-empty
1	Empty
bit 6~0	RAM write pointer

Write this register will acknowledge special MPU401 IRQ.

RAM-DATA **Read only**

bit 7~0	MIDI-DATA in Special-MPU401 mode

FM synthesizer :

Refer to "ALS120 FM synthesizer specification"

ESP Register Definition:

ESP-RESET-PORT:

Write only

Bit 0	0	normal
	1	reset ESP
Bit 7..1	X	reserved

ESP_RESET should do the following things:

a. Reset ESP to no operation status and clear ESP busy flag.
b. Flush primary output FIFO.
c. Reset any flag that may affect command execution.
d. Reset data latched by SB D/A to middle range.
e. Reset sample frequency to 44.1KHz.
f. Reset DMA block length to 0x7ff.

ESP-RD-STATUS

Read only

Bit 7	0	no data on ESP-READ-DATA
	1	data available at ESP-READ-DATA port
Bit 6..0	X	reserved (same as ESP-READ-DATA bit 6..0)

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Read ESP-RD-STATUS8 will clear interrupt generated by the ESP for **non-BX type DMA** and MIDI.
Read ESP-RD-STATUS16 will clear interrupt for **BX type DMA**.
After CPU read the data from ESP-READ-DATA port, bit 7 of this read status port will reset to 0 (no data) until the next read data is available and bit 7 set to 1 (data available).

ESP-READ-DATA
Read only

Bit 7..0	X	the data return by ESP

ESP-COMMAND/DATA
Write only

Bit 7..0	X	the command or data to ESP

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ESP-WR-STATUS:
Read only

Bit 7	0	ESP is available for next command/data
	1	ESP is busy
Bit 6..0	X	reserved (same as ESP-READ-DATA bit 6..0)

After CPU write the command/data to the ESP-COMMAND/DATA port, bit 7 of this write status will set to 1 (busy) until the ESP processed the written command/data and waiting for the next command/data by reset bit 7 to 0 (not busy). Any acknowledge byte must be readback before any new command is issued. ESP will be set busy if any DMA operation is started and will be set not busy if command port is read twice.

Interrupt Acknowledge Procedure:

1. IO read(ESP-RD-STATUS8), clear non BX type DMA IRQ
2. IO read(ESP-RD-STATUS16), clear BX type DMA IRQ .
3. IO read(MIDI-DATA), clear MPU401 MIDI interrupt
4. **Write RAM-CNT clear Special-MIDI type IRQ**
5. **No acknowledge is required for SB-Mixer IRQ.**

MPU-401 MIDI Register Definition:

MIDI-STATUS
Read only

Bit 7	0	MIDI input data is available
	1	no MIDI input
Bit 6	0	ready for MIDI data output or new MIDI command
	1	MIDIOUT FIFO full or MIDIOUT FIFO not empty when MIDI_RESET (if CR3.5=0) Special MPU401 RAM is full (if CR3.5=1)
Bit 5		MIDI RAM status (Effective in special MIDI mode)
	0	Not Full
	1	Full
Bit 5-0		reserved

MIDI-COMMAND
Write only

Bit 7..0	command to MIDI controller

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In **pass-thru** mode,

ENTER_UART 03Fh
Return ack byte (0FEh) in **midi-data**, generate an interrupt if switch to UART mode successfully. Reading data port will clear the interrupt signal.

MIDI_RESET 0FFh
Return ack byte (0FEh) in **midi-data**, generate an interrupt, stay in **pass-thru** mode.

In UART mode,

MIDI_RESET 0FFh
Flush MIDIIN FIFO, wait until MIDIOUT FIFO/MIDI RAM empty, go to **pass-thru** mode .

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MIDI-DATA
Read/write

Read
Bit 7..0 MIDI data input in UART mode or acknowledge byte

Write
Bit 7..0 MIDI data output in UART mode

ALS300 Mixer Register Definition:

MIXER-INDEX
Read/write

Bit 7 0 mixer
1 control

Bit 6..0 index

MIXER-DATA
Read/write

Bit 7..0 mixer or control data register by **mixer-index**

MX00-MX7F mixer data register 00-7F base on **mixer-index** value
CR00-CR3F control data register 00-3F base on **mixer-index** value with bit 7 and 6 = 1.
SBCONFIGn = MX80-MXBF

Write the following mixer register will generate a SB-Mixer type IRQ to "PCI block" :

MX00, MX02, MX04, MX06, MX08, MX0A, MX0C, MX22
MX24, MX26, MX28, MX2E, MX30, MX31, MX32, MX33
MX34, MX35, MX36, MX37, MX38, MX39, MX3A, MX3B
MX3C,MX3D,MX3E, MX3F, MX40, MX41, MX42, MX4C
MX80, MX81, MXC6,MXC8

Sound Blaster Pro:

MX00 mixer reset
Write only

Any write to this port will reset MX00-MX7F to default value. ESP_RESET() does not affect any of the mixer register.

MX02 master volume

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Ghost register

Write
Bit 7 X
Bit 6 X
Bit 5 X
Bit 4 X
Bit 3 MX30.7 & MX31.7
Bit 2 MX30.6 & MX31.6
Bit 1 MX30.5 & MX31.5
Bit 0 MX30.4 & MX31.4

Bit 3 MX30.3
Bit 3 MX31.3

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Read
Bit 7 MX30.7
Bit 6 MX30.6
Bit 5 MX30.5
Bit 4 MX30.4
Bit 3 MX31.7
Bit 2 MX31.6
Bit 1 MX31.5
Bit 0 MX31.4

Bit 7..4 reserved
Bit 3..0 0 to 15, master volume left and right in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX04 digital audio left/right volume
Ghost register

Write
Bit 7 MX32.7
Bit 6 MX32.6
Bit 5 MX32.5
Bit 4 MX32.4
Bit 3 MX33.7
Bit 2 MX33.6
Bit 1 MX33.5
Bit 0 MX33.4

Bit 7 MX32.3
Bit 3 MX33.3

Read
Bit 7 MX32.7
Bit 6 MX32.6
Bit 5 MX32.5
Bit 4 MX32.4
Bit 3 MX33.7
Bit 2 MX33.6
Bit 1 MX33.5
Bit 0 MX33.4

Bit 7..4 0 to 15, digital audio left volume in 3 dB step

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Bit 3..0 0 to 15, digital audio right volume in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX06 music volume
Ghost register

Write
Bit 7 X
Bit 6 X
Bit 5 X
Bit 4 X
Bit 3 MX34.7 & MX35.7
Bit 2 MX34.6 & MX35.6
Bit 1 MX34.5 & MX35.5
Bit 0 MX34.4 & MX35.4

Bit 3 MX34.3
Bit 3 MX35.3

Read
Bit 7 MX34.7
Bit 6 MX34.6
Bit 5 MX34.5
Bit 4 MX34.4
Bit 3 MX35.7
Bit 2 MX35.6
Bit 1 MX35.5
Bit 0 MX35.4

Bit 7..4 reserved
Bit 3..0 0 to 15, music volume left and right in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX08 CD-audio volume
Ghost register

Write
Bit 7 X
Bit 6 X
Bit 5 X
Bit 4 X
Bit 3 MX36.7 & MX37.7
Bit 2 MX36.6 & MX37.6
Bit 1 MX36.5 & MX37.5
Bit 0 MX36.4 & MX37.4

Bit 3 MX36.3
Bit 3 MX37.3

Read
Bit 7 MX36.7
Bit 6 MX36.6
Bit 5 MX36.5
Bit 4 MX36.4

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Bit 3 MX37.7
Bit 2 MX37.6
Bit 1 MX37.5
Bit 0 MX37.4

Bit 7..4 reserved
Bit 3..0 0 to 15, CD-audio volume left and right in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX0A microphone volume
Ghost register

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Write
Bit 7..3 X
Bit 2 MX3A.7
Bit 1 MX3A.6
Bit 0 MX3A.5

Bit 2 MX3A.4
Bit 1 MX3A.3

Read
Bit 7..3 X
Bit 2 MX3A.7
Bit 1 MX3A.6
Bit 0 MX3A.5

Bit 7..3 reserved
Bit 2..0 0 to 7, microphone volume in 6 dB step

0 -42 dB (off)
7 0 dB (maximum volume)

MX0C digital audio input control
Default 00h
Dummy read/write register

Bit 7,6 reserved
Bit 5 input filter enable
Bit 4 reserved
Bit 3 input filter high/low
Bit 2,1 input source
Bit 0 reserved

Input filter enable and input filter high/low are dummy read/write bits for Sound Blaster Pro compatibility.

Input filter enable: 0 - input low-pass filter on, 1 - off

Input filter high/low: 0 - low filter (3.2 KHz low pass), 1 - high filter (8.8 KHz low pass)

Input source

Bit 2	Bit 1	
0	0	microphone (MX3D & MX3E = 1)
0	1	CD-audio (MX3D = 04h, MX3E = 02h)
1	0	microphone (MX3D & MX3E = 1)

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1 1 external line-in (MX3D = 10h, MX3E = 08h)

Write to input source will update MX3D and MX3E input mixer left/right control register and 2 dummy bits. Read from input source register will return 2 dummy bits.

MX0E digital audio output control
Default 00h

Bit 7,6 reserved
Bit 5 output filter enable
Bit 4..2 reserved
Bit 1 stereo switch
Bit 0 reserved

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Output filter enable is dummy read/write bit for Sound Blaster Pro compatibility.

Output filter enable: 0 - output low-pass filter on, 1 - off

Stereo switch: 1 - stereo output, 0 - mono output

Stereo switch is not used in ESP command BXh and CXh.

MX22 master left/right volume
Ghost register

Write
Bit 7 MX30.7
Bit 6 MX30.6
Bit 5 MX30.5
Bit 4 MX30.4
Bit 3 MX31.7
Bit 2 MX31.6
Bit 1 MX31.5
Bit 0 MX31.4

Bit 7 MX30.3
Bit 3 MX31.3

Read
Bit 7 MX30.7
Bit 6 MX30.6
Bit 5 MX30.5
Bit 4 MX30.4
Bit 3 MX31.7
Bit 2 MX31.6
Bit 1 MX31.5
Bit 0 MX31.4

Bit 7..4 0 to 15, master left volume in 3 dB step
Bit 3..0 0 to 15, master right volume in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX24 digital audio left/right volume
Same as MX04

MX26 music left/right volume

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Ghost register

Write
Bit 7 MX34.7
Bit 6 MX34.6
Bit 5 MX34.5
Bit 4 MX34.4
Bit 3 MX35.7
Bit 2 MX35.6
Bit 1 MX35.5
Bit 0 MX35.4

Bit 7 MX34.3
Bit 3 MX35.3

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Read
Bit 7 MX34.7
Bit 6 MX34.6
Bit 5 MX34.5
Bit 4 MX34.4
Bit 3 MX35.7
Bit 2 MX35.6
Bit 1 MX35.5
Bit 0 MX35.4

Bit 7..4 0 to 15, music left volume in 3 dB step
Bit 3..0 0 to 15, music right volume in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX28 CD-audio left/right volume
Ghost register

Write
Bit 7 MX36.7
Bit 6 MX36.6
Bit 5 MX36.5
Bit 4 MX36.4
Bit 3 MX37.7
Bit 2 MX37.6
Bit 1 MX37.5
Bit 0 MX37.4

Bit 7 MX36.3
Bit 3 MX37.3

Read
Bit 7 MX36.7
Bit 6 MX36.6
Bit 5 MX36.5
Bit 4 MX36.4
Bit 3 MX37.7
Bit 2 MX37.6
Bit 1 MX37.5
Bit 0 MX37.4

Bit 7..4 0 to 15, CD-audio left volume in 3 dB step

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Bit 3..0 0 to 15, CD-audio right volume in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

MX2E external line left/right volume
Ghost register

Write
Bit 7 MX38.7
Bit 6 MX38.6
Bit 5 MX38.5
Bit 4 MX38.4
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Bit 3 MX39.7
Bit 2 MX39.6
Bit 1 MX39.5
Bit 0 MX39.4

Bit 7 MX38.3
Bit 3 MX39.3

Read
Bit 7 MX38.7
Bit 6 MX38.6
Bit 5 MX38.5
Bit 4 MX38.4
Bit 3 MX39.7
Bit 2 MX39.6
Bit 1 MX39.5
Bit 0 MX39.4

Bit 7..4 0 to 15, external line left volume in 3 dB step
Bit 3..0 0 to 15, external line right volume in 3 dB step

0 -45 dB (off)
15 0 dB (maximum volume)

Sound Blaster 16 (Physical Register):

MX30 master left volume **(Dummy R/W)**
Default 90h

Bit 7..3 0 to 31, master left volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX31 master right volume **(Dummy R/W)**
Default 90h

Bit 7..3 0 to 31, master right volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX32 digital audio left volume **(Dummy R/W)**

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Default 90h

Bit 7..3 0 to 31, digital audio left volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX33 digital audio right volume **(Dummy R/W)**
Default 90h

Bit 7..3 0 to 31, digital audio right volume in 1.5 dB step
Bit 2..0 reserved

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0 -46 dB (off)
31 0 dB (maximum volume)

MX34 music left volume **(Dummy R/W)**
Default 90h

Bit 7..3 0 to 31, music left volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX35 music right volume **(Dummy R/W)**
Default 90h

Bit 7..3 0 to 31, music right volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX36 CD-audio left volume **(Dummy R/W)**
Default 00h

Bit 7..3 0 to 31, CD-audio left volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX37 CD-audio right volume **(Dummy R/W)**
Default 00h

Bit 7..3 0 to 31, CD-audio right volume in 1.5 dB step
Bit 2..0 reserved

0 -46 dB (off)
31 0 dB (maximum volume)

MX38 external line left volume **(Dummy R/W)**
Default 00h

Bit 7..3 0 to 31, external line left volume in 1.5 dB step
Bit 2..0 reserved

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0	-46 dB (off)
31	0 dB (maximum volume)

MX39 external line right volume **(Dummy R/W)**
Default 00h

Bit 7..3	0 to 31, external line right volume in 1.5 dB step
Bit 2..0	reserved

0	-46 dB (off)
31	0 dB (maximum volume)

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MX3A microphone volume **(Dummy R/W)**
Default 00h

Bit 7..3	0 to 31, microphone volume in 1.5 dB step
Bit 2..0	reserved

0	-46 dB (off)
31	0 dB (maximum volume)

MX3B PC speaker/mono input volume **(Dummy R/W)**
Default 00h

Bit 7,6	0 to 3, mono input volume in 6 dB step
Bit 5..0	reserved

0	-18 dB (off)
3	0 dB (maximum volume)

MX3C output mixer control 1 **(Dummy R/W)**
Default 1Fh

Bit 7..5	reserved
Bit 4	external line left enable
Bit 3	external line right enable
Bit 2	CD-audio left enable
Bit 1	CD-audio right enable
Bit 0	microphone enable

0	mute
1	enable audio output

MX3D input mixer left control **(Dummy R/W)**
Default 15h

Bit 7	reserved
Bit 6	music left enable
Bit 5	dummy read/write bit
Bit 4	external line left enable
Bit 3	dummy read/write bit
Bit 2	CD-audio left enable
Bit 1	dummy read/write bit
Bit 0	microphone enable

0	mute
1	enable audio input

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MX3E input mixer right control **(Dummy R/W)**
Default 0Bh

Bit 7 reserved
Bit 6 dummy read/write bit
Bit 5 music right enable
Bit 4 dummy read/write bit
Bit 3 external line right enable
Bit 2 dummy read/write bit
Bit 1 CD-audio right enable
Bit 0 microphone enable

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0 mute
1 enable audio input

MX3F input left mixer gain **(Dummy R/W)**
Default 00h
Read/write

Bit 7,6 input left mixer gain control
00 no gain
01 2 X
10 4 X
11 4 X
Bit 5..0 reserved

MX40 input right mixer gain **(Dummy R/W)**
Default 00h
Read/write
Bit 7,6 input right mixer gain control
00 gain = 1
01 gain = 2
10 gain = 4
11 gain = 4
Bit 5..0 reserved

MX41 output left mixer gain **(Dummy R/W)**
Default 00h
Bit 7,6 output left mixer gain
00 gain = 1
01 gain = 2
10 gain = 4
11 gain = 4
Bit 5..0 reserved

MX42 output right mixer gain **(Dummy R/W)**
Default 00h
Bit 7,6 output right mixer gain
00 gain = 1
01 gain = 2
10 gain = 4
11 gain = 4
Bit 5..0 reserved

MX43 microphone automatic gain control (AGC) **(Dummy R/W)**
Default 00h
Dummy read/write register

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Bit 7..1 reserved
Bit 0 dummy read/write bit AGC enable

MX44 treble left control **(Dummy R/W)**
Default 80h
Dummy read/write register
Bit 7..4 dummy read/write bit
Bit 3..0 reserved

MX45 treble right control **(Dummy R/W)**
Default 80h
Dummy read/write register
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Bit 7..4 dummy read/write bit
Bit 3..0 reserved

MX46 bass left control **(Dummy R/W)**
Default 80h
Dummy read/write register
Bit 7..4 dummy read/write bit
Bit 3..0 reserved

MX47 bass right control **(Dummy R/W)**
Default 80h
Dummy read/write register
Bit 7..4 dummy read/write bit
Bit 3..0 reserved

MX4C output mixer control 2 **(Dummy R/W)**
Default 1Fh

Bit 7~5 Reserved
Bit 4 music left enable
Bit 3 music right enable
Bit 2 digital audio D/A left enable
Bit 1 digital audio D/A right enable
Bit 0 mono input enable
0 mute
1 enable audio into output mixer

Sound Blaster 16 Configuration Register:

MIXER.80 Sound Blaster interrupt setup
Default 00h

Bit 7..5 reserved (read as 1)
Bit 4 IRQ11
Bit 3 IRQ10
Bit 2 IRQ7
Bit 1 IRQ5
Bit 0 IRQ9

0 : disable interrupt
1 : enable interrupt

Only 1 bit can be set at any time

Any write to PnP logical device 0 port 70h will set and reset corresponding bit in this register.
Write this register will generate SB-MIXER IRQ except in PnP configuration state.

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MIXER.81 Sound Blaster DMA setup 1
Default 00h

Bit 7..4 reserved, read as 0
Bit 3 DMA3 for SB DMA command
Bit 2 reserved, read as 0
Bit 1 DMA1 for SB DMA command
Bit 0 DMA0 for SB DMA command

0: disable DMA
1: enable DMA

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Any write to PnP logical device 0 port 74h will set one of this register bit3-0 as 1.
Write this register will generate SB-MIXER IRQ except in PnP configuration state.

MIXER.82 interrupt status
Read only
Default 00h

Bit 7~4 reserved
Bit 3 Special MPU401 interrupt request
Bit 2 MPU-401 MIDI interrupt request
Bit 1 BX type command DMA interrupt request
Bit 0 non-BX type command DMA interrupt request

0 : no interrupt
1 : interrupt triggered

Bit 0,1 always use SB IRQ line, bit 2 can share SB IRQ line only when MPU401 IRQ line is programmed to be the same as SB IRQ line by PnP manager. Normally bit 2 use MPU401 IRQ line.

MIXER.8D ALS300 backward compatible register
Default 03h **(Version F or latter Default = 07h)**
Read/write

Bit 7..3 reserved,read as 0
Bit 2 continuous DMA operation mode
0 IRQ controlled continuous DMA mode.
1 FIFO controlled continuous DMA mode.
Bit1,0 reserved(read as 1)

MX8D.2 is the ghost bit of CR0.1.

Control Register Definition:

CR0 Sound Blaster configuration
Default 00h **(Version F or latter Default = 06h)**
Read/write

Bit 7..6 reserved, read as 0
Bit 5 Reserved, read as 0
Bit 4 DMA block enable for SB DMA command
Bit 3 DMA block request size
Bit 2 DMA mode control for 90h command
Bit 1 continuous DMA mode control
Bit 0 reserved

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Bit 4:	0	single cycle DMA request
	1	block cycle DMA request
Bit 3:	0	block cycle DMA requset when PCM FIFO is not full : playback not empty: record
	1	DMA requset when PCM FIFO is less then half full during playback or less then half empty during recording
Bit 2	0	IRQ controlled 90h command (SB16 version)
	1	FIFO controlled 90h command (SBPRO version)
BIT 1	0	IRQ controled continuous DMA mode
	1	FIFO controlled continuous DMA mode

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CR2 MISC.control
Default 00h
Read/write

Bit 7	**Reserved**
Bit 6	**Reserved**
Bit 5	Reserved
Bit 4	**Read AS 1**
Bit 3	reserved, read as 0
Bit 2	**Reserved**
Bit 1	reserved, read as 0
Bit 0	**Reserved,(read as 0)**

CR3 configuration
Default 23h

Bit 7-2	read/write
Bit 1-0	read only
Bit 6	read only
Bit 7	Reserved
Bit 6	**E^2PROM control (Read only)**
Bit 5	internal/external MPU401 midi output select
Bit 4	Reserved
Bit 3	reserved
Bit 2	reserved
Bit 1,0	chip version number (**read as 11**)

Bit 1	Bit 0	
0	0	ALS007SP
0	1	ALS100
1	0	ALS007/WTA2000
1	1	ALS200/ALS110//ALS120/ALS300

Power up input value
MIDIOUT,ROMCS is tri-state with internal 50K pull low resisters when power up reset.

MIDIOUT	
0	external 10K pull down

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1 internal pull up
ROMCS
0 external 10K pull up
1 internal pull down

Power up latched value
CR3.6 !ROMCS
CR3.5 MIDIOUT

CR3.6 0 E^2PROM is disabled
1 E^2PROM is enabled (Default)
CR3.5 0 external Wave Blaster midi (Standard-MPU401)
1 internal Wave engine midi (Special-MPU401)

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CR4 (For Testing)
Same as PNP0-60
CR5 (For Testing)
Same as PNP0-61
CR6
Same as PNP0-70
CR7
Same as PNP1-60
CR8
Same as PNP0-74
CRA
Same as PNP3-30
CRB
Same as PNP1-61
CRC
Same as PNP3-60
CRD
Same as PNP3-61
CRE
Same as PNP3-70
CRF
Same as PNP2-60
CR11
Same as PNP2-61
CR17 FIFO status
Default 00h
Bit 7-3 read only
Bit 2-0 read/write

Bit 7 Reserved
Bit 6 Reserved
Bit 5 1 primary PCM FIFO underrun flag
Bit 4 1 MIDI output FIFO full flag
Bit 3 1 MIDI input FIFO overrun flag
Bit 2 1 flush MIDI in and out FIFO
Bit 1 1 flush primary PCM FIFO
Bit 0 1 active XRST_ to reset internal OPL3

Any time during DMA playback by primary FIFO, if the FIFO is empty when new sample is needed, bit 5 will be set.
Any time midi output FIFO is full, bit 4 will be set.
Any time a new midi input data is received and the midi input FIFO is full, bit 3 will be set.
Reading this register will clear all flags(ie. Bit 7-3).
Bit 2-0 are sticky, that is, hardware will not clear them automatically and it is need for software to clear the bits.

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CR18 ESP major version number
Read/write
Default 04h

CR19 ESP minor version number
Read/write
Default 02h

CR1A MPU401 MIDI UART mode control
CR1A.7-5 R/W
CR1A.4-0 R
Default 0Xh

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Bit 7	0	internal midiin from external midiin pad
	1	internal midiin from internal midiout
Bit 6	0	internal midiout to external midiout pad
	1	external midiin pad to external midiout pad
Bit 5	0	regular midi clock
	1	fast midi clock(14.318mhz)
Bit 4	X	reserved
Bit 3	0	MPU401 midi at pass-thru mode
	1	MPU401 midi at UART mode
Bit 2	X	reserved
Bit 1	X	reserved
Bit 0	X	reserved

When midi is in **pass-thru** mode, midi clock is stopped. Internal midiin is tied high and external midiout is connected to external midiin pad.

In MPU-401 UART mode, the internal midiin input, the external midiout output and the midi clock are controlled by CR1A.7-5 bits.

In midi loop back mode, when midiin FIFO is full, midi clock will be stop until midiin is not full. This will aviod midi FIFO overrun.
Special MIDI mode don't support loop-back function even MIDI is configured as loop-back mode.

CR20
Same as PNP1-30
CR21
Same as PNP2-30
CR3A MISC control register
Default 20h
Bit 7 Joystick/game-pad select
0 Joystick Mode (Analog Game-Port)
1 Game-Pad Mode (Digital Game-Port)
Bit 6~4 GD0 floating period select
000 300us

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001 400us
…
110 900us
111 1000us

Bit 3 Reserved

Bit 2 FIFO CRC check control

0 Normal

1 Clear CRC-32 shift register contents.

Bit 1 Reserved

Bit 0 0 disable SB16 E3 command
1 enable SB16 E3 command

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When CR3A.7=1(Game-Pad mode), ALS300 will drive GD0 to low. When SW write port 201h, ALS300 will release it for a period defined in CR3A.6~4 and drive it to low again until next IO write 201h. For other operation, digital Game-Port is identical to analog Game-Port.

CR3B CRC-32 Byte 0
Default : 00h
Bit 7~0 CRC-32 bit 7~0

CR3C CRC-32 Byte 1
Default : 00h
Bit 7~0 CRC-32 bit 15~8

CR3D CRC-32 Byte 2
Default : 00h
Bit 7~0 CRC-32 bit 23~16

CR3E CRC-32 Byte 3
Default : 00h
Bit 7~0 CRC-32 bit 31~24

CR3F SCRACH
8 bit read/write register
Default 00h
Bit 7..0 X dummy read/write bit for s/w switch

Plug And Play Register:
PNPy-xx Device **y** PnP index **xx** register
PNPxx Card level PnP index **xx** register
Sound Blaster Configuration

PNP0-30 Default :00h Device control

Bit	Type	Function
7:1		Reserved , read as 0
0	R/W	Device 0 control, 0 : Disable 1 : Enable

PNP0-31 Default : 00h IO check control

Bit	Type	Function
7:2		Reserved , read as 0
1	R/W	IO range check control, 0 : Disable 1 : Enable
0	R/W	IO range check return data 0 : 0xaa 1 : 0x55

PNP0-60 Default : 00h Device 0 Base address high byte

Bit	Type	Function
7:2		Reserved , read as 0
1:0	R/W	SBBASE[9..8]

PNP0-61 Default : 00h Device 0 Base address low byte

Bit	Type	Function
7:4	R/W	SBBASE[7..4]
3:0		Reserved, read as 0

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PNP0-70 Default : 00h Device 0 IRQ select

Bit	Type	Function
7:4		Reserved , read as 0
3:0	R/W	SB IRQ

PNP0-71 Default : 02h Device 0 IRQ type

Bit	Type	Function
7:0	R	Read as 02h

PNP0-74 Default : 04h Device 0 DMA select 1

Bit	Type	Function
7:3		Reserved , read as 0
2:0	R/W	SB DMA channel

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ADLIB Configuration

PNP1-30 Default : 00h Device control

Bit	Type	Function
7:1		Reserved , read as 0
0	R/W	Device 1 control, 0 : Disable 1 : Enable

PNP1-31 Default : 00h IO check control

Bit	Type	Function
7:2		Reserved , read as 0
1	R/W	IO range check control, 0 : Disable 1 : Enable
0	R/W	IO range check return data 0 : 0xaa 1 : 0x55

PNP1-60 Default : 03h Device 1 Base address high byte

Bit	Type	Function
7:3	R	Read as 0
2:0	R/W	ADLIBBASE[10..8]

PNP1-61 Default : 88h Device 1 Base address low byte

Bit	Type	Function
7:3	R/W	ADLIBBASE[7..3]
2:0		Reserved

Game Port Configuration

PNP2-30 Default : 00h Device control

Bit	Type	Function
7:1		Reserved , read as 0
0	R/W	Device 1 control, 0 : Disable 1 : Enable

PNP2-31 Default : 00h IO check control

Bit	Type	Function
7:2		Reserved , read as 0
1	R/W	IO range check control, 0 : Disable 1 : Enable
0	R/W	IO range check return data 0 : 0xaa 1 : 0x55

PNP2-60 Default : 02h Device 2 Base address high byte

Bit	Type	Function
7:3	R	Read as 0
2:0	R/W	GAMEBASE[10..8]

PNP2-61 Default : 00h Device 2 Base address low byte

Bit	Type	Function
7:3	R/W	GAMEBASE[7..3]
2:0	R	Read as 0

MPU401 Configuration

PNP3-30 Default : 00h Device control

Bit	Type	Function

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7:1		Reserved , read as 0
0	R/W	Device 1 control, 0 : Disable 1 : Enable

PNP3-31 Default : 00h IO check control

Bit	Type	Function
7:2		Reserved , read as 0
1	R/W	IO range check control, 0 : Disable 1 : Enable
0	R/W	IO range check return data 0 : 0xaa 1 : 0x55

PNP3-60 Default : 00h Device 3 Base address high byte

Bit	Type	Function
7:2		Reserved, read as 0
1:0	R/W	MPUBASE[9..8]

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PNP3-61 Default : 00h Device 3 Base address low byte

Bit	Type	Function
7:4	R/W	MPUBASE[7..4]
3:0		Reserved, read as 0

PNP3-70 Default : 00h Device 3 IRQ select

Bit	Type	Function
7:4		Reserved , read as 0
3:0	R/W	MPU401 IRQ

PNP3-71 Default : 02h Device 3 IRQ type

Bit	Type	Function
7:0	R	Read as 02h

All other plug and play registers not specified are read only as 0 except 74h,75h which should return 04h.

CRC-32 for FIFO check :

ALS300 build-in CRC-32 check circuit for speed up testing. It can help verification in development stage. To start CRC check, toggle CR3A.2 1 time. The clock of CRC-32 shift register is the clock of SB primary FIFO. When CPU read CR3B~3E,ALS300 return CRC-32 shift register content to CPU.

EXTERNAL SERIAL E^{2}PROM ACCESS:

EXTERNAL SERIAL E^{2}PROM IS ENABLED WHEN **CR3.6 = 1.**
ALS300 ONLY SUPPORTS NS9346 SERIES (OR COMPATIBLE CLONE UNIT) SERIAL E^{2}PROM WHICH HAS THE FOLLOWING PHYSICAL STORAGE ORGANIZATION:

64 X 16 (1024 BITS, 64 STORAGE CELL, EACH 16 BITS WIDE,**Little endian**)

IF THE EXTERNAL SERIAL E^{2}PROM IS ENABLED, ALS300WILL READ THE FOLLOWING DATA FROM EXTERNAL E^{2}PROM WHEN ALS120 IS RESET (H/W RESET).

PCI Subsystem Vendor ID	**BYTE 0-1**
PCI Subsystem ID	**BYTE 2-3**
PNP HEADER	**BYTE 4-12**
PNP VERSION	**BYTE 13-15**
IDENTIFIER STRING	**BYTE 16-59**
RESOURCE CHECKSUM 00	**BYTE 60 (CR3.4=0,CR3.3=0)**

THE ORIGNAL PNP HEADER,IDENTIFIER STRING AND RESOURCE CHECKSUM WILL BE UPDATED BY THE ABOVE DATA. THEIR DEFAULT VALUE ARE LISTED IN "PLUG AND PLAY HEADER/RESOURCE DATA".

ALS300 WILL NOT READ E^{2}PROM EXCEPT ALS300 IS RESET AGAIN.

After reading PCI subsystem Vendor ID/subsystem ID (byte 0~3), ALS300 "SB logic" send these data to ALS300 "PCI interface".

Test Mode Access:

Access GCR90 will enter the test mode you set.

Power Management:

Try the best power management for both active and inactive stage of ALS300 for notebook application.

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Pay special attention to data bus and address bus inside ALS300 because this may be the very heavy power consumption source.

Use internal block chip select signal to be the block power control signal as much as possible.

The pull up resistors on any power up configuration pin must be disconnected from VCC after reset.

H/W power-down pin is disabled.

S/w power down mode is the same as h/w power down mode except RST and I/O access to power down register are still enable.

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The I/O access of the following register does not need power management control and must have real time response.

POWER DOWN REGISTER

FIFO Control Attention:

Whenever new continuous DMA command for 8/16 bit wave playback is received, SB16 ESP should always flush primary PCM FIFO.

ALS300 should has a primary FIFO r/w counter reset indicator, ISA reset or ESP RESET should reset this indicator. When current DMA operation is 8 bit stereo or 16 bit mono, if DMA transfer times is not even, this indicator should indicate bit 0 of FIFO r/w counter must be reset by ESP when new DMA command is received. When current DMA operation is 16 bit stereo, if DMA transfer times is not multiple times of 4, this indicator should indicate that bit 0 and bit 1 of FIFO r/w counter must be reset by ESP when new DMA command is received.

Any time when new DMA command is received, this indicator must be reset after primary FIFO r/w counter control.

MIDIOUT FIFO Size : 16 bytes
MIDIIN FIFO Size : 8 bytes
MIDIOUT RAM Size : 128 bytes

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Appendix A : ALS300 PnP Resource Data

ALS300 Plug And Play Definition:

Plug and play function block can be enabled by either the standard ISA plug and play initial key sequence or our self-defined initial key sequence. Please refer to the ISA plug and play spec 1.0 to get the standard initial key sequence. Our self-defined initial key sequence is as follows:

95,CA,E5,F2, F9,FC,7E,BF,
5F,2F, 17,0B, 05, 82,C1,E0,
70, 38,1C,0E, 87, 43, 21,90,
48, 24,12 ,89, C4, 62, B1,D8

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Plug And Play Header/Resource Data:

200 byte ROM

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; PLUG AND PLAY HEADER        ; 9 bytes RAM
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
DB    0X05,0X93               ; VENDOR ID "ALS"
DB    0X03,0X00               ; CHIP ID "300"
DB    0XFF,0XFF,0XFF,0XFF     ; SERIAL NUMBER FFFFFFFF
DB    0X99                    ; LFSR CHECKSUM

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
; PLUG AND PLAY RESOURCE DATA
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

DB    0X0A                    ; PLUG AND PLAY VERSION NUMBER
DB    0X10                    ; VERSION 1.0
DB    0X00                    ; ALS300 VERSION 0.0

DB    0X82                    ; ANSI IDENTIFIER STRING
DB    0X29,0X00               ; STRING LENGTH
DB    0X50,0X6E,0X50,0X20
DB    0X53,0X6F,0X75,0X6E
DB    0X64,0X20,0X43,0X68
DB    0X69,0X70,0X20,0X20
DB    0X20,0X20,0X20,0X20
DB    0X20,0X20,0X20,0X20
DB    0X20,0X20,0X20,0X20
DB    0X20,0X20,0X20,0X20
DB    0X20,0X20,0X20,0X20
DB    0X20,0X20,0X20,0X20,0x20        ;"PnP Sound Chip                    "
;
; LOGICAL DEVICE 0
; SOUND BLASTER RESOURCE
;
DB    0X15                    ; LOGICAL DEVICE ID
DB    0X00,0X00               ; DEVICE ID 0-SOUND BLASTER BASE
DB    0X00,0X03               ; ALS300
DB    0X02                    ; SUPPORT I/O RANGE CHECK
;
DB    0X31,0X00               ; BEST CASE DEFAULT
DB    0X47,0X01               ; I/O PORT SELECT, 16 BIT I/O ADDRESS DECODE
DB    0X20,0X02               ; MIN. I/O BASE 0X0220
```


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```
DB      0X20,0X02               ; MAX. I/O BASE 0X0220
DB      0X10                    ; I/O ALIGN EVERY 16 BYTE
DB      0X10                    ; I/O LENGTH 16 BYTE
DB      0X22                    ; IRQ FORMAT, HIGH EDGE TRIGGERED
DB      0X20,0X00               ; IRQ 5
DB      0X2A                    ; DMA FORMAT 0
DB      0X02                    ; DMA CHANNEL 1
DB      0X68                    ; 8 BIT DMA TYPE F, BYTE COUNT

DB      0X31,0X01               ; AVERAGE CASE
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X20,0X02               ; MIN. I/O BASE 0X0220
DB      0X80,0X02               ; MAX. I/O BASE 0X0280
DB      0X20                    ; I/O ALIGN EVERY 32 BYTE
DB      0X10                    ; I/O LENGTH 16 BYTE
DB      0X22                    ; IRQ FORMAT, HIGH EDGE TRIGGERED
DB      0XA0                    ; IRQ 5,7
DB      0X0E                    ; IRQ 9,10,11
DB      0X2A                    ; DMA FORMAT 0
DB      0X0B                    ; DMA CHANNEL 0,1 OR 3
DB      0X68                    ; 8 BIT DMA TYPE F, BYTE COUNT

DB      0X31,0X02               ; WORST CASE
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X00,0X01               ; MIN. I/O BASE 0X0100
DB      0XF0,0X03               ; MAX. I/O BASE 0X03F0
DB      0X10                    ; I/O ALIGN EVERY 16 BYTE
DB      0X10                    ; I/O LENGTH 16 BYTE
DB      0X22                    ; IRQ FORMAT,HIGH EDGE TRIGGERED
DB      0XA0                    ; IRQ 5,7
DB      0X0E                    ; IRQ 9,10,11
DB      0X2A                    ; DMA FORMAT 0
DB      0X0B                    ; DMA CHANNEL 0,1 OR 3
DB      0X68                    ; 8 BIT DMA TYPE F, BYTE COUNT
DB      0X38                    ; END OF CASES
;
; LOGICAL DEVICE 1
; ADLIB RESOURCE
;
DB      0X15                    ; LOGICAL DEVICE ID
DB      0X01,0X00               ; DEVICE ID 1-ADLIB
DB      0X00,0X03               ; ALS300
DB      0X02                    ; SUPPORT I/O  RANGE CHECK
;
; WHEN I/O RANGE CHECK ENABLE, ALS300 WILL NOT ENABLE ANY
;  KIND OF  INTERNAL OR EXTERNAL FM CHIP SELECT SIGNAL .
; ALS300 WILL DRIVE SD0-7 AS 0X55 OR 0XAA AS DEFINED BY THE SPEC.
;
DB      0X31,0X00               ; BEST CASE
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X88,0X03               ; MIN. I/O BASE 0X0388
DB      0X88,0X03               ; MAX. I/O BASE 0X0388
DB      0X08                    ; I/O ALIGN EVERY 8 BYTE
DB      0X04                    ; I/O LENGTH 4 BYTE
;
DB      0X31,0X01               ; WORST CASE (1997,5,13)
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X00,0X03               ; MIN. I/O BASE 0X0300 (1997,5,13)
```


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```
DB      0XFF,0X07               ; MAX. I/O BASE 0X07FF (1997,5,13)
DB      0X08                    ; I/O ALIGN EVERY 8 BYTE (1997,6,12)
DB      0X04                    ; I/O LENGTH 4 BYTE (1997,5,13)
;
DB      0X38                    ; END CASE (1997,5,13)
;
; LOGICAL DEVICE 2
; GAME PORT
;
DB      0X15                    ; LOGICAL DEVICE ID
DB      0X02,0X00               ; DEVICE ID 2-GAME PORT
DB      0X00,0X03               ; ALS300
DB      0X02                    ; SUPPORT I/O RANGE CHECK
;
; WHEN I/O RANGE CHECK ENABLE, ALS300 WILL NOT ENABLE NORMAL
; OR ENHANCED MODE  GAMEPORT READ  AND WRITE.
; ALS300 WILL DRIVE SD0-7 AS 0X55 OR 0XAA AS DEFINED BY THE SPEC.
;
DB      0X31,0X00               ; BEST CASE
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X00,0X02               ; MIN. I/O BASE 0X0200
DB      0X00,0X02               ; MAX. I/O BASE 0X0200
DB      0X08                    ; I/O ALIGN EVERY 8 BYTE
DB      0X08                    ; I/O LENGTH 8 BYTE
;
DB      0X31,0X01               ; WORST CASE (1997,5,13)
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X00,0X02               ; MIN. I/O BASE 0X0200
DB      0XFF,0X07               ; MAX. I/O BASE 0X07FF
DB      0X08                    ; I/O ALIGN EVERY 8 BYTE
DB      0X08                    ; I/O LENGTH 8 BYTE
;
DB      0X38                    ; END CASE (1997,5,13)
;
; LOGICAL DEVICE 3
; MPU401 MIDI RESOURCE
;
DB      0X15                    ; LOGICAL DEVICE ID
DB      0X03,0X00               ; DEVICE ID 3-MPU401 MIDI
DB      0X00,0X03               ; ALS300
DB      0X02                    ; SUPPORT I/O RANGE CHECK
;
DB      0X31,0X00               ; BEST CASE DEFAULT
DB      0X47,0X01               ; I/O PORT SELECT, 16 BIT I/O ADDRESS DECODE
DB      0X30,0X03               ; MIN. I/O BASE 0X0330
DB      0X30,0X03               ; MAX. I/O BASE 0X0330
DB      0X10                    ; I/O ALIGN EVERY 16 BYTE
DB      0X04                    ; I/O LENGTH 4 BYTE
DB      0X22                    ; IRQ FORMAT, HIGH EDGE TRIGGERED
DB      0X00,0X02               ; IRQ 9
;
DB      0X31,0X01               ; AVERAGE CASE
DB      0X47,0X01               ; I/O PORT SELECT,16 BIT I/O ADDRESS DECODE
DB      0X00,0X01               ; MIN. I/O BASE 0X0100
DB      0XF0,0X03               ; MAX. I/O BASE 0X03F0
DB      0X10                    ; I/O ALIGN EVERY 16 BYTE
DB      0X04                    ; I/O LENGTH 4 BYTE
DB      0X22                    ; IRQ FORMAT, HIGH EDGE TRIGGERED
```


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```
DB      0XA0                    ; IRQ 5, 7
DB      0X0E                    ; IRQ 9, 10, 11
;
DB      0X38                    ; END OF CASES
;
;END OF RESOURCE DATA

DB      0X79            ; END TAG
;**************************
;       CHECKSUM
;**********************
DB      1D                      ; CHECK SUM
```

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Appendix B : ESP command set

ALS300 only support playback and it's related command.

* Undocumented
$ Sound Blaster Pro only
# Sound Blaster 16 only

0Xh	reserved
1Xh	set audio output mode for 4:1 ADPCM 2 to 8 bit playback
3Xh	reserved
4Xh	set sample rate and continuos/special DMA block length
5Xh	reserved
6Xh	reserved
7Xh	set audio output for all ADPCM, 8 bit playback
8Xh	output silence
9Xh	8 bit special DMA mode playback/record
AXh	set MONO/Stereo input mode
BXh	16 bit DMA audio I/O
CXh	8 bit DMA audio I/O
DXh	control DMA and speaker
EXh	ESP version and diagnostic test
FXh	test IRQ and ESP ROM

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All 8-bit ESP command is unsigned PCM except CXh command.

All 8-bit ESP command is MONO except command 14h,1Ch,9Xh and CXh

8 Bit And 4:1 ADPCM 2 To 8 Bit Output
1Xh

Bit 3	0	direct/normal DMA mode
	1	continuous DMA mode
Bit 2	0	direct mode
	1	DMA mode
Bit 1	0	8 bit data
	1	4:1 ADPCM 2 to 8 bit mode
Bit 0	0	normal
	1	the first ADPCM block with reference byte

10h 8 bit direct mode output

a. ESP_WRITE(10h)
b. ESP_WRITE(single-sample)
c. Wait for next sample time, go to a.

14h 8 bit normal DMA output

a. ESP_WRITE(14h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(lenght.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

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16h 4:1 ADPCM 2 to 8 bit normal DMA output

a. ESP_WRITE(16h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

17h first 4:1 ADPCM 2 to 8 bit normal DMA output

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a. ESP_WRITE(17h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

1Ch 8 bit continuous DMA output

ESP_WRITE(1Ch)

ESP will generate an interrupt for every specified block size transferred.

1Eh 4:1 ADPCM 2 to 8 bit continuous DMA output

ESP_WRITE(1Eh)

ESP will generate an interrupt for every specified block size transferred.

1Fh first 4:1 ADPCM 2 to 8 bit continuous DMA output

ESP_WRITE(1Fh)

ESP will generate an interrupt for every specified block size transferred.

Set Sample Rate And Continuous/Special DMA Block Length
4Xh

40h set sample rate time constant

Time constant = 256d - (1,000,000d / (channel * sampling rate))

Channel = 1 for mono or BX,CX type command, 2 for stereo

a. ESP_WRITE(40h)
b. ESP_WRITE(time constant)

#41h set playback sample rate

a. ESP_WRITE(41h)
b. ESP_WRITE(frequency.high)
c. ESP_WRITE(frequency.low)

Sampling frequency = 4 KHz TO 48 KHz, either mono or stereo

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48h set block length for continuous and special DMA

a. EPS_WRITE(48h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after transferred the block of data.

After reset, the default block size is 2048. Length = 07FFh

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All ADPCM 8 Bit Output
7Xh

Bit 3	0	normal DMA mode
	1	continuous DMA mode

Bit 2	Bit 1	
0	0	reserved
0	1	4:1 ADPCM 2 to 8 bit mode
1	0	2:1 ADPCM 4 to 8 bit mode
1	1	3:1 ADPCM 2.6 to 8 bit mode

Bit 0	0	normal
	1	the first ADPCM block with reference byte

*72h 4:1 ADPCM 2 to 8 bit normal DMA output

a. ESP_WRITE(72h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

*73h first 4:1 ADPCM 2 to 8 bit normal DMA output

a. ESP_WRITE(73h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

74h 2:1 ADPCM 4 to 8 bit normal DMA output

a. ESP_WRITE(74h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

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75h first 2:1 ADPCM 4 to 8 bit normal DMA output

a. ESP_WRITE(75h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

76h 3:1 ADPCM 2.6 to 8 bit normal DMA output

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a. ESP_WRITE(76h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

77h first 3:1 ADPCM 2.6 to 8 bit normal DMA output

a. ESP_WRITE(77h)
b. ESP_WRITE(length.low)
c. ESP_WRITE(length.high)

Length = # of byte transfer - 1

ESP will generate an interrupt after the specified size of data transferred.

*7Ah 4:1 ADPCM 2 to 8 bit continuous DMA output

ESP_WRITE(7Ah)

ESP will generate an interrupt for every specified block size transferred.

*7Bh first 4:1 ADPCM 2 to 8 bit continuous DMA output

ESP_WRITE(7Bh)

ESP will generate an interrupt for every specified block size transferred.

7Ch 2:1 ADPCM 4 to 8 bit continuous DMA output

ESP_WRITE(7Ch)

ESP will generate an interrupt for every specified block size transferred.

7Dh first 2:1 ADPCM 4 to 8 bit continuous DMA output

ESP_WRITE(7Dh)

ESP will generate an interrupt for every specified block size transferred.

7Eh 3:1 ADPCM 2.6 to 8 bit continuous DMA output

ESP_WRITE(7Eh)

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ESP will generate an interrupt for every specified block size transferred.

7Fh first 3:1 ADPCM 2.6 to 8 bit continuous DMA output

ESP_WRITE(7Fh)

ESP will generate an interrupt for every specified block size transferred.

Output Silence
8Xh

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Bit 3..0 X reserved

80h silence audio for a duration

a. ESP_WRITE(80h)
b. ESP_WRITE(duration.low)
c. ESP_WRITE(duration.high)

Duration = # of silence sample period - 1

After the specified duration elapses, ESP will generate an interrupt. During silence period, ESP out 0x80 to PCM D/A.

8 Bit Special DMA Playback/Record
9Xh

All special DMA mode use command 48h to set the transfer block size. The non-continuous special DMA mode will interrupt the CPU at the end of the transfer block and wait for new command. Use RESET-ESP() to end the continuous special DMA, all other parameters remains the same after RESET-ESP( ).

Special DMA playback:
MONO MX0E.1 = 0
Stereo MX0E.1 = 1

Default MONO after ISA reset or mixer reset

Default MONO after ISA reset or ESP reset

Bit 3 1 audio input
Bit 3 0 audio output
Bit 2 X reserved
Bit 1 X reserved
Bit 0 0 continuous DMA
Bit 0 1 non-continuous DMA

$90h 8 bit continuous special DMA output

ESP_WRITE(90h)

ESP will generate an interrupt for every specified block size transferred.

ALS300 use CR0.2 to control the DMA running mode of 90h command. When CR0.2 is 1, ESP will continue DMA transfer no matter whether the interrupt is acknowledged, this is SBPRO 90

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command. When CR0.2 is 0, ESP will continue DMA transfer after the interrupt is acknowledged, this is SB16 90h command.

$91h 8 bit non-continuous special DMA output

ESP_WRITE(91h)

ESP will generate an interrupt after the specified size of data transferred.

For non-continuous special DMA output, every time when ESP receives the 91h command, ESP will use the block length that most recently set by command 48h to begin the special DMA transfer. So if every block of DMA data is the same size, software needs only set block length one time by using command 48h. When each block is transfered over, software needs only send 91h command to ESP, the DMA transfer will then continue with previous block length.

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16 Bit DMA Audio I/O
#BXh

Bit 3	0	audio output (Bit 3 should be "0" in ALS300)
	1	audio input
Bit 2	0	non-continuous DMA
	1	continuous DMA
Bit 1	X	reserved
Bit 0	X	reserved

FIFO will reset when ESP receives any digital audio I/O command.
FIFO is always on.

a. ESP_WRITE(BXh)
b. ESP_WRITE(mode)
c. ESP_WRITE(length.low)
d. ESP_WRITE(length.high)

Mode		
Bit 7	X	reserved
Bit 6	X	reserved
Bit 5	0	MONO
	1	stereo
Bit 4	0	unsigned (0--8000h--FFFFh)
	1	signed (8000h--0--7FFFh)
Bit 3	X	reserved
Bit 2	X	reserved
Bit 1	X	reserved
Bit 0	X	reserved

Length = # of 16 bit sample -1

ESP will generate an interrupt after the specified size of data transferred (if non-continuous) or every block(if continuous).

8 Bit DMA Audio I/O
#CXh

Bit 3	0	audio output (Bit 3 should be "0" in ALS300)
	1	audio input
Bit 2	0	non-continuous DMA
	1	continuous DMA
Bit 1	X	reserved

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Bit 0 X reserved

FIFO will reset when ESP receives any digital audio I/O command.
FIFO is always on.

a. ESP_WRITE(CXh)
b. ESP_WRITE(mode)
c. ESP_WRITE(length.low)
d. ESP_WRITE(length.high)

Mode

Bit 7	X	reserved
Bit 6	X	reserved
Bit 5	0	MONO
	1	stereo
Bit 4	0	unsigned (0--80h--FFh)
	1	signed (80h--0--7Fh)
Bit 3	X	reserved
Bit 2	X	reserved
Bit 1	X	reserved
Bit 0	X	reserved

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Length = # of 8 bit sample -1

ESP will generate an interrupt after the specified size of data transferred (if non-continuous) or every block(if continuous).

Control DMA And Digital Audio
DXh

D0h pause non BX type DMA transfer

ESP_WRITE(D0h)

The DMA request is stopped after this command. Internal FIFO will continue until the FIFO is empty (playback) or full (record). The DMA request will resume after command D4h or any of new DMA command is issued.

D1h turn digital audio on

ESP_WRITE(D1h)

Set digital audio status flag for D8h command.

D3h turn digital audio off

ESP_WRITE(D3h)

Reset digital audio status flag for D8h command.
Audio status flag is reset after system reset or ESP_RESET().

D4h resume non BX type DMA transfer

ESP_WRITE(D4h)

The DMA request that is suspended by the command D0h is enable again. The internal FIFO is working as usual in pause or resume DMA mode.

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#D5h pause BX type DMA mode transfer

ESP_WRITE(D5h)

The DMA request is stopped after this command. Internal FIFO will continue until the FIFO is empty (playback) or full (record). The DMA request will resume after command D6h or any of new DMA command is issued

#D6h resume BX type DMA mode transfer

ESP_WRITE(D6h)

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The DMA request that is suspended by the command D5h is enable again. The internal FIFO is working as usual in pause or resume DMA mode. This command is no use to non-BX type command DMA transfer.

D8h get digital audio status

a. ESP_WRITE(D8h)
b. ESP_READ(status)
c. Status = 00h (digital audio off) or FFh (digital audio on)

#D9h exit current BX type continuous DMA transfer

ESP_WRITE(D9h)

Causes the ESP to finish the current block, then cease transferring. Use this command while the DMA is transferring the last block of audio data from/to ESP. ESP-RESET() or any of new DMA command should reset this flag.

DAh exit current non-BX type continuous DMA transfer

ESP_WRITE(DAh)

Causes the ESP to finish the current block, then cease transferring. Use this command while the DMA is transferring the last block of audio data from/to ESP. ESP-RESET() or any of new DMA command should reset this flag.

ESP Version And Diagnostic
EXh

*E0h read/write diagnostic test

a. ESP_WRITE(E0h)
b. ESP_WRITE(test-data)
c. ESP_READ(result)
d. If result = bit invert of test-data, ESP is working

E1h get ESP version number

a. ESP_WRITE(E1h)
b. ESP_READ(major.version)
c. ESP_READ(minor.version)

Sound Blaster Pro default version	3.02
Sound Blaster 16 default version	4.02

ALS300 default 4.02

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Major version = CR18
Minor version = CR19

*E2 DMA testing

Computes The Subroutine's Starting Address for Digital Sound
Playback or Recording According to The Dedicated Algorithm.
Sends Back The Result To System via DMA Method(Two Bytes Transfered).

a. ESP_WRITE(E2h)
b. ESP_WRITE(first byte b1),return r1 via DMA
c. ESP_WRITE(E2h)
d. ESP_WRITE(second byte b2),return r2 via DMA

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Formula for r1:
r1 = (b1.7..5 + 1) * 0x40 + b1.3 * 0x10 + b1.0 * 0x02 - b1 (this is 8 bit unsigned operation)
Formula for r2:
1. r2_h = 0xe0 + b2.4 * 0x20 - b2.6 * 0x80
2. r2_h = r2_h + b1 & 0xe0 - b2 & 0xf0
3. r2_l = 0x05 + b2.1 * 0x04 - b2 & 0x0f
4. r2 = r2_h & 0xf0 + r2_l & 0x0f + b1.0 * 0x01 - b1 & 0x1e
5. r2 = r2 + b1.3 * 0x10
(this is 8 bit unsigned operation)

*E3 copyright message

a. ESP_WRITE(E3h)
b. ESP_READ(message)

Message :
TEXT "COPYRIGHT (C) CREATIVE TECHNOLOGY LTD, 1992.",0h)
HEX 43 4F 50 59 52 49 47 48 54 20 28 43 29 20
43 52 45 41 54 49 56 45 20 54 45 43 48 4E 4F 4C 4F 47 59 20
4C 54 44 2C 20 31 39 39 32 2E 00
This command is valid only when CR3A.0 = 1.

*E4 send test byte for command E8h

a. ESP_WRITE(E4h)
b. ESP_WRITE(test-data)

*E8 read diagnostic byte

a. ESP_WRITE(E4h)
b. ESP_WRITE(test-data)
c. ESP_WRITE (E8h)
c. ESP_READ(result)
d. If result = test-data, ESP is working

Testing
FXh

*F2h generate an interrupt for test

ESP_WRITE(F2h)

ESP will generate an interrupt immediately after this command.

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*F8 read back dedicated byte 00
a. ESP_WRITE(F8h)
b. ESP_READ(result)
c. If result = 00,ESP is working

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Appendix C : PCM Data Format

Digitized Sound Data Format And Order:

Length	Format	Min value	Mid value	Max value
8 Bit	Unsigned	00h	80h	FFh
8 Bit	Signed	80h	00h	7Fh
16 Bit	Unsigned	0000h	8000h	FFFFh
16 Bit	Signed	8000h	0000h	7FFFh

PCM Sample Order:

- **8 Bit Mono**

Byte No.	N	N+1	N+2	N+3	N+4
Sample	PCM 0	PCM 1	PCM 2	PCM 3	PCM 4

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- **8 Bit Stereo With 1Xh And 9Xh Type Command**

Byte No.	2N	2N+1	2N+2	2N+3	2N+4
Sample	PCM0.R	PCM0.L	PCM1.R	PCM1.L	PCM2.R

- **8 Bit Stereo With Cxh Type Command**

Byte No.	2N	2N+1	2N+2	2N+3	2N+4
Sample	PCM0.L	PCM0.R	PCM1.L	PCM1.R	PCM2.L

- **16 Bit Mono**

Byte No.	2N	2N+1	2N+2	2N+3	2N+4
Sample	PCM0.LOW	PCM0.HIGH	PCM1.LOW	PCM1.HIGH	PCM2.LOW

- 16 Bit Stereo

Byte No.	4N	4N+1	4N+2	4N+3	4N+4
Sample	PCM0.L.Low	PCM0.L.High	PCM0.R.Low	PCM0.R.High	PCM1.L.Low

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Appendix D : ESP/MPU401 Programming Guide

ESP Procedure:

ESP Read Data Procedure:

ESP_READ(return_byte)

1. If I/O read(ESP-RD-STATUS) bit 7 = 1 goto 2 else 1
2. Return_byte = I/O read(ESP-READ-DATA)

ESP Write Procedure:

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ESP_WRITE(command/data)

1. If I/O read(ESP-WR-STATUS) bit7 = 0 goto 2 else 1
2. I/O write(ESP-COMMAND/DATA, command/data)

ESP Reset Procedure:

ESP_RESET( )

1. I/O write(ESP-RESET-PORT, 1), and wait 3 us
2. I/O write(ESP-RESET-PORT, 0)
3. ESP_READ(status), if status = AAh goto 4 else 3
4. End of reset

You can use ESP_RESET() procedure to immediately terminate the special DMA transfer.

Digitized Sound Transfer Method:

1. Direct Mode

ESP is programmed to do audio input/output on each command. All delay time is controlled by CPU delay loop or timer interrupt. Only 8 bit mono input/output is supported.

Output:

a. ESP_WRITE(10h)
b. ESP_WRITE(next 8 bit mono PCM)
c. Wait until next sample time, goto a.

2. DMA Mode

2.1 Normal DMA Mode

ESP is programmed to make one transfer with a specified block size. At the end of transfer, the ESP will generate an interrupt and wait for next command.

2.2 Continuous DMA Mode

ESP is programmed to make continuous transfer to/from CODEC. After each transfer of a specified block size, ESP will generate an interrupt and continue the next transfer of the same block size after the interrupt is acknlwoedged.

There are two ways to terminate continuous DMA mode transfer.

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1.Program ESP to switch to normal DMA mode transfer. At the end of the current DMA transfer, ESP will exit from continuous DMA mode and continue to transfer using the specified normal DMA mode.
2.Send the exit continuous command. The ESP will exit continuous DMA mode at the end of current block and terminate the transfer.

2.3 Special DMA Mode

Once ESP is in the special DMA mode, it will not accept any further commands or data until the DMA mode is terminated by
Either

1. Non-continuous special DMA mode will exit special DMA mode automatically at the end of transfer.

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Or

2. For continuous special DMA mode, a ESP_RESET() is needed to exit special DMA mode.

The ESP_RESET() will only stop special DMA transfer, all other parameters remain the same.

I/O Transfer Rate Setup:

Either
1. Sound Blaster Pro (time constant)
Time constant = 256d - (1,000,000d / (channel * sampling rate))
Channel = 1 for mono or BX,CX type DMA command, 2 for stereo
a. ESP_WRITE(40h)
b. ESP_WRITE(time constant)
Or
2. Sound Blaster 16 (sampling frequency)
Output:
a. ESP_WRITE(41h)
b. ESP_WRITE(frequency.high)
c. ESP_WRITE(frequency.low)
Sampling frequency = 4 KHz to 48 KHz, either mono or stereo

MPU-401 MIDI Programming:

1. MPU-401 pass-thru mode
After reset, midi is in **pass-thru** mode. MIDIIN data is directly connected to MIDIOUT data.
Any write to **midi-data** will be ignored. MIDI-COMMAND will support either MIDI_RESET (0FFh) or ENTER_UART (03Fh).
Both command will return with interrupt and acknowledge byte (0FEh).

2. MPU-401 UART mode
After enter UART mode, all write to **midi-data** will go to MIDIOUT FIFO, any MIDIIN data will go to MIDIIN FIFO. **(In Special MIDI mode, any write to MIDI-DATA will go to MIDIOUT RAM)**
MIDI-STATUS bit 7 = MIDIIN FIFO empty.
MIDI-STATUS bit 6 = MIDIOUT FIFO full + MIDIOUT FIFO not empty when MIDI_RESET
MIDI-STATUS bit 5 = MIDIOUT RAM full
MIDI INTERRUPT =(MIDIIN FIFO not empty & not I/O read(MIDI-DATA))
or (MIDIOUT RAM is not empty in special MPU401 mode)

To end the UART mode, send MIDI_RESET (0FFh) to **midi-command** port. MIDIIN FIFO will be flushed, any data in MIDIOUT FIFO/MIDIOUT RAM will be output. When both FIFO are empty, MPU-401 will enter **pass-thru** mode .

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Part II : Specification for PCI I/F and Wave Engine

DRAM configuration :

11 X 11 : 4M X 4 (DTYPE[1,0]=10)

CASA#/CAS0# : A_{21},A_9~ A_0 **CASB#/CAS1#** : Inactive

RASA#/RAS# : A_{20},A_{19}~ A_0

12 X 10 : 4M X 4 (DTYPE[1,0]=11)

CASA#/CAS0# : A_9~ A_0 **CASB#/CAS1#** : Inactive

RASA#/RAS# : A_{21}~ A_{10}

10 X 10 : One 1M X 4 (DTYPE[1,0]=00)

CASA#/CAS0# : A_9~ A_0 (A_{20}=0)

CASB#/CAS1# : A_9~ A_0 (A_{20}=1)

RASA#/RAS# : A_{19}~ A_{10}

10 X 10 : Two 1M X 4 (DTYPE[1,0]=01)

CASA#/CAS0# : A_9~ A_0 (A_{20}=0)

CASB#/CAS1# : A_9~ A_0 (A_{20}=1)

RASA#/RAS# : A_{19}~ A_{10}

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DRAM Access mode :

Mode 1 : DRAM is controlled by PCI DRAM controller.
Access : Memory Read/Write.

Mode 2 : DRAM is controlled by Wave engine.
Access : Program GCR8B to start bus master function. It support write function only.

Arbitration between PCI D/A and SB D/A :

PCI/SB# (Re-sample source select,GCR8C.28)

0 Select SB D/A (Default)

1 Select PCI D/A

PCI/SB#	PCI/SB# Toggle condition
1	SBVLID low go high edge
0	PCIVLID=1

Arbitration between OPL3 D/A and Wave Engine D/A :

WVE/FM# (Re-sample source select,GCR8C.1)

0 Select OPL3 D/A (Default)

1 Select Wave Engine D/A

WVE/FM#	WVE/FM# Toggle condition
1	FMREQ low go high edge
0	(RAMW# low go high edge) | (FMPWED#=0)

FIFO/Latch arrangement :

- **AC97 serial output buffer :**

Name	Size	Slot No.	Description
INDX	8 X 1	1	AC97 CMD/Address **latch**
DOUT	16 X 1	2	AC97 ouput data **latch**
PCILO	16 X 8	3	PCI playback left channel **FIFO**
PCIRO	16 X 8	4	PCI playback right channel **FIFO**
MOUT	16 X 1	5	Modem-Out **latch**
INDX connect to high byte of 16-bit bus			

- **AC97 serial input buffer :**

Name	Size	Slot No.	Description
DIN	16 X 1	2	AC97 input data **latch**
PCILI	16 X 8	3	PCI record left channel **FIFO**

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PCIRI	16 X 8	4	PCI record right channel **FIFO**
MIN	16 X 1	5	Modem-In **latch**
MICIN	16 X 8	6	Mic-In **FIFO**

- **DRAM-Write FIFO for mode 2: (Enabled on DRAM access mode 2)**

Name	Size	Description
DRAMO	32 X 2	DRAM write **FIFO**

FIFO Management :

Underrun FIFO should do the following things :

1.Send the current data to AC97 I/F when AC97 I/F read FIFO.

2.Keep read pointer until new data arrived and set corresponding flag.

Paused output FIFO should do the following things :

1.Take the same action as normal condition until FIFO is empty.

2.When FIFO is empty, keep read pointer until pause command stop. Don‘t set any flag.

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Overrun FIFO should do the following things :

1.Disable FIFO update by AC97 I/F until data is fetched.

2.Keep write pointer until data is fetched and set corresponding flag.

When transfer stop (GCR85.16/GCR88.16=0), ALS300 will discard arriving data.

Paused input FIFO should do the following things :

1.Take the same action as normal condition until FIFO is full.

2.When FIFO is full, keep write pointer until pause command stop. Don‘t set any flag.

ALS300 flush FIFO once when starting recording.

ALS300 implement sampling rate transformation and data type transformation for playback only. For recording, it is implemented by software. Because ALS300 implement DMA operation by PCI bus master, playback or record by PCI command has no compatibility issue and ALS300 support address increment transfer only.

All PCI playback/record command is continuous except DRAM-Write transfer and non-autoinitialization transfer.

non-continuous playback.

Modem I/O management :

There are 3 states for Modem I/O : **OFF, STANDBY and TRANSMISSION.**

OFF Ignore all Modem I/O and Ring signal.

STANDTBY Waiting for Ring signal.

TRANSMISSION Transmit/Receive data to/from remote Modem.

State\Definition	**GCR8C.12**	**GCR8C.11**
OFF	0	0
STANDBY	0	1
TRANSMISSION	1	0

When a Ring-In have detected, RD# will be driven low and ALS300 will generate an IRQ for service. Modem driver will do the following thing to answer the call from remote Modem when Ring-In IRQ is served.

1. Disable Ring-In IRQ (Clear GCR8C.11)

2.Enable HOOK output capability and set proper value on HOOK.

3.Enable Modem-In IRQ.

In TRANSMISSION state, ALS300 will generate an IRQ and set corresponding bit of IRQ-STATUS if receiving data from AC97 serial input. For output , driver handle write operation completely.

When transmission is complete, driver will do the following things:

1.Disable Modem-In IRQ

2.Set HOOK to inactive state.

3.Enable Ring-In IRQ.

Relation of AC-Link and Internal 16-bit data bus : (implemented in “PCI”)

AC Link Bit 19 ↔ Internal data bus bit 15

AC Link Bit 18 ↔ Internal data bus bit 14

: :

AC Link Bit 4 ↔ Internal data bus bit 0

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AC Link Bit 3 ↔ (Output : stuffed with 0 , Input : discarded)
: :
AC Link Bit 0 ↔ (Output : stuffed with 0 , Input : discarded)

PCM Sample Order:

- **8 Bit Mono**

Byte No.	3	2	1	0
Sample	PCM 3	PCM 2	PCM 1	PCM 0

- **8 Bit Stereo**

Byte No.	3	2	1	0
Sample	PCM1.R	PCM1.L	PCM0.R	PCM0.L

- **16 Bit Mono**

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Byte No.	3	2	1	0
Sample	PCM1.HIGH	PCM1.LOW	PCM0.HIGH	PCM0.LOW

- **16 Bit Stereo**

Byte No.	3	2	1	0
Sample	PCM0.R.High	PCM0.R.Low	PCM0.L.High	PCM0.L.Low

Transformation between different PCM data type :

The PCM data type for AC97 is **16-bit signed** PCM data. The transformations are described below :

Unsigned → Signed 16-bit(8-bit)

Unsigned value	Signed value
FFFFh(FFh)	7FFFh(7Fh)
:	:
8001h(81h)	0001h(01h)
8000h(80h)	0000h(00h)
7FFFh(7Fh)	FFFFh(FFh)
:	:
0000h(00h)	8000(80h)

Mono → Stereo

Duplicated Left channel to Right channel.

8-bit → 16-bit

Stuff low byte with 0.

The transformation sequence are :

❶ Unsigned → Signed
❷ 8-bit → 16-bit
❸ Mono → Stereo

AC97 Mixer Read procedure :

1.Check AC97-STATUS bit 7, if bit7=1 go to 1,else go to 2.
2.Write mixer index to AC97-ACCESS(bit 24~31) with bit 31=1(Read operation)
3.Check AC97-STATUS bit 6, if bit 6=0 goto 3, else goto 4.
4.Read data from AC97-READ.

AC97 Mixer Write procedure :

1.Check AC97-STATUS bit 7, if bit 7 =1 go to 1,else go to 2.
2.Write index and data to AC97-ACCESS with bit 31=0

Wave Engine RAM access :

The working RAM of wave engine is 128 x 32 RAM. It can be accessed via “Address” port and 32-bit “Data” port.

Note for Interrupt Service Routine(ISR) and TSR :

Because ALS300 share one IRQ line with multiple IRQ request., the TSR developer will pay more attention to decide which request to be served.

For TSR :

1.Mask INTA# output. (Set GCR8C.15) ,check IRQ-STATUS and acknowledge IRQs.
2.Call corresponding **ISR**s (higher-priority ISR first)

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3.Enable INTA# output capability again.(Clear GCR.15) and return to main program

For ISR :

1.Serve IRQ request.

Power down sequence :

❶Enable power down clock (set RCCLKEN as 1)
❷Wait power down clock stable and power down wave engine/FM/SB/MPU401
❸ Wait 384 clocks of BITCLK (at least 31.2us) and power down AC-Link
❹Disable 14.318 MHz output (set VCO-OSCEN# as 1)

Power on sequence :

❶Activate AC-Link
❷Enable 14.318MHz output (Clear VCO-OSCEN# as 0)
❸Power on SB/Wave engine/MPU401/FM (wait for 14.318M clock stable if power on FM)
❹Disable power clock (2MHz) output. (Clear RCCLKEN as 0)

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IRQ acknowledge method and suggested IRQ priority for TSR :

Type	Priority	Condition to generate	Acknowledgment
MIN	0	Modem-In data is available	Write **IRQ-STATUS** bit 1 with 1
Ring-In	1	RING# input is low	Write **IRQ-STATUS** bit 0 with 1
PCI-Play	2	End of a block of playback transfer	Write **IRQ-STATUS** bit 3 with 1
MICIN	3	End of a block of Mic-In transfer	Write **IRQ-STATUS** bit 4 with 1
PCI-Rec	4	End of a block of record transfer	Write **IRQ-STATUS** bit 2 with 1
SB/MPU	5	SB playback/MPU401	Write **IRQ-STATUS** bit 7 with 1
SB-Mixer	6	Write SB mixer	Write **IRQ-STATUS** bit 5 with 1
DRAM	7	End of a block of DRAM transfer	Write **IRQ-STATUS** bit 6 with 1
0: highest priority 6 : lowest priority			

Memory Space and IO Space in "PCI" :

Memory space : 2M bytes

The starting address is defined in PCI configuration registers. This memory space is mapping to DRAM.

ALS300 IO Space 0 : 64 bytes

Address	Byte 3	Byte 2	Byte 1	Byte 0
IOBASE0+00h	AC97-ACCESS (**R/W**)			
IOBASE0+04h	IRQ-STATUS(**R/W**)	AC97-STATUS(**R**)	AC97-READ (**R**)	
IOBASE0+08h	GCR/RAM-DATA (**R/W**)			
IOBASE0+0Ch	Reserved			GCR/RAM-INDEX (**R/W**)

❶IOBASE0 = Base address defined in configuration space
❷ALS300 support DW/Word/Byte access. When access PnP alias port for PnP configuration, ALS300 support byte command only.
❸Only byte command transformation is permitted for IOBASE0 + 10h ~23h.
❹SBBASE+0~3 is equivalent to OPLBASE+0~3.

AC97-ACCESS Default : XXXXXXXXh IOBASE + 00-03h

Bit	Type	Function
31	R/W	R/W control , 0 : Write 1 : Read
30:24	R/W	AC97 mixer index
23:16		Reserved
15:0	R/W	AC97 write data

❶The programmer should write index and data at the same time or write data before writing index. This ensure index and data will output in the same frame.

AC97-READ Default : XXXXh IOBASE + 04-05h

Bit	Type	Function
15:0	R	Data return from AC97 CODEC

AC97-STATUS Default : 00h IOBASE + 06h

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Bit	Type	Function
7	R	**INDX** status 0 : Ready for AC97 mixer access 1 : AC97 is busy
6	R	**DIN** status 0 : Empty 1 : AC97 mixer data is available
5	R	**MOUT** status 0 : AC97 is ready for Modem-Out transfer 1 : AC97 Modem-Out is busy
4	**R**	**MPU401 IRQ flag 0 : No IRQ 1 : IRQ generated (For D version only)**
3	R	**PCILO/PCIRO** FIFO status 0 : empty 1 : non-empty
2	R	**PCILI/PCIRI** FIFO status 0 : empty 1 : non-empty
1	R	**MICIN** FIFO status 0 : empty 1 : non-empty
0	R	**DRAM** FIFO status 0 : empty 1 : non-empty

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❶An IO-Write to AC97-ACCESS with bit 31=1 will clear bit 6.

❷**Read IOBASE+4~7 will clear bit 4 automatically. (For D Version)**

IRQ-STATUS Default : 00h IOBASE + 07h

Bit	Type	Function
7	R/W	SB/MPU IRQ flag : 0 : Normal 1 : IRQ generated
6	R/W	DRAM IRQ flag : 0 : Normal 1 : IRQ generated
5	R/W	SB-Mixer IRQ flag : 0 : Normal 1 : IRQ generated
4	R/W	**MICIN** IRQ flag : 0 : Normal 1 : IRQ generated
3	R/W	**PCI-Play** IRQ flag : 0 : Normal 1 : IRQ generated
2	R/W	**PCI-Rec** IRQ flag : 0 : normal 1: IRQ generated
1	R/W	**Modem-In** IRQ flag : 0 : Normal 1 : IRQ generated
0	R/W	**Ring-In** IRQ flag : 0 : Normal 1 : IRQ generated

❶**Write this register with "1" will clear the corresponding IRQ flag.**
Write this register with "0" will keep the corresponding IRQ flag.

❷**When bit 7 is set, TSR should read MX82 to identify the requesting device. Write 1 to this bit will clear the flag too. TSR should acknowledge the IRQ by access acknowledge port in "SB logic". Note that IRQ request from SB core is routed to INTA# directly. Bit 7 is a flag only**

❸**The MPU401 IRQ status located at different register for different version.**

Version	Location	Acknowledge
A	IRQ-STATUS bit 7	Write IRQ-STSTUS with bit 7 as 1
C	IRQ-STATUS bit 7	Write IRQ-STSTUS with bit 7 as 1
D	AC97-STATUS bit 4	Read AC97-STSTUS once
E,F,G	IOBASE+E bit 4	Read IOBASE+C~E

GCR/RAM-DATA Default : XXXXXXXXh IOBASE + 08-0Bh

Bit	Type	Function
31:0	R/W	GCR/Wave engine RAM data

GCR/RAM-Index Default : XXh IOBASE + 0Ch

Bit	Type	Function
7	R/W	GCR/Wave engine select 0 : Wave engine RAM 1 : GCR
6:0	R/W	GCR/Wave engine RAM index

EXT-IRQ-STATUS Default : 00h IOBASE + 0Eh

Bit	Type	Function
7:5		Reserved
4	R	**MPU401** IRQ flag : 0 : Normal 1 : IRQ generated **(implemented for version latter than E)**
3:1		Reserved
0	R	**FFLP** (Internal Flip-Flop , **implemented for version latter than F**)

❶Read IOBASE+0Eh will clear bit 4 automatically

❷Bit 0 will use as low/high byte pointer when driver take IO trapping skill.

ALS300 Global Control Register Array :

Index Port : GCR/RAM-Index

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Data Port : GCR/RAM-DATA

GCR80 Default XXXXXXXXh Playback starting address

Bit	Type	Function
31:2	R/W	Playback starting address SA[31..2]
1:0		Reserved

GCR81 Default XXXXXXXXh Playback end address

Bit	Type	Function
31:2	R/W	Playback end address EA[31..2]
1:0		Reserved

GCR82 Default : 0000XXXXh Playback control

Bit	Type	Function
31:22	R/W	PCI Playback sampling rate PCIFS[9..0]
21	R/W	PCILO/PCIRO FIFO threshold control 0 : 4DW 1 : 2DW
20	R/W	PCM type 1 : unsigned 0 : signed
19	R/W	Mono/Stereo select : 1 : Mono 0 : Stereo
18	R/W	8/16 bit select : 1 : 8-bit 0 : 16-bit
17	R/W	Playback FIFO control 0 : Normal 1 : Pause
16	R/W	Playback transfer control 0 : Stop 1 : start
15:2	R/W	Playback block length BL[15..2]
1:0	R	Reserved, Read as 1

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❶ PCIFS formula :

bit 9 1 D=2
0 D=1
bit 8 1 O=1
0 O=0
bit7~0 N

PCIFS = F_{clk}/(M*18*D)

where M = (N+1)*2+O , F_{clk} = 14.318 MHz

❷When (no. of byte in Playback FIFO) ≤ threshold,ALS300 will generate a request to bus master for data transfer until playback FIFO is full. The bus master will transfer data from system memory to ALS300 if bit 16=1.

❸Block length = (# of data byte) - 1 (ex. 0FFFh→ 4K bytes)
ALS300 will generate an interrupt for every specified block size transfered.

GCR83 Default XXXXXXXXh Record starting address

Bit	Type	Function
31:2	R/W	Record starting address SA[31..2]
1:0		Reserved

GCR84 Default XXXXXXXXh Record end address

Bit	Type	Function
31:2	R/W	Record end address EA[31..2]
1:0		Reserved

GCR85 Default : 0000XXXXh Record control

Bit	Type	Function
31:22		Reserved
21	R/W	Record FIFO threshold control 0 : 4 DW 1 : 2 DW
20:18		Reserved
17	R/W	Record FIFO control 0 : Normal 1 : Pause
16	R/W	Record transfer control 0 : Stop 1 : start
15:2	R/W	Record block length BL[15..2]
1:0	R	Reserved, Read as 1

❶When (no. of byte in Record FIFO) ≥ threshold,ALS300 will generate a request to bus master for data transfer until Record FIFO is empty. The bus master will transfer data from ALS300 to system memory if enabled by bit 16.

❷Block length = (# of data byte) - 1 (ex. 0FFFh→ 4K bytes)
ALS300 will generate an interrupt for every specified block size transfered.

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GCR86 Default XXXXXXXXh Mic record starting address

Bit	Type	Function
31:2	R/W	Mic-In starting address SA[31..2]
1:0		Reserved

GCR87 Default XXXXXXXXh Mic record end address

Bit	Type	Function
31:2	R/W	Mic-In end address EA[31..2]
1:0		Reserved

GCR88 Default : 0000XXXXh Mic record control

Bit	Type	Function
31:22		Reserved
21	R/W	**MICIN** FIFO threshold control 0 : 4 DW 1 : 2 DW
20:18		Reserved
17	R/W	**MICIN** FIFO control 0 : Normal 1 : Pause
16	R/W	Mic-In transfer control 0 : Stop 1 : start
15:2	R/W	Mic-In block length BL[15..2]
1:0	R	Reserved, Read as 1

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❶When (no. of byte in Mic-In FIFO) ≥ threshold,ALS300 will generate a request to bus master for data transfer until Mic-In FIFO is empty. The bus master will transfer data from ALS300 to system memory if enabled by bit 16.

❷Block length = (# of data byte) - 1 (ex. 0FFFh→ 4K bytes)
ALS300 will generate an interrupt for every specified block size transfered.

GCR89 Default XXXXXXXXh DRAM-Write starting address

Bit	Type	Function
31:2	R/W	DRAM-Write starting address SA[31..2]
1:0		Reserved

GCR8A Default XXXXXXXXh DRAM-Write end address

Bit	Type	Function
31:2	R/W	DRAM-Write end address EA[31..2]
1:0		Reserved

❶After whole buffer is accessed, GCR8B.16 is cleared.

GCR8B Default : 0010XXXXh DRAM-Write control

Bit	Type	Function
31:24		Reserved
23:22	R/W	DRAM type select (DTYPE[1..0]) 0 0 One 1M X 4 (10 X 10) 0 1 Two 1M X 4 (10 X 10) 1 0 4M X 4 (11 X 11) 1 1 4M X 4 (12 X 10)
21:20	R/W	MUXRA delay select 0 0 6 ns 0 1 10 ns (default) 1 0 14 ns 1 1 18 ns
19:18		Reserved
17	R/W	DRAM access mode 0 : mode 1 1 : mode 2
16	R/W	DRAM-Write transfer control 0 : Stop 1 : start (Effective when bit 17 =1)
15:2	R/W	DRAM-Write block length BL[15..2]
1:0	R	Reserved, Read as 1

❶ When DRAM-Write FIFO is not full ,ALS300 will generate a request to bus master for data transfer until DRAM-Write FIFO is full. The bus master will transfer data from ALS300 to system memory if enabled by bit 16.

❷Block length = (# of data byte) - 1 (ex. 0FFFh→ 4K bytes)
ALS300 will generate an interrupt for every specified block size transfered.

❸SW should detect DRAM type when system is power-on.

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❹It spend 12 clocks of BITCLK (12.288MHz) to switch between DRAM access mode 1 and mode 2. The programmer should wait until the state transition is complete.

GCR8C Default XXXX0011h Miscellaneous control

Bit	Type	Function
31:30		Reserved
29	**R**	**279/A79 snoop control 0 : Enable 1 : Disable**
28	R	PCI/SB# status 1 : PCI wave 0 : SB wave
27		Reserved
26	R	ALS300 clock source 0 : Internal PLL 1 : External crystal
25	R	PnP port IOEN gating control 0 : No gating 1 : gating
24	R	PnP emulation H/W control bit 0 : Enable 1 : Disable
23	R/W	PLL or crystal oscillator control (VCO-OSCEN#) 0:Enable(Default) 1:Disable
22	R/W	RC oscillator control (RCCLKEN) 0:Disable(Default) 1:Enable
21	**R/W**	**Music mute control (MMUTE#) 1 : Normal 0 : Mute (Default : 1)**
20	**R/W**	**Voice mute control (VMUTE#) 1 : Normal 0 : Mute (Default : 1)**
19:16	R	Chip revision number
15	R/W	INTA# mask control 0 Enable IRQ output 1 Disable IRQ output (Drive INTA# to inactive state) **Version F or latter :** 1 Enable IRQ output 0 Disable IRQ output (Drive INTA# to inactive state)
14	R/W	AC97 interface loop-back control (**ACLB**) 0 : Normal 1 : Loop-back (AC serial output → AC serial input)
13	R/W	FIFO loop-back control 0 : Disable 1 : Enable (PCILO→PCILI,PCIRO→PCIRI,PCILO→MICIN)
12	R/W	MIN IRQ control 0 : Disable 1 : Enable
11	R/W	Ring-In IRQ control 0 : Disable 1 : Enable
10	R/W	Digital sum control 0 $PCM_{sum} = PCM_{voice} + PCM_{music}$ 1 $PCM_{sum} = PCM_{voice}/2 + PCM_{music}/2$
9	R/W	Legacy-DMA read control 0 : disable (Default) 1 : Enable
8	**R/W**	**Special Data latch control 0 : Normal 1 : SiS5513**
7	**R**	**Level latch from HOOK when system reset.**
6:5	R/W	AC97 reset mode select 00 : Normal 01 : Warm reset 10 : Cold reset 11 : Reserved
4	R/W	PCM playback mute control 0 : mute 1 : unmute
3	R/W	HOOK output capability control 0 : Float 1 : Drive bit 2 to pad
2	R/W	Data drived to HOOK
1	**R**	**Synthesizer MUX status (WVE/FM#)** **1 : Internal Wave engine 0 : FM synthesizer**
0	R/W	Wave engine mute control (WMUTE#) 0 : mute 1 : Normal

❶Chip-ID will increase by 1 when chip tape-out.

❷WVEREQ low-go-high edge will select wave engine as musical synthesizer.

❸Actually the PnP emulation control signal ,PNPEN, is

PNPEN = BOND & (!GCR8C.24&GCR8C.29)

❹When GCR8C.5 or GCR8C.6 is set, it will be cleared when AC97 reset operation is complete.

❺GCR8C.24 is latched from DQ0 when system reset.
GCR8C.25 is latched from DQ1 when system reset.
GCR8C.26 is latched from DQ2 when system reset.

GCR8D Default : 00XXXXXXh DRAM address of mode 2 access

Bit	Type	Function
31:21		Reserved
20:2	R/W	DRAM address DA[20..2] (Byte address)
1:0	R	Read as 0

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When ALS300 start DRAM data transfer, DA[20..2] is the starting address of the DRAM memory space. This address will increase automatically during the transfer period. SW should update this register content before the beginning of next block transfer.

GCR8E Default : XXXXXXXXh Music/Voice volume

Bit	Type	Function
31:27	R/W	Music-Left volume in 1.5Db step , **00h : 0dB , 1Fh : -46dB**
26:24		Reserved
23:19	R/W	Music-Right volume in 1.5Db step , **00h : 0dB , 1Fh : -46dB**
18:16		Reserved
15:11	R/W	Voice-Left volume in 1.5Db step , **00h : 0dB , 1Fh : -46dB**
10:8		Reserved
7:3	R/W	Voice-Right volume in 1.5Db step , **00h : 0dB , 1Fh : -46dB**
2:0		Reserved

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❶SW should set a default volume after system reset.

GCR8F Default : XXXXXXXXh Modem I/O

Bit	Type	Function
31:16	W	Modem-Out data bit 15~0
15:0	R	Modem-In data bit 15~0

GCR90 Default : XX5A0000h Test mode register

Bit	Type	Function
31:24	R/W	Reserved
23:22	R/W	RC oscillator output divider 00:2 01:4 10:8 11:16
21:20	R/W	VCO V-I stage resistor select 00:5.2K 01:4.5K 10:3.7K 11:3K
19	R/W	RC oscillator input current control 0:30u 1:45u
18	R/W	VCO input current control 0:30u 1:45u
17:16	R/W	Band Gap resister control 00:2.5K 01:2.2K 10:1.9K 11:1.6K
15:8	R/W	SB test mode register (Normal = 00h)
7:6	R/W	Wave engine test mode register
5	R/W	PLL test (PLLTEST) 0 : 14.318M/256 1: 2M/32
4:0	R/W	Wave engine test mode register (Normal = 00h)

❶PLLTEST 0 XCLK output 14.318M/256 clock
1 XCLK output OSC2 clock (2M/32 Hz)

GCR91 Default : 00FFFFFFh DMA 0 starting address

Bit	Type	Function
31:24		Reserved
23:0	R	DMA channel 0 starting address SA0[23..0]

❶Stuff SA0[31..24] with 0 when implemented.

GCR92 Default : 0000FFFFh DMA 0 mode register and base byte count

Bit	Type	Function
31:22		Reserved
21	R	Address increment/decrement select. 0 : increment 1 : decrement
20	R	Auto-initialization enable 0 : Disable 1 : Enable
19:18	R	Transfer mode 01 : Write 10 : Read Others : Reserved
17:16		Reserved
15:0	R	DMA channel 0 base byte count BBC0[15..0]

❶Write transfer ALS300 → Memory
Read transfer ALS300 ← Memory

GCR93 Default : 00FFFFFFh DMA 1 starting address

Bit	Type	Function
31:24		Reserved
23:0	R	DMA channel 1 starting address SA1[23..0]

❶Stuff SA1[31..24] with 0 when implemented.

GCR94 Default : 0000FFFFh DMA 1 mode register and base byte count

Bit	Type	Function

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31:22		Reserved
21	R	Address increment/decrement select. 0 : increment 1 : decrement
20	R	Auto-initialization enable 0 : Disable 1 : Enable
19:18	R	Transfer mode 01 : Write 10 : Read
17:16		Reserved
15:0	R	DMA channel 1 base byte count BBC1[15..0]

❶Write transfer ALS300 → Memory
Read transfer ALS300 ← Memory

GCR95 Default : 00FFFFFFh DMA 3 starting address

Bit	Type	Function
31:24		Reserved
23:0	R	DMA channel 3 starting address SA3[23..0]

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❶Stuff SA[31..24] with 0 when implemented.

GCR96 Default : 0000FFFFh DMA 3 mode register and base byte count

Bit	Type	Function
31:22		Reserved
21	R	Address increment/decrement select. 0 : increment 1 : decrement
20	R	Auto-initialization enable 0 : Disable 1 : Enable
19:18	R	Transfer mode 01 : Write 10 : Read
17:16		Reserved
15:0	R	DMA channel 3 base byte count BBC3[15..0]

❶Write transfer ALS300 → Memory
Read transfer ALS300 ← Memory

GCR97 Default XX004071h

Bit	Type	Function
31:24	R	PnP read port address RA[9..2], RA[1..0]=[1,1]
23:20		Reserved
19	**R/W**	**SBBASE decode control 0 : Enable 1 : Disable**
18	**R/W**	**OPLBASE decode control 0 : Enable 1 : Disable**
17	**R/W**	**GAMEBASE decode control 0 : Enable 1 : Disable**
16	**R/W**	**MPUBASE decode control 0 : Enable 1 : Disable**
15:8	R/W	GAMEBASE[10..3] (Default : 40h)
7:0	R/W	OPLBASE[10..3] (Default : 71h)

❶When PnP emulation is disabled, SW can access PnP alias ports (GCR99.31~16) to configure SB logic. The configuration process is identical to that of PnP specification except the IO address. The new address map are :

GCR99.31~24 Write data port (A79h)

Note that there is no alias port for PnP read data port. In alias configuration process, **ALS300 will not catch the data that writing to PnP registers.**

❷Bit 19~16 control the legacy IO

GCR98 Default B0002233h

Bit	Type	Function
31	R	DMA 3 mask 1 : mask DMA operation (Default : 1)
30		Reserved
29	R	DMA 1 mask 1 : mask DMA operation (Default : 1)
28	R	DMA 0 mask 1 : mask DMA operation (Default : 1)
27		Reserved
26:24	R/W	SB DMA (PNP0-74.2~0) (Default 00)
23	R/W	SB IO range check control(PNP0-31.1) 0 : Disable 1 : Enable
22	R/W	OPL3 IO range check control(PNP1-31.1) 0 : Disable 1 : Enable
21	R/W	Game-Port IO range check control(PNP2-31.1) 0 : Disable 1 : Enable
20	R/W	MPU401 IO range check control(PNP3-31.1) 0 : Disable 1 : Enable
19	R/W	SB activate (PNP0-30.0) 0 : Disable 1 : Enable
18	R/W	OPL3 activate (PNP1-30.0) 0 : Disable 1 : Enable

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17	R/W	Game-Port activate (PNP2-30.0) 0 : Disable 1 : Enable
16	R/W	MPU401 activate (PNP2-30.0) 0 : Disable 1 : Enable
15		Reserved
14	R	DMA channel group enable 0 : Enable 1 : Disable
13:8	R/W	SBBASE[9..4] (Default : 22h)
7:6	R	PnP Device number (PNP07[1..0])
5:0	R/W	MPUBASE[9..4] (Default : 33h)

❶When DMA group enable bit (GCR98.14) is set, it will disable DMA 0,1,3 emulation. When this bit is clear, DMA emulation is controlled by mask bit (GCR98.31,29,28).

❷SB DMA
000 DMA 0
001 DMA 1
011 DMA 3
100 No DMA select
others Reserved

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❸If auto-initialized mode is disabled, GCR98.31,29,28 will be set when TC=1.

GCR99 Default 00000000h

Bit	Type	Function
31:24	W	A79h alias port
23:16	W	279h alias port
15:6	R/W	DDMA base address DDMABA[15..6]
5:1		Reserved
0	R/W	DDMA enable 0 : Disable 1 : Enable **(Default : 0)**

❶When DDMA is enabled, ALS300 ignore legacy DMAC IO cycle and claim DDMA IO cycle.

❷When access 279h/A79h alias port, it is strongly commended to issue byte command.

GCR9A Default XXXXXXXXh PCI-play block counter

Bit	Type	Function
31:16		Reserved
15:0	R	value of block counter

GCR9B Default XXXXXXXXh PCI-Rec block counter

Bit	Type	Function
31:16		Reserved
15:0	R	value of block counter

GCR9C Default XXXXXXXXh Mic-In block counter

Bit	Type	Function
31:16		Reserved
15:0	R	value of block counter

GCR9D Default XXXXXXXXh DRAM block counter

Bit	Type	Function
31:16		Reserved
15:0	R	value of block counter

GCR9E Default XXXXXXXXh Wave engine test register 0

Bit	Type	Function
31:0	R/W	For test mode only

GCR9F Default XXXXXXXXh Wave engine test register 1

Bit	Type	Function
31:8		Reserved
7:0	R/W	For test mode only

DMA Emulation Design Suggestion :

❶CBC decrease by 1 each time when 1-byte transfer is complete.

❷CA will decrease/increase by 1 each time when DRQx is activated. ALS300 will discard CA [1..0] for fetching next data. One layer latch is enough for DMA emulation.

PCI Configuration Registers :

Vendor ID register :

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Index : 00-01h Read only
Bit 15~8 40h (Vendor ID high byte)
Bit 7~0 05h (Vendor ID low byte)

Device ID register :

Index : 02-03h Read only
Bit 15~8 03h (Device ID high byte)
Bit 7~0 00h (Device ID low byte)

Command register :

Default 00h
Index : 04-05h R/W
Bit 2~0 0 Disable
1 Enable
Bit 15~3 Reserved, read as 0
Bit 2 Bus Master enable
Bit 1 Memory access enable
Bit 0 IO access enable

Write PCI configuration register indexed 04h will reset ALS300 bus master.

Status register :

Index : 06-07h Read only
Default 00h
Read :
Bit 15~11 Reserved ,read as 0
Bit 10,9 DEVSEL# Timing
Read as 01 (Medium Timing)
Bit 8 Data Parity Reported
0 Normal
1 Data parity error detected
Bit 7~0 Reserved, read as 0
Write one bit with 1 will clear this bit.

Class code register :

Index : 09~0Bh Read only
Read as 040100h (Multimedia Audio Device)

Latency Timer Register :

Index: 0Dh R/W
Default : 00h
Bit 7~4 No. of PCI clock that ALS300 retain ownership of bus.
Bit 3~0 Reserved , read as 0

Base Address Register 0 : (IO SPACE 0)

Index : 10~13h R/W
Default : 0001h
Bit 0 Read as 1 (IO base address indicator)
Bit 4~1 Reserved, read as 0
Bit 31~5 IOBASE bit 31~5 (32-bytes IO space)

Base Address Register 1 : (Memory Space)

Index 14~17h R/W
Default : 0000h
Bit 20~0 Read as 0
Bit 31~21 DRAMBASE bit 31~21 (2M bytes)

Subsystem Vendor ID :

Index : 2C~2Dh Read only
Default : 4005h
Bit 15~0 Subsystem Vendor ID
If external E^2PROM is enabled, subsystem vendor ID will be load from E^2PROM after reset.

Subsystem ID :

Index : 2E~2Fh Read only
Default : 0000h
Bit 15~0 Subsystem ID

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If external E^2PROM is enabled, subsystem ID will be load from E^2PROM after reset.

Interrupt Line Register :

Index : 3Ch R/W
Default : 0x00
Bit 7~0 IRQ number

Interrupt Pin Register :

Index : 3Dh Read only
Default : 01h (INTA#)

PNP register array : (write only PNPS[1..0]=[1x])

index register 279h (Write only)
write data port A79h (Write only)

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PNP00 Read Port Register

Write only (Enabled when PNPS[1..0]=1X)
Bit 7~0 GCR97.31~24

PNP07 Device Number register

Write only(Enabled when PNPS[1..0]=1X)
Bit 7~2 Reserved
Bit 1~0 GCR98.7~6

PNP0-30 SB activate register

Write only(Enabled when PNPS[1..0]=1X)
Bit 0 GCR98.19
Bit 7~1 Reserved

PNP0-31 SB IO range check

Write only(Enabled when PNPS[1..0]=1X)
Bit 7~2 Reserved
Bit 1 GCR98.23
Bit 0 Reserved

PNP0-60 SB Base-high

Write only(Enabled when PNPS[1..0]=1X)
Bit7~2 Reserved
Bit 1 SBBASE.9 (GCR98.13)
Bit 0 SBBASE.8 (GCR98.12)

PNP0-61 SB Base-low

Write only (Enabled when PNPS[1..0]=1X)
Bit 7~4 SBBASE.7~4 (GCR98.11~8)
Bit 3~0 Reserved

PNP0-74 SB DMA

Write only (Enabled when PNPS[1..0]=1X)
Bit7~3 Reserved
Bit 2~0 SBDMA (GCR98.26~24)

PNP1-30 OPL3 activate register

Write only (Enabled when PNPS[1..0]=1X)
Bit 7~1 Reserved
Bit 0 GCR98.18

PNP1-31 OPL3 IO range check

Write only(Enabled when PNPS[1..0]=1X)
Bit 7~2 Reserved
Bit 1 GCR98.22
Bit 0 Reserved

PNP1-60 OPL3 Base-high

Write only(Enabled when PNPS[1..0]=1X)
Bit7~3 Reserved
Bit 2~0 OPLBASE.10~8 (GCR97.7~5)

PNP1-61 OPL3 Base-low

Write only (Enabled when PNPS[1..0]=1X)
Bit 7~3 OPLBASE.7~3 (GCR97.4~0)

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Bit 2~0 Reserved

PNP2-30 Game-Port activate register

Write only (Enabled when PNPS[1..0]=1X)

Bit 7~1 Reserved

Bit 0 GCR98.17

PNP2-31 Game-Port IO range check

Write only(Enabled when PNPS[1..0]=1X)

Bit 7~2 Reserved

Bit 1 GCR98.21

Bit 0 Reserved

PNP2-60 Game-Port Base-high

Write only(Enabled when PNPS[1..0]=1X)

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Bit7~3 Reserved

Bit 2 GAMEBASE.10~8 (GCR97.15~13)

PNP2-61 Game-Port Base-low

Write only (Enabled when PNPS[1..0]=1X)

Bit 7~3 GAMELBASE.7~3 (GCR97.12~8)

Bit 2~0 Reserved

PNP3-30 MPU401 activate register

Write only (Enabled when PNPS[1..0]=1X)

Bit 7~1 Reserved

Bit 0 GCR98.16

PNP3-31 MPU401 IO range check

Write only(Enabled when PNPS[1..0]=1X)

Bit 7~2 Reserved

Bit 1 GCR98.20

Bit 0 Reserved

PNP3-60 MPU401 Base-high

Write only (Enabled when PNPS[1..0]=1X)

Bit7~2 Reserved

Bit 1~0 MPUBASE.9~8 (GCR98.5~4)

PNP3-61 MPU401 Base-low

Write only (Enabled when PNPS[1..0]=1X)

Bit 7~4 MPUBASE.7~4 (GCR98.3~0)

Bit3~0 Reserved

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Appendix A : PnP and DMA Emulation

PNP state :

PNP state	PNPS[1..0]
Wait-for-key	00
Sleep	01
Configuration	10
Isolation	11

The PnP specification define PnP register indexed 00h~2Fh as card level register, others as device level register. For simplicity, we define

PNPxx : PNP card level register xx, where xx is in range of 00h to 2fh.

PNPy-xx : PNP device **y** register xx, where xx is in range of 30h to ffh

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Note that PNPxx and PNPy-xx implemented in PCI interface are write-only for PnP compatibility. The write operation is enabled only when PNPS[1..0]=1x.

ALS300 "PnP emulation block" decode the following address range for "SB logic" when GCR9A.1=0 :

Address	Length	Type	Enabled condition
SBBASE[15..0]	16 bytes	IO R/W	(PNP0-30.0=1)|(PNP0.31.1=1)
OPLBASE[15..0]	**4 bytes**	**IO R/W**	**(PNP1-30.0=1)|(PNP1-31.1=1)**
GAMEBASE[15..0]	8 bytes	IO R/W	(PNP2-30.0=1)|(PNP2-31.1=1)
MPUBASE[15..0]	4 bytes	IO R/W	(PNP3-30.0=1)|(PNP3-31.1=1)
279h	1 byte	IO W	*Note*
A79h	1 byte	IO W	*Note*
RA[9..0]	1 byte	IO R	PNPS[1..0]=[1x]

Note : ❶ALS300 claim write cycle of A79h only when
[(PNPS[1..0]=01) & CSN0&(PNP index = 03)]
where CSN0 is the flag indicating CSN=0. CSN0=1 means CSN = 0.
For other conditions, ALS300 "snoop" it only. Remember that ALS300 always forward write cycle of A79h to SB logic.

❷For 279h decoding, ALS300 always snoop and forward to SB core logic.

❸For PnP read port decoding, ALS300 snoop and forward to SB logic only when PNPS[1..0]=1x.

DMA emulation by BUS Master function :

ALS300 implement 2 types of DMA emulation scheme : Legacy DMA and Distributed DMA (DDMA). ALS300 emulate the assigned channel (0,1,3) only.

Internal Registers/Flags :

RETRY The flag decide whether read status from 8237 or not.(Effective in Legacy-DMA)
1 Enabled read (Default)
0 Disable read

FFLP 1_bit Flip-Flop function as low/high byte pointer for DMA IO register (00~07h) (Effective in Legacy-DMA)
Write 0x0c will clear FFLP to 0.FFLP is default 0 after reset. Any access to 00h~07h will toggle it's value.

CA 24-bit address counter of DMA emulation.

CBC 16-bit byte counter of DMA emulation.

DMA Emulation Scheme for Legacy-DMA mode and DDMA mode :

- **Legacy-DMA Mode :**

ALS300 decode the following IO command :

Address	Command	Function	Enabled
00h	IO write	FFLP=0: Write to GCR91.7~0 FFLP=1: Write to GCR91.15~8	Always
00h	IO read	FFLP=0: read from CA.7~0 FFLP=1: read from CA.15~8	SBDMA = 000
01h	IO write	FFLP=0: Write to GCR92.7~0 FFLP=1: Write to GCR92.15~8	Always
01h	IO read	FFLP=0: read from CBC.7~0	SBDMA

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		FFLP=1: read from CBC.15~8	= 000
87h	IO write	write to GCR91.23~16	Always
02h	IO write	FFLP=0: Write to GCR93.7~0 FFLP=1: Write to GCR93.15~8	Always
02h	IO read	FFLP=0: read from CA.7~0 FFLP=1: read from CA.15~8	SBDMA = 001
03h	IO write	FFLP=0: Write to GCR94.7~0 FFLP=1: Write to GCR94.15~8	Always
03h	IO read	FFLP=0: read from CBC.7~0 FFLP=1: read from CBC.15~8	SBDMA = 001
83h	IO write	write to GCR93.23~16	Always
06h	IO write	FFLP=0: Write to GCR95.7~0 FFLP=1: Write to GCR95.15~8	Always
06h	IO read	FFLP=0: read from CA.7~0 FFLP=1: read from CA.15~8	SBDMA = 003
07h	IO write	FFLP=0: Write to GCR96.7~0 FFLP=1: Write to GCR96.15~8	Always
07h	IO read	FFLP=0: read from CBC.7~0 FFLP=1: read from CBC.15~8	SBDMA = 003
82h	IO write	write to GCR95.23~16	Always
08h	IO read	Return the combined status	**$$$**
08h	IO write	Write bit 2 to GCR98.14	Always
0Ah	IO write	Bit 1, Bit 0 0 0 Write bit 2 to GCR98.28 0 1 Write bit 2 to GCR98.29 1 0 No action 1 1 Write bit 2 to GCR98.31	Always
0Bh	IO write	Bit 1, Bit 0 0 0 Write bit 5~2 to GCR92 bit 21~18 0 1 Write bit 5~2 to GCR94 bit 21~18 1 0 No action 1 1 Write bit 5~2 to GCR96 bit 21~18	Always
0Ch	IO write	Clear FFLP to 0	Always
0Dh	**IO write**	**Clear FFLP,DMA group enable(GCR98.14),DMA status and set mask bit (GCR98.31,29,28)**	**Always**
0Eh	IO write	Clear mask bit (GCR98.31,29,28)	Always
0Fh	IO write	Write all mask bit (Write bit 3,1,0 to GCR98.31,29,28)	Always

For DMA register access, ALS300 take different action for read and write operation :

Write Operation "Snoop" it,fetch data and save to corresponding registers.

Read Operation Controlled by GCR8C.9

When Legacy-DMA read is enabled, ALS300 will claim the read command For DMA status read operation, ALS300 will take action depending on RETRY. If RETRY=1, ALS300 issue PCI retry to terminate the cycle and request the bus. When granting the bus, ALS300 issue 8237 status read cycle to get the status. After getting the status, ALS300 combined it with current status of the emulated DMA channel and clear RETRY. The constructed data is :

SBDMA=000 Replace 8237-Status bit 4,0 with internal status
SBDMA=001 Replace 8237-Status bit 5,1 with internal status
SBDMA=011 Replace 8237-Status bit 7,3 with internal status

If RETRY=0, ALS300 return the status. After status is read, RETRY is set again.

For current address/byte read, ALS300 claim the command for the DMA channel emulated only. For IO read from 87h.82h/83h, it's not necessary to claim these IO command.

- **DDMA Mode :**

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ALS300 implemented DDMA register for system chipset access. The DDMA address is calculated as follow :

DDMABASE[31..16]=0
DDMABASE[15..6]=GCR99.15~6
DDMABASE[5..4]= 00 SBDMA=000
01 SBDMA=001
11 SBDMA=011
DDMABASE[3..0] map to the following operation.

DDMABASE[3..0]	Type	Function
00h	W	SBDMA=000 Write to GCR91.7~0 SBDMA=001 Write to GCR93.7~0 SBDMA=011 Write to GCR95.7~0
00h	R	Read from CA.7~0
01h	W	SBDMA=000 Write to GCR91.15~8 SBDMA=001 Write to GCR93.15~8 SBDMA=011 Write to GCR95.15~8
01h	R	Read from CA.15~8
02h	R/W	SBDMA=000 Access GCR91.23~16 SBDMA=001 Access GCR93.23~16 SBDMA=011 Access GCR95.23~16
03h		Reserved
04h	W	SBDMA=000 Write to GCR92.7~0 SBDMA=001 Write to GCR94.7~0 SBDMA=011 Write to GCR96.7~0
04h	R	Read from CBC.7~0
05h	W	SBDMA=000 Write to GCR92.15~8 SBDMA=001 Write to GCR94.15~8 SBDMA=011 Write to GCR96.15~8
05h	R	Read from CBC.15~8
06h~07h		Reserved
08h	W	Write bit 2 to GCR98.14
08h	R	Read internal DMA status
09h	W	Terminate the cycle only
0Ah		Reserved
0Bh	W	SBDMA=000 Write bit5~2 to GCR92.21~18 SBDMA=001 Write bit5~2 to GCR94.21~18 SBDMA=011 Write bit5~2 to GCR96.21~18
0Ch		Reserved
0Dh	W	**Clear FFLP,DMA group enable(GCR98.14),DMA status and set mask bit (GCR98.31,29,28)**
0E		Reserved
0F	W	SBDMA=000 Write bit 0 to GCR98.28 SBDMA=001 Write bit 0 to GCR98.29 SBDMA=011 Write bit 0 to GCR98.31

For DMA compatibility issue, CA/CBC load starting value according the condition as follow :

Source	Enabled condition
GCR91 GCR92	(SBDMA=0)&[(write PNP0-74) | (IO write GCR91,GCR92.15~0) | (TC=1 in auto-initialization mode)]
GCR93 GCR94	(SBDMA=1)&[(write PNP0-74) | (IO write GCR93,GCR94.15~0) | (TC=1 in auto-initialization mode)]
GCR95 GCR96	(SBDMA=3)&[(write PNP0-74) | (IO write GCR95,GCR96.15~0) | (TC=1 in auto-initialization mode)]

Note : TC=1 when CBC reach FFFFh.

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Appendix B : ALS300 Frequency Code Table

Code	Fs(Khz)	Code	Fs(Khz)	Code	Fs(Khz)	Code	Fs(Khz)
162	3.997	14B	5.199	134	7.434	11D	13.040
062	4.017	04B	5.233	034	7.504	01D	13.257
161	4.038	14A	5.268	133	7.576	11C	13.482
061	4.058	04A	5.303	033	7.648	01C	13.714
160	4.079	149	5.339	132	7.723	11B	13.955
060	4.100	049	5.375	032	7.798	01B	14.204
15F	4.121	148	5.411	131	7.876	11A	14.463
05F	4.143	048	5.448	031	7.954	01A	14.730
15E	4.165	147	5.486	130	8.035	119	15.008
05E	4.187	047	5.524	030	8.117	019	15.297
15D	4.209	146	5.563	12F	8.200	118	15.597
05D	4.231	046	5.602	02F	8.286	018	15.909
15C	4.254	145	5.641	12E	8.373	117	16.233
05C	4.277	045	5.682	02E	8.462	017	16.572
15B	4.300	144	5.723	12D	8.553	116	16.924
05B	4.323	044	5.764	02D	8.646	016	17.292
15A	4.347	143	5.806	12C	8.741	115	17.676
05A	4.371	043	5.849	02C	8.838	015	18.078
159	4.395	142	5.892	12B	8.938	114	18.499
059	4.419	042	5.936	02B	9.039	014	18.939
158	4.444	141	5.981	12A	9.143	113	19.401
058	4.469	041	6.026	02A	9.249	013	19.886
157	4.494	140	6.072	129	9.358	112	20.396
057	4.520	040	6.119	029	9.470	012	20.993
156	4.545	13F	6.166	128	9.584	111	21.498
056	4.571	03F	6.214	028	9.700	011	22.096
155	4.598	13E	6.263	127	9.820	110	22.727
055	4.625	03E	6.313	027	9.943	010	23.395
154	4.652	13D	6.364	126	10.069	10F	24.104
054	4.679	03D	6.415	026	10.198	00F	24.858
153	4.707	13C	6.467	125	10.330	10E	25.659
053	4.735	03C	6.520	025	10.466	00E	26.515
152	4.763	13B	6.574	124	10.605	10D	27.429
052	4.792	03B	6.629	024	10.749	00D	28.409
151	4.821	13A	6.684	123	10.896	10C	29.461
051	4.850	03A	6.741	023	11.048	00C	30.594
150	4.880	139	6.799	122	11.203	10B	31.818
050	4.910	039	6.857	022	11.363	00B	33.143
14F	4.941	138	6.917	121	11.528	10A	34.584
04F	4.972	038	6.978	021	11.698	00A	36.156
14E	5.003	137	7.039	120	11.872	109	37.878
04E	5.034	037	7.102	020	12.052	009	39.772
14D	5.066	136	7.166	11F	12.238	108	41.805
04D	5.099	036	7.231	01F	12.429	008	44.191
14C	5.132	135	7.298	11E	12.626	107	46.791
04C	5.165	035	7.365	01E	12.830		

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Code	Fs(Khz)	Code	Fs(Khz)	Code	Fs(Khz)	Code	Fs(Khz)
231	3.977	225	5.233	219	7.649	20D	14.205
330	4.018	324	5.303	318	7.799	30C	14.731
230	4.059	224	5.375	218	7.955	20C	15.297
32F	4.100	323	5.448	317	8.117	30B	15.909
22F	4.146	223	5.524	217	8.286	20B	16.572
32E	4.187	322	5.602	316	8.462	30A	17.292
22E	4.231	222	5.682	216	8.646	20A	18.078
32D	4.277	321	5.764	315	8.838	309	18.939
22D	4.323	221	5.849	215	9.039	209	19.886
32C	4.371	320	5.936	314	9.250	308	20.903
22C	4.419	220	6.026	214	9.470	208	22.096
32B	4.469	31F	6.119	313	9.701	307	23.396
22B	4.520	21F	6.215	213	9.943	207	24.858
32A	4.572	31E	6.313	312	10.198	306	26.515
22A	4.625	21E	6.415	212	10.497	206	28.409
329	4.679	31D	6.520	311	10.749	305	30.594
229	4.735	21D	6.629	211	11.048	205	33.144
328	4.792	31C	6.741	310	11.364	304	36.157
228	4.850	21C	6.857	210	11.698	204	39.772
327	4.910	31B	6.978	30F	12.052	303	44.191
227	4.972	21B	7.102	20F	12.429	203	32.000
326	5.035	31A	7.232	30E	12.830	202	16.000
226	5.099	21A	7.365	20E	13.258	201	8.000
325	5.165	319	7.504	30D	13.715	000	48.000

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Appendix C : Register contents of ALS300 Wave Engine

Wave engine RAM index : (Bit 7 = 0) **IOBASE+8**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Channel Number (N)					Register index	

N : Channel number of Wave engine

Note : SW should set all RAM to their default value to avoid causing noise.

Register 0 **Default Value : 00000000h**

Bit	Type	Function
31		Reserved
30:16	R/W	Repeat offset (RO)
15		Reserved
14:0	R/W	2's complement of samples per instrument (TL)

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❶RO is the starting point (in sample) in the wave-form of instrument that could repeat.

Register 1 **Default Value : 00000000h**

Bit	Type	Function
31	R/W	Key on control (KON) 1 : Key on 0 : Key off
30:28	R/W	Frequency Modulation Coefficient (FMC)
27	R/W	8-bit flag (F8) 1 : 8-bit data 0 : 10-bit or 12-bit data
26:24	R/W	Amplitude Modulation Coefficient (AMC)
23:21	R/W	Modulation Tone (MT)
20:0	R/W	Starting address of wave samples (SA)

❶ FMC/AMC table

FMC/AMC	AM magnitude	FM percent (FN<180h)	FM percent (FN≥180h)
0	0 dB	0 %	0 %
1	1.78 dB	0.8 %	1.6 %
2	2.91 dB	1.2 %	2.0 %
3	3.66 dB	2.0 %	3.1 %
4	4.50 dB	2.7 %	3.9 %
5	5.91 dB	5.9 %	8.6 %
6	7.41 dB	11.7 %	17.2 %
7	11.92 dB	23.4 %	34.4 %

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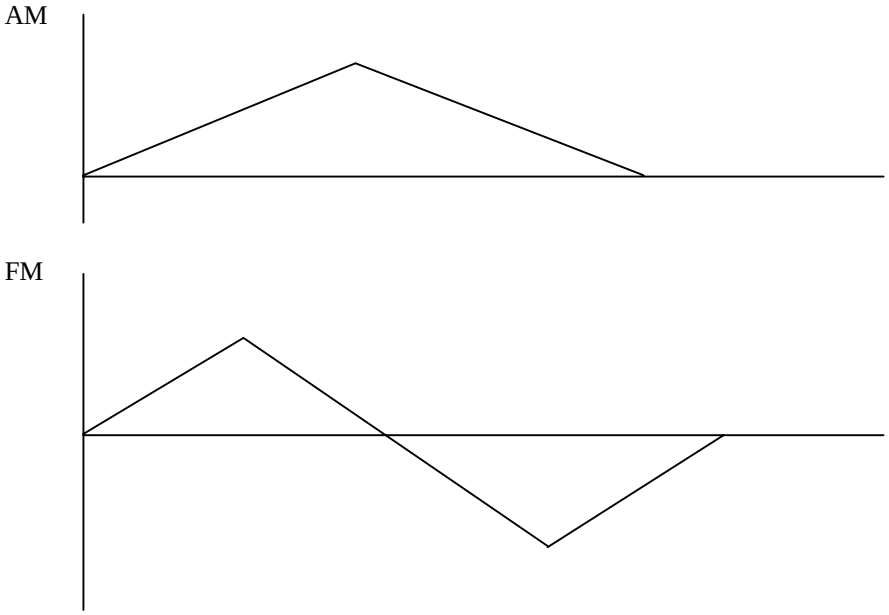

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❷MT is only effective for channel 0. For other channels , it is fixed on MT=0.

MT	Modulation frequency (Hz)
0	0.183105468
1	2.014147656
2	3.173828125
3	4.211425781
4	5.126953125
5	5.859317000
6	6.347656250
7	7.080078125

Register 2 **Default Value : 00000FFFh**

Bit	Type	Function
31	R/W	Keyboard split point (KSP)
30:28	R/W	Pitch Octave (OCT)
27:26	R/W	Voice volume adjustment (VVA)
25:16	R/W	Frequency number (FN)
15:12	R/W	Sustain level (SL)
11:10	R/W	Envelop Flag (EF) 00:Attack 01:Overshoot 10:Decay 11: Release
9:0	R/W	Envelop Attenuation (EA)

❶KSP 0 The pitch is higher than or equal to that of sample pitch
1 The pitch is lower than that of sample pitch

❷VVA Attenuation = -12*bit1 -6*bit0 (dB)

❸FN $F_{out} = F_{wave} * (FN + FM + 2^{10}) * 2^{-8*KSP+OCT-10}$

where F_{out} = final output frequency
F_{wave} = frequency of sample wave

Register 3 **Default Value : 00000000h**

Bit	Type	Function
31:28	R/W	Key Scale Ratio (KSR)
27:24	R/W	PAN -Low (Stereo control)
23	R/W	PAN MSB
22:16	R/W	Volume (VOL)
15:12	R/W	Attack Rate (AR)
11:8	R/W	Overshoot Rate (OR)

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7:4	R/W	Decay Rate (DR)
3:0	R/W	Release Rate (RR)

❷PAN table :

(unit :dB)

PAN	Left	Right	PAN	Left	Right
00	0	0	10	-96.0	-96.0
01	-1.5	0	11	0	-96.0
02	-3.0	0	12	0	-21.0
03	-4.5	0	13	0	-19.5
04	-6.0	0	14	0	-18.0
05	-7.5	0	15	0	-16.5
06	-9.0	0	16	0	-15.0
07	-10.5	0	17	0	-13.5
08	-12.0	0	18	0	-12.0
09	-13.5	0	19	0	-10.5
0A	-15.0	0	1A	0	-9.0
0B	-16.5	0	1B	0	-7.5
0C	-18.0	0	1C	0	-6.0
0D	-19.5	0	1D	0	-4.5
0E	-21.0	0	1E	0	-3.0
0F	-96.0	0	1F	0	-1.5

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Reference :

1.DDMA : Intel 82371AB data sheet.
2.PnP : “Plug and Play ISA specification” Ver 1.0a
3.DMA : Intel 8237 DMA controller
4.PCI audio : “Implementing Legacy Audio on the PCI Bus” Rev 2.1a
5.SB : ALS120 specification
6.AC97 : AC97 Specification Ver 1.03
7.PCI : PCI specification 2.1

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