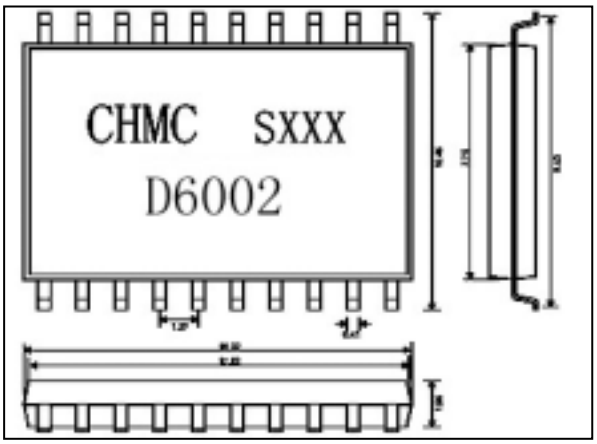
RADIO CONTROLLED RECEIVER IC D6002

DESCRIPTION

Outline Drawing



The D6002 is a bipolar integrated straight through receiver circuit in the frequency range from 40kHz up to 200kHz with ASK modulation. The IC receivers and demodulates time code signals transmitted by DCF77,MSF , WWVB and G2AS.

The devices is designed for radio controlled clock applications with very high sensitivity.

Integrated functions as stand by mode and complementary output stages offer features for universal applications.

The BIP2 technology makes all the above features possible for very low cost applications.

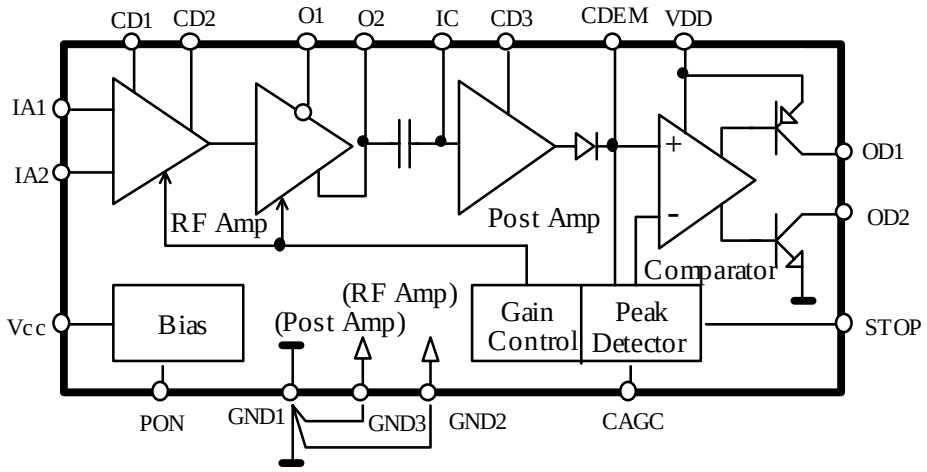
FEATURE

- Single chip straight through receiver.
- Low power battery applications(1.1~3.6V)
- Very low power consumption.
- Power down modus.
- Wide frequency range (40~200kHz)
- Very high sensitivity.
- High selectivity by quartz resonator.
- Complementary output stages.
- Minimum external components.

APPLICATIONS

- Receiver for time code transmitter signal's
- Receiver for ASK modulated date signal's.

BLOCK DIAGRAM



PIN DEFINITION

Pin	Symbol	Description	Pin	Symbol	Description
1	GND2	Ground 2 (RF stages).	11	PON	Power on
2	CD1	Decoupling capacitor C1	12	STOP	AGC stop
3	CD2	Decoupling capacitor C1	13	CAGC	AGC capacitor
4	IA1	Antenna input 1	14	CDEM	Demodulation capacitor
5	Vcc	Supply voltage	15	GND3	Ground 3(Post amplifier)
6	IA2	Antenna input 2	16	NC	Not connected
7	V_{DD}	Supply voltage for comparator and output stage	17	CD3	Decoupling capacitor C2
8	OD1	Data output 1 (pull down)	18	IC	Crystal input
9	OD2	Data output 2 (pull up)	19	O2	Non-inverting RF output
10	GND1	Ground 1(output stages)	20	O1	Inverting RF output

PON Power on/off control

If PON is connected to GND/Vcc the D6002 receiver is active/stand-by.

OD1 Data output 1

The output signal can directly decoded by a microprocessor.

The output OD1 is a PNP open collector stage with high active logic. The connection with an external resistor of 100kΩ to GND is possible.

OD2 Data output 2

The output OD2 is a NPN open collector stage with low active logic. The connection with an external resistor of 100kΩ to Vcc is possible.

GND1 Ground 1

GND1 is the control ground potential for the complete circuit. GND1 have to connected to GND2/GND3.

GND2 Ground 2

The Pin GND2 is the ground potential for the RF amplifier and has to connected to GND1.

GND3 Ground 3

The Pin GND3 is the ground potential for the Post amplifier and has to connected to GND1.

STOP AGC stop

If STOP is connected to GND/Vcc the AGC circuit is off/on

CAGC AGC capacitor

The Pin CAGC is connected to an external capacitor against GND. It is necessary to generate the peak value of the demodulator output voltage signal. The peak value controls the AGC.

CDEM Demodulation capacitor

The Pin CDEM is connected to an external capacitor against GND. It is necessary for the demodulation of the AM signal.

CD3 Decoupling capacitor C2

The Pin CD3 is connected to an external capacitor against GND. It is necessary for the stability of the post amplifier. The values of the external capacitor influence the frequency response of the post amplifier.

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

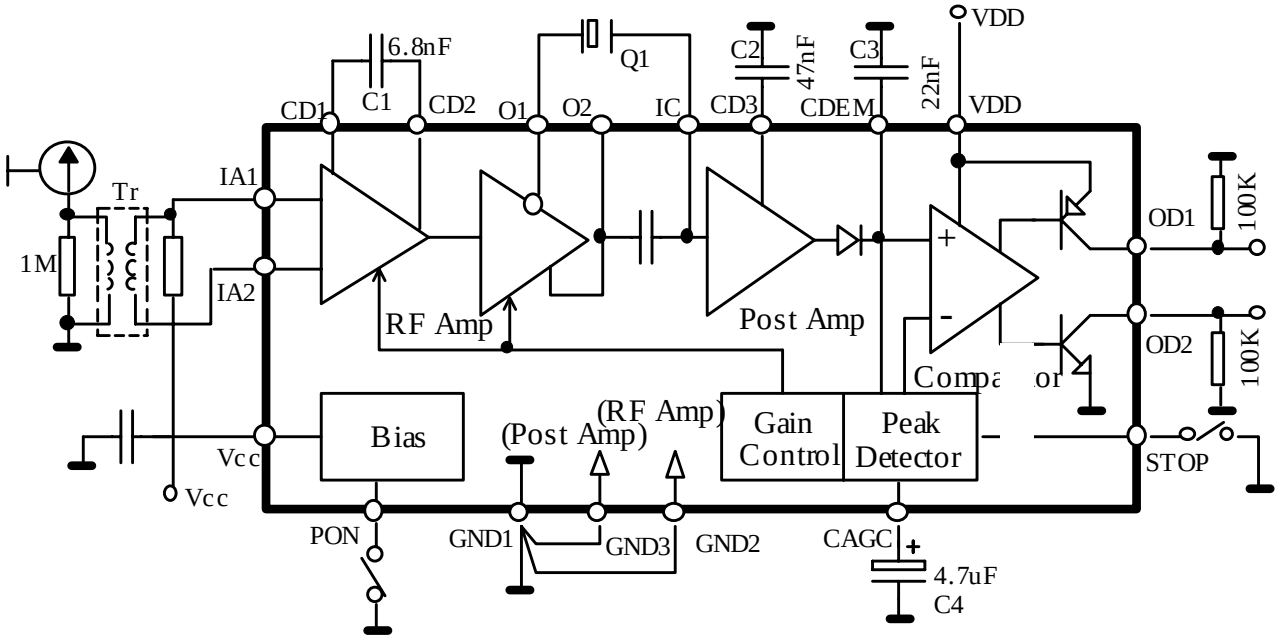
Characteristic	Symbol	Min	Max	Unit
Supply Voltage Vcc	Vcc	0	5.5	V
Supply Voltage V_{DD}	V_{DD}	0	5.5	V
Output Voltage OD1	V_{OD1}	-0.3	V_{DD} +0.3	V
Output Voltage OD2	V_{OD2}	-0.3	V_{DD} +0.3	V
Switch Voltage STOP	V_{STOP}	-0.3	V_{DD} +0.3	V
Switch Voltage PON	V_{PON}	-0.3	V_{DD} +0.3	V
Junction Temperature	Tj	-55	150	°C
Storage Temperature Range	Tstg	-55	150	°C
Electrostatic handling (MIL standard 863C)	ESD	-2000	+2000	V

ELECTRICAL CHARACTERISTICS

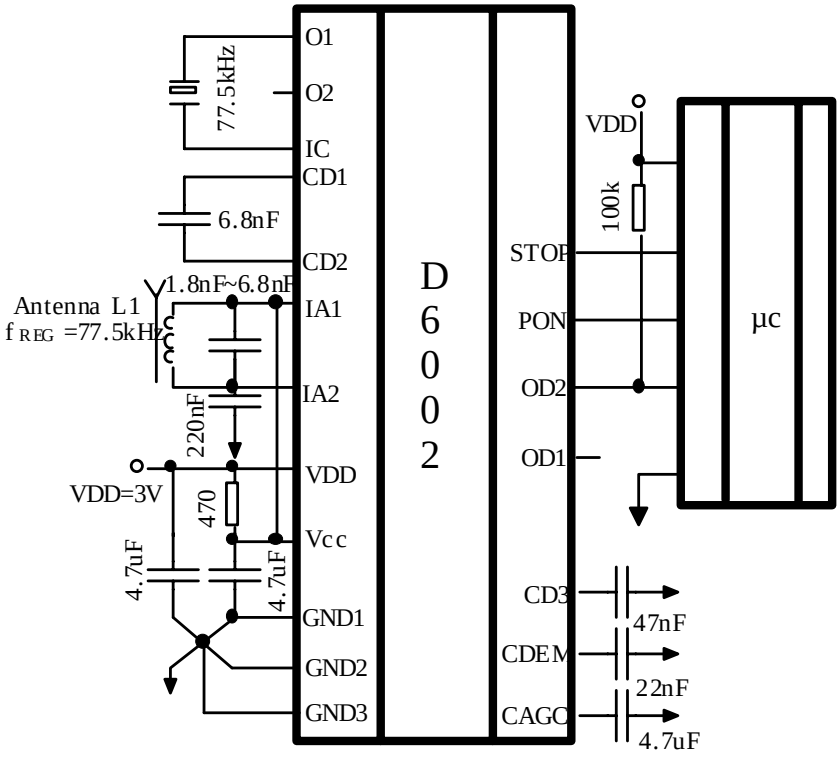
(They apply within the specified operating conditions unless otherwise specified.)

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Output pulse Duration(OD1,OD2)	t_{WODk}		170	195	230	ms
Input Voltage(IC)	$V_{IN\ IC}$		30		300	μVrms
Input Resistance(IA1,IA2)	R_{IN}			600		kΩ
Input Resistance(IC)	R_{IN}			400		kΩ
Input Resistance Demodulator	R_{IN}			50		kΩ
RF-gain	$G_{RF\ max}$	V_{CAGC}=0V		56		dB
RF gain	$G_{RF\ min}$	V_{CAGC}=Vcc		-40		dB
Output Voltage Demodulator	$V_{OUT\ DEM}$			0.25		Vp-p

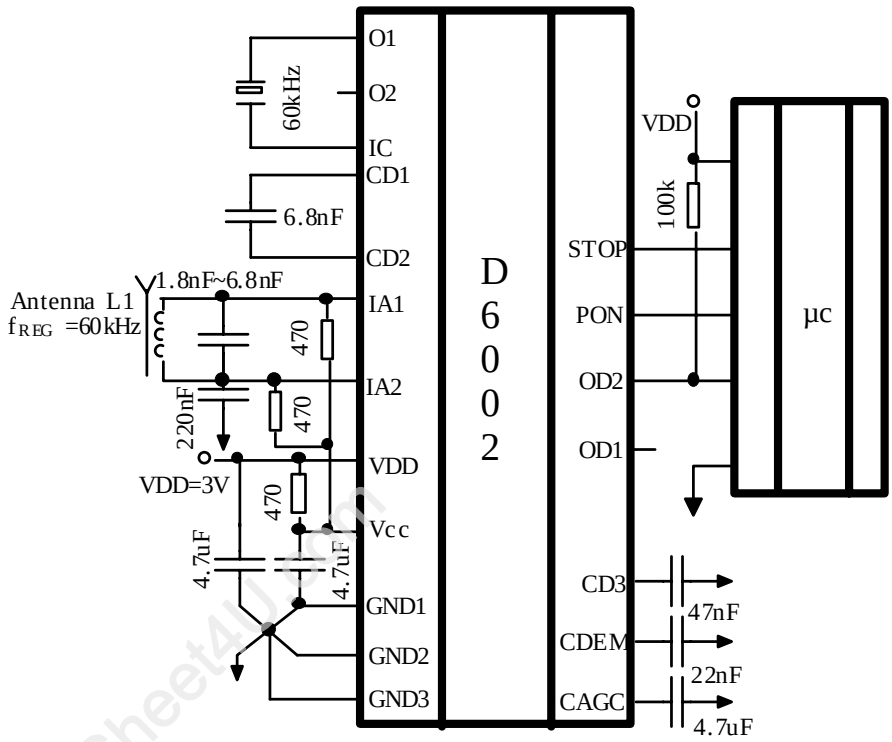
TEST CIRCUIT



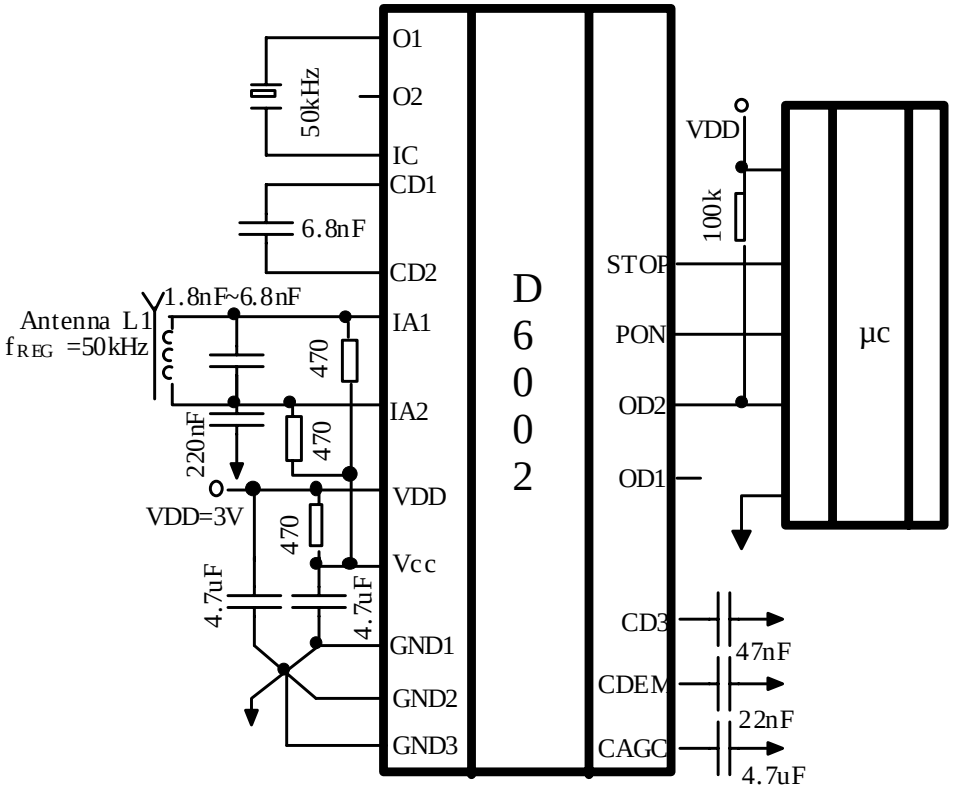
TYPICAL APPLICATION CIRCUIT



APPLICATION CIRCUIT for WWVB 60kHz



APPLICATION CIRCUIT for MSF 50kHz



APPLICATION HINT'S

- The PCB has to be designed for RF conditions.
- The ferrite antenna is a critical devices of the complete clock receiver.
- The dimensioning of the antenna resonant resistance is a compromise between high signal voltage and low antenna noise voltage. The Q-factor of antenna should be high for attenuation of inference signal's. In the application circuit is the Rref < 100k, Q=80.
- To achieve a high selectivity the parasitic parallel capacitance of the crystal should be 1~1.5pF.
- For a trouble-free reception the capacitor on GND and CD3 have to be arranged nearby the chip foot prints.