Microelectronics

CE2752

Stereo Audio DAC, 24-bit, 192kHz

DESCRIPTION

The CE2752 is a mixed signal CMOS monolithic audio digital to analog converter. It contains dual multi-bit sigma delta DAC. The system consists of 128-time interpolation filters, 3th order multi-bit ΣΔ modulators, switch capacitors and analog reconstruction filters. The multi-bit ΣΔ converter offers high tolerance to clock jitter and linearity.

The CE2752 support data conversion from 32K to 192KHz. This chip operates at 3.3 volt to reduce the power consumption and the noise caused by the digital circuit switching. The CE2752 is ideal for DVD player, AV receiver and set-top box application.

The CE2752 support 24, 20, 18 and 16-bit input data. It also support sampling frequency up to 192K.

FEATURES

- Stereo Audio DAC.
  - 100 dB SNR (A Weighted).
  - - 88dB THD + N Ratio (A Weighted).
  - 32K - 192 KHz. Sampling Rates.
  - I^2S and Left Justified Digital Input Formats.
  - On -chip Reconstruction Filters.
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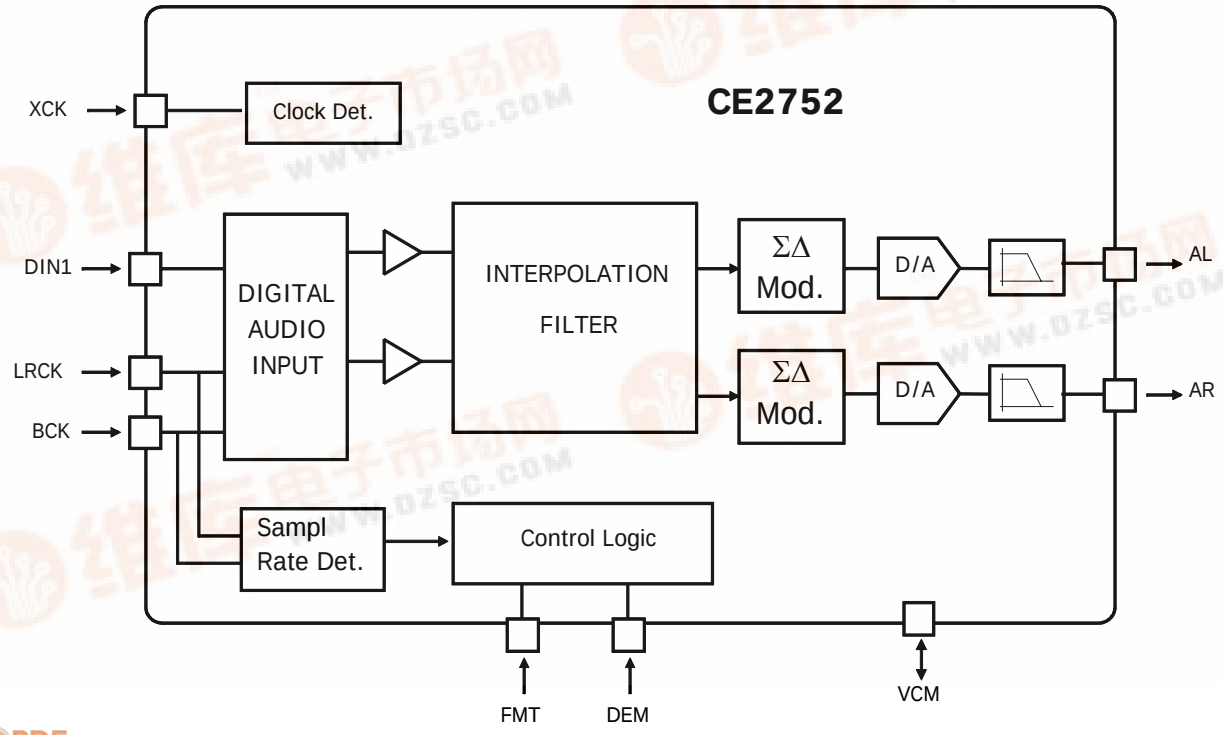
- 3.3 - 5 Volt Power Supply. Ideal for portable application.

Applications

- Digital Surround Sound For Home Theatre.
- DVD Player.
- Car Audio.
- Portable CD.

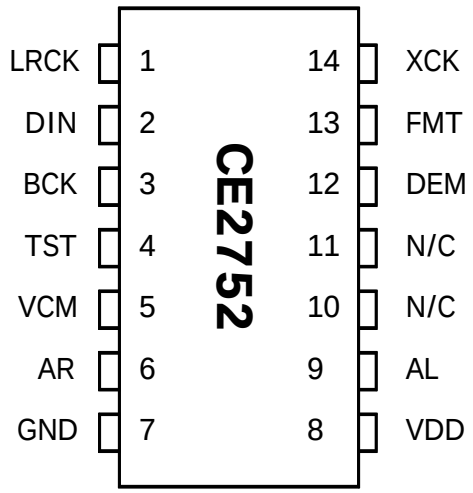
Block Diagram



DAC Performance

Item	PERFORMANCE SPECIFICATIONS	Spec.
1	Audio Output Level (Vdd= 3.3 volt)	0.71 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.04 dB
3	SNR (A-weight)	>100dB
4	THD +Noise (0dB, A-weight)	<88 dB
5	Dynamic Range (A-weight)	94 dB
6	Channel Separation	< -90 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
LRCk	1	I	Left/Right Channel Clock pin. For Left justified mode, a high in SF indicates Left Channel Data, a low in SF indicates Right Channel Data. For I2S mode, a low in SF indicates Left Channel Data, a high in SF indicates Right Channel Data.
DIN	2	I	Serial Audio Data Input.
BCK	3	I	Audio Serial Data Clock Input.
TST	4	I	Test pin. This pin should be connected to ground.
VCM	5	I/O	Common voltage De-coupling Pin Should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.
AR	6	O	Analog right channel output
GND	7	GND	ground
DVDD	8	+3.3V	3.3 or 5 volt power supply.
AL	9	O	Analog left channel output
N/C	10,11	N/C	Not used. can connected to ground.
DEM	12	I	‘low’ in normal operation, ‘high’ to enable de-emphasis filter.
FMT	13	I	‘low’ if the input is left justified format. ‘high’ if the input is I^2S format.
XCK	14	I	Master clock input.

INTRODUCTION

The CE2752 is designed to supports DVD audio with sampling rate support from 32K up to 192K. It receives 24-16 bit digital sampled audio data either in left justified or I^2S format. The received data are interpolated 128 times before they are sent to a multi-bit SD digital to analog converter. The analog section includes switch capacitor and continuous filters to reduce the out of band noise. A second order filter is required to boots the signal from 0.7 Vrms to 2 Vrms and further filter the modulation noise. The master clock, XCK, frequency for the respected sampling rate are specified in the following table.

XCK Frequency Requirement

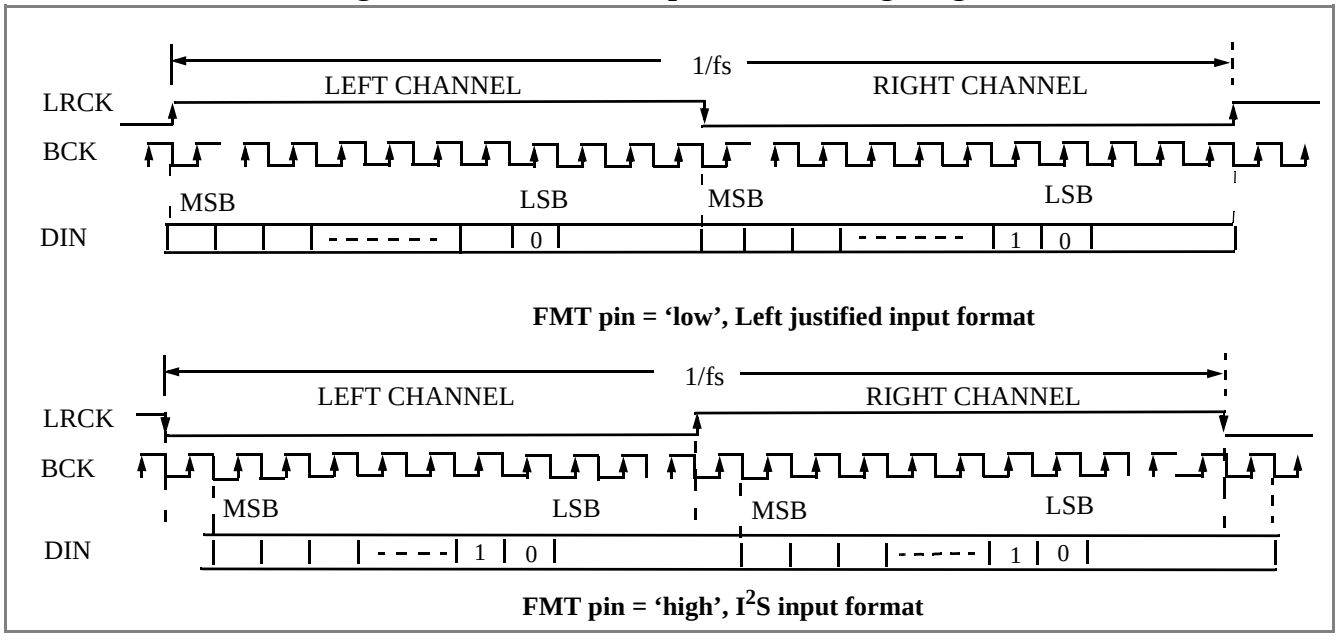
Sampling Rate	XCK Freq.				
fs	128*fs	192*fs	256*fs	384*fs	512*fs
32 K			8.192 MHz	12.288 MHz	16.384 MHz
44.1			11.29 Mhz.	16.934 Mhz	22.58 Mhz.
48 K			12.288 Mhz.	18.432 MHz	24.5768 Mhz.
96 K			24.576 Mhz.	36.864 Mhz	
192 K	24.576 Mhz.	36.864 Mhz			

The chip included a 44.1 K de-emphasis filter. To enable the de-emphasis the pin 12, DEM, has to be pull high.

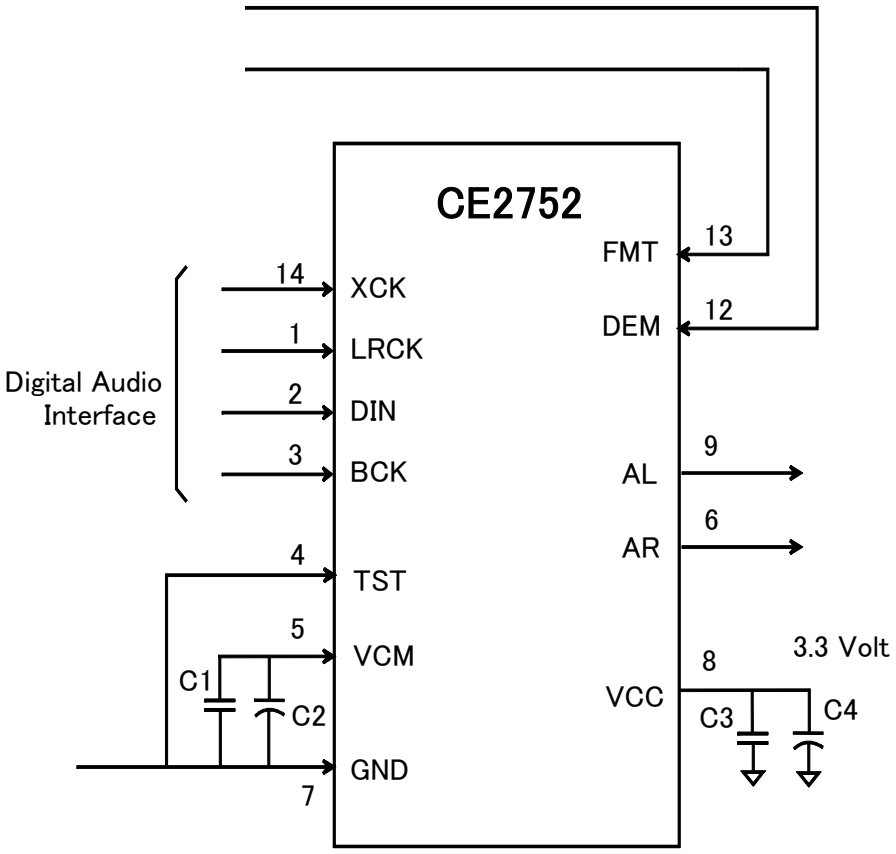
DIGITAL AUDIO SERIAL INTERFACE

The digital serial interface consists of a input data pin, DIN, and a serial clock input pin, BCK, and one left/right indicator input pin, LRCK. The data are 2's complement MSB first numbers. The CE2752 supports up to 24 bit resolution. The input can be either I2S or left justified input selected by the 'FMT' pin.

Figure 1. Audio Serial Input Data Timing Diagram



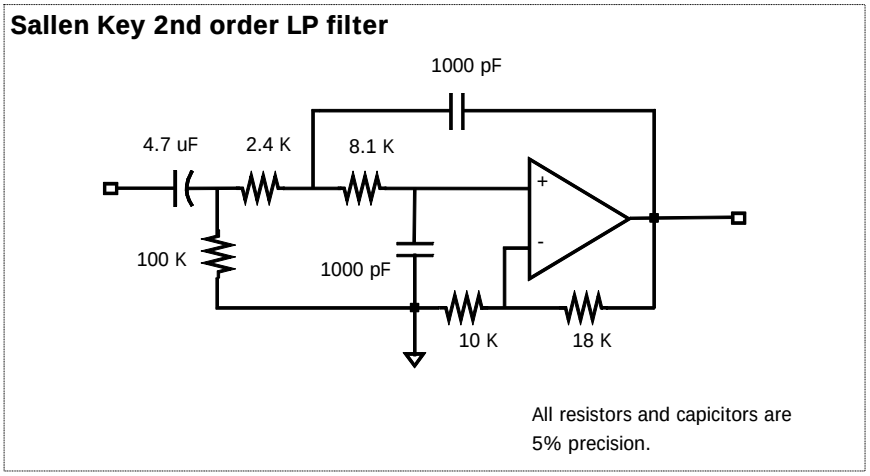
APPLICATION CONNECTION EXAMPLE:

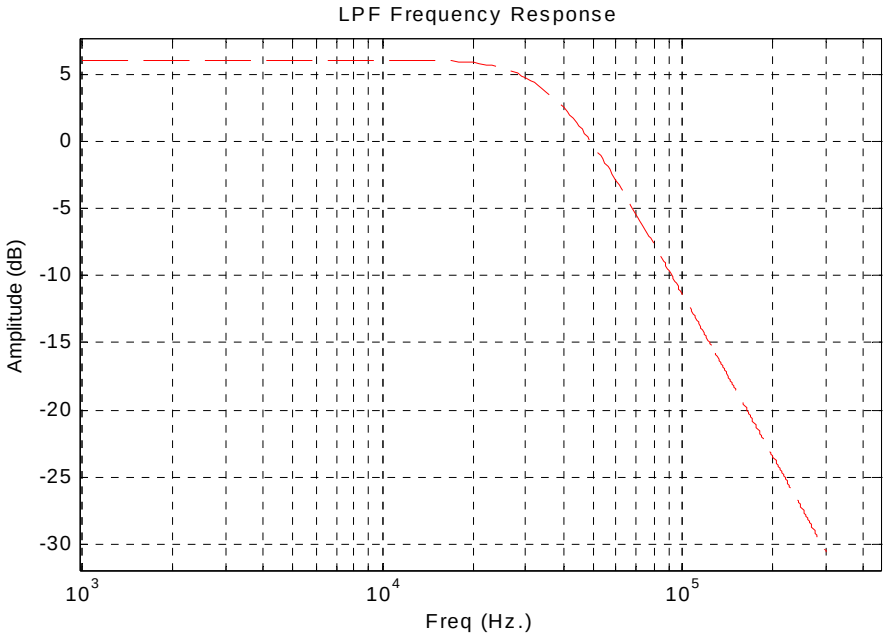


Note: C1 and C3 are 0.1 uF Capacitors
C2 and C4 are 10 uF Capacitors

SUGGESTED ANALOG RECONSTRUCTION FILTER

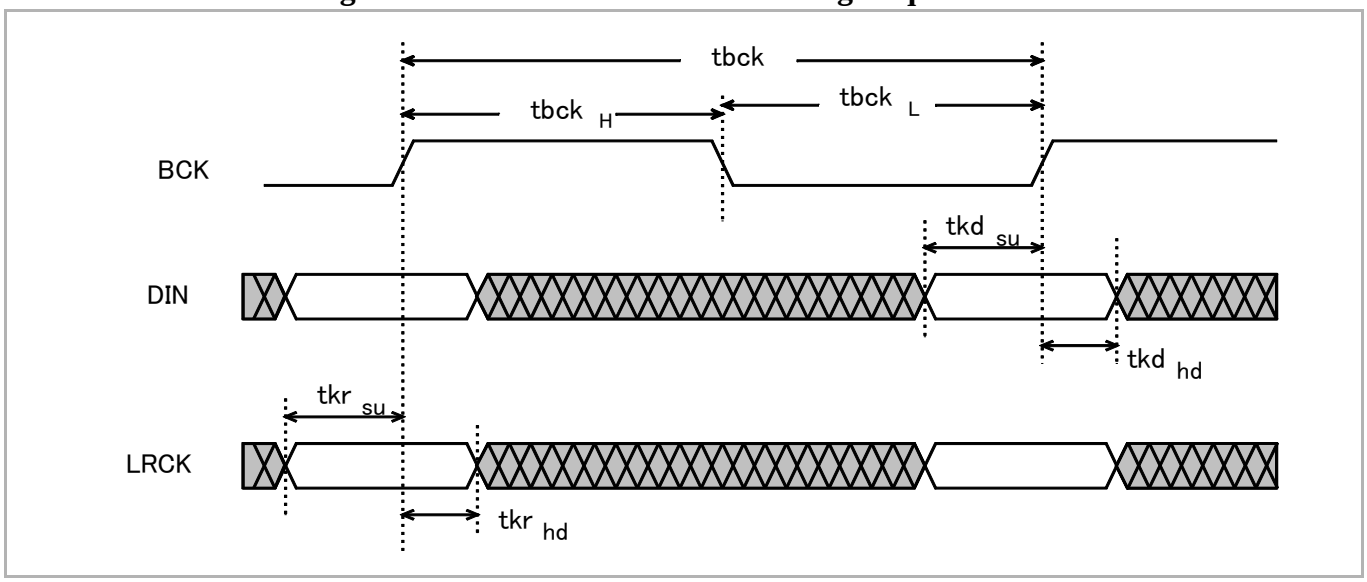
A second Sallen Key low pass reconstruction filter is recommend to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.





TIMING DIAGRAM

Figure 2. Audio Serial Interface Timing Requirement



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	6	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4" from pin)		280	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
Tstor	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
VDD	Power Supply Voltage	2.9	3.3	5	V
I_{DD}	Power Supply Current (VDD at 3.3 Volt)		20	23	mA
I_{DD}	Power Supply Current (VDD at 5 Volt)		27	30	mA
Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
V_{OL}	Digital Output Voltage, Logic LOW, (680 ohm pull up to 3.3 Volt)	0		0.8	V
Audio DAC Characteristics					
Full scale output	10 K load, 3.3 volt Vdd		0.71		Vrms
Passband ripple	0 to 0.46 fs (fs <= 96K)		0.02	0.04	dB
Out of band rejection	0.6 to 1 fs (fs <= 96K)	-60			dB
Reference Voltage					
Vref	Reference Voltage		VDD/2		V
Audio Serial Interface Timing					
tbck	BCK Cycle Time	100			ns
$tbck_H$	BCK Pulse Width, HIGH	50			ns
$tbck_L$	BCK Pulse Width, LOW	50			ns
tkd_{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	15			ns
tkd_{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr_{su}	Audio LRCK Setup Time With Respect To Rising Edge of BCK	15			ns

Parameter	Characteristics	Min	Typ	Max	Units
tkr_{hd}	Audio LRCK Hold Time With Respect To Rising Edge of BCK	15			ns

PACKAGING INFORMATION

Dimensions

	mm.				mm.		
	min	**norm**	**max**		**min**	**norm**	**max**
A	1.35		1.75	E1	3.8	3.9	4.0
A1	0.10		0.25	E2	5.8	6.0	6.2
b	0.33		0.51	e		1.27	
C	0.19		0.25	L	0.4	0.9	1.27
D	8.55	8.65	8.75				

14-Pin (SOIC 3.9 mm. wide body)