SILICON CONNECTIONS CORPORATION

PRELIMINARY

SC2001 - 4 X 4 X 20 BiCMOS CROSSBAR SWITCH

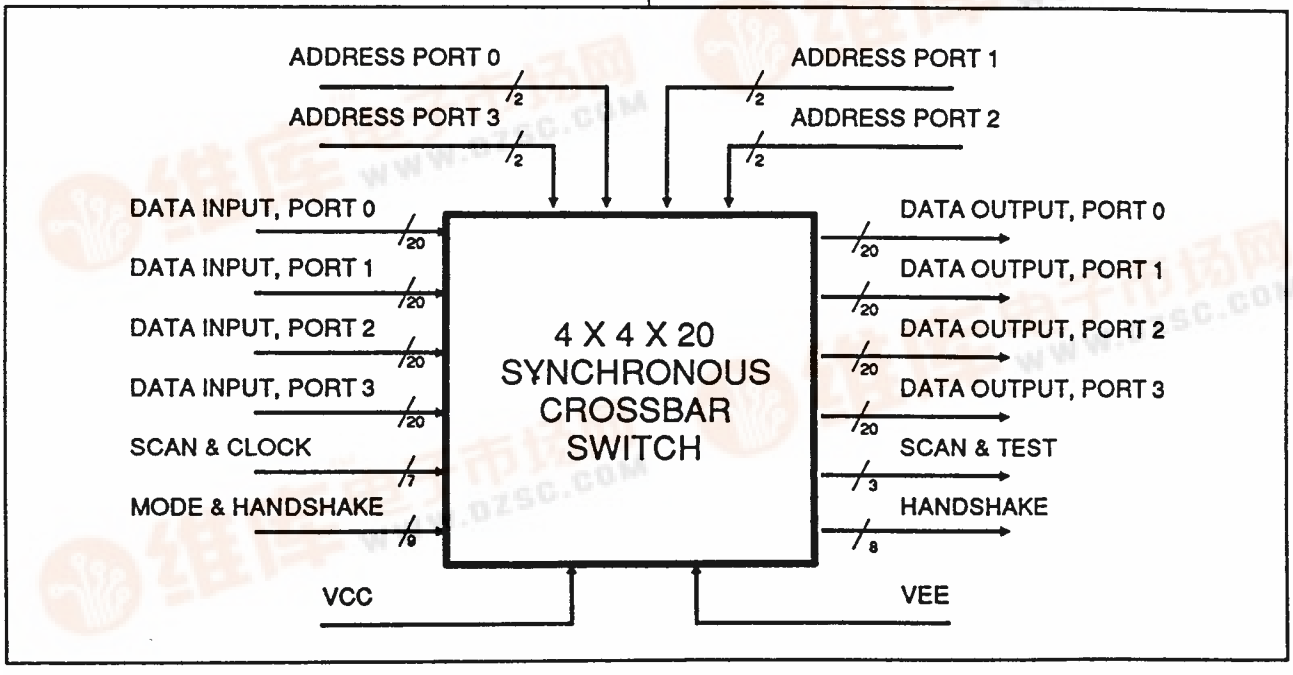
GENERAL DESCRIPTION

The SC2001 is a high speed (8 gigabits/sec) digital crossbar switch which provides simultaneous, multi-source to multi-destination, synchronous switching of data paths at up to 100 MHz (10 nS) cyclic rates.

Four independent input data ports, each 20 bits wide, are switched through to four 20-bit wide output ports during each cycle. Each of these input ports may be directed to as many as four output ports, but no output port may contain more than one input. Two modes of output port addressing are provided, either input port priority arbitration or direct output port address selection.

FEATURES

- 100 MHz Simultaneous Switching
- Four 20-bit input ports and four 20-bit output ports
- Port Addresses can change at 100 MHz
- Devices are cascadable
- Priority arbitration of input address request - or - direct "no arbitration" selection by output port
- Fully Clock Synchronous ECL I/O
- Low Power - 7.2 Watts @ 100 MHz
- Fully SCAN Testable
- 235 Pin PGA Package
- Advanced 1.2 micron BiCMOS Technology



Absolute Maximum Ratings

Storage Temperature ..... -55°C to +150°C
V_{EE} Potential to V_{CC} ..... -7.0V to +0.5V
Input Voltage (DC) ..... V_{EE} to V_{CC}
Maximum Junction Temperature .....+150 °C
Output Current (DC Output High) ..... -50 mA
Latch-up Current .....>200 mA
Static Discharge Voltage .....>2000 V

AC Test Conditions

Input Rise and Fall Times .....0.7 nS min
2.0 nS max
Timing Reference ..... 50% of Clock
AC Test Circuit .....Figure 1

Capacitance

Input Pin (C_{IN}) .....5.0 pF
Output Pin (C_{OUT}) ..... 8.0 pF

DC Electrical Characteristics

V_{EE} = -5.2V ±5%, V_{CC} = Ground, Outputs Terminated with 50 ohms to -2.0V

			T_C = 0°C		T_C = 75°C		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
V_{IH}	Input HIGH Voltage		-1.17		-1.07		Volts
V_{IL}	Input LOW Voltage			-1.48		-1.45	Volts
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(MAX)}$ or $V_{IL(MIN)}$	-1.00	-0.84	-0.92	-0.73	Volts
V_{OL}	Output LOW Voltage	V_{IN} = $V_{IH(MAX)}$ or $V_{IL(MIN)}$	-1.90	-1.60	-1.90	-1.60	Volts
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(MAX)}$		420		260	uA
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(MAX)}$	0.5		0.3		uA
I_{EE}	Power Supply Current	f_o = 100 MHz				1500	mA

Signal Names and Descriptions

Inputs

Description	Name
Data Inputs, Port 0 - 3, Bits 0 - 19	DI 0 - 3, 0 - 19
Address Port, 0 - 3, Address 0 - 3	AP 0 - 3, 0 - 1
Valid Input, Port 0 - 3	VI 0 - 3
Accepted Output, Port 0 - 3	AO 0 - 3
Mode Select	Mode
Differential System Clock	CLK and NCLK
SCAN Data Input	SCIN
SCAN Mode Select	SCMS 0 - 2
SCAN Clock Input	SCLK

Outputs

Description	Name
Data Output, Port 0 - 3, Bits 0 - 19	DO 0 - 3, 0 - 19
Valid Output, Port 0 - 3	VO 0 - 3
Input Taken, Port 0 - 3	IT 0 - 3
Differential Clock Test Point	TP and NTP
SCAN Data Output	SCOUT

Description of Operation

This VLSI circuit simultaneously switches four 20-bit wide input ports (In-ports) to four output ports (Out-ports) every clock cycle, up to 100 MHz.

Two different modes of operation are available to the user. The first is a "handshake" interface with simple priority arbitration logic to permit any or all requesting In-port addresses to contend for a single Out-port. When contention occurs, the highest priority In-port is selected and the other ports are held until a subsequent cycle(s) permits successful data transfer. The effect of a "stall" requires an interface handshake at both In-ports and Out-ports. When an In-port requesting address is presented, the requestor raises (HIGH) the "valid input" signal to the port. If and when the In-port is vacant, from a previous operation, the "Input Taken" signal will be asserted (HIGH) in response. Similarly at the Out-port, a HIGH "output accepted" signals that the output data has been taken, and the latch is free to accept new data. "Valid Output" (HIGH) indicates that the data on the output is "valid." This is useful during system start-up conditions. It should be noted that lack of acknowledgment or handshake at either In-port or Out-port will cause a stall in that selected path only.

The second mode of operation is without any path arbitration. The "port address" becomes the In-port address for each of the four Out-ports, e.g., a binary value of 01 applied to Port 3 address causes In-port 1 data to be directed to Out-port 3. No decision delay is involved. Note that any In-port data may be simultaneously routed to any and all Out-ports. This mode of operation is initiated by setting the "mode input" to "0" (LOW). While in this mode all "valid input" and "output accepted" signals should be held at "1" (HIGH). "Input Taken" will be LOW and "Valid Output" will be undefined after the first system clock.

All I/O operations are synchronous. This means all input data and control signals are immediately latched with the clock's HIGH to LOW transition. The output data and control signals are latched with the clock's LOW to HIGH transition. The user may view this crossbar logic as the intraconnect within a global set of master-slave flip flops; the inputs being the master half while the outputs are the slave half. **NOTE: All inputs must be stable within two nanoseconds after the trailing edge of the clock.** Outputs are one clock cycle delayed from the controlling inputs. Latches are provided on all inputs and outputs. The input latches are enabled when the internal clock is HIGH and the output latches are enabled when the internal clock is LOW.

For high performance operation (up to 100 MHz) the device requires differential clock inputs. For single ended clock versions please contact SCC. Details on the clock function are presented on page 10.

The device fully supports boundary and internal SCAN test. These SCAN tests maybe implemented at the user's discretion. Details on the SCAN functions are presented on page 11.

AC Timing Characteristics - No Priority Mode of Operation

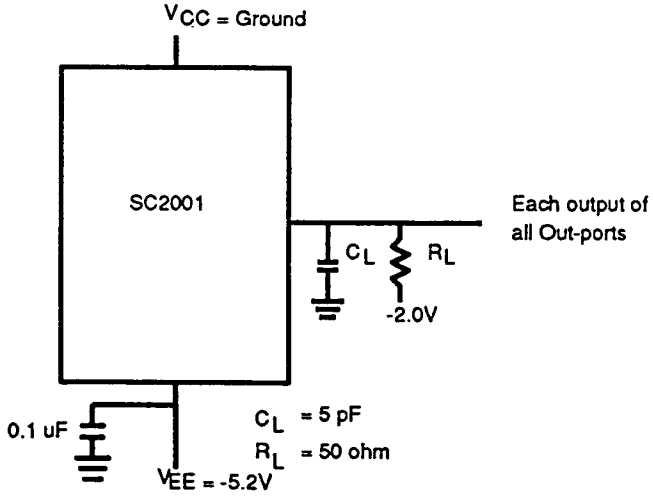
V_{EE} = -5.2V ±5%, V_{CC} = Ground, T_C = 0°C to + 75°C

Symbol	Parameter		SC2001-10 WORST CASE	SC2001-10 Typ	SC2001-13 WORST CASE	SC2001-13 Typ	Units
Tpd	Clock Cycle Period	Min	5.7	3.8	7.1	4.8	nS
Tpd(cas)	Clock Cycle Period when Cascaded	Min	10.2	6.7	12.8	8.4	nS
Tsi	Input Set-up Time	Min	2.0	1.3	2.5	1.6	nS
Thi	Input Hold Time	Min	4.0	2.6	5.0	3.2	nS
Tho	Data & Handshake Output Holdover	Min	2.0	1.3	2.5	1.6	nS
Tdio	Total Tsi to Tvd Delay (Late Input w.r.t. CLK)	Max	10.2	6.7	12.8	8.4	nS
Tvd	Data & Handshake Valid (Early Input w.r.t. CLK)	Max	7.0	4.6	8.8	5.8	nS

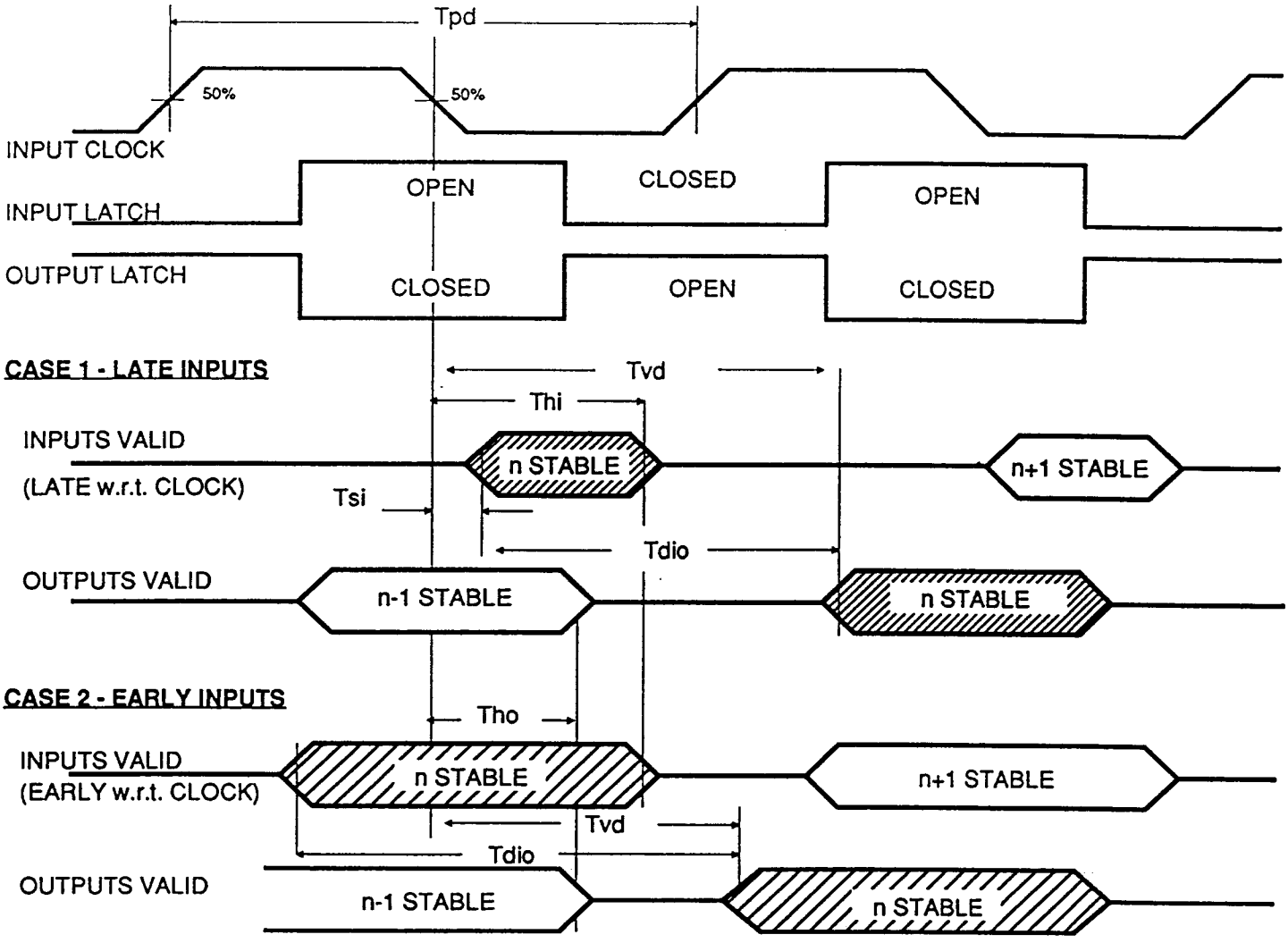
AC Timing Characteristics - Priority Mode of Operation

Tpd	Clock Cycle Period	Min	8.6	5.7	10.8	7.1	nS
Tpd(cas)	Clock Cycle Period when Cascaded	Min	11.2	8.5	13.5	10.6	nS
Tsi	Input Set-up Time	Min	2.0	1.3	2.5	1.6	nS
Thi	Input Hold Time	Min	4.0	2.6	5.0	3.2	nS
Tho	Data & Handshake Output Holdover	Min	2.0	1.3	2.5	1.6	nS
Tdio	Total Tsi to Tvd Delay (Late Input w.r.t. CLK)	Max	11.2	7.4	13.5	9.2	nS
Tvd	Data & Handshake Valid (Early Input w.r.t. CLK)	Max	7.0	4.6	8.8	5.8	nS

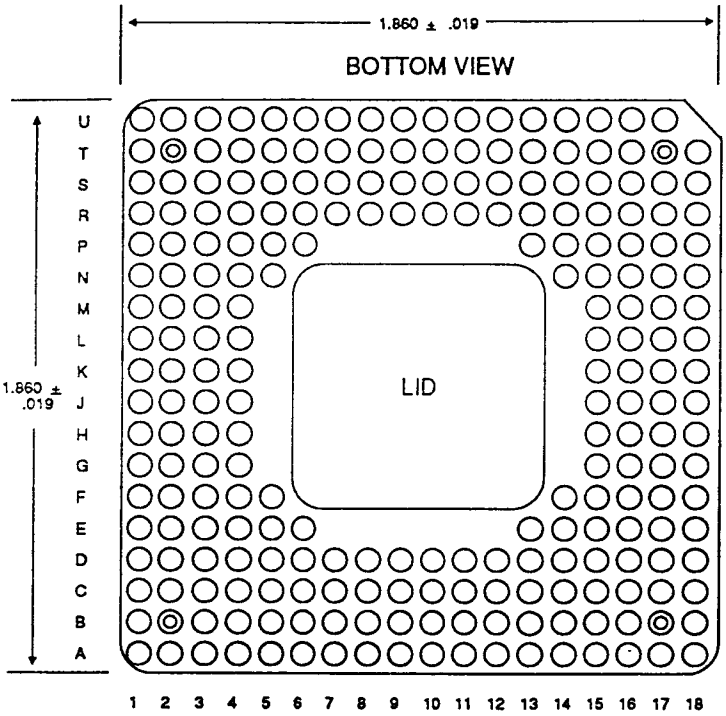
Figure 1 - AC Test Circuit

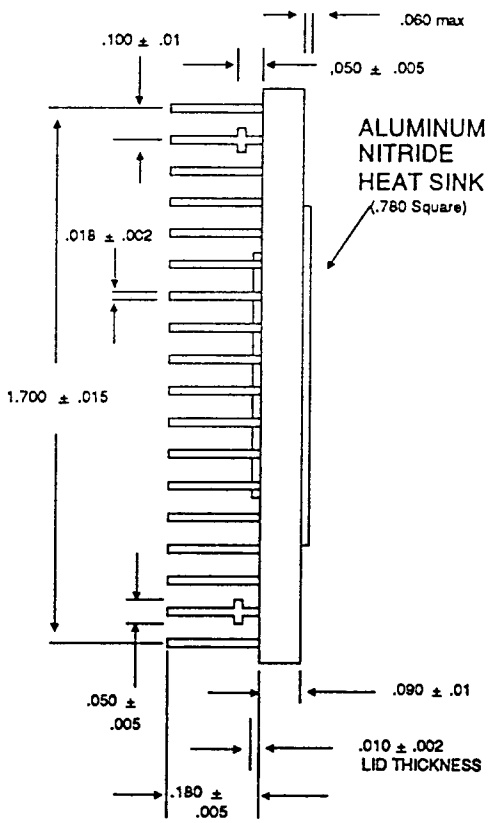


AC Timing


Tpd
50%
50%
INPUT CLOCK
INPUT LATCH
OPEN
CLOSED
OPEN
OUTPUT LATCH
CLOSED
OPEN
CLOSED
CASE 1 - LATE INPUTS
Tvd
Thi
INPUTS VALID
(LATE w.r.t. CLOCK)
n STABLE
n+1 STABLE
Tsi
Tdio
OUTPUTS VALID
n-1 STABLE
n STABLE
CASE 2 - EARLY INPUTS
Tho
INPUTS VALID
(EARLY w.r.t. CLOCK)
n STABLE
n+1 STABLE
Tvd
Tdio
OUTPUTS VALID
n-1 STABLE
n STABLE

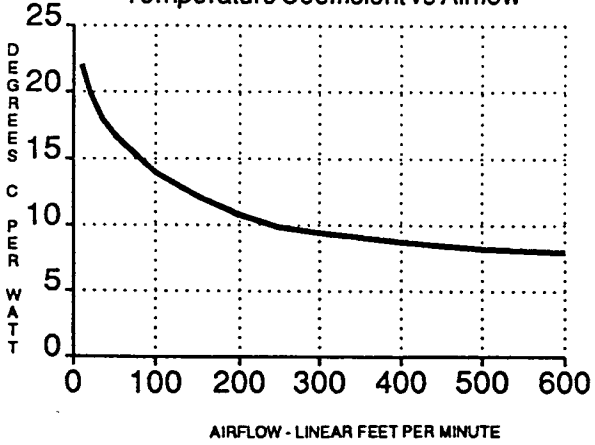
Package - 235 Pin PGA





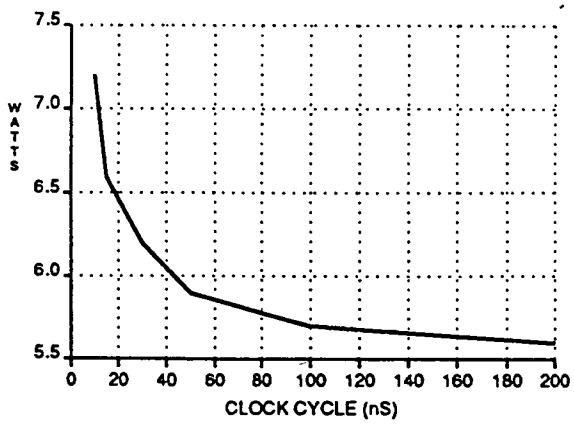
Thermal Characteristics

Temperature Coefficient vs Airflow



Power Dissipation

Power Dissipation vs Clock Frequency



Pinout

ROW A

COL 1	VALID INPUT-VI2	COL 6	DATA INPUT-DI2,14	COL 11	DATA INPUT-DI3,1	COL 16	DATA INPUT DI3,16
COL 2	DATA INPUT-DI2,2	COL 7	DATA INPUT-DI2,16	COL 12	DATA INPUT-DI3,3	COL 17	MODE SEL.-MODE
COL 3	DATA INPUT-DI2,6	COL 8	DATA INPUT-DI2,18	COL 13	DATA INPUT-DI3,5	COL 18	NOT CONNECTED
COL 4	DATA INPUT-DI2,10	COL 9	ADD. PORT-AP 3,1	COL 14	DATA INPUT-DI3,7		
COL 5	DATA INPUT-DI2,12	COL 10	ACCPT'D OUT-AO 3	COL 15	DATA INPUT-DI3,12		

ROW B

COL 1	ADD. PORT-AP 2,0	COL 6	DATA INPUT-DI2,5	COL 11	DATA INPUT-DI3,2	COL 16	DATA INPUT-DI3,18
COL 2	DATA OUT-DO 1,19	COL 7	DATA INPUT-DI2,11	COL 12	DATA INPUT-DI3,8	COL 17	DATA OUT-DO 0,16
COL 3	DATA INPUT-DI2,0	COL 8	DATA INPUT-DI2,15	COL 13	DATA INPUT-DI3,11	COL 18	CLOCK-CLK
COL 4	DATA INPUT-DI2,4	COL 9	ADD. PORT-AP 3,0	COL 14	DATA INPUT-DI3,10		
COL 5	DATA INPUT-DI2,8	COL 10	DATA INPUT-DI3,0	COL 15	DATA INPUT-DI3,14		

ROW C

COL 1	NCLCK TEST-NTP	COL 6	DATA INPUT-DI2,3	COL 11	DATA INPUT-DI3,6	COL 16	NOT CONNECTED
COL 2	CLCK TEST PT-TP	COL 7	DATA INPUT-DI2,9	COL 12	DATA INPUT-DI3,9	COL 17	DATA OUT-DO 0,9
COL 3	DATA OUT-DO 1,15	COL 8	DATA INPUT-DI2,13	COL 13	DATA INPUT-DI3,13	COL 18	SCAN CLOCK-SCLK
COL 4	NO CONNECTION	COL 9	DATA INPUT-DI2,19	COL 14	DATA INPUT-DI3,15		
COL 5	DATA INPUT-DI2,1	COL 10	VALID INPUT-VI3	COL 15	NOT CLOCK-NCLK		

ROW D

COL 1	DATA OUT-DO 1,16	COL 6	VEE	COL 11	DATA INPUT-DI3,4	COL 16	DATA OUT-DO 0,13
COL 2	DATA OUT-DO 1,18	COL 7	DATA INPUT-DI2,7	COL 12	VCC	COL 17	DATA OUT-DO 0,19
COL 3	DATA OUT-DO 1,12	COL 8	VCC	COL 13	DATA INPUT-DI3,17	COL 18	DATA OUT-DO 0,17
COL 4	DATA OUT-DO 1,17	COL 9	DATA INPUT-DI2,17	COL 14	DATA INPUT-DI3,19		
COL 5	ACCPT'D OUT-AO 2	COL 10	VEE	COL 15	DATA OUR-DO 0,18		

ROW E

COL 1	DATA OUT-DO 1,11	COL 4	DATA OUT-DO 1,14	COL 13	VEE	COL 16	DATA OUT-DO 0,11
COL 2	DATA OUT-DO 1,13	COL 5	VCC	COL 14	VCC	COL 17	DATA OUT-DO 0,14
COL 3	DATA OUT-DO 1,10	COL 6	ADD. PORT-AP 2,1	COL 15	DATA OUT-DO 0,15	COL 18	DATA OUT-DO 0,12

ROW F

COL 1	DATA OUT-DO 1,7	COL 4	VCC	COL 15	VCC	COL 18	DATA OUT-DO 0,8
COL 2	DATA OUT-DO 1,9	COL 5	VEE	COL 16	DATA OUT-DO 0,7		
COL 3	DATA OUT-DO 1,8	COL 14	VEE	COL 17	DATA OUT-DO 0,10		

ROW G

COL 1	DATA OUT-DO 1,3	COL 3	DATA OUT-DO 1,6	COL 15	VEE	COL 17	DATA OUT-DO 0,6
COL 2	DATA OUT-DO 1,5	COL 4	VEE	COL 16	DATA OUT-DO 0,5	COL 18	DATA OUT-DO 0,4

ROW H

COL 1	DATA OUT-DO 1,2	COL 3	DATA OUT-DO 1,4	COL 15	VCC	COL 17	DATA OUT-DO 0,3
COL 2	DATA OUT-DO 1,1	COL 4	VCC	COL 16	DATA OUT-DO 0,2	COL 18	DATA OUT-DO 0,1

ROW J

COL 1	DATA OUT-DO 1,0	COL 3	VALID OUTPUT-VO 1	COL 15	VEE	COL 17	DATA OUT-DO 0,0
COL 2	DATA OUT-DO 2,19	COL 4	VEE	COL 16	INPUT TAKEN-IT 0	COL 18	VALID OUTPUT-VO 0

Pinout (continued)

ROW K

COL 1	INPUT TAKEN - IT 1	COL 3	VEE	COL 15	VCC	COL 17	DATA OUT - DO 3,18
COL 2	DATA OUT - DO 2,18	COL 4	VCC	COL 16	DATA OUT - DO 3,19	COL 18	DATA OUT - DO 3,17

ROW L

COL 1	DATA OUT - DO 2,17	COL 3	DATA OUT - DO 2,13	COL 15	VCC	COL 17	DATA OUT - DO 3,16
COL 2	DATA OUT - DO 2,15	COL 4	VCC	COL 16	DATA OUT - DO 3,14	COL 18	DATA OUT - DO 3,15

ROW M

COL 1	DATA OUT - DO 2,16	COL 3	DATA OUT - DO 2,9	COL 15	VCC	COL 17	DATA OUT - DO 3,11
COL 2	DATA OUT - DO 2,11	COL 4	VCC	COL 16	DATA OUT - DO 3,12	COL 18	DATA OUT - DO 3,13

ROW N

COL 1	DATA OUT - DO 2,14	COL 4	VEE	COL 15	DATA OUT - DO 3,5	COL 18	DATA OUT - DO 3,9
COL 2	DATA OUT - DO 2,10	COL 5	DATA OUT - DO 2,2	COL 16	DATA OUT - DO 3,10		
COL 3	DATA OUT - DO 2,7	COL 14	VEE	COL 17	DATA OUT - DO 3,7		

ROW P

COL 1	DATA OUT - DO 2,12	COL 4	VALID OUTPUT - VO 2	COL 13	DATA INPUT - DI 1,17	COL 16	DATA OUT - DO 3,8
COL 2	DATA OUT - DO 2,6	COL 5	VCC	COL 14	VCC	COL 17	DATA OUT - DO 3,2
COL 3	DATA OUT - DO 2,5	COL 6	VEE	COL 15	DATA OUT - DO 3,3	COL 18	DATA OUT - DO 3,4

ROW R

COL 1	DATA OUT - DO 2,8	COL 6	DATA INPUT - DI 0,3	COL 11	VCC	COL 16	DATA OUT - DO 3,6
COL 2	DATA OUT - DO 2,1	COL 7	VCC	COL 12	DATA INPUT - DI 1,9	COL 17	VALID OUTPUT - VO 3
COL 3	DATA OUT - DO 2,4	COL 8	DATA INPUT - DI 0,12	COL 13	VEE	COL 18	DATA OUT - DO 3,1
COL 4	SCAN INPUT - SCIN	COL 9	VEE	COL 14	DATA INPUT - DI 1,19		
COL 5	ACCPT'D OUT. - AO 0	COL 10	ACCPT'D OUT. - AO 1	COL 15	INPUT TAKEN - IT 3		

ROW S

COL 1	DATA OUT - DO 2,3	COL 6	DATA INPUT - DI 0,7	COL 11	DATA INPUT - DI 1,5	COL 16	DATA OUT - DO 3,0
COL 2	INPUT TAKEN - IT 2	COL 7	DATA INPUT - DI 0,8	COL 12	DATA INPUT - DI 1,7	COL 17	NOT CONNECTED
COL 3	ADD. PORT - AP 0,1	COL 8	DATA INPUT - DI 0,14	COL 13	DATA INPUT - DI 1,13	COL 18	SCAN MODE - SCMS 0
COL 4	DATA INPUT - DI 0,1	COL 9	DATA INPUT - DI 0,18	COL 14	DATA INPUT - DI 1,15		
COL 5	DATA INPUT - DI 0,5	COL 10	ADD. PORT - AP 1,1	COL 15	SCAN MODE - SCMS 1		

ROW T

COL 1	DATA OUT - DO 2,0	COL 6	DATA INPUT - DI 0,9	COL 11	DATA INPUT - DI 1,3	COL 16	DATA INPUT - DI 1,16
COL 2	NOT CONNECTED	COL 7	DATA INPUT - DI 0,10	COL 12	DATA INPUT - DI 1,11	COL 17	NOT CONNECTED
COL 3	ADD. PORT - AP 0,0	COL 8	DATA INPUT - DI 0,16	COL 13	DATA INPUT - DI 1,4	COL 18	SCAN MODE - SCMS 2
COL 4	DATA INPUT - DI 0,0	COL 9	ADD. PORT - AP 1,0	COL 14	DATA INPUT - DI 1,8		
COL 5	DATA INPUT - DI 0,4	COL 10	DATA INPUT - DI 1,1	COL 15	DATA INPUT - DI 1,12		

ROW U

COL 1	SCAN OUT - SCOUT	COL 6	DATA INPUT - DI 0,11	COL 11	VALID INPUT - VI 1	COL 16	DATA INPUT - DI 1,14
COL 2	NOT CONNECTED	COL 7	DATA INPUT - DI 0,13	COL 12	DATA INPUT - DI 1,0	COL 17	DATA INPUT - DI 1,18
COL 3	VALID INPUT - VI 0	COL 8	DATA INPUT - DI 0,15	COL 13	DATA INPUT - DI 1,2		
COL 4	DATA INPUT - DI 0,2	COL 9	DATA INPUT - DI 0,17	COL 14	DATA INPUT - DI 1,6		
COL 5	DATA INPUT - DI 0,6	COL 10	DATA INPUT - DI 0,19	COL 15	DATA INPUT - DI 1,10		

Pinout (Listed by Signal Function)

DATAINPUTS

DI 0,0 ..... T4	DI 0,1 ..... S4	DI 0,2 ..... U4	DI 03 ..... R6	DI 0,4 ..... T5	DI 0,5 ..... S5
DI 0,6 ..... U5	DI 0,7 ..... S6	DI 0,8 ..... S7	DI 0,9 ..... T6	DI 0,10 ..... T7	DI 0,11 ..... U6
DI 0,12 ..... R8	DI 0,13 ..... U7	DI 0,14 ..... S8	DI 0,15 ..... U8	DI 0,16 ..... T8	DI 0,17 ..... U9
DI 0,18 ..... S9	DI 0,19 ..... U10				
DI 1,0 ..... U12	DI 1,1 ..... T10	DI 1,2 ..... U13	DI 1,3 ..... T11	DI 1,4 ..... T13	DI 1,5 ..... S11
DI 1,6 ..... U14	DI 1,7 ..... S12	DI 1,8 ..... T14	DI 1,9 ..... R12	DI 1,10 ..... U15	DI 1,11 ..... T12
DI 1,12 ..... T15	DI 1,13 ..... S13	DI 1,14 ..... U16	DI 1,15 ..... S14	DI 1,16 ..... T16	DI 1,17 ..... P13
DI 1,18 ..... U17	DI 1,19 ..... R14				
DI 2,0 ..... B3	DI 2,1 ..... C5	DI 2,2 ..... A2	DI 2,3 ..... C6	DI 2,4 ..... B4	DI 2,5 ..... B6
DI 2,6 ..... A3	DI 2,7 ..... D7	DI 2,8 ..... B5	DI 2,9 ..... C7	DI 2,10 ..... A4	DI 2,11 ..... B7
DI 2,12 ..... A5	DI 2,13 ..... C8	DI 2,14 ..... A6	DI 2,15 ..... B8	DI 2,16 ..... A7	DI 2,17 ..... D9
DI 2,18 ..... A8	DI 2,19 ..... C9				
DI 3,0 ..... B10	DI 3,1 ..... A11	DI 3,2 ..... B11	DI 3,3 ..... A12	DI 3,4 ..... D11	DI 3,5 ..... A13
DI 3,6 ..... C11	DI 3,7 ..... A14	DI 3,8 ..... B12	DI 3,9 ..... C12	DI 3,10 ..... B14	DI 3,11 ..... B13
DI 3,12 ..... A15	DI 3,13 ..... C13	DI 3,14 ..... B15	DI 3,15 ..... C14	DI 3,16 ..... A16	DI 3,17 ..... D13
DI 3,18 ..... B16	DI 3,19 ..... D14				

DATAOUTPUTS

DO 0,0 ..... J17	DO 0,1 ..... H18	DO 0,2 ..... H16	DO 0,3 ..... H17	DO 0,4 ..... G18	DO 0,5 ..... G16
DO 0,6 ..... G17	DO 0,7 ..... F16	DO 0,8 ..... F18	DO 0,9 ..... C17	DO 0,10 ..... F17	DO 0,11 ..... E16
DO 0,12 ..... E18	DO 0,13 ..... D16	DO 0,14 ..... E17	DO 0,15 ..... E15	DO 0,16 ..... B17	DO 0,17 ..... D18
DO 0,18 ..... D15	DO 0,19 ..... D17				
DO 1,0 ..... J1	DO 1,1 ..... H2	DO 1,2 ..... H1	DO 1,3 ..... G1	DO 1,4 ..... H3	DO 1,5 ..... G2
DO 1,6 ..... G3	DO 1,7 ..... F1	DO 1,8 ..... F3	DO 1,9 ..... F2	DO 1,10 ..... E3	DO 1,11 ..... E1
DO 1,12 ..... D3	DO 1,13 ..... E2	DO 1,14 ..... E4	DO 1,15 ..... C3	DO 1,16 ..... D1	DO 1,17 ..... D4
DO 1,18 ..... D2	DO 1,19 ..... B2				
DO 2,0 ..... T1	DO 2,1 ..... R2	DO 2,2 ..... N5	DO 2,3 ..... S1	DO 2,4 ..... R3	DO 2,5 ..... P3
DO 2,6 ..... P2	DO 2,7 ..... N3	DO 2,8 ..... R1	DO 2,9 ..... M3	DO 2,10 ..... N2	DO 2,11 ..... M2
DO 2,12 ..... P1	DO 2,13 ..... L3	DO 2,14 ..... N1	DO 2,15 ..... L2	DO 2,16 ..... M1	DO 2,17 ..... L1
DO 2,18 ..... K2	DO 2,19 ..... J2				
DO 3,0 ..... S16	DO 3,1 ..... R18	DO 3,2 ..... P17	DO 3,3 ..... P15	DO 3,4 ..... P18	DO 3,5 ..... N15
DO 3,6 ..... R16	DO 3,7 ..... N17	DO 3,8 ..... P16	DO 3,9 ..... N18	DO 3,10 ..... N16	DO 3,11 ..... M17
DO 3,12 ..... M16	DO 3,13 ..... M18	DO 3,14 ..... L16	DO 3,15 ..... L18	DO 3,16 ..... L17	DO 3,17 ..... K18
DO 3,18 ..... K17	DO 3,19 ..... K16				

ADDRESSPORTS

AP 0,0 ..... T3	AP 0,1 ..... S3	AP 1,0 ..... T9	AP 1,1 ..... S10	AP 2,0 ..... B1	AP 2,1 ..... E6
AP 3,0 ..... B9	AP 3,1 ..... A9				

HANDSHAKESIGNALS

VI 0 ..... U3	VI 1 ..... U11	VI 2 ..... A1	VI 3 ..... C10	AO 0 ..... R5	AO 1 ..... R10
AO 2 ..... D5	AO 3 ..... A10	VO 0 ..... J18	VO 1 ..... J3	VO 2 ..... P4	VO 3 ..... R17
IT 0 ..... J16	IT 1 ..... K1	IT 2 ..... S2	IT 3 ..... R15		

CLOCK AND CONTROL

MODE A17	CLK B18	NCLK C15

SCAN AND TEST

SCIN R4	SCMS 0 ..... S18	SCMS 1 ..... S15	SCMS 2 ..... T18	SCLK C18	TP C2
NTP C1	SCOUT U1				

VCC AND VEE

VCC D8	VCC D12	VCC E14	VCC F15	VCC H15	VCC L15
VCC K15	VCC M15	VCC P14	VCC R11	VCC R7	VCC P5
VCC M4	VCC K4	VCC L4	VCC H4	VCC F4	VCC E5
VEE D6	VEE D10	VEE E13	VEE F14	VEE J15	VEE G15
VEE N14	VEE R13	VEE R9	VEE P6	VEE N4	VEE K3
VEE J4	VEE G4	VEE F5			

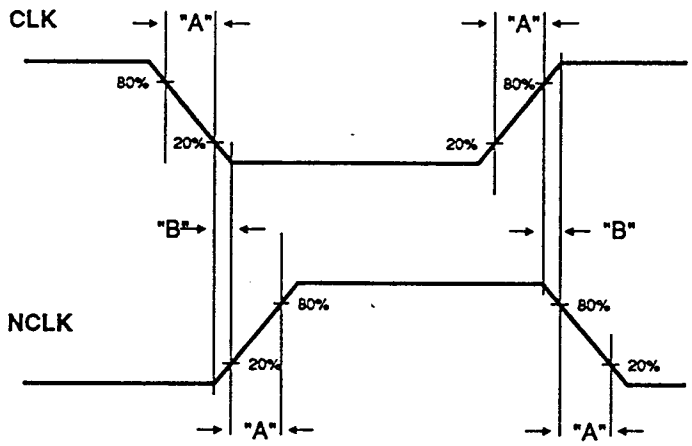
SYSTEM CLOCK FUNCTION

The crossbar switch's clock input (CLK and NCLK) is a differential pair that must maintain certain symmetries and duty factors. A 50%-50% duty factor is recommended but factors up to 20%-80% may be used if a minimum of 5.0 nS is apportioned to all clock pulse periods. Additionally, CLK's and NCLK's rising and falling edges must overlap by a minimum of 0.5 nS. TRISE and TFALL must be less than 2.0 nS. Please see Figure 2.

The system clock must be stopped for SCAN functions. The device does support single cycle operations.

Additionally, the device provides a clock monitoring test point (TP and NTP). This is a nominally loaded, internal final clock distribution branch which is available for use in measuring and "de-skewing" clocks at the board level.

Figure 2 - Clock Symmetry and Overlap



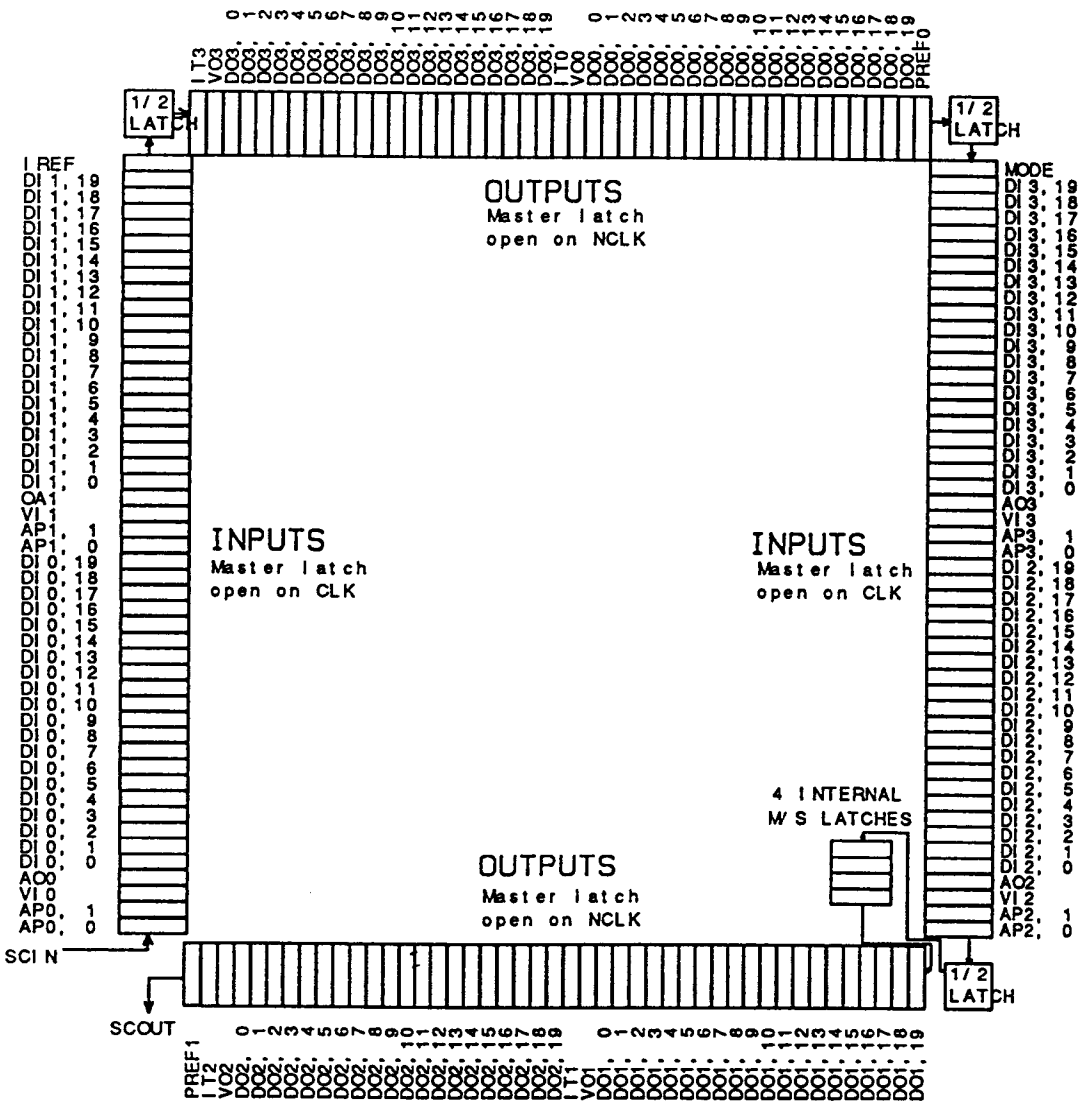
"A" = TRISE OR TFALL, 20% to 80% = 2.0 nS Maximum
"B" = TRISE and TFALL Overlap = 0.5 nS Minimum

SCAN FUNCTIONS

Each of SCC's leadership products has full boundary, I/O pad and internal SCAN circuitry built-in. Boundary and internal SCAN testing is available at the packaged device level. It's use is completely optional.

SCAN Chain Order

The SCAN Chain begins at the SCIN Pin with AP 0,0 and ends with PREF1 at the SCOUT Pin.



Note: PREF0, PREF1, and IREF are unbonded signals used for wafer test only.

Output latches contain inverted data, i.e. if DOX latch contains a "0" then DOX signal pin will be a "1".

SCAN FUNCTIONS (continued)

SCAN Clock - SCLK

SCAN clock is a single ended, low speed clock used to replace system clock when the device is in a SCAN mode of operation. SCAN mode is initiated when SCMS> 0. **NOTE: Switching between system clock (CLK) and SCAN Clock (SCLK) must only occur with both clock sources in the false or "not" state.** The SCAN clock (SCLK) can run from D.C. to a maximum of 10 MHz.

SCAN Input - SCIN

SCAN input is a serial input data shift path. It is enabled by the appropriate SCMS selection.

SCAN Output - SCOUT

SCAN output is a serial output data shift path. It is enabled by the appropriate SCMS selection.

SCAN Mode Select - SCMS (x,x,x)

These three inputs are decoded to provide SCAN mode selection as defined below:

SCMS (0,0,0) = 0	Normal device operation. All SCAN functions disabled.
SCMS (0,0,1) = 1	Reserved - performance monitor
SCMS (0,1,0) = 2	Reserved - pad SCAN
SCMS (0,1,1) = 3	SCAN input (SCIN) to SCAN output (SCOUT) - a serpentine shift through all scan flip flops.
SCMS (1,0,0) = 4	Reserved - pad SCAN
SCMS (1,0,1) = 5	Reserved
SCMS (1,1,0) = 6	Reserved
SCMS (1,1,1) = 7	SCAN path bypass - SCAN input to SCAN output

Ordering Codes

Package Type	Part Number
Ceramic Pin Grid Array	SC2001G-10/13

Order Placement

Silicon Connections Corporation

Attention: Order Entry

6160 Lusk Blvd., Suite C-204

San Diego, CA 92121

Phone: 619-535-0442

FAX: 619-535-1635