FOCUS enhancements
superior video technology

FS401, FS402, FS403 PC to TV Video Scan Converters

Features

- Frame rate Conversion †
- Programmable 2D scaling †
- Pan and Zoom †
- Advanced 2-D flicker filter †
- Frame-store memory controller
- Supports Multiple Progressive Input Resolutions †

–Minimum 640x 400
–Maximum 2048 x 1536

- Supports Interlaced Input

–XGA and above

- Input refresh rates up to 150Hz
- Multiple Output Standards

–NTSC, NTSC-EIAJ, PAL-B/G/H/I †
–Composite, S-Video, SCART
–RGB, YUV

▪Standard NTSC and PAL
▪Super NTSC & PAL
▪VGA Progressive
▪SVGA Progressive
▪NTSC Progressive
▪PAL 100Hz Interlaced

- Automatically detects input active video area
- Automatically selects the best output and scaling for any input resolution
- Programmable sharpness, brightness, contrast and color saturation
- Customizable On Screen Display via glueless integration with Freescale, Zilog and Philips OSD Microprocessors (FS403)
- C, H, and V Sync tri-state outputs
- H and V Sync monitoring for DPMS Support
- Exceeds all PC97 and PC98 requirements
- General Purpose Output Pins (2 on FS401 & FS402, 7 on FS403)
- Genlock (FS403)
- 8-bit A/D converters with frequency adaptive input filtering support
- 10-bit output D/A converters
- Digital RGB Inputs (FS403)
- Macrovision 7 compliant (FS402)
- $I^2C^{\ddagger}$ compatible port controls (SIO)
- 100 pin PQFP (FS401, FS402)
- 128 pin PQFP (FS403)
- 3.3V operation

†Note: Covered under US Patent # 5,862,268, # 5,905,536, # 5,966,184 and/or patents pending.

Description

The FS400 family is a fourth generation video scan converter. It accepts many input resolutions and rates and converts them to NTSC or PAL standards compliant with SMPTE-170M and CCIR-656 standards. Also available as output options are VGA 640 x 480 at 60Hz progressive, SVGA 800 x 600 at 60Hz progressive, and 100 Hz interlaced. The chip has a programmable down scaler to fit the incoming resolution to the output display format. Within the FS400 are capture and encoder engines separated by the frame buffer memory controller. Required external components are minimal: a single 16M SDRAM memory, clocks and passive parts.

Analog progressive RGB inputs are digitized and converted to the YUV 4:2:2 format. Vertical scaling and flicker filtering are implemented at the computer frame rate ahead of the frame store interface.

Interlaced input is supported for XGA resolution and above. In this mode, only the first field is processed.

The Flicker Filter is an advanced 2 dimensional filter that enhances text quality. Flicker Filter parameters are programmable to allow user tradeoffs between flicker and sharpness.

The FS400 family contains controls for programmable sharpness, brightness, contrast, and color saturation. These controls allow output to be tuned to match user desires and tastes.

Frame rate conversion is implemented by a Frame Store Controller that interfaces with an external SDRAM frame store memory.

YUV 4:2:2 data is recovered from the memory at the outgoing frame rate. Data is scaled prior to the digital video encoder that generates Y/C and Composite Video outputs. For RGB and YUV outputs, the

encoder may be bypassed via a YUV to RGB transcoder for SCART compatible video, and for output to VGA or SVGA displays.

The FS400 has built in capability to automatically detect the incoming video mode and automatically select optimal sampling and scaling parameters. The chip can detect the location of the active video in the input, and can automatically center the input on the TV screen. All parameters can be read and written via the SIO serial port.

The FS403 has support for glueless integration with Zilog and Philips On Screen Display (OSD) microcontrollers. The OSD interface allows a customized on screen user interface that can contain opaque or halftone video backgrounds.

The FS403 has direct digital inputs, bypassing the built-in ADCs.

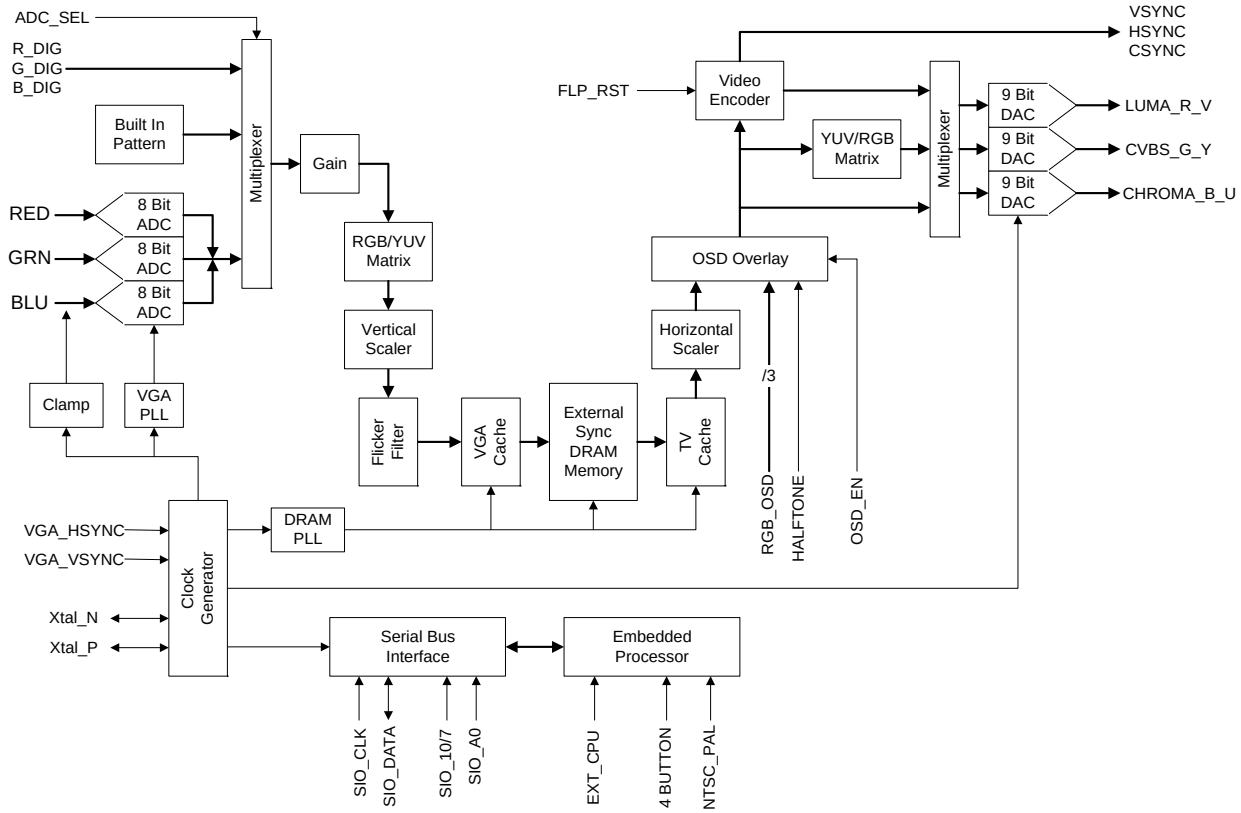
The FS402 incorporates Macrovision 7 anti copy protection technology.

Power is derived from +3.3V digital and analog supplies. Packages are 100-lead (FS401 and FS402) or 128-lead (FS403) Plastic Quad Flat Pack (PQFP).

Applications

- PC video out
- PC ready TV's
- Video Text Displays
- Web Appliances
- PC-to-TV Scan Converter Peripherals
- Video Kiosks

Architectural Block Diagram



Contents

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1. Architectural Overview

Overall design principles are included in this section. Details of how to use and setup the FS400 are included in the ***Error! Reference source not found.*** section, FS400 Product Specification

RGB video inputs are asynchronously converted to either NTSC/PAL, YUV or RGB video formats. Architecturally, the FS400 is divided into five major sections:

1. Video Capture Engine
2. Clock Processor
3. Frame Store Controller
4. Video Encoder Engine
5. Serial Bus Interface

Besides power and a few external passive components, the FS400 requires only a single 16M external SDRAM and external clocks to implement a high quality video scan converter.

Either analog or digital inputs (FS403 only) with separate horizontal and vertical sync signals are accepted. Analog VGA video must be RGB. Digital video (FS403 only) must be 24-bit RGB clocked by external clock, VGACK_IN.

A wide range of resolution formats can be accepted, including common standards such as 320x240, 640x400, 720x400, 640x480, 800x600, 832x624, 1024x768, 1152x864, 1280x1024, and 1600x1200. Incoming RGB signals are converted to either the NTSC or PAL TV Standards, 100Hz PAL, or progressive scan VGA, SVGA, or NTSC. Output video format can be selected to be either composite and Y/C (NTSC and PAL only), or RGB or YUV (all standards).

Incoming frame rate may range to over 150 Hz according to the table below. The Video Capture engine runs asynchronously relative to the Video Encoder Engine. An external frame store memory separates the two engines with write and read access controlled by the FS400.

Transformation operations include overscan, underscan, pan and zoom. Scaling operations are separated by the frame store with vertical down-sampling incorporated into the Capture Engine and horizontal up-sampling incorporated into the Encoder Engine.

1.1 Video Capture Engine

Triple 8-bit A/D converters digitize the analog RGB inputs at rates of up to 50 MHz. Internal A/D sample clock, ADCK is derived from a phase locked loop referenced to the leading edge of horizontal sync. Either positive or negative sync polarity is accepted.

The selected input (A/D converter outputs or digital RGB) is transcoded by the color matrix into a 16-bit YC_RC_B 4:2:2 format. A vertical scaler filters the number of incoming video lines by the selected scaling factor. A flicker filter averages lines to eliminate flicker between lines or boundaries.

The Video Capture Engine is programmable as to the number of horizontal samples it takes. The limiting factor in the sample rate is the A/D Converters. By programming fewer samples per line, higher incoming data rates can be accommodated. The following table illustrates the capability:

Active Samples	**720 CCIR 601**	**640**	**500**
Maximum Line Frequency	56kHz	63kHz	80kHz
640 x 480	106Hz	119Hz	152Hz
800 x 600	89Hz	100Hz	128Hz
1024 x 768	70Hz	78Hz	100Hz
1152 x 864	59Hz	66Hz	85Hz
1280 x 1024	53Hz	59Hz	76Hz
1600 x 1200	44Hz	50Hz	64Hz

1.2 Frame Store Memory Controller

Inserted between the capture and the encoder engines the frame store has two functions: 1) to act as a reservoir of pixels to match the incoming frame rate to the outgoing field or frame rate; 2) to support vertical scaling by allowing lines to be written into the frame store intermittently, but read out at a constant rate.

Frame store clock, FS_CK is derived from the OSC1 clock by a second phase locked loop.

1.3 Video Encoder Engine

Pixels are retrieved from the external frame store memory asynchronously relative to the incoming frames. Outgoing video timing is set to the selected TV (NTSC or PAL) or progressive scan standard.

Incoming data sampling is normally set to fill complete lines in the Frame Store Memory. Horizontal scaling is applied to pixels exiting the Frame Store. Pixels may be routed through either a digital video encoder or a YC_RC_B-to-RGB transformation matrix. Either output is connected to a triple 10-bit D/A converter to generate the video output that may be Composite Video and Y/C, RGB or YUV.

Encoder Engine timing is derived from many clock sources. These standards are shown below.

Encoder Standard	Total Pixels	Total Lines	Vertical Mode	Clock Rate	Line Freq.
NTSC	910	525	60I	14.318 MHz	15.73 KHz
PAL	1135.0064	625	50I	17.734 MHz	15.62 KHz
RGB NTSC	910	525	60I	14.318 MHz	15.73 KHz
RGB PAL	1135	625	50I	17.734 MHz	15.62 KHz
Super RGB NTSC	1280	525	60I	20.140 MHz	15.73 KHz
Super RGB PAL	1280	625	50I	20.000 MHz	15.62 KHz
VGA	800	525	60P	25.175 MHz	31.5 KHz
SVGA	1024	625	60P	38.400 MHz	37.5 KHz
Progressive NTSC	910	525	60P	28.636 MHz	31.5 KHz
100Hz PAL	1135	625	100I	35.468 MHz	31.25 KHz

1.4 Serial Control Port

FS400 setup is programmed by 39 16-bit registers that are accessible via the $I^2C^{\ddagger}$ compatible serial port (SIO). Status and Revision ID can also be read from the registers.

‡Note: I^2C is a registered trademark of Philips Corporation. The FS400 SIO bus is similar but not identical to Philips I^2C bus.

1.5 Typical System Configurations

1.5.1 External Scan Converter

The FS403 has been optimized for scan converter designs. It provides a maximum amount of flexibility while minimizing system cost. When combined with a Zilog Z902xx Family or Philips P8xC055/145/845 Families, the FS403 provides overlaid On-Screen Display pixels specified by the programmer without any additional external components thus minimizing expense, complexity, and size while maximizing flexibility and features.

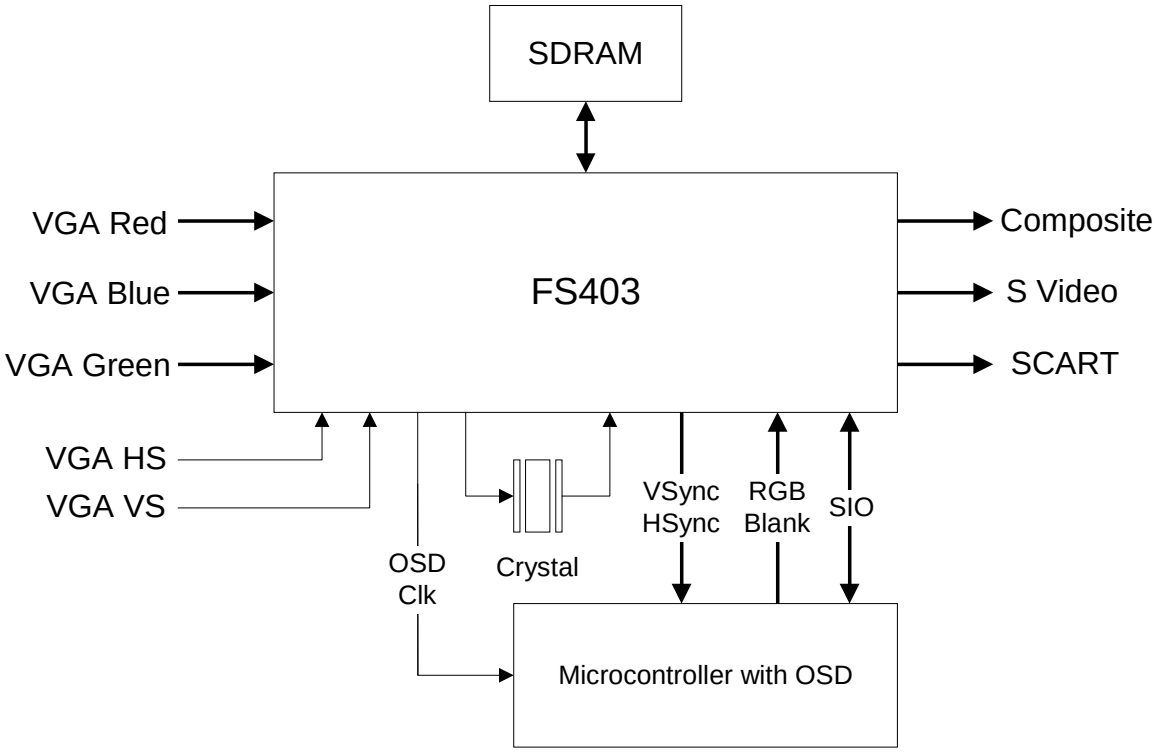


Figure 1: External Scan Converter Block Diagram

1.5.2 Embedded Television Interface

The FS401 has been optimized for television designs. With its built in microprocessor, the FS401 can run freely with minimal control from the television processor while providing complete plug-n-play capability. Simple commands can be sent to the FS401 via the SIO bus to implement remote control functions such as zoom, pan, sizing, positioning, and video quality control (such as brightness, contrast, saturation, flicker, and sharpness). The only components required are the FS401 and a single SDRAM for a truly minimal incremental system cost.

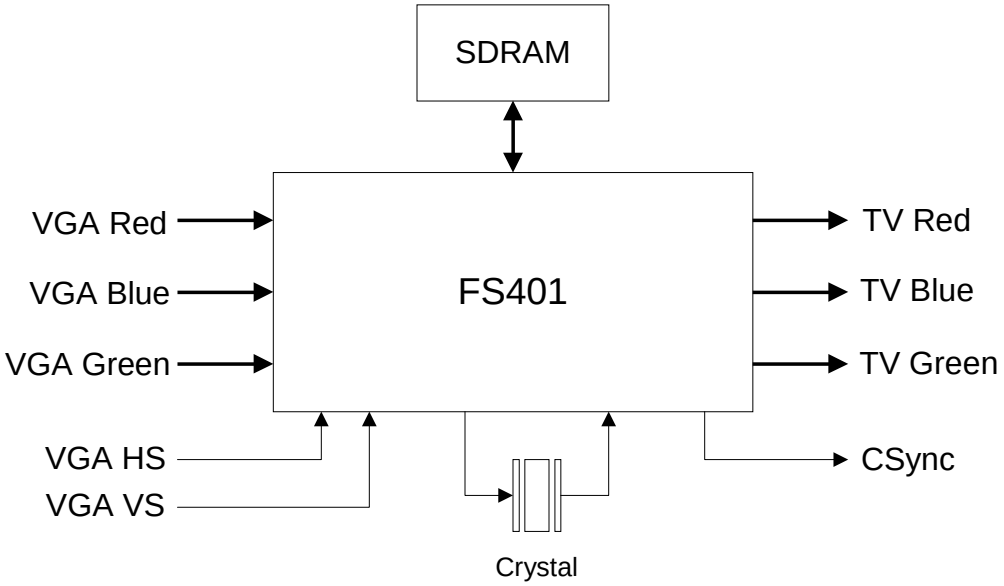


Figure 2: Embedded Television Design Block Diagram

1.5.3 Embedded PC-TV Interface

The FS402 has been optimized for embedded PC and Laptop designs with very low power dissipation, low standby current, Macrovision 7 compliant output, small package size, and a total integrated solution. The FS402 requires only the addition of a low power 16Mb SDRAM plus video connectors to provide a very small footprint while providing the highest quality video.

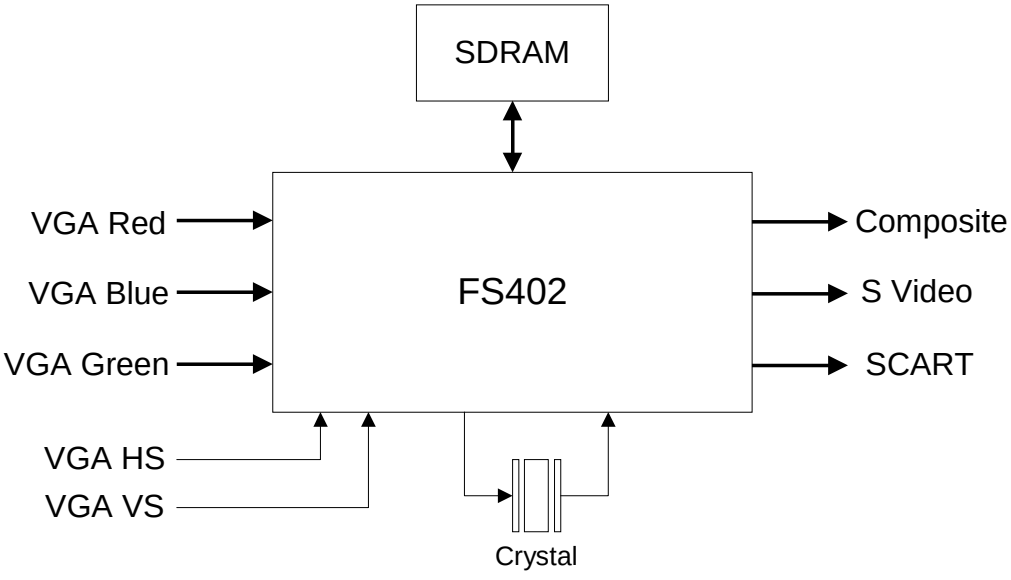


Figure 3: Embedded PC-TV Design Block Diagram

1.5.4 Professional and Pro-Consumer Video Designs

In the Professional and Pro-Consumer Video Market, Video quality, video timing accuracy, and Genlock are very important features. Also the system will use external ADCs and PLLs of the highest quality. Genlock to an external studio Black Burst (black screen TV picture) will be used to synchronize the scan converter to the rest of the video studio.

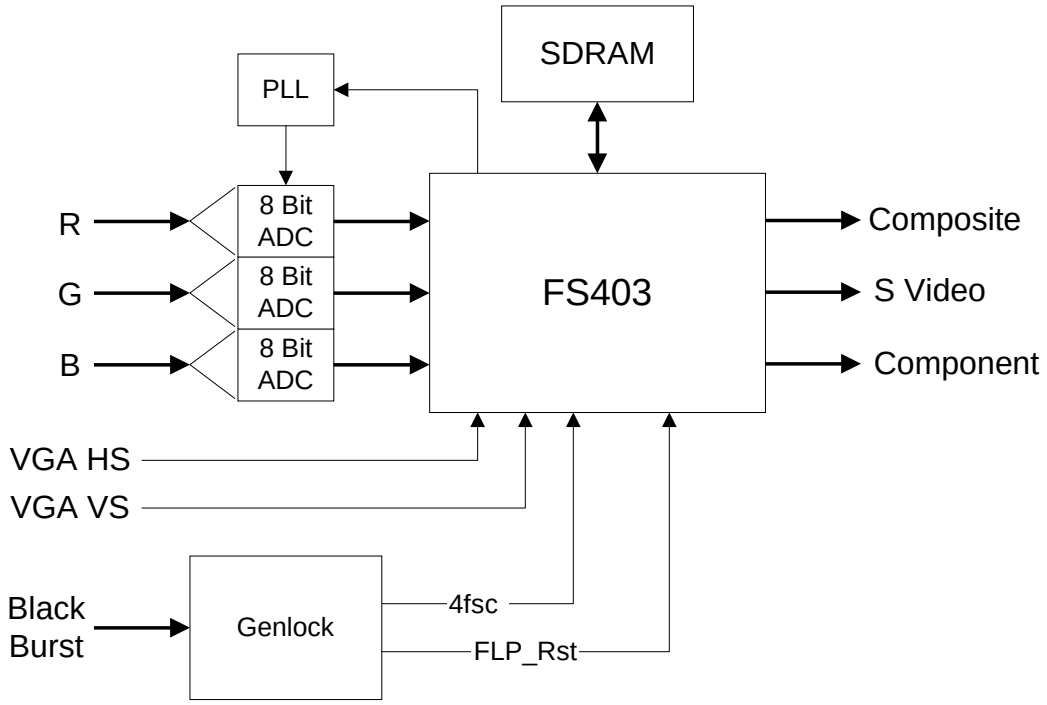


Figure 4: Professional & Pro-Consumer Video Design Block Diagram

2. Specifications

2.1 Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{DD} (Measured to V_{SS})	-0.5	3.3	4.6	V
V_{DDAD} (Measured to V_{SSAD})	-0.5	3.3	4.6	V
V_{DDPA} and V_{DDPF} (Measured to V_{SSPA} and V_{SSPF})	-0.5	3.3	4.6	V
V_{DDDA} (Measured to V_{SSDA})	-0.5	3.3	4.6	V
V_{SSAD}, V_{SSPA}, V_{SS}, V_{SSPA}, V_{SSDA} (delta)	-0.5		0.5	V
Digital Inputs				
3.3 V logic applied voltage (Measured to V_{SS})[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to V_{SSAD})[2]	-0.5		V_{DDDA} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
3.3 V logic applied voltage (Measured to V_{SS})[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-20		110	°C

Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)[1]			220	°C
Storage[1]	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

2.2 Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Digital Power Supply Voltage	3.15	3.3	3.45	V
V_{DDAD}, V_{DDDA}	A/D and D/A Supply Voltage	3.15	3.3	3.45	V
V_{DDPA}, V_{DDPF}	PLLs Supply Voltage	3.15	3.3	3.45	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RT}	Reference Voltage, Top	0.5	0.75	2.0	V
V_{IN}	Analog Input Range	0		VRT	V
V_{REF}	External Reference Voltage		1.276		V
I_{REF}	D/A Converter Reference Current (I_{REF} = V_{REF}/R_{REF}, flowing out of the R_{REF} pin)		3.15		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		392		Ω
R_L	DAC Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C

2.3 Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DD}	3.3 volt current	FSCK–IN = 80MHz		159		mA
I_{DDAD}	3.3 volt Analog current	ADXCK=40MHz		66		mA
I_{DDDA}	3.3 volt Analog current	ADXCK=40MHz		90		mA
I_{DDPA}	3.3 volt Analog current	ADXCK=40MHz		4		mA
I_{DDPF}	3.3 volt Analog current	ADXCK=40MHz		16		mA
I_{DDT}	3.3 volt Total Current	CKNTSC=20MHz		350		mA
Digital Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD} = max., V_{IN} = max.			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = max., V_{IN} = 0 V			±200	µA
I_{ILP}	Input Current, LOW with pull-up	V_{DD} = max., V_{IN} = 0 V	-100			µA
V_{IHTTL}	Input Voltage, Logic HIGH (TTL)		2.0			V
V_{ILTTL}	Input Voltage, Logic LOW (TTL)				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				2.0	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -2mA	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = 2mA			0.4	V
Analog Inputs						
C_{AI}	A/D Input Capacitance	ADCLK = LOW ADCLK = HIGH		4 12		pF pF
R_{IN}	A/D Input Resistance		500	1000		kΩ
I_{CB}	A/D Input Current				±15	µA
V_{RO}	Voltage Reference Output	Internal Reference	1.15	1.276	1.40	V
I_{RO}	VREF Output Current	External V_{REF}	-150		+150	µA
Analog Outputs						
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	C_{OUT} = 0 mA, Freq. = 1 MHz		15		pF
I_{OS}	Short-Circuit Current		-20		-80	mA

2.4 Switching Characteristics

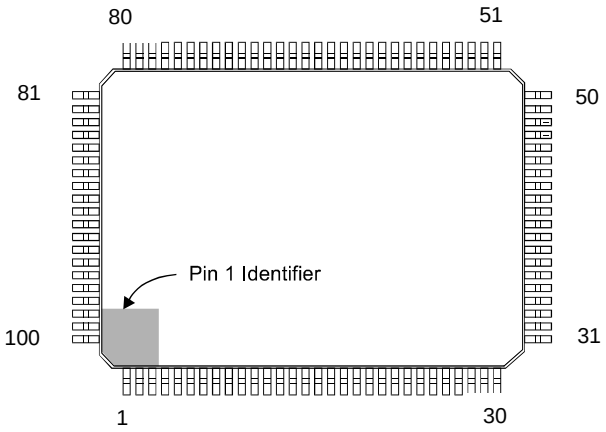
Parameter		Conditions	Min	Typ[1]	Max	Unit
Clocks						
f_{CKIN_N}	NTSC Reference Clock Frequency			14.31818		MHz
f_{CKIN_P}	PAL Reference Clock Frequency			17.734475		MHz
f_{XTOL}	Reference Clock Frequency Tolerance			50	50[2]	ppm
t_{PWH}	Reference Clock Pulse Width, HIGH			40		ns
t_{PWL}	Reference Clock Pulse Width, LOW			40		ns
Reset	Assert time on RESET to reset the part		8			Clocks
Incoming Syncs						
f_H	HS_IN frequency		24		100	KHz
f_V	VS_IN frequency		50		130	Hz
N_H	Number of lines per frame		100		4095	
t_{PWHS}	HS_IN Pulsewidth		1			µs
t_{VS-HS}	VS_IN to HS_IN Delay		0			ns
t_{DS}	Sync Delay (VGA Sync to Sync Out)			100		ns
Video Output						
t_{DOV}	Analog Output Delay ($4f_{SC}$ clock to Video Out)				30	ns
t_R	D/A Output Current Risetime (10% to 90%)				10	ns
t_F	D/A Output Current Falltime (90% to 10%)				10	ns
SKEW	D/A to D/A Skew		-3	0	3	ns
SDRAM Frame Buffer Interface						
t_{FCKL}	FS_CK pulse width, LOW		5.0			ns
t_{FCKH}	FS_CK pulse width, HIGH		5.0			ns
t_{FSCO}	FS_CK to RAS\, CAS\, WE\ DQM\ out delay		2.0			ns
t_{FDSU}	FS_CK to data setup time		3.0			ns
t_{FDHO}	FS_CK to data hold time		3.0			ns
t_{FDO}	FS_CK to data out delay		2.0			ns
t_{FAO}	FS_CK to address out delay		2.0			ns
Serial Microprocessor Interface						
t_{DAL}	SIOCLK Pulse Width, LOW			1.3		µs
t_{DAH}	SIOCLK Pulse Width, HIGH			0.6		µs
t_{STAH}	SIODATA Start Hold Time			0.6		µs
t_{STASU}	SIOCLK to SIODATA Setup Time (Stop)			0.6		µs
t_{STOSU}	SIOCLK to SIODATA Setup Time (Start)			0.6		µs
t_{BUFF}	SIODATA Stop Hold Time Setup			1.3		µs
t_{DSU}	SIODATA to SIOCLK Data Setup Time			300		ns
t_{DHO}	SIODATA to SIOCLK Data Hold Time			300		ns

Notes:
1. Values shown in Typ column are typical for $V_{DD} = V_{DDA} = +3.3V$ and $T_A = 25°C$
2. TV subcarrier acceptance band is $\pm$ 300 Hz.

2.5 System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Unit
A/D Converter Input						
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 0.7V		±1		LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 0.7V		±1		LSB
E_{OT}	Offset Voltage, Top	$V_{RT} – V_{IN}$ for most positive code transition		150		mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition		150		mV
D/A Converter Output						
RES	D/A Converter Resolution		10	10	10	Bits

Notes:
1. Values shown in Typ column are typical for $V_{DD} = V_{DDA} = +3.3V$ and $T_A = 25°C$



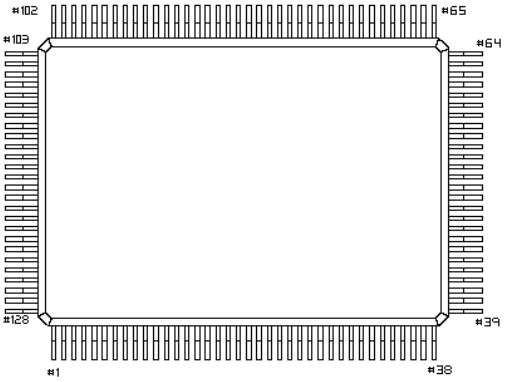
Pin Assignments

2.6 100-Lead PQFP Package (FS401)

Table 1. Pin Designations (FS401, 100-pin package)

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1.	V_{DDPF}	31.	TV_VSYNC	51.	V_{SS}	81.	GPO6
2.	OSC1	32.	TV_HSYNC	52.	EXTVGASEL\	82.	V_{DD}
3.	OSC1BUF	33.	V_{DDAD}	53.	VGACLKIN	83.	A0
4.	OSC2	34.	V_{SSAD}	54.	V_{DD}	84.	A1
5.	OSC2BUF	35.	V_{SSAD}	55.	V_{SS}	85.	A2
6.	V_{SS}	36.	R_IN	56.	V_{SS}	86.	A3
7.	V_{SSDA}	37.	V_{DDAD}	57.	DQM	87.	A4
8.	C_{COMP}	38.	V_{DDAD}	58.	WE\	88.	A5
9.	I_{REF}	39.	G_IN	59.	INTCPUEN	89.	A6
10.	V_{DDDA}	40.	V_{SSAD}	60.	RAS\	90.	A7
11.	C_{BYPASS}	41.	V_{TOUT}	61.	CAS\	91.	A8
12.	Y/R/V	42.	V_{ADCREF}	62.	D0	92.	A9
13.	V_{DDDA}	43.	V_{SSAD}	63.	D1	93.	A10
14.	V_{SSDA}	44.	B_IN	64.	D2	94.	A11
15.	CVBS/G/Y	45.	V_{DDAD}	65.	D3	95.	V_{DD}
16.	V_{DDDA}	46.	CLAMP_REF	66.	D4	96.	GPO0
17.	C/B/U	47.	V_{DDPA}	67.	D5	97.	V_{SSPF}
18.	V_{DDDA}	48.	V_{SSPA}	68.	D6	98.	RAMCK_SEL\
19.	V_{DD}	49.	VS_IN	69.	D7	99.	RAMCK_OUT
20.	CSYNC	50.	HS_IN	70.	D8	100.	RAMCK_IN
21.	V_{SS}			71.	D9		
22.	V_{SS}			72.	D10		
23.	SIOCLK			73.	D11		
24.	SIODATA			74.	V_{DD}		
25.	$SIOA_{10/7}$			75.	V_{SS}		
26.	$SIOA_0$			76.	D12		
27.	V_{DD}			77.	D13		
28.	Reserved (V_{SS})			78.	D14		
29.	Reserved (V_{SS})			79.	D15		
30.	RESET			80.	V_{SS}		

NOTE: FS402 INFORMATION INCLUDING PINOUTS ARE AVAILABLE ONLY TO MACROVISION LICENSEES.



2.7 128-Lead PQFP Package (FS403)

Table 2. Pin Designations (FS403, 128-pin package)

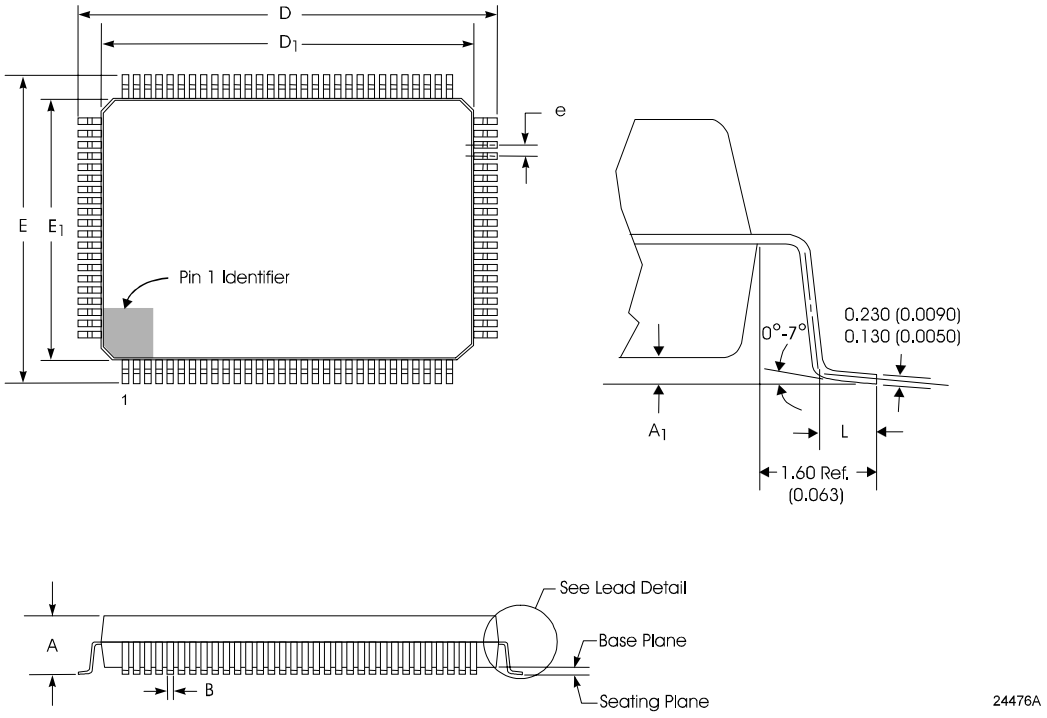
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1.	OSC1	33.	V_{DD}	65.	VGACLKDIV	97.	D12
2.	OSC1BUF	34.	Reserved (V_{SS})	66.	EXTVGASEL\	98.	D13
3.	OSC2	35.	FLP_RST	67.	VGACLKIN	99.	D14
4.	OSC2BUF	36.	Reserved (V_{SS})	68.	V_{DD}	100.	D15
5.	V_{SS}	37.	RESET	69.	V_{SS}	101.	V_{SS}
6.	V_{SSDA}	38.	R0/TV_VSYNC	70.	G3	102.	B7/GPO7
7.	C_{COMP}	39.	R1/TV_HSYNC	71.	G2	103.	B6/GPO6
8.	I_{REF}	40.	R2/OSDEN	72.	G1	104.	B5/GPO5
9.	V_{DDDA}	41.	R3	73.	G0	105.	B4/GPO4
10.	C_{BYPASS}	42.	V_{DDAD}	74.	V_{SS}	106.	V_{DD}
11.	Y/R/V	43.	V_{SSAD}	75.	DQM	107.	A0
12.	V_{DDDA}	44.	V_{SSAD}	76.	WE\	108.	A1
13.	V_{SSDA}	45.	R_IN	77.	INTCPUEN	109.	A2
14.	CVBS/G/Y	46.	V_{DDAD}	78.	RAS\	110.	A3
15.	V_{DDDA}	47.	V_{DDAD}	79.	CAS\	111.	A4
16.	C/B/U	48.	G_IN	80.	V_{DD}	112.	A5
17.	V_{DDDA}	49.	V_{SSAD}	81.	D0	113.	A6
18.	V_{DD}	50.	V_{TOUT}	82.	D1	114.	A7
19.	OSDCLK	51.	V_{ADCREF}	83.	D2	115.	A8
20.	CSYNC	52.	V_{SSAD}	84.	D3	116.	A9
21.	V_{SS}	53.	B_IN	85.	D4	117.	A10
22.	V_{SS}	54.	V_{DDAD}	86.	D5	118.	A11
23.	EXADSEL	55.	CLAMP_REF	87.	D6	119.	V_{DD}
24.	G6/OSDB	56.	R4	88.	D7	120.	B3/GPO3
25.	G5/OSDG	57.	R5	89.	V_{SS}	121.	B2/GPO2
26.	G4/OSDR	58.	R6	90.	V_{DD}	122.	B1/GPO1
27.	G7/OSDHT	59.	R7	91.	D8	123.	B0/GPO0
28.	V_{SS}	60.	V_{DDPA}	92.	D9	124.	V_{SSPF}
29.	SIOCLK	61.	V_{SSPA}	93.	D10	125.	RAMCK_SEL\
30.	SIODATA	62.	VS_IN	94.	D11	126.	RAMCK_OUT
31.	$SIOA_{10/7}$	63.	HS_IN	95.	V_{DD}	127.	RAMCK_IN
32.	$SIOA_0$	64.	V_{SS}	96.	V_{SS}	128.	V_{DDPF}

3. Mechanical Dimensions

3.1 100-Lead PQFP (KH) Package, FS401 and FS402

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A				3.00	
A1			0.05	-	
A2			2.55	2.75	
B			0.25	0.40	3,5
C			0.10	0.25	5
D			23.60	24.20	
D_1			19.80	20.20	
E			17.30	18.20	
E1			13.80	14.20	
e			0.65 BSC		
L			0.60	1.00	4
N	100		100		
ND	30		30		
NE	20		20		
α			0	8°	
ccc			-		

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling Dimension is millimeters
3. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the “B” dimension. Dambar cannot be located on the lower radius or the foot.
4. “L” is the length of terminal for soldering to a substrate.
5. “b” & “C” include lead finish thickness.

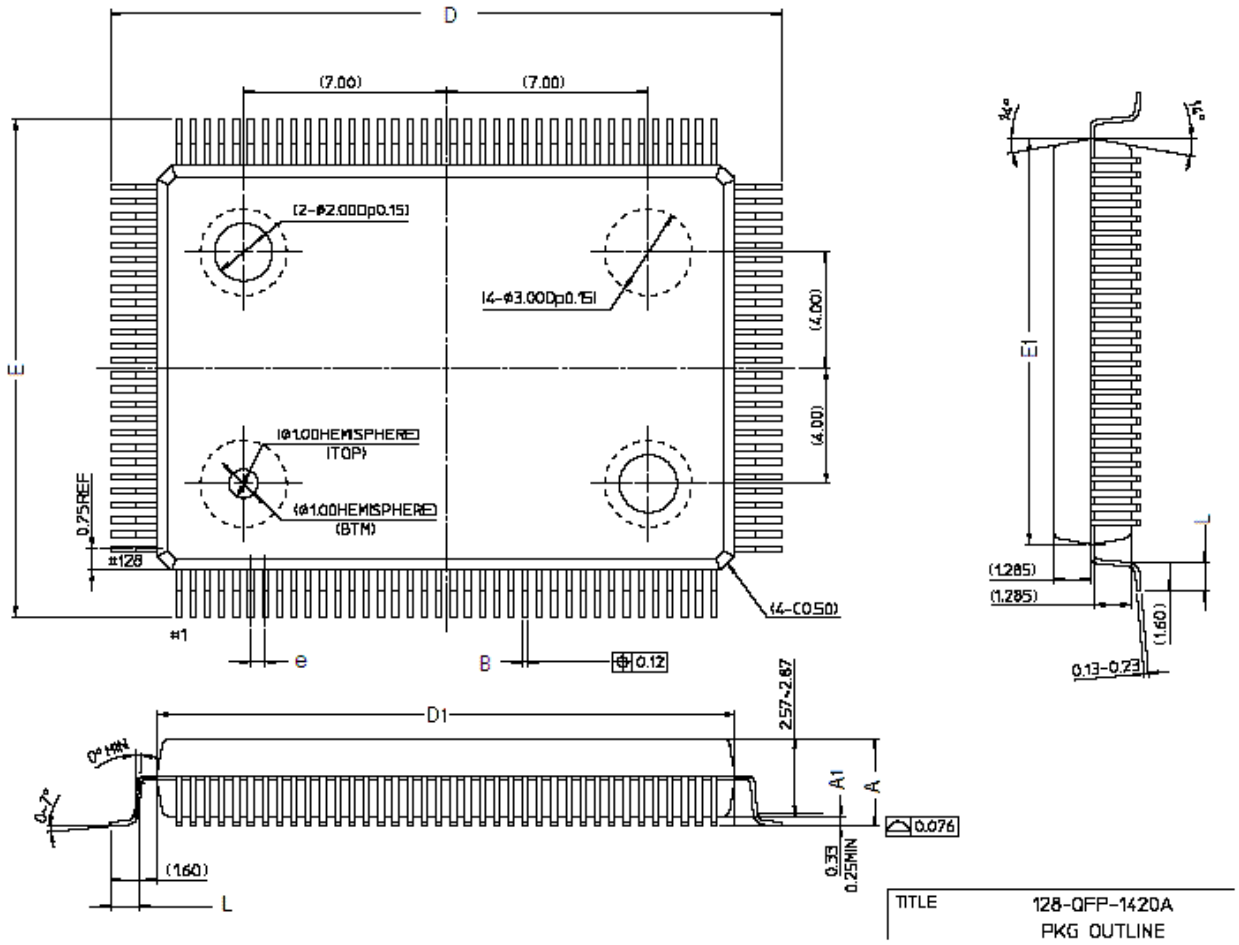


3.2 128-Lead PQFP Package, FS403 LF & FS403

Symbol	FS403LF		FS403		Notes
	Min.	Max.	Min.	Max.	mm
A	-	3.40	-	2.40	
A1	0.25		0.05		
B	0.13	0.28	0.15	0.30	3,5
D	23.20 BSC		21.70	22.30	
D_1	19.80	20.00	19.80	20.20	
E	17.2 BSC		15.70	16.30	
E1	13.80	14.10	13.80	14.20	
e	0.50 BSC		0.50 BSC		
L	0.73	1.03	0.30	0.70	4
N	128		128		Pins
ND	38		38		Pins
NE	26		26		Pins

Notes:

6. All dimensions and tolerances conform to ANSI Y14.5M-1982.
7. Controlling Dimension is millimeters
8. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the “B” dimension. Dambar cannot be located on the lower radius or the foot.
9. “L” is the length of terminal for soldering to a substrate.
10. “B” includes lead finish thickness.



4. Revision History

3/3/99: First Release, V1.0

4/2/99: Second Release, V1.1: p. 1, added DPMS support & adaptive input filtering selection; p. 13, added GPO_0 description; p. 17, moved OHO & OVO to list of registers used by on-board processor; p. 19-24, corrected typo on register names & added better DSICAL description; p. 66, added reminder about loop delay.

7/16/99: Third Release, V1.2: p. 10, 11, 16: documented need to ground “reserved” pins; p. 11 & 13, EXADSEL sense changed from early silicon to high true input (high selects external A/D on FS403); p. 19-24, corrected typo on register names & added better DSICAL description, description of new SCR bits, new HOHOS & HOVOS registers, SFLK change from register to bits in SCR; p. 26-27, new software reset values and new HOHOS, HOVOS registers & SCR bits; p. 38, proper VGAINTDET definition; p. 53, new SCR definitions; p. 55-57, new SSR, HCRS, and HCRES bit definitions; p. 58-63, HPO, VPO, HSS, VSS, HPP, VPP all require up to 25ms (vs. 10ms) to calculate limits; ; p. 68-69, new HOHOS & HOVOS registers definitions; p. 71-73, new Configuration Register definitions; p. 87, comment about Philips vs. FOCUS SIO addressing added; p. 88, errors in table corrected (p. 15 was correct, not table 5); p. 103, part number change.

9/2/99: Fourth Release, V1.3: p. 13, documented internal pull-down on EXADSEL; p. 14, corrected C_{COMP} pull down; p. 96, deleted reference to FS_CKIN to FC_CKOUT resistor, resistor not recommended; p. 103, package marking.

7/25/00: Fifth Release, V1.4: p. 1, new patent received; p. 5, corrected reference to external VGACKIN source; p. 19 section 4.2.1.2, corrected first section regarding DSICAL bit (deleted reference to ICALRDY bit); p. 25, Status Port changed to Status Register; p. 84, corrected oscillator settings for Super NTSC and Super PAL; p. 91, 92: V_{REF} changed to 1.276V typical, new min/max.

1/23/03: Sixth Release, V1.5: Table 2, corrected FS403 signal assignments on pin 24 (now G_6) and pin 26 (now G_4). Section 3, corrected descriptions of FS403 pin 24 (now G_6) and pin 26 (now G_4). Section 4.5.25, refined the definition of the GPO register.

11/27/05: Seventh Release, V1.6 Table 8.2 modified to include FS403LF dimensions. Removed unreferenced rows in that table.

4/5/06: Eighth Release, V1.6 created a new abbreviated version of the data sheet for posting on the Website. Removed from Pin Description to Mechanical Dimensions.

5. Ordering Information

Order Number	Temperature Range	Screening	Package	Package Marking
444-2121	0°C to 70°C	Commercial	100 Lead PQFP	FS401
444-2121LF	0°C to 70°C	Commercial	100 Lead PQFP	FS401LF
444-2122	0°C to 70°C	Commercial	100 Lead PQFP	FS402
444-2123	0°C to 70°C	Commercial	128 Lead PQFP	FS403
444-2123LF	0°C to 70°C	Commercial	128 Lead PQFP	FS403LF

Additionally, a FS400 Hardware Development Kit is available for purchase, Order # 444-2020.

Package Markings:

FOCUS
Enhancements
FS40x
<Date Code (YYWWLA) and Revision Letter>
<fab lot id>

where x = 1, 2, or 3.

Please forward suggestions and corrections as soon as possible to info@focusinfo.com. The information herein is accurate to the best of FOCUS' knowledge, but not all specifications have been characterized or tested at the time of the release of this document. Parameters will be updated as soon as possible and updates made available.

For further information on the FS400 family of scan converters, contact your Focus representative and request reference schematics, application notes, and source code (as appropriate).

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Focus Enhancements components are not designed for use in Critical Applications. Critical Applications are products whose use may involve risks of death, personal injury, severe property damage or environmental damage or life support applications, devices, or systems, wherein a failure or malfunction of the component can reasonably be expected to result in death or personal injury. The user of Focus Enhancements components in Critical Applications assumes all risk of such use and indemnifies Focus Enhancements against all damages.

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