TEA5761UK

Low voltage single-chip FM stereo radio

Rev. 01 — 2 August 2006 Product data sheet

1. General description

The TEA5761UK is a single-chip electronically tuned FM stereo radio for low-voltage applications with fully integrated IF selectivity and demodulation.

The radio is completely adjustment free and only requires a minimum of small and low cost external components. The radio can tune to the European, US and Japanese FM bands. The radio does not meet all of the requirements of EN55020; a trade off has been implemented to achieve the following features.

2. Features

- High sensitivity due to integrated low noise RF input amplifier
- FM mixer for conversion of the US and Europe FM band (87.5 MHz to 108 MHz) and Japanese FM band (76 MHz to 90 MHz) to IF
- Preset tuning to receive Japanese TV audio up to 108 MHz, raster 100 kHz
- Auto search tuning, 100 kHz grid
- RF automatic gain control circuit
- LC tuner oscillator operating with one low-cost chip inductor; no need for external varicap
- Fully integrated FM IF selectivity
- Fully integrated FM demodulator; no external discriminator
- Crystal oscillator at 32768 Hz, or external reference frequency at 32768 Hz
- PLL synthesizer tuning system
- IF counter; 7-bit output via the I^2C-bus
- Level detector; 4-bit level information output via the I^2C-bus
- Soft mute: signal dependent mute function
- Mono/stereo blend: gradual change from mono to stereo, depending on signal; Stereo Noise Cancelling (SNC)
- Soft mute and SNC can be switched off via the I^2C-bus
- Adjustment-free stereo decoder
- I^2C-bus interface
- Autonomous search tuning function
- Standby mode
- MPX output
- One software programmable port
- Interrupt flag

PHILIPS

3. Applications

- FM stereo radio

4. Quick reference data

Table 1: Quick reference data

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.The listed parameters are valid when a crystal is used that meets the requirements as stated in Table 31.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General [1]							
V_{CCA}	analog supply voltage			2.5	2.7	3.6	V
V_{CCD}	digital supply voltage			2.5	2.7	3.6	V
I_{CCA}	analog supply current	Operating mode		10	14	16.5	mA
		Standby mode		-	2.0	6.0	µA
I_{CCD}	digital supply current	Operating mode		5	-	20	µA
		Standby mode		1	3.3	20	µA
Reference voltage							
$V_{VREFDIG}$	digital reference voltage for I²C-bus interface	$V_{VREFDIG} \leq V_{CC}$		1.65	1.8	V_{CCD}	V
$I_{VREFDIG}$	digital reference supply current	Operating mode; $V_{VREFDIG}$ = 1.65 V to V_{CCD}		-	0.5	2.0	µA
T_{amb}	ambient temperature	V_{CD1} = 2.7 V; $V_{VREFDIG}$ = 1.8 V	[1]	–20	-	+85	°C
FM overall system parameters							
$f_{i(FM)}$	FM input frequency			76	-	108	MHz
$V_{sens(EMF)}$	sensitivity EMF value voltage	f_{RF} = 76 MHz to 108 MHz; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; TC_{deem} = 75 µs; A-weighting filter; B_{aud} = 300 Hz to 15 kHz		-	2.2	3.6	µV
$IP3_{in}$	in-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tune} = 76 MHz to 108 MHz; RF_{agc} = off		81	87	-	dBµV
$IP3_{out}$	out-of-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$	Δf_1 = 4 MHz; Δf_2 = 8 MHz; f_{tune} = 76 MHz to 108 MHz; RF_{agc} = off		87	93	-	dBµV
S	selectivity	f_{tune} = 76 MHz to 108 MHz	[2]				
		high-side: Δf = +200 kHz		39	43	-	dB
		low-side: Δf = –200 kHz		32	36	-	dB
V_{VAFL}	left audio output voltage on pin VAFL	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs		60	75	90	mV
V_{VAFR}	right audio output voltage on pin VAFR	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs		60	75	90	mV

Table 1: Quick reference data *...continued*

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified. The listed parameters are valid when a crystal is used that meets the requirements as stated in Table 31.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(S+N)/N(m)	maximum signal-to-noise ratio, mono	V_{RF} = 1 mV; Δf = 22.5 kHz; L = R; f_{mod} = 1 kHz; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz + A-weighted filter	53	57	-	dBA
α_{cs}	channel separation	V_{RF} = 1 mV; Δf = 75 kHz; including 9 % pilot deviation; R = 0 and L = 1 or R = 1 and L = 0; f_{mod} = 1 kHz; bit MST = 0; bit SNC = 1; B_{aud} = 300 Hz to 15 kHz	22	27	-	dB
THD	total harmonic distortion measured (at pins VAFL and VAFR)	V_{RF} = 1 mV; Δf = 75 kHz; f_{mod} = 1 kHz; L = R; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz	-	0.4	1	%

[1] Crystal influence not included.

[2] Low-side and high-side selectivity can be measured by changing the mixer LO injection from high-side to low-side.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TEA5761UK	WLCSP34	wafer level chip-size package; 34 bumps; 3.5 × 3.5 × 0.6 mm	NAU000

6. Block diagram

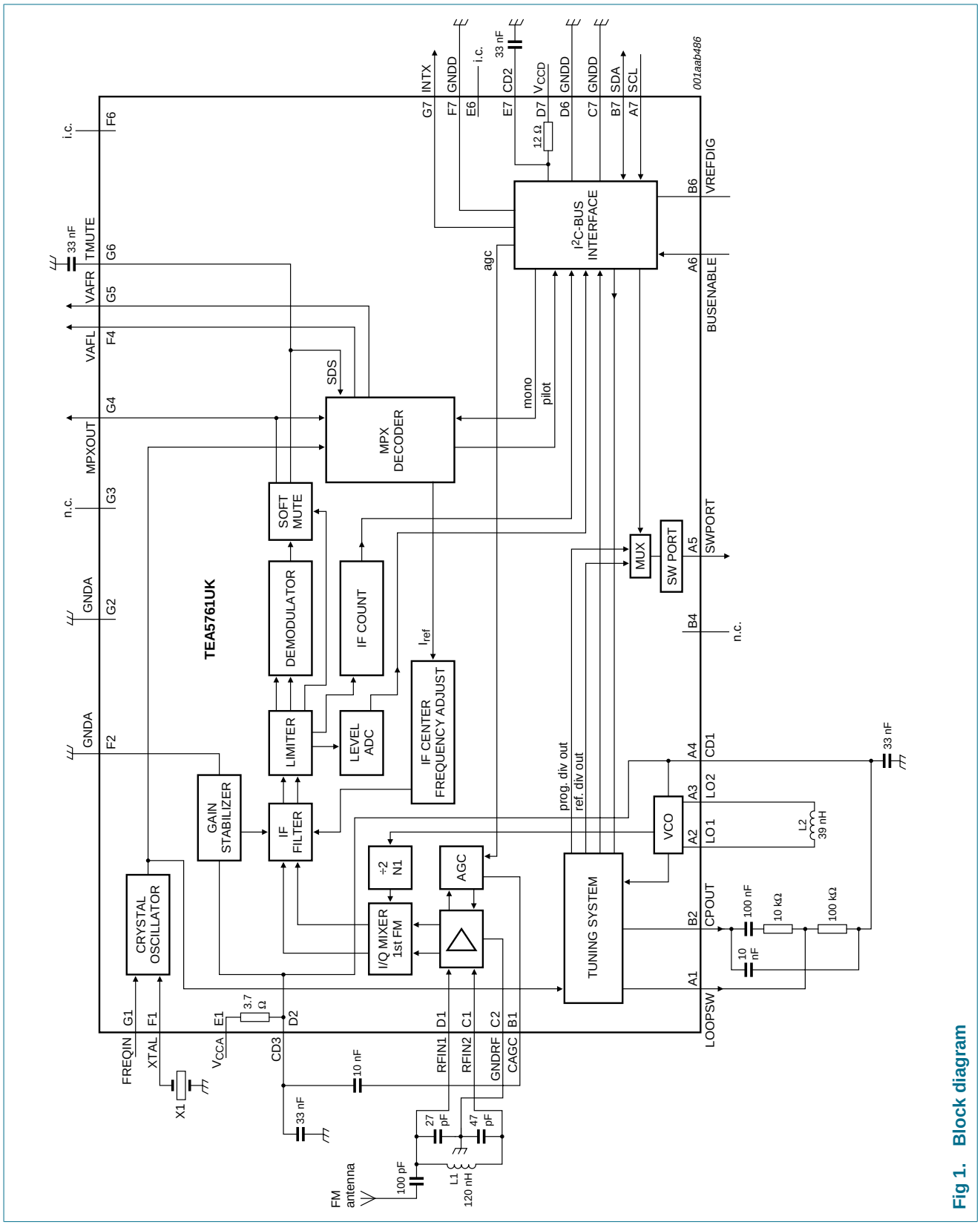


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

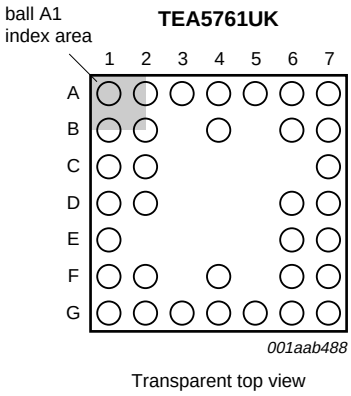


Fig 2. Pin configuration of WLCSP34 package

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
LOOPSW	A1	synthesizer PLL loop filter switch output
LO1	A2	local oscillator coil connection 1
LO2	A3	local oscillator coil connection 2
CD1	A4	VCO supply decoupling capacitor
SWPORT	A5	software programmable port output
BUSENABLE	A6	I^2C-bus enable input
SCL	A7	I^2C-bus clock line input
CAGC	B1	RF AGC time constant capacitor
CPOUT	B2	charge pump output of synthesizer PLL
n.c.	B4	not connected
VREFDIG	B6	digital reference voltage for I^2C-bus
SDA	B7	I^2C-bus data line input and output
RFIN2	C1	RF input 2
GNDRF	C2	RF ground
GNDD	C7	digital ground
RFIN1	D1	RF input 1
CD3	D2	V_{CCA} decoupling capacitor
GNDD	D6	digital ground
V_{CCD}	D7	digital supply voltage
V_{CCA}	E1	analog supply voltage
i.c.	E6	internally connected; leave open
CD2	E7	V_{CCD} decoupling capacitor

Table 3: Pin description *...continued*

Symbol	Pin	Description
XTAL	F1	crystal oscillator input
GNDA	F2	analog ground
VAFL	F4	left audio output
i.c.	F6	internally connected; leave open
GNDD	F7	digital ground
FREQIN	G1	32.768 kHz reference frequency input
GNDA	G2	analog ground
n.c.	G3	not connected
MPXOUT	G4	FM demodulator MPX output
VAFR	G5	right audio output
TMUTE	G6	soft mute time constant capacitor
INTX	G7	interrupt flag output

8. Functional description

8.1 Low noise RF amplifier

The LNA input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

8.2 I/Q mixer 1st FM

The FM quadrature mixer converts FM RF (76 MHz to 108 MHz) to IF.

8.3 VCO

The LC tuned VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is from 150 MHz to 217 MHz. No external varactor is required.

8.4 Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or via an external 32.768 kHz reference clock source connected to pin FREQIN. Selection between a reference clock or a reference crystal can be done by software programming via the I^2C-bus. When a clock crystal is used, pin FREQIN must be left open-circuit, or when external clocking is used, there should be no crystal connected to pin XTAL.

The temperature drift of 32.768 kHz clock crystals limits the operational temperature range. The preferred crystal specifications are given in Table 31.

The crystal oscillator generates the reference frequency for:

- Synthesizer PLL tuning system
- Timing for the IF counter
- Free running frequency adjustment of the stereo decoder VCO
- Center frequency adjustment of the IF filters

8.5 PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz reference frequency generated by the crystal oscillator or a reference clock of 32.768 kHz fed into the TEA5761UK. To tune the radio to the required frequency requires the PLL word to be calculated and then programmed to the register. The PLL word is 14 bits long; see Table 12 and Table 13. Calculation of this 14-bit word can be done as follows.

Formula for high-side injection:

$$N_{DEC} = \frac{4 \times (f_{RF} + f_{IF})}{f_{ref}} \quad (1)$$

Formula for low-side injection:

$$N_{DEC} = \frac{4 \times (f_{RF} - f_{IF})}{f_{ref}} \quad (2)$$

where:

N_{DEC} = decimal value of PLL word

f_{RF} = wanted tuning frequency (Hz)

f_{IF} = intermediate frequency of 225 kHz

f_{ref} = reference frequency of 32.768 kHz

Example for receiving a channel at 100.1 MHz:

$$N_{DEC} = \frac{4 \times (100.1 \times 10^6 + 225 \times 10^3)}{32768} = 12246.704 \quad (3)$$

The result found using Equation 1 or Equation 2 must always be rounded to the lowest integer value. If rounded down to the lowest integer value of N_{DEC} = 12246, the PLL word becomes 2FD6h.

This value can be written to register FRQSET via the I^2C-bus and the TEA5761UK will then start an autonomous search at this frequency or go to a preset channel at this frequency. When the application is built according to the application diagram (see Figure 13) and with the preferred components, the PLL will settle to the new frequency within 40 ms.

The PLL is triggered by writing to any one of the bytes FRQSETMSB, FRQSETLSB, TNCTRL1, TNCTRL2, TESTBITS, TESTMODE.

Accurate validation of the PLL locking on the new frequency can take 40 ms. When a lock is detected bit LD is set.

8.6 Band limits

The TEA5761UK can be switched to the Japanese FM band or to the US and Europe FM band. Setting bit BLIM to logic 0 the band range is 87.5 MHz to 108 MHz; setting bit BLIM to logic 1 selects the Japanese band range of 76 MHz to 90 MHz.

8.7 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels. The RF AGC is on by default and can be turned off via the I^{2}C-bus.

The TEA5761UK also has an in-band AGC to prevent overloading by the wanted channel. The in-band AGC is always turned on.

8.8 Local or long distance receive

If bit LDX = 1, the LNA gain is reduced by 6 dB to prevent distortion when a transmitter is very near. If bit LDX = 0, the LNA gain is normal to receive long distance (DX) stations.

8.9 IF filter

A fully integrated IF filter with a center frequency of 225 kHz is built-in.

8.10 FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

8.11 IF counter

The received signal is mixed to an IF of 225 kHz. The result of the mixing is counted. A good IF count result indicates that the radio is tuned to a valid channel instead of an image or a channel with much interference. The IF counter outputs a 7-bit count result via the I^{2}C-bus. The IF counter is continuously active and can be read at any time via the I^{2}C-bus. It also activates a flag when the IF count result is outside the IF count valid result window; see Section 9.2.2. The IF count period can be set to 1.953 ms or 15.625 ms by bit IFCTC.

8.12 Voltage level generator and analog-to-digital converter

The voltage level indicates the field strength received by the antenna. The voltage level is analog-to-digital converted to a 4-bit word and output via the I^{2}C-bus. The ADC level is continuously active and can be read at any time via the I^{2}C-bus. It also activates a flag when the voltage level falls under a predefined selectable threshold. Bit LHSW allows either large or small hysteresis steps to be chosen; see Table 21 and Section 9.2.3.

8.13 Mute

8.13.1 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels: the audio output is faded and hence also the noise (curves 1 and 2 of Figure 12).

The soft mute function can also be toggled via the I^{2}C-bus, using bit SMUTE.

8.13.2 Hard mute

The audio outputs VAFL and VAFR can be hard muted by bit MU in byte TNCTRL2 which means they are put into 3-state. This can also be done by setting bits Left Hard Mute (LHM) or Right Hard Mute (RHM) in byte TESTBITS, which allows either one or both channels to be muted and forces the TEA5761UK to Mono mode. When the TEA5761UK is in Standby mode the audio outputs are hard muted.

8.13.3 Audio frequency mute

The audio signal is muted by setting bit AFM of the TNCTRL1 register to logic 1. In the soft mute attenuator the audio signal is blocked and so pins VAFL and VAFR will be at their DC biasing point with no signal.

The audio is automatically muted during a preset as shown in the flowchart of Figure 3. When the audio must be muted during Search mode, it is done by setting bit AFM to logic 1 before the search action and resetting it to logic 0 afterwards.

Table 4: Specification of Mute modes

Mute mode	Bit	MPX output		VAFL output (left)		VAFR output (right)	
		Impedance	State	Impedance	State	Impedance	State
Audio frequency mute	AFM = 1	500 Ω	muted	50 Ω	muted	50 Ω	muted
Hard mute	MU = 1	500 Ω	muted	3-state	muted	3-state	muted
Left hard mute	LHM = 1	500 Ω	audio	3-state	muted	50 Ω	mono audio
Right hard mute	RHM = 1	500 Ω	audio	50 Ω	mono audio	3-state	muted
Standby mute	PUPD = 0	3-state	muted	3-state	muted	3-state	muted
Soft mute	SMUTE = 1	RF level sensitive audio level; has no influence on mute or output impedance					

8.14 MPX decoder

The PLL stereo decoder is adjustment free. It can be switched to mono via the I^2C-bus.

8.15 Signal dependent mono/stereo blend (stereo noise cancellation)

If the RF input level decreases, the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono-to-stereo blend can also be programmed via the I^2C-bus to an RF level dependent switched mono-to-stereo transition. Stereo noise cancellation can be switched off via the I^2C-bus by bit SNC.

8.16 Software programmable port

The software programmable port (CMOS output) can be addressed via the I^2C-bus:

- Bit SWPM = 1: port functions as the output for bit FRRFLAG.
- Bit SWPM = 0: port outputs the level corresponding to bit SWP.

In Test mode, the software port outputs signals according to Table 23. Test mode is selected by setting bit TM of byte TESTMODE to logic 1.

The programmed output status of the software port remains, independent of bit PUPD; see Section 8.17.

8.17 Standby mode

The radio can be put into Standby mode by Power-Up / Power-Down bit PUPD. In this mode, the FM part can be turned off. The TEA5761UK is still accessible via the I²C-bus but takes only very low power from the supply. In Standby mode, the audio outputs are hard muted.

When the supply voltages V_{CCA} and V_{CCD} are made 0 V and VREFDIG = HIGH, all inputs and outputs, the audio outputs and the reference clock input are in high-impedance state.

The power supplies can be switched on in any order.

8.18 Power-on reset

After start-up of V_{CCA} and V_{CCD} a power-on reset circuit will generate a reset pulse and the registers will be set to their default values. The power-on reset is effectively generated by V_{CCD}.

At power-on reset, the mute is set and all other bits are set to the reset value as given in Table 9. To initialize the TEA5761UK all bytes have to be transferred.

8.19 I²C-bus interface

The I²C-bus interface operates with a maximum clock frequency of 400 kHz.

When, during operation, the signal on pin BUSENABLE is toggled, the device will not generate an I²C-bus acknowledge bit on the first following I²C-bus transmission. It is then necessary to send either the I²C-bus address two times prior to the complete transmission or send the complete I²C-bus transmission twice. After this, the I²C-bus communication is restored in the normal behavior. Now an I²C-bus acknowledge is generated on each transmitted byte again.

8.20 Auto search and Preset mode

8.20.1 Search mode

In Search mode the IC can search channels automatically; see Figure 3.

When the INTX signal is used as an interrupt to the microcontroller to indicate a search stop, the INTMSK register must be reset and only bit FRRMSK must be set. In this way the microcontroller will only be interrupted when the search or preset algorithm is ready.

Search mode is initiated by setting bit SM in byte FRQSETMSB to logic 1. The search direction is set by bit SUD; bit SUD = 0 (search down), bit SUD = 1 (search up). The tuner starts searching at the frequency from where it is or at a start frequency set in bytes FRQSETLSB and FRQSETMSB. The Search Stop Level (SSL) bits define the field strength level at which a desired channel is detected. The tuner will stop on a channel with a field strength equal to or higher than this reference level and then checks the IF frequency; when both are valid, the search stops. If the level check or the IF count fails, the search continues. If no channels are found, the TEA5761UK stops searching when it has reached the band limit, setting bit BLFLAG HIGH. A search always stops when the FRRFLAG is set and on the occurrence of a hardware interrupt, this procedure is shown in Figure 3.

The search algorithm can stop at a frequency that is offset from the IF by up to a maximum of 12 kHz. The maximum offset can be limited to 8 kHz by applying a preset. For optimum tuning, it is recommended that a preset is applied after a search and when the found frequency has an offset that is above 8 kHz.

After this interrupt the TEA5761UK will not update the tuner registers INTREG, FRQCHK and TUNCHK for a period of 15 ms. The state of the TEA5761UK can be checked by reading registers INTREG, FRQCHK and TUNCHK. Table 5 shows the possible states of these registers after an auto search.

8.20.2 Preset mode

A preset occurs by setting bit SM to logic 0 and writing a frequency to register FRQSET. The tuner jumps to the selected frequency and sets bit FRRFLAG when it is ready.

After this interrupt the TEA5761UK will not update the tuner registers INTREG, FRQCHK and TUNCHK for a period of 15 ms. The state of the TEA5761UK can be checked by reading registers INTREG, FRQCHK and TUNCHK. Table 5 shows the possible states after a preset.

Table 5: Tuner truth table

Bit			Comment
IFFLAG	BLFLAG	FRRFLAG	
0	0	0	if pin INTX = LOW and bits IFMSK, LEVMSK, FRRMSK and BLMSK were set, then this cannot occur
0	0	1	channel found during search; bits BLMSK and FRRMSK are set
0	1	0	not a valid combination
0	1	1	channel found and the band limit has been reached during a search; bits BLMSK and FRRMSK are set
1	0	0	not possible during a preset or a search
1	0	1	a preset or search has been done and the wanted channel has a valid RSSI level but the IF count fails; if bit AHLSI = 1, then bit HLSI must be toggled and a new PLL value must be programmed
1	1	0	not a valid combination
1	1	1	band limit is reached during search; no valid channel found

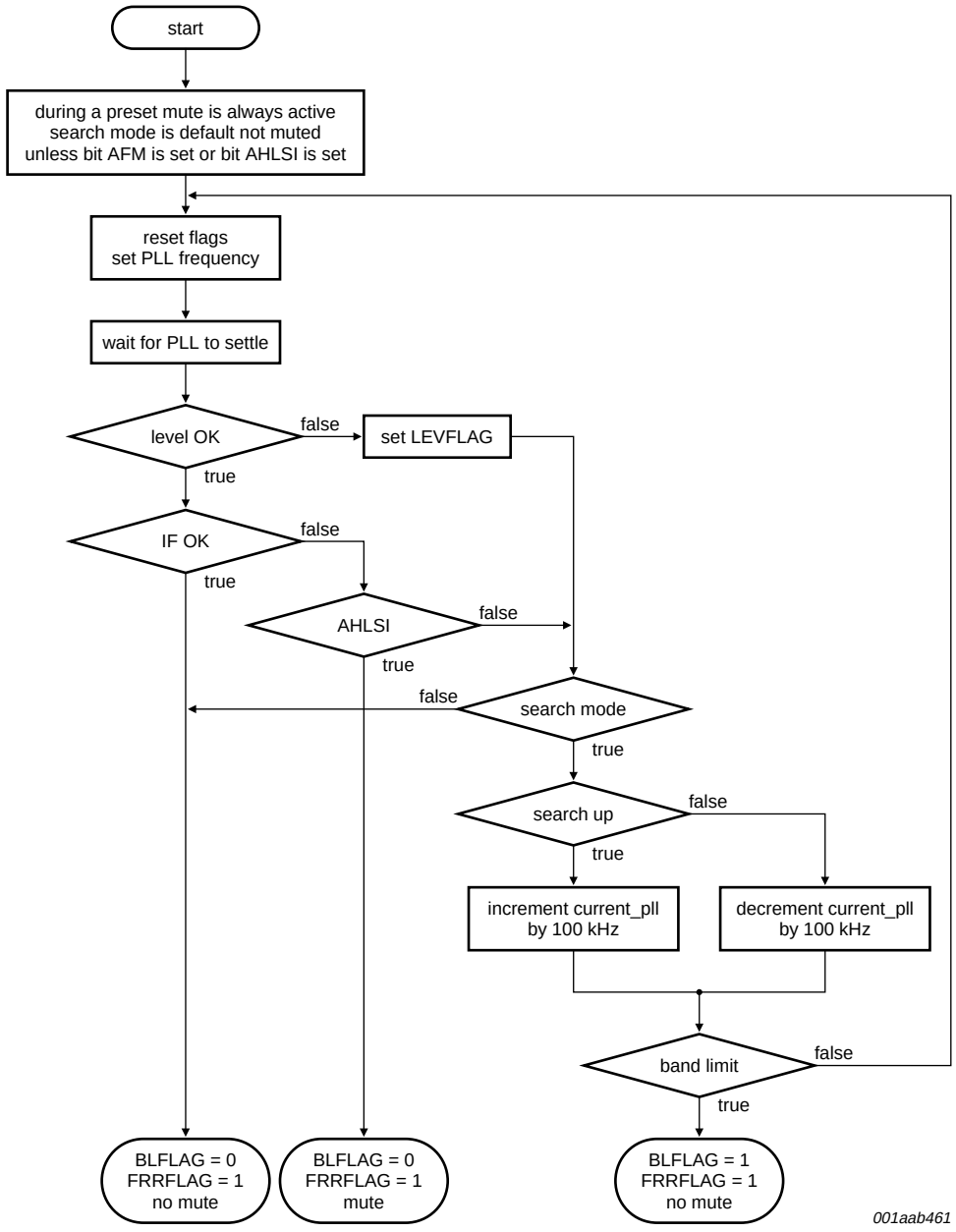


Fig 3. Flowchart auto search or preset

8.20.3 Auto high-side and low-side injection stop switch

When a channel is searched or a preset is done, reception can sometimes be improved when Local Oscillator (LO) injection is done at the other side of the wanted channel.

Bit HLSI toggles the injection of the local oscillator from high-side (bit HLSI = 1) to low-side (bit HLSI = 0). When bit HLSI is toggled, a new PLL setting must be sent to the TEA5761UK.

When bit AHLSI is set to logic 1, the search or preset algorithm will stop after a channel has a valid RSSI level check, but fails the IF count. The microcontroller can now respond by toggling bit HLSI and sending a new PLL value to the tuner.

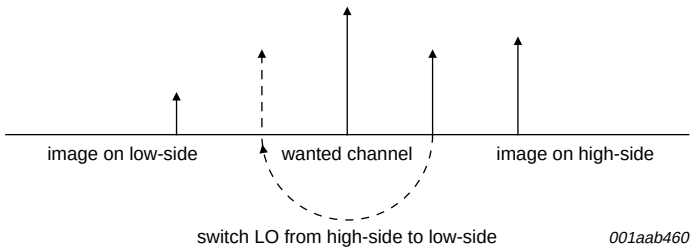


Fig 4. Switch LO from high-side injection to low-side injection using bit HLSI

8.20.4 Muting during search or preset

During a preset the tuner is always muted and is implemented by the algorithm.

A search is not muted by default unless bit AFM = 1 or bit AHLSI = 1.

When bit AHLSI = 1 and the tuner stops during a preset or a search because of a wrong IF count, the tuner stays muted; this allows the microcontroller to switch LO injection mode quietly and wait for the new result.

The tuner is always muted if bit AFM = 1 and is independent of a search or a preset. A search can be muted by setting bit AFM to logic 1 before a search is initiated and resetting it to logic 0 when the tuner is ready (only set bit FRRMSK when initiating a search or preset).

All these mute actions are done by blocking the audio signal inside the soft mute attenuator, so the audio output will keep its DC level and stay low-impedance i.e. 50 Ω (a hard mute set by bit MU will cause a plop).

9. Interrupt handling

9.1 Interrupt register

The first two bytes of the I^2C-bus register contain the interrupt masks and the interrupt flags. A flag is set when it is a logic 1.

Table 6: INTFLAG register- byte0R

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IFFLAG	LEVFLAG	-	FRRFLAG	BLFLAG

Table 7: INTMSK register - byte0W or byte1R

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IFMSK	LEVMSK	-	FRRMSK	BLMSK

The interrupt flag register contains the flags set according to the behavior outlined in Section 9.2. When these flags are set they can also cause pin INTX to go active (hardware interrupt line) depending on the status of the corresponding mask bit in Table 7. A logic 1 in the mask register enables the hardware interrupt for that flag.

Hence, it is conceivable that, with all the mask bits cleared, the software could operate in a continuous polling mode that reads the interrupt flag register for any bits that may be set.

Interrupt mask bits are always cleared after reading the first two bytes of the interrupt register. This is to control multiple hardware interrupts; see Figure 5.

9.1.1 Interrupt clearing

The interrupt flag and mask bits are always cleared after:

- they have been read via the I^2C-bus
- a power-on reset

9.1.2 Timing

The timing sequence for the general operation interrupts is shown in Figure 5 and shows a read access of the interrupt register INTFLAG and a subsequent (though not necessarily immediate) write to the mask register INTMSK. It also indicates the two key timing points A and B_1 or B_2.

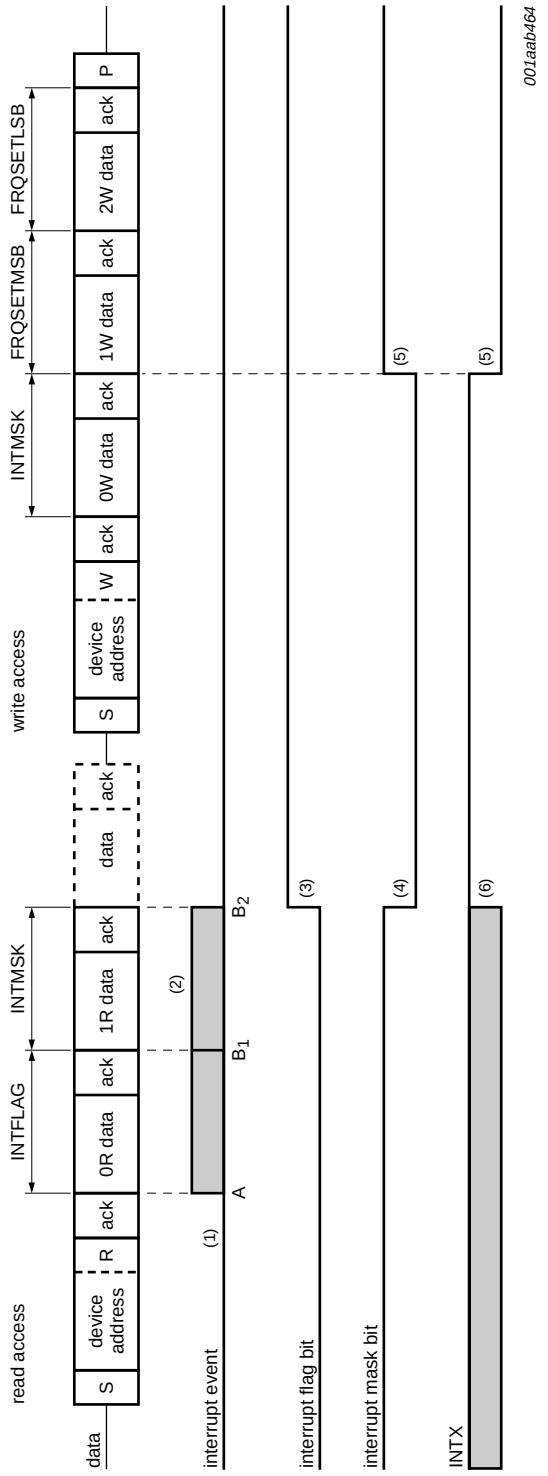
If an interrupt event occurs while the register is being accessed (after point A), it must be held until after the mask register is cleared at the end of the read operation (point B_2).

Point A is after the R/W bit has been decoded and point B_2 is where the acknowledge has been received from the master after the first two bytes have been sent.

The LOW time for the INTX line (t_L) has a maximum value specified in Table 30. However, it can be shorter if a read of the INTMSK and INTFLAG registers occurs within t_L.

9.1.3 Reset

A reset can be performed at any time by a simple read of the interrupt registers (byte0R and byte1R), which automatically clears the interrupt flags and masks.



(1) Interrupt events that occur outside of the region A to B_1 or B_2 set their respective flag bits in the normal way immediately and can thus trigger a hardware interrupt if the mask bits are set.

(2) The blocking of interrupts is marked by the region A to B_1 or B_2, depending on the actual read cycle.
B_1 is when only the INTFLAG register is read and a stop condition is received (only INTFLAG is read, so only this will be cleared).
B_2 is when both registers are read and hence cleared; this is terminated by either an acknowledge or stop bit.

(3) Interrupt events that occur between A and B_1 or B_2 set their respective flags after the mask bits are cleared. This means that in this diagram an interrupt event occurred in period A to B_1 or B_2, so after period A to B_2 the flag goes to logic 1.

(4) All interrupt mask bits are cleared after the interrupt flag and mask registers are read.

(5) Software writes to the mask register and enables the required mask bits. Any flags currently set will then trigger a hardware interrupt.

(6) Pin INTX is set HIGH (inactive) after the interrupt flag and mask registers are read.

Fig 5. I^2C-bus interrupt sequence, read and write operation

9.2 Interrupt flags and behavior

9.2.1 Multiple interrupt events

If the interrupt mask register bit is set then the setting of an interrupt flag for that bit causes a hardware interrupt (pin INTX goes LOW). If the event occurs again, before the flag is cleared, then this does not trigger any further hardware interrupts until that specific flag is cleared. However, two different events can occur in sequence and generate a sequence of hardware interrupts. A second interrupt can be generated only after the INTMSK byte is read, followed by a write as the first interrupt blocks the input of the INTX one-shot generator.

If subsequent interrupts occur within the INTX LOW period then these do not cause the INTX period to extend beyond its specified maximum period (see Section 9.3).

9.2.2 IF frequency flag

During automatic frequency search or preset, the FM part of the TEA5761UK performs a check of the received IF frequency. If an incorrect IF frequency is received, it indicates a detuning situation or the presence of either strong interferers or tuning to an image which sets bit IFFLAG in the INTFLAG register. Also a preset to a channel with no signal may result in a wrong IF count value and hence the setting of bit IFFLAG.

When a search or preset is finished, bit FRRFLAG will be set to indicate this and an interrupt is generated. The microcontroller can now read the outcome of the registers which will contain the IF count value and the IFFLAG status of the channel it is tuned to.

15 ms after the FRRFLAG flag has been set the IF counter will start to run continuously on the tuned frequency and if the conditions for correct frequency are not met then this sets bit IFFLAG in the interrupt register. When bit IFMSK is set this will also cause an interrupt.

Bit IFFLAG is cleared by reading byte0R, or by starting the tuning algorithm.

9.2.3 RSSI threshold flag

The RSSI level voltage reflects the field strength received by the antenna. The voltage level is analog-to-digital converted to a 4-bit value and output via the I^2C-bus. This 4-bit level value can be compared to a threshold level (see Table 21). The level ADC (which converts the analog value to digital) can be triggered to convert in two ways:

1. During a tuning step, which can be a search or a preset, it is triggered by these algorithms and compares the level with the threshold set by bits SSL[1:0]. Bit LEVFLAG is set if the RSSI level drops below the threshold level set by bits SSL[1:0]; see Table 15. The hardware interrupt is only generated if the corresponding mask bit is set.
2. After a search or a preset, the threshold for comparison is switched to the hysteresis level. The hysteresis level is set by the level bits and can be selected using bit LHSW (see Table 21). Then it waits 15 ms and the level ADC starts to run automatically and compares the level each 500 µs with this hysteresis level. Bit LEVFLAG is set if the RSSI level drops below the threshold level set by the LH bits; the hardware interrupt is only generated if the corresponding mask bit is set. Bit LHSW allows either a small or a large hysteresis to be selected. When a search or preset is done with the ADC level set to 3 then when the algorithm has finished, the threshold level is set to 0. Hence the LEVFLAG will never be set.

Bit LEVFLAG is cleared when the interrupt register INTFLAG is read.

9.2.4 Frequency ready flag

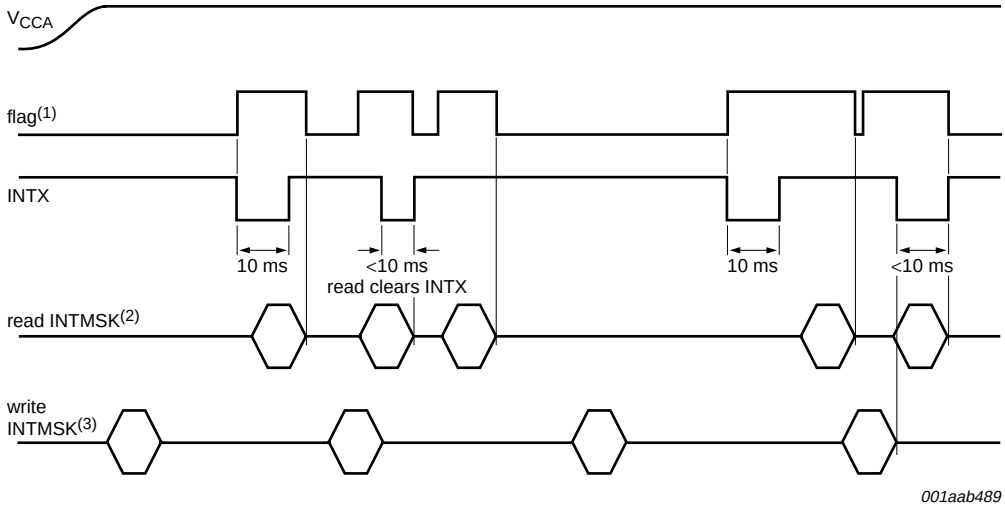
The frequency ready flag bit FRRFLAG is set to logic 1 when the automatic tuning has finished a search or preset. The description of this bit is given in Table 5. This bit is cleared when the INTMSK register is read.

9.2.5 Band limit flag

The band limit bit BLFLAG is set to logic 1 when the automatic tuning has detected the end of the tuning band or when the PLL cannot lock on a certain frequency. This bit is described in Table 5. This bit is cleared when the INTMSK register is read.

9.3 Interrupt output

The interrupt line driver is a MOS transistor with a nominal sink current of 380 μA. It is pulled HIGH by an 18 kΩ resistor connected to pin VREFDIG. The interrupt line can be connected to one other similar device with an interrupt output and an 18 kΩ pull-up resistor providing a wired-OR function. This allows any of the drivers to pull the interrupt line LOW by sinking the current. When a flag is set and not masked it generates an interrupt; see Figure 6.



(1) When flag is set, the next interrupts are blocked until INTMSK is read from or written to.

(2) Reading INTMSK clears flag, INTMSK and INTX.

(3) Writing INTMSK enables INTX.

Fig 6. Interrupt line behavior

10. I²C-bus interface

The I²C-bus interface is based on *The I²C-bus specification*, version 2.1 January 2000, expanded by the following definitions.

10.1 Write and Read mode

S	BYTE 1		A	BYTE 2	A	BYTE n	A	BYTE 8	NAK	P
	chip address	R/$\overline{W}$		byte0W		.....		byte6W		
	0010 0000	0		xxxx xxxx		xxxx xxxx		xxxx xxxx		

001aac341

Fig 7. Write mode

S	BYTE 1		A	BYTE 2	A	BYTE n	A	BYTE 17	A	P
	chip address	R/W		byte0R		.....		byte15R		
	0010 0000	1		xxxx xxxx		xxxx xxxx		xxxx xxxx		

001aac342

Fig 8. Read mode

Table 8: I²C-bus transfer description

Code	Description
S	START condition
Byte 1	I²C-bus chip address (7 bits)
	R/$\overline{W}$ = 0 for write action and R/$\overline{W}$ = 1 for read action
A	acknowledge (SDA = LOW)
Byte 2, etc.	data byte (8 bits)
NAK	non acknowledge (SDA = HIGH)
P	STOP condition

10.2 Data transfer

Structure of the I²C-bus:

- Slave transceiver
- Subaddresses not used
- Maximum LOW-level input voltage: $V_{IL} = 0.3 \times V_{VREFDIG}$
- Minimum HIGH-level input voltage: $V_{IH} = 0.7 \times V_{VREFDIG}$

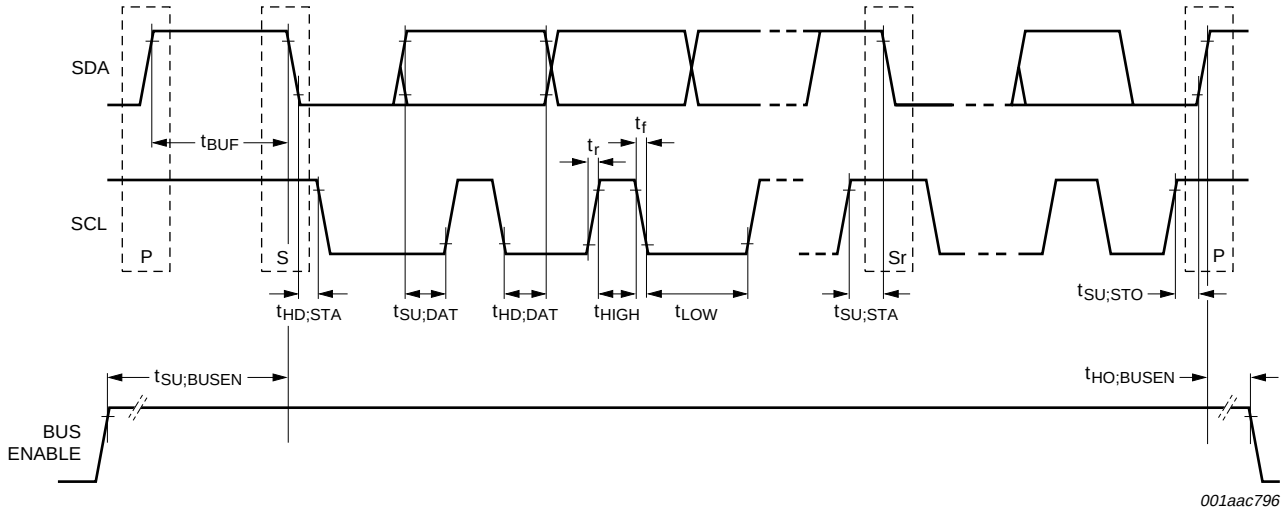
Remark: The I²C-bus operates at a maximum clock rate of 400 kHz. It is not allowed to connect the TEA5761UK to an I²C-bus operating at a higher clock rate.

Data transfer to the TEA5761UK:

- Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.
- The LSB indicates the write or read action.
- The data becomes valid byte-wise at the appropriate falling edge of the SCL clock.
- A STOP condition after any byte can shorten transmission times. When writing to the transceiver by using the STOP condition before completion of the whole transfer:
  - The remaining bytes will contain the old information.
  - If the transfer of a byte is not completed the new bits will be used, but a new tuning cycle will not be started.

I^2C-bus activity:

- With bit PUPD the TEA5761UK can be switched in a low current Standby mode. The I^2C-bus is then still active.
- When the I^2C-bus interface is deactivated, by making pin BUSENABLE LOW and without programmed Standby mode, the TEA5761UK keeps its normal operation, but is isolated from the I^2C-bus lines.
- Bus traffic can be started 10 µs after activating the bus again by making pin BUSENABLE HIGH.



t_f = fall time of both SDA and SCL signals: 20 + 0.1 C_b < t_f < 300 ns, where C_b = total capacitance on bus line in pF.

t_r = rise time of both SDA and SCL signals: 20 + 0.1 C_b < t_r < 300 ns, where C_b = total capacitance on bus line in pF.

$t_{HD;STA}$ = hold time (repeated) START condition. After this period, the first clock pulse is generated: > 600 ns.

t_{HIGH} = HIGH period of the SCL clock: > 600 ns.

$t_{SU;STA}$ = setup time for a repeated START condition: > 600 ns.

$t_{HD;DAT}$ = data hold time: 300 < $t_{HD;DAT}$ < 900 ns.

Remark: 300 ns lower limit is added because the ASIC has no internal hold time for the SDA signal.

$t_{SU;DAT}$ = data setup time: $t_{SU;DAT}$ > 100 ns. If ASIC is used in a standard mode I^2C-bus system, $t_{SU;DAT}$ > 250 ns.

$t_{SU;STO}$ = setup time for STOP condition: > 600 ns.

t_{BUF} = bus free time between a STOP and a START condition: > 600 ns.

C_b = capacitive load of one bus line: < 400 pF.

$t_{SU;BUSEN}$ = bus enable setup time: $t_{SU;BUSEN}$ > 10 µs.

$t_{HO;BUSEN}$ = bus enable hold time: $t_{HO;BUSEN}$ > 10 µs.

Fig 9. Bus timing diagram

10.3 Register map

Table 9: Register overview

Byte number		Byte name	Access	Reset value	Reference
Read	Write				
0R		INTFLAG	R	00h	Table 10
1R	0W	INTMSK	R/W	00h	Table 11
2R	1W	FRQSETMSB	R/W	80h	Table 12
3R	2W	FRQSETLSB	R/W	00h	Table 13
4R	3W	TNCTRL1	R/W	08h	Table 14
5R	4W	TNCTRL2	R/W	D2h	Table 15
6R		FRQCHKMSB	R	-	Table 16
7R		FRQCHKLSB	R	-	Table 17
8R		IFCHK	R	-	Table 18
9R		LEVCHK	R	-	Table 19
10R	5W	TESTBITS	R/W	00h	Table 20

Table 9: Register overview *…continued*

Byte number		Byte name	Access	Reset value	Reference
Read	Write				
11R	6W	TESTMODE	R/W	00h	Table 22
12R		MANID1	R	40h	Table 24
13R		MANID2	R	2Bh	Table 25
14R		CHIPID1	R	57h	Table 26
15R		CHIPID2	R	61h	Table 27

10.4 Byte description

Table 10: INTFLAG - interrupt flag byte0R description

Bit	Symbol	Access	Reset	Description
7 to 5	-	-	-	reserved
4	IFFLAG	R	0	1 = IF count is not correct
3	LEVFLAG	R	0	continuous checking of the RSSI level 1 = RSSI level has dropped below $V_{SSL[1:0]} - V_{hys}$ during a tuning cycle (preset or search) 1 = RSSI level has dropped below $V_{SSL[1:0]}$
2	-	-	-	-
1	FRRFLAG	R	0	1 = tuner state machine is ready
0	BLFLAG	R	0	1 = during a search the band limit has been reached or time out

Table 11: INTMSK - interrupt mask byte1R and byte0W description

Bit	Symbol	Access	Reset	Description
7 to 5	-	-	-	reserved
4	IFMSK	R/W	0	masks bit IFFLAG
3	LEVMSK	R/W	0	masks bit LEVFLAG
2	-	-	-	reserved
1	FRRMSK	R/W	0	masks bit FRRFLAG
0	BLMSK	R/W	0	masks bit BLFLAG

Table 12: FRQSETMSB - frequency setting MSB byte2R and byte1W description

Bit	Symbol	Access	Reset	Description
7	SUD	R/W	1	1 = search up
				0 = search down
6	SM	R/W		1 = Search mode
			0	0 = Preset mode

Table 12: FRQSETMSB - frequency setting MSB byte2R and byte1W description *...continued*

Bit	Symbol	Access	Reset	Description
5	FR13	R/W	0	PLL frequency set bits
4	FR12	R/W	0	
3	FR11	R/W	0	
2	FR10	R/W	0	
1	FR09	R/W	0	
0	FR08	R/W	0	

Table 13: FRQSETLSB - frequency setting LSB byte3R and byte2W description

Bit	Symbol	Access	Reset	Description
7	FR07	R/W	1	PLL frequency set bits
6	FR06	R/W	1	
5	FR05	R/W	0	
4	FR04	R/W	1	
3	FR03	R/W	0	
2	FR02	R/W	0	
1	FR01	R/W	1	
0	FR00	R/W	0	

Table 14: TNCTRL1 - tuner control register byte4R and byte3W description

Bit	Symbol	Access	Reset	Description
7	-	-	0	reserved
6	PUPD0	R/W		power-up and power-down
				1 = FM on
			0	0 = FM off
5	BLIM	R/W		1 = Japanese FM band 76 MHz to 90 MHz
			0	0 = US/Europe FM band 87.5 MHz to 108 MHz
4	SWPM	R/W		1 = output pin SWPORT is bit FRRFLAG
			0	0 = output pin SWPORT is bit SWP
3	IFCTC	R/W	1	1 = IF count time is 15.625 ms
				0 = IF count time is 1.953 ms
2	AFM	R/W		1 = left and right audio muted
			0	0 = audio not muted
1	SMUTE	R/W		1 = soft mute on
			0	0 = soft mute off
0	SNC	R/W		1 = stereo noise cancellation on
			0	0 = stereo noise cancellation off

Table 15: TNCTRL2 - tuner control register byte5R and byte4W description

Bit	Symbol	Access	Reset	Description
7	MU	R/W	1	1 = left and right audio hard mute
				0 = no hard mute
6 to 5	SSL[1:0]	R/W		search stop level (see Table 21)
				00 = ADC3
				01 = ADC5
			10	10 = ADC7
				11 = ADC10
4	HLSI	R/W	1	1 = high-side injection
				0 = low-side injection
3	MST	R/W		1 = forced mono
			0	0 = stereo on
2	SWP	R/W		1 = pin SWPORT is HIGH
			0	0 = pin SWPORT is LOW
1	DTC	R/W	1	1 = de-emphasis time constant = 50 µs
				0 = de-emphasis time constant = 75 µs
0	AHLSI	R/W		1 = tuner will stop during search on failed IF count and correct level
			0	0 = tuner will search continuously

Table 16: FRQCHKMSB - frequency check register byte6R description

Bit	Symbol	Access	Reset	Description
7	-	-	-	reserved
6	-	-	-	reserved
5	PLL13	R	-	frequency found bit 13 (MSB)
4	PLL12	R	-	frequency found bit 12
3	PLL11	R	-	frequency found bit 11
2	PLL10	R	-	frequency found bit 10
1	PLL09	R	-	frequency found bit 9
0	PLL08	R	-	frequency found bit 8

Table 17: FRQCHKLSB - frequency check register byte7R description

Bit	Symbol	Access	Reset	Description
7	PLL07	R	-	frequency found bit 7
6	PLL06	R	-	frequency found bit 6
5	PLL05	R	-	frequency found bit 5
4	PLL04	R	-	frequency found bit 4
3	PLL03	R	-	frequency found bit 3
2	PLL02	R	-	frequency found bit 2
1	PLL01	R	-	frequency found bit 1
0	PLL00	R	-	frequency found bit 0 (LSB)

Table 18: IFCHK - tuner check register byte8R description

Bit	Symbol	Access	Reset	Description
7	IF6	R	-	IF count bit 6 (MSB)
6	IF5	R	-	IF count bit 5
5	IF4	R	-	IF count bit 4
4	IF3	R	-	IF count bit 3
3	IF2	R	-	IF count bit 2
2	IF1	R	-	IF count bit 1
1	IF0	R	-	IF count bit 0 (LSB)
0	TUNTO	R	-	1 = PLL tuning time out
				0 = PLL has settled

Table 19: LEVCHK - tuner check register byte9R description

Bit	Symbol	Access	Reset	Description
7	LEV3	R	-	level count bit 3 (MSB)
6	LEV2	R	-	level count bit 2
5	LEV1	R	-	level count bit 1
4	LEV0	R	-	level count bit 0 (LSB)
3	LD	R	-	1 = PLL is locked
				0 = PLL is not locked
2 [1]	STEREO	R	-	1 = Pilot detected
				0 = no Pilot detected
1	-	-	-	reserved
0	-	-	-	reserved

[1] This bit does not switch the radio from mono to stereo, this depends on the RF input level as shown in sections ‘Mono stereo blend’ and Mono stereo switched’ in Table 33.

Table 20: TESTBITS - test bits register byte10R and byte5W description

Bit	Symbol	Access	Reset	Description
7	LHM	R/W		1 = left audio output is hard muted
			0	0 = left audio output is not hard muted
6	RHM	R/W		1 = right audio output is hard muted
			0	0 = right audio output is not hard muted
5	-	-	0	-
4	LHSW	R/W		1 = level hysteresis is large (see Table 21)
			0	0 = level hysteresis is small
3	TRIGFR	R/W		1 = reference frequency selected pin FREQIN
			0	0 = crystal as reference pin XTAL
2	LDX	R/W		1 = local DX on, –6 dB gain of LNA
			0	0 = local DX off, LNA has normal gain

Table 20: TESTBITS - test bits register byte10R and byte5W description *...continued*

Bit	Symbol	Access	Reset	Description
1	RFAGC	R/W		1 = RF AGC off
			0	0 = RF AGC on
0	INTCTRL	R/W		1 = interrupt generation on pin INTX enabled
			0	0 = interrupt generation disabled

Table 21: LH - RSSI level hysteresis

Bits SSL[1:0]	RSSI ADC search stop level	Bit LHSW	RSSI hysteresis threshold level
00	3	X	0
01	5	1	1
		0	2
10	7	1	3
		0	4
11	10	1	5
		0	7

Table 22: TESTMODE - Test mode register byte11R and byte6W description

Bit	Symbol	Access	Reset	Description
7	DETT	R/W		1 = fast 4 ms
			0	0 = slow 8 ms
6	-	-	-	reserved
5	-	-	-	reserved
4	TM	R/W		1 = TEA5761UK in Test mode and software port outputs according to Table 23
			0	0 = normal operation
3	TB3	R/W	0	test bits select the signals outputted to pin SWPORT when bit SWPM = 0; see Table 23
2	TB2	R/W	0	
1	TB1	R/W	0	
0	TB0	R/W	0	

Table 23: Test bits (SWPM = 0)

TB3	TB2	TB1	TB0	Pin SWPORT output
0	0	0	0	bit SWP of byte 4W or bit FRRFLAG (SWPM = 1)
0	0	0	1	oscillator output 32.768 kHz (TM = 1)
0	0	1	0	lock detect bit LD (TM = 1)
0	0	1	1	pilot detected (TM = 1)
0	1	0	0	programmable divider (TM = 1)
0	1	0	1	reserved
:	:	:	:	:
1	1	1	1	reserved

Table 24: MANID1 - manufacturer identification register byte12R description

Bit	Symbol	Access	Reset	Description
7	VERSION3	R	0	version code; default 0100
6	VERSION2	R	1	
5	VERSION1	R	0	
4	VERSION0	R	0	
3	MANID10	R	0	manufacturer ID code; default 0000 (001 0101)
2	MANID9	R	0	
1	MANID8	R	0	
0	MANID7	R	0	

Table 25: MANID2 - manufacturer identification register byte13R description

Bit	Symbol	Access	Reset	Description
7	MANID6	R	0	manufacturer ID code; default (0000) 001 0101
6	MANID5	R	0	
5	MANID4	R	1	
4	MANID3	R	0	
3	MANID2	R	1	
2	MANID1	R	0	
1	MANID0	R	1	
0	IDAV	R	1	1 = chip has manufacturer ID
				0 = chip has no ID

Table 26: CHIPID1 - chip identification register byte14R description

Bit	Symbol	Access	Reset	Description
7	CHIPID15	R	0	TEA5761UK chip identification code: 1st digit = 5
6	CHIPID14	R	1	
5	CHIPID13	R	0	
4	CHIPID12	R	1	
3	CHIPID11	R	0	TEA5761UK chip identification code: 2nd digit = 7
2	CHIPID10	R	1	
1	CHIPID9	R	1	
0	CHIPID8	R	1	

Table 27: CHIPID2 - chip identification register byte15R description

Bit	Symbol	Access	Reset	Description
7	CHIPID7	R	0	TEA5761UK chip identification code: 3rd digit = 6
6	CHIPID6	R	1	
5	CHIPID5	R	1	
4	CHIPID4	R	0	

Table 27: CHIPID2 - chip identification register byte15R description *...continued*

Bit	Symbol	Access	Reset	Description
3	CHIPID3	R	0	TEA5761UK chip identification code: 4th digit = 1
2	CHIPID2	R	0	
1	CHIPID1	R	0	
0	CHIPID0	R	1	

11. Limiting values

Table 28: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCD}	digital supply voltage			–0.3	+5.5	V
V_{CCA}	analog supply voltage			–0.3	+8	V
V_{LO1}	VCO tuned circuit output 1			–0.3	+8	V
V_{LO2}	VCO tuned circuit output 2			–0.3	+8	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		CDM	[2]	-	±500	V
		MM	[3]	-	±200	V

[1] Human body model (R = 1.5 kΩ, C = 100 pF).

[2] Charged device model (*"JEDEC standard JESD22-C101"*).

[3] Machine model (R = 0 Ω, C = 200 pF).

12. Static characteristics

Table 29: Supply characteristics

The listed parameters are valid when a crystal is used with the requirements stated in Table 31.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA}	analog supply voltage			2.4	2.7	3.6	V
V_{CCD}	digital supply voltage			2.4	2.7	3.6	V
I_{CCA}	analog supply current	V_{CCA} = 2.7 V					
		Operating mode		10	14	16.5	mA
		Standby mode		-	2.0	6.0	µA
I_{CCD}	digital supply current	V_{CCD} = 2.7 V					
		Operating mode		5	15	20	µA
		Standby mode		1	3.3	20	µA
T_{amb}	ambient temperature	$V_{CCA} = V_{CCD}$ = 2.7 V; V_{CD1} = 2.7 V; $V_{VREFDIG}$ = 1.8 V	[1]	–20	-	+85	°C
P_{tot}	total power dissipation			-	38	-	mW

[1] Crystal influence not included.

Table 30: Control input and output characteristics

$V_{CCA} = V_{CCD}$ = 2.7 V; T_{amb} = 25 °C; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference for I²C-bus interface: pin VREFDIG						
$V_{VREFDIG}$	digital reference voltage	$V_{VREFDIG} \leq V_{CCD}$	1.65	1.8	V_{CCD}	V
$I_{VREFDIG}$	digital reference current	Operating mode; $V_{VREFDIG}$ = 1.65 V to V_{CCD}	-	0.5	2.0	µA
Logic inputs: pins BUSENABLE, SCL and SDA						
R_i	input resistance		10	-	-	MΩ
V_{IH}	HIGH-level input voltage	input switching level up	$0.7 \times V_{VREFDIG}$	-	$V_{VREFDIG}$ + 0.3	V
V_{IL}	LOW-level input voltage	input switching level down	0	-	$0.3 \times V_{VREFDIG}$	V
Software programmable output port: pin SWPORT						
V_{OH}	HIGH-level output voltage	I_{source} = 150 µA	$V_{VREFDIG}$ – 0.45	-	$V_{VREFDIG}$	V
V_{OL}	LOW-level output voltage	I_{sink} = 150 µA	0	0.2	0.45	V
$I_{sink(max)}$	maximum sink current		250	-	2000	µA
$I_{source(max)}$	maximum source current		250	-	500	µA
Interrupt output: pin INTX [1]						
V_{OH}	HIGH-level output voltage	$V_{VREFDIG}$ = 1.65 V; pull-up resistance of second device connected to INTX is 18 kΩ, or maximum load current is 100 µA	$V_{VREFDIG}$ – 0.2	-	$V_{VREFDIG}$ + 0.2	V
V_{OL}	LOW-level output voltage		0.13	0.22	0.4	V

Table 30: Control input and output characteristics *...continued*

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{source(max)}$	maximum source current (pull-down)	including internal pull-up resistor	260	380	615	µA
R_{pu}	pull-up resistance		14.4	18	22.5	kΩ
t_L	LOW time	one-shot pulse time; when the LOW period is not shortened by a read action	9.9	9.98	10	ms

[1] $V_{VREFDIG} \geq 1.65$ V; R_{pu} of second device connected to pin INTX is 18 kΩ ± 20 %.

13. Dynamic characteristics

Table 31: Oscillators, clocks and synthesizer characteristics

V_{CCA} = V_{CCD} = 2.7 V; $V_{VREFDIG}$ = 1.8 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage controlled oscillator						
f_{osc}	oscillator frequency		150	-	217	MHz
Reference frequency input: pin FREQIN						
V_I	DC input voltage	oscillator externally clocked	0	-	1.95	V
R_i	input resistance	oscillator externally clocked with f_i = 32.768 kHz	500	-	-	kΩ
C_i	input capacitance	oscillator externally clocked with f_i = 32.768 kHz	5	6	7	pF
f_{rsn}	resonance frequency		-	32.768	-	kHz
Δf_{rsn}	resonance frequency deviation		–20	-	+20	ppm
		T_{amb} = –20 °C to +75 °C	–150	-	+150	ppm
δ	duty cycle	square wave	30	-	70	%
V_{IH}	HIGH-level input voltage	square wave	0.9	-	1.95	V
V_{IL}	LOW-level input voltage	square wave	0	-	0.55	V
J	jitter	integrated over 300 Hz to 15 kHz	-	-	1	Hz
Crystal oscillator input 32.768 kHz: pin XTAL						
f_{rsn}	resonance frequency		-	32.768	-	kHz
Δf_{rsn}	resonance frequency deviation		–20	-	+20	ppm
C_{shunt}	shunt capacitance		-	-	3.5	pF
C_m	motional capacitance		1.5	-	3.0	fF
R_s	series resistance		-	-	75	kΩ

Table 31: Oscillators, clocks and synthesizer characteristics *...continued*

V_{CCA} = V_{CCD} = 2.7 V; $V_{VREFDIG}$ = 1.8 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Synthesizer						
Programmable divider						
D/D_{prog}	programmable divider ratio	FRQSETMSB[5:0] = XX01 1111; FRQSETLSB[7:0] = 1111 1111	-	-	8191	
		FRQSETMSB[5:0] = XX00 1000; FRQSETLSB[7:0] = 0000 0000	2048	-	-	
$D_{step(prog)}$	programmable divider step size		-	1	-	
Charge pump output: pin CPOUT						
$I_{M(sink)}$	peak sink current	V_{CPOUT} = 0.2 V to (V_{CD1} – 0.2 V); $f_{VCO} > f_{ref} \times$ div_ratio	2	4	8	µA
$I_{M(source)}$	peak source current	V_{CPOUT} = 0.2 V to (V_{CD1} – 0.2 V); $f_{VCO} < f_{ref} \times$ div_ratio	–2	–4	–8	µA

Table 32: IF counter characteristics

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF counter						
N	length		-	7	-	bit
V_{sens}	sensitivity voltage		-	6	18	µV (EMF)
n_{count}	count result for search stop	20 µV < V_{RF} < 1 V	31h	-	3Ch	
T	period	f_{xtal} = 32768 Hz				
		bit IFCTC = 1	-	15625	-	µs
		bit IFCTC = 0	-	1953	-	µs
f_{res}	frequency resolution	f_{xtal} = 32768 Hz	-	4096	-	Hz

Table 33: FM signal channel characteristics

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM RF input: pins RFIN1 and RFIN2						
$f_{i(FM)}$	FM input frequency		76	-	108	MHz
$V_{sens(EMF)}$	sensitivity EMF value voltage	f_{RF} = 76 MHz to 108 MHz; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; TC_{deem} = 75 µs, A-weighting filter; B_{aud} = 300 Hz to 15 kHz; see Figure 10	-	2.2	3.6	µV (EMF)
$IP3_{in}$	in-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tune} = 76 MHz to 108 MHz; RF_{agc} = off	81	87	-	dBµV
$IP3_{out}$	out-of-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$	Δf_1 = 4 MHz; Δf_2 = 8 MHz; f_{tune} = 76 MHz to 108 MHz; RF_{agc} = off	87	93	-	dBµV

Table 33: FM signal channel characteristics *…continued*

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_i	input resistance	connected to pin GNDRF	75	100	125	Ω
C_i	input capacitance	connected to pin GNDRF	2.5	4	6	pF
In-band AGC						
$V_{i(AGC)(min)}$	minimum RF AGC input voltage	f_{RF} = 98 MHz; $\Delta V_{ind(IF)}$ / $\Delta V_{i(RF)}$ < 4 mV/dBµV	55	61	67	dBµV
Wideband AGC						
$V_{i(RF)}$	RF input voltage	f_{RF1} = 93 MHz; f_{RF2} = 98 MHz; V_{RF2} = 50 dBµV; $\Delta V_{ind(IF)}$ / $\Delta V_{i(RF)}$ < 4 mV/dBµV; radio tuned to 98 MHz	66	72	78	dBµV
IF filter						
f_{center}	center frequency		215	225	235	kHz
B	bandwidth		85	94	102	kHz
S	selectivity	f_{tune} = 76 MHz to 108 MHz [1]				
		high-side; Δf = +200 kHz	39	43	-	dB
		low-side; Δf = –200 kHz	32	36	-	dB
		high-side; Δf = +100 kHz	8	12	-	dB
		low-side; Δf = –100 kHz	8	12	-	dB
IR	image rejection	f_{tune} = 76 MHz to 108 MHz; V_{RF} = 50 dBµV	24	30	-	dB
FM IF level detector and mute voltage						
Level detector RF input						
$V_{ADC(start)}$	ADC start voltage		2	3	5	µV
G_{step}	step resolution gain	correct code integrity tested	2	3	5	dB
Mute output: pin TMUTE						
$V_{ind(IF)}$	IF indication voltage	V_{RF} = 0 µV	1.5	1.6	1.75	V
		V_{RF} = 3 µV	1.55	1.65	1.8	V
$V_{slope(ind)IF}$	IF indication voltage slope	definition: $\Delta V_{slope(ind)IF}$ = $\Delta V_{ind(IF)}$ / ΔV_{RF}; V_{RF} = 10 µV to 500 µV	130	165	200	mV/ 20dB
R_{TMUTE}	pin TMUTE output resistance		280	400	520	kΩ
FM demodulator: MPX output						
(S+N)/N(m)	maximum signal-to-noise ratio, mono	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs; A-weighting filter; B_{aud} = 300 Hz to 15 kHz	53	57	-	dBA
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; f_{mod} = 1 kHz; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz				
		Δf = 75 kHz	-	0.4	1	%
		Δf = 100 kHz; see Figure 12	-	-	1.5	%

Table 33: FM signal channel characteristics *...continued*

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

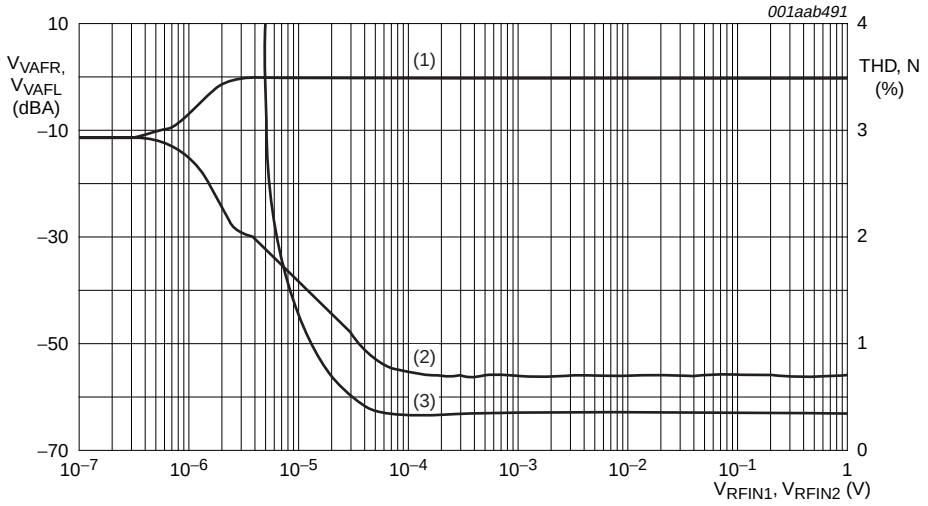
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM_{sup}	AM suppression	L = R; f_{mod} = 1 kHz; V_{RF} = 100 µV to 10 mV; m = 0.3; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz	40	-	-	dB
FM demodulator output: pin MPXOUT						
V_o	output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz	60	75	85	mV
R_o	output resistance		-	-	500	Ω
I_{sink}	sink current		30	-	-	µA
Soft mute; SMUTE = 1; Δf = 22.5 kHz; f_{mod} = 1 kHz						
$V_{start(mute)}$	mute start voltage	relative to V_{VAFL} at V_{RF} = 1 mV; α_{mute} = 3 dB	3	5	10	µV
α_{mute}	mute attenuation	V_{RF} = 1 µV; L = R; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz	10	20	30	dB
MPX decoder						
α_{ODi}	input overdrive range	THD < 3 %	4	-	-	dB
α_{cs}	channel separation	V_{RF} = 1 mV; Δf = 75 kHz; including 9 % pilot deviation; R = 0 and L = 1 or R = 1 and L = 0; f_{mod} = 1 kHz; bit MST = 0; bit SNC = 1; B_{aud} = 300 Hz to 15 kHz	22	27	-	dB
f_u	upper –3 dB bandwidth	V_{RF} = 1 mV; Δf = 22.5 kHz; L = R; pre-emphasis = 75 µs; de-emphasis = 75 µs; no audio filter	13	15	17	kHz
f_l	lower –3 dB bandwidth		-	20	30	Hz
(S+N)/N(m)	maximum signal-to-noise ratio, mono	V_{RF} = 1 mV; Δf = 22.5 kHz; L = R; f_{mod} = 1 kHz; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz; A-weighting filter	53	57	-	dBA
(S+N)/N(s)	maximum signal-to-noise ratio, stereo	V_{RF} = 1 mV; Δf = 22.5 kHz; L = R; f_{mod} = 1 kHz; f_{pilot} = 6.75 kHz; TC_{deem} = 75 µs; B_{aud} = 300 Hz to 15 kHz; A-weighting filter	49	53	-	dBA
THD	total harmonic distortion, stereo	V_{RF} = 1 mV; Δf = 75 kHz; L = R; including 9 % pilot deviation; f_{mod} = 1 kHz; TC_{deem} = 75 µs	-	0.9	2.5	%
$\alpha_{sup(pilot)}$	pilot suppression	measured at pins VAFL and VAFR related to Δf = 75 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs	40	50	-	dB
Δf_{pilot1}	pilot frequency deviation 1	V_{RF} = 1 mV; bit STEREO = 1	2.5	-	5.8	kHz
Δf_{pilot2}	pilot frequency deviation 2	V_{RF} = 1 mV; bit STEREO = 0	1.0	-	3.6	kHz
$\alpha_{hys(pilot)}$	pilot tone detection hysteresis	definition: $f_{pilot(hys)} = \Delta f_{pilot1} / \Delta f_{pilot2}$; V_{RF} = 1 mV	2	-	6	dB
TC_{deem}	de-emphasis time constant	V_{RF} = 1 mV				
		bit DTC = 1	38	50	62	µs
		bit DTC = 0	57	75	93	µs

Table 33: FM signal channel characteristics *…continued*

V_{CCA} = V_{CCD} = 2.7 V; T_{amb} = 25 °C; measured with test circuit in Figure 13; all AC values are given in RMS; minimum and maximum values include spread due to the applied voltage from 2.5 V to 3.6 V and process spread; unless otherwise specified; all RF input values are defined in potential difference (PD), except when EMF is explicitly stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MPX decoder output: pins VAFR and VAFL						
V_{VAFL}	left audio output voltage on pin VAFL	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs	60	75	90	mV
V_{VAFR}	right audio output voltage on pin VAFR	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; TC_{deem} = 75 µs	60	75	90	mV
$\Delta V_{O(VAFL-VAFR)}$	output voltage difference between pins VAFL and VAFR	definition: $\Delta V_{O(VAFL-VAFR)} = V_{VAFL} / V_{VAFR}$; V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz, including 9 % pilot deviation; TC_{deem} = 75 µs	–0.5	-	+0.5	dB
$R_{O(VAFL)}$	output resistance pin VAFL	MU = LHM = RHM = 0	50	-	100	Ω
		MU = LHM = RHM = 1	500	-	-	kΩ
$R_{O(VAFR)}$	output resistance pin VAFR	MU = LHM = RHM = 0	50	-	100	Ω
		MU = LHM = RHM = 1	500	-	-	kΩ
$I_{sink(VAFL)}$	sink current on pin VAFL		170	-	-	µA
$I_{sink(VAFR)}$	sink current on pin VAFR		170	-	-	µA
Mono stereo blend: bit SNC = 1						
$V_{start(blend)}$	blend start voltage	stereo channel separation = 1 dB; with increasing input levels the radio switches gradually from mono to stereo	7	10	18	µV
α_{cs}	channel separation	V_{RF} = 40 µV; Δf = 75 kHz; R = 0 and L = 1 or R = 1 and L = 0; including 9 % pilot deviation; f_{mod} = 1 kHz; bit MST = 0	4	10	16	dB
Mono stereo switching; Δf = 75 kHz including 9 % pilot deviation; f_{mod} = 1 kHz; SNC = 0						
α_{cs}	channel separation	MST = 0; R = 1 and L = 0 or R = 0 and L = 1				
		from mono to stereo with increasing RF input level	22	-	-	dB
		from stereo to mono with decreasing RF input level	-	-	1	dB
V_{sw}	switching voltage		25	35	60	µV
hys	hysteresis		1	3	4	dB
Bus driven mute functions						
Tuning mute; AFM = 1						
α_{mute}	mute depth on pins VAFL and VAFR	bit AFM = 1	–60	-	-	dB
$\alpha_{mute(VAFR)}$	mute depth on pin VAFR	bit AFM = 1; bit RHM = 1	–80	-	-	dB
$\alpha_{mute(VAFL)}$	mute depth on pin VAFL	bit AFM = 1; bit LHM = 1	–80	-	-	dB

[1] Low-side and high-side selectivity can be measured by changing the mixer LO injection from high-side to low-side.

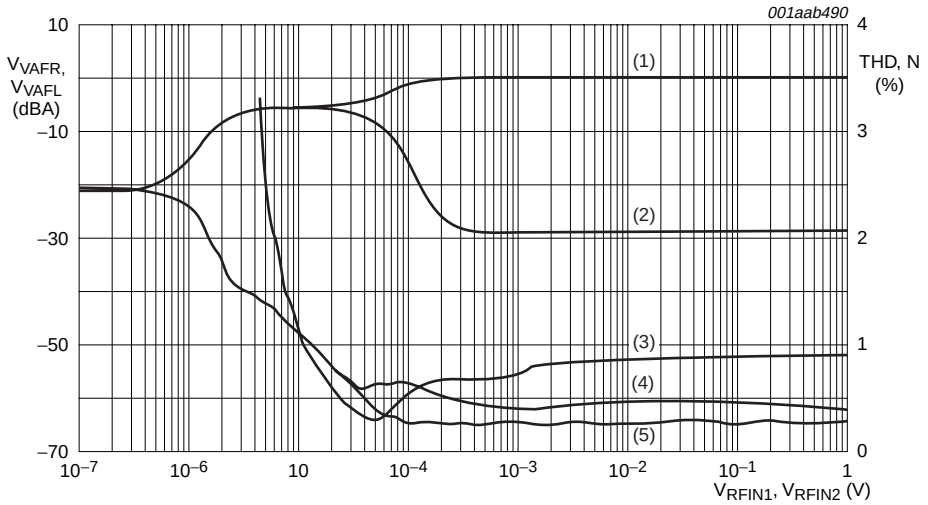


(1) Mono signal: soft mute off, Δf = 22.5 kHz.

(2) Noise in Mono mode, soft mute off, Δf = 0 kHz.

(3) Total harmonic distortion, Δf = 75 kHz.

Fig 10. FM characteristics mono



(1) V_{AFL} signal, modulation left, SNC on, Δf = 67.5 kHz; Δf_{pilot} = 6.75 kHz.

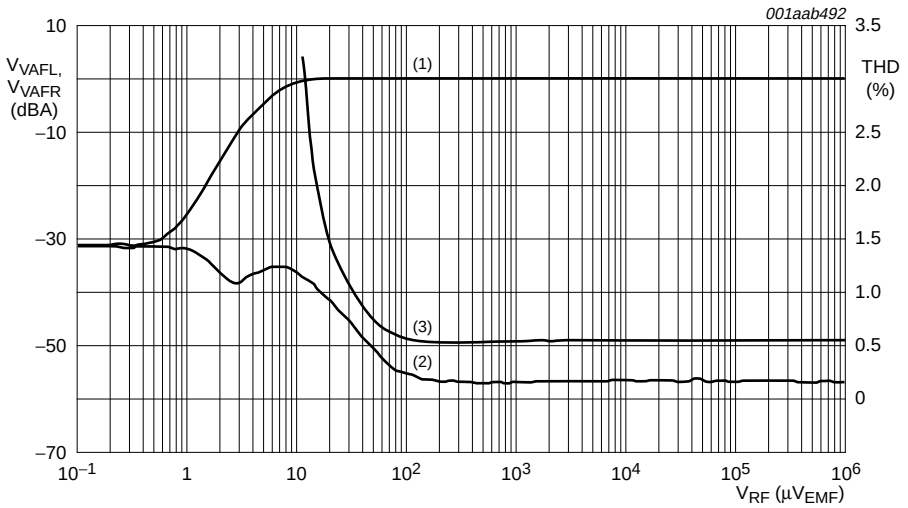
(2) V_{AFR} signal, modulation left, SNC on, Δf = 67.5 kHz; Δf_{pilot} = 6.75 kHz.

(3) Noise in Stereo mode, SNC on, Δf = 0 kHz; Δf_{pilot} = 6.75 kHz.

(4) Total harmonic distortion: Δf = 67.5 kHz; Δf_{pilot} = 6.75 kHz.

(5) Noise in Mono mode, SNC off, Δf = 0 kHz; Δf_{pilot} = 0 kHz.

Fig 11. FM characteristics stereo



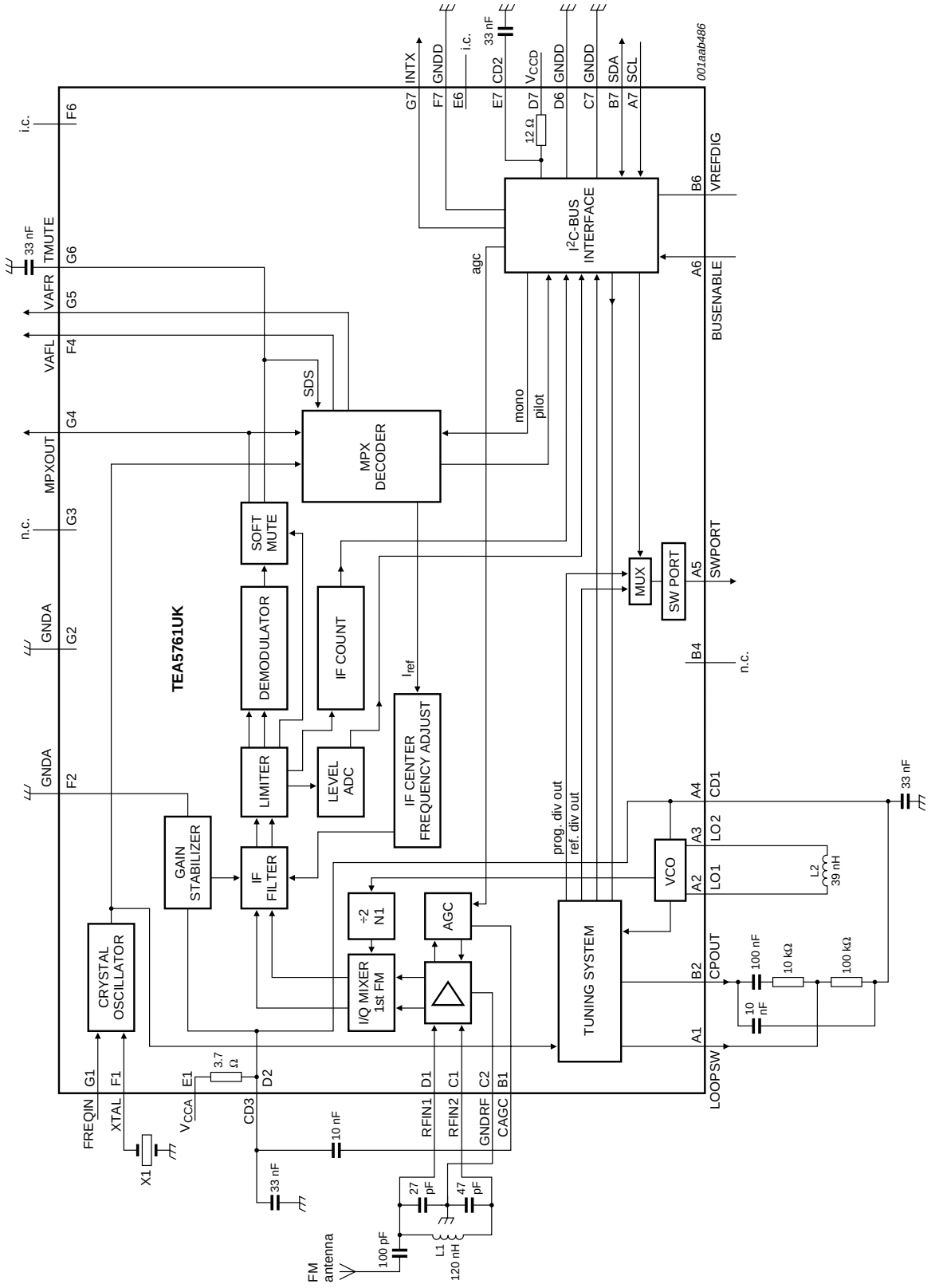
(1) Mono signal, soft mute on, Δf = 22.5 kHz.

(2) Noise in Mono mode, soft mute on, Δf = 0 kHz.

(3) Total harmonic distortion, Δf = 100 kHz.

Fig 12. FM characteristics mono, soft mute active and THD at 100 kHz deviation

14. Application information



Total of 15 external components.

Fig 13. Application diagram

Table 34: List of components

Number	Component	Description	Type	Manufacturer
1	L1	RF band filter coil	120 nH; 0603CS series or equivalent; Q_{min} = 20; tolerance: ±5 %	Coilcraft, Murata, Epcos, Panasonic
2	L2	VCO coil	39 nH to 47 nH; 0603CS series or equivalent; Q_{min} = 25; tolerance: ±5 %	Coilcraft, Murata, Epcos, Panasonic
3	X1	32.768 kHz crystal	see Table 31	
4	R	10 kΩ	±10 % (max)	
5		100 kΩ	±10 % (max)	
6	C	27 pF	±10 % (max)	
7		47 pF	±10 % (max)	
8		100 pF	±10 % (max)	
9		10 nF	±10 % (max)	
10		10 nF	±10 % (max)	
11		33 nF	±10 % (max)	
12		33 nF	±10 % (max)	
13		33 nF	±10 % (max)	
14		33 nF	±10 % (max)	
15		100 nF	±10 % (max)	

Table 35: DC operating points

V_{CCA} = V_{CCD} = $V_{VREFDIG}$ = 2.7 V.

Symbol	Ball	Mode		Unit
		Active	Standby	
LOOPSW	A1	2.6	2.7	V
LO1	A2	1.8	2.7	V
LO2	A3	1.8	2.7	V
CD1	A4	2.6	2.7	V
SWPORT	A5	0.2	0.2	V
BUSENABLE	A6	2.7	2.7	V
SCL	A7	-	-	V
CAGC	B1	1.2	2.2	V
CPOUT	B2	0.5 to 2.5	0	V
n.c.	B4	0	0	V
VREFDIG	B6	2.7	2.7	V
SDA	B7	-	-	V
RFIN2	C1	0.5	0	V
GNDRF	C2	0	0	V
GNDD	C7	0	0	V
RFIN1	D1	0.5	0	V
CD3	D2	2.6	2.7	V
GNDD	D6	0	0	V

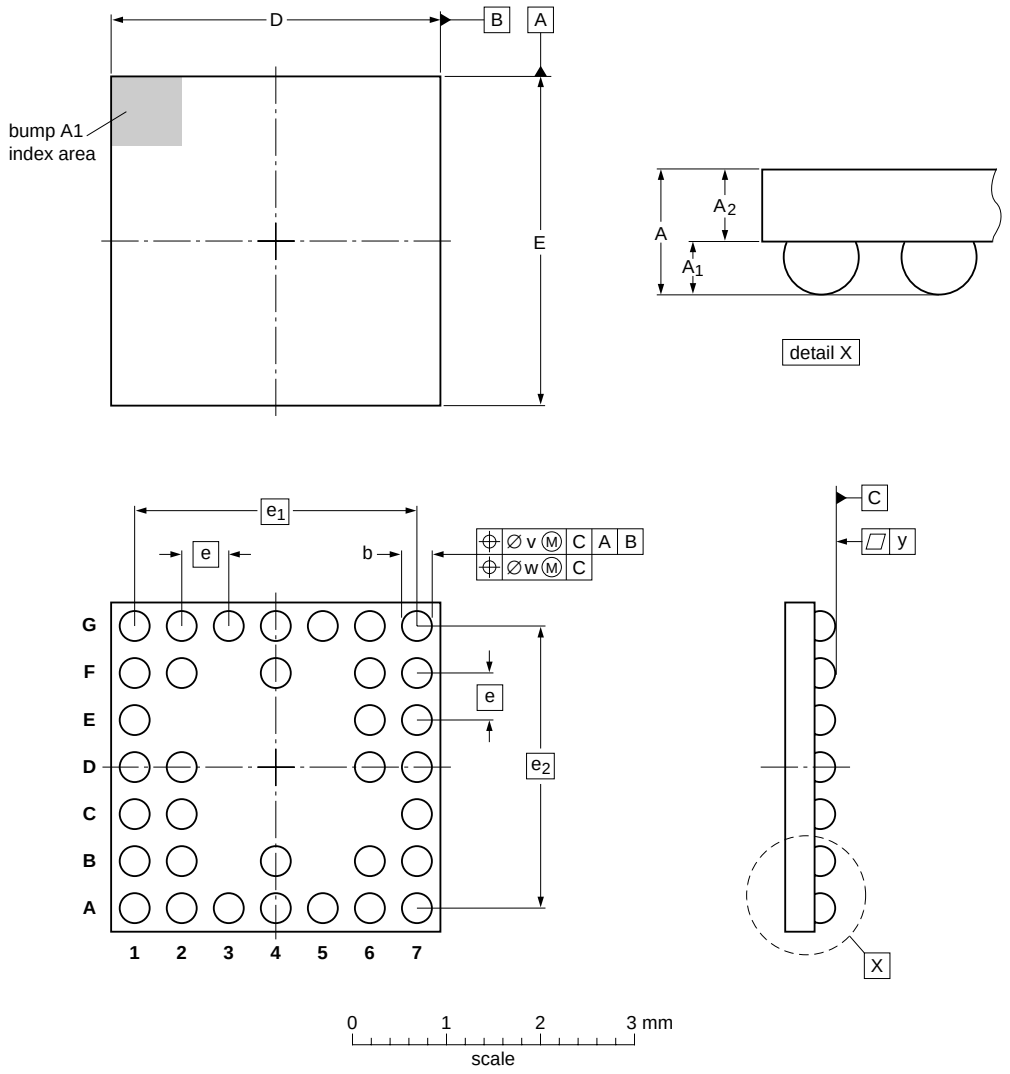
Table 35: DC operating points *…continued*

V_{CCA} = V_{CCD} = $V_{VREFDIG}$ = 2.7 V.

Symbol	Ball	Mode		Unit
		Active	Standby	
V_{CCD}	D7	2.7	2.7	V
V_{CCA}	E1	2.7	2.7	V
i.c.	E6	0	0	V
CD2	E7	2.7	2.7	V
XTAL	F1	1.7	2.5	V
GNDA	F2	0	0	V
VAFL	F4	0.8	0	V
i.c.	F6	0	0	V
GNDD	F7	0	0	V
FREQIN (no load)	G1	-	0	V
TRIGFR = 0		0	-	V
TRIGFR = 1		1.5	-	V
GNDA	G2	0	0	V
n.c.	G3	0	0	V
MPXOUT	G4	0.8	2.4	V
VAFR	G5	0.8	0	V
TMUTE	G6	1.9	2.3	V
INTX	G7	2.7	2.7	V

15. Package outline

WLCSP34: wafer level chip-size package; 34 bumps; 3.5 x 3.5 x 0.6 mm **TEA5761UK**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	3.6 3.5	3.6 3.5	0.5	3	3	0.01	0.04	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TEA5761UK						~~05-11-28~~ 05-12-02

Fig 14. Package outline TEA5761UK (WLCSP34)

16. Soldering

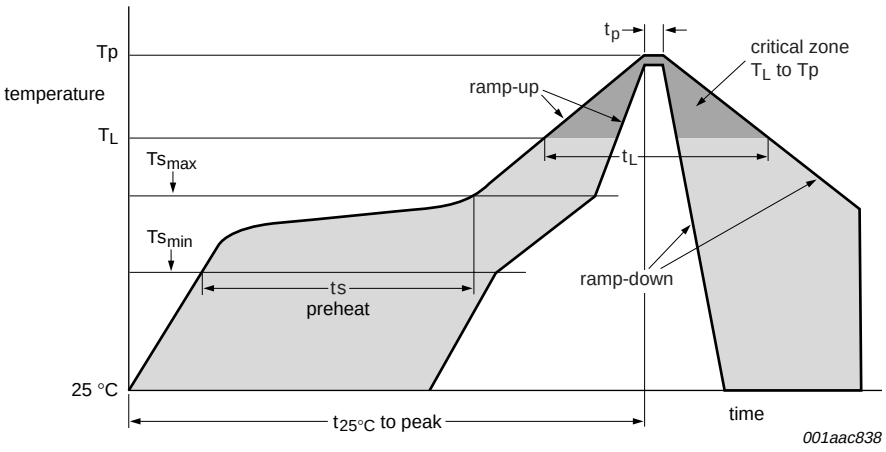
16.1 Introduction to soldering WLCSP packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering WLCSP packages can be found in *"AN10365. Application note for wafer level CSPs"*. Wave soldering is not suitable for this package.

16.2 Reflow soldering process

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

16.2.1 Solder reflow profile



Tp = 260 °C.

T_L = 217 °C.

Ts_{min} = 150 °C.

Ts_{max} = 200 °C.

t_p = 20 s to 40 s.

ts_{min} to ts_{max} = 60 s to 180 s.

Time from 25 °C to peak temperature is maximal 8 minutes.

Fig 15. Solder reflow profile

16.2.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.2.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip may be damaged. In that case it is recommended not using the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in this document.

16.2.4 Cleaning

Cleaning can be done after reflow soldering.

17. References

[1] **The I²C-bus specification —** version 2.1 January 2000

[2] **JESD22-C101 —** JEDEC standard for CDM test

[3] **AN10365 —** Application note for wafer level CSPs

18. Revision history

Table 36: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TEA5761UK_1	20060802	Product data sheet	-	9397 750 13451	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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24. Contents

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