Pin Information for the Cyclone™ EP1C3T144 Device
Version 1.4

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	DQS for x8 in the T144
B1	VREF0B1	IO	LVDS4p	INIT_DONE	1	DM1L
B1	VREF0B1	IO	LVDS4n	CRC_ERROR	2	DQ1L0
B1	VREF0B1	IO	LVDS3p	CLKUSR	3	DQ1L1
B1	VREF0B1	IO	LVDS3n		4	
B1	VREF0B1	IO	VREF0B1		5	
B1	VREF0B1	IO	LVDS2p		6	DQ1L2
B1	VREF0B1	IO	LVDS2n		7	DQ1L3
B1	VREF0B1	VCCIO1			8	
B1	VREF0B1	GND			9	
B1	VREF0B1	IO	DPCLK1		10	DQS0L
B1	VREF1B1	IO	VREF1B1		11	
B1	VREF1B1	IO		nCSO	12	
B1	VREF1B1	DATA0		DATA0	13	
B1	VREF1B1	nCONFIG		nCONFIG	14	
	VREF1B1	VCCA_PLL1			15	
B1	VREF1B1	CLK0	LVDSCLK1p		16	
B1	VREF1B1	CLK1	LVDSCLK1n		17	
	VREF1B1	GNDA_PLL1			18	
	VREF1B1	GNDG_PLL1			19	
B1	VREF1B1	nCEO		nCEO	20	
B1	VREF1B1	nCE		nCE	21	
B1	VREF1B1	MSEL0		MSEL0	22	
B1	VREF1B1	MSEL1		MSEL1	23	
B1	VREF1B1	DCLK		DCLK	24	
B1	VREF1B1	IO		ASDO	25	
B1	VREF1B1	IO	PLL1_OUTp		26	
B1	VREF1B1	IO	PLL1_OUTn		27	
B1	VREF2B1	IO	DPCLK0		28	DQS1L
B1	VREF2B1	VCCIO1			29	
B1	VREF2B1	GND			30	
B1	VREF2B1	IO	VREF2B1		31	
B1	VREF2B1	IO			32	DQ1L4
B1	VREF2B1	IO	LVDS1p		33	DQ1L5
B1	VREF2B1	IO	LVDS1n		34	DQ1L6
B1	VREF2B1	IO	LVDS0p		35	DQ1L7
B1	VREF2B1	IO	LVDS0n		36	
B4	VREF2B4	IO	LVDS33p		37	
B4	VREF2B4	IO	LVDS33n		38	
B4	VREF2B4	IO	LVDS32p		39	DQ1B7
B4	VREF2B4	IO	LVDS32n		40	DQ1B6
B4	VREF2B4	IO	LVDS31p		41	DQ1B5
B4	VREF2B4	IO	LVDS31n		42	DQ1B4
B4	VREF2B4	GND			43	
B4	VREF2B4	VCCIO4			44	
	VREF2B4	GND			45	
	VREF2B4	VCCINT			46	
B4	VREF2B4	IO	DPCLK7		47	DQS1B
B4	VREF2B4	IO	VREF2B4		48	
B4	VREF2B4	IO			49	
B4	VREF2B4	IO	LVDS30p		50	
B4	VREF2B4	IO	LVDS30n		51	
B4	VREF1B4	IO	LVDS29p		52	
B4	VREF1B4	IO	LVDS29n		53	
B4	VREF1B4	IO	LVDS28p		54	
B4	VREF1B4	IO	LVDS28n		55	
B4	VREF1B4	IO	VREF1B4		56	

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Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	DQS for x8 in the T144
B4	VREF1B4	IO	LVDS27p		57	DM1B
B4	VREF1B4	IO	LVDS27n		58	
B4	VREF1B4	IO	LVDS26p		59	
B4	VREF0B4	IO	LVDS26n		60	
B4	VREF0B4	IO	VREF0B4		61	
B4	VREF0B4	IO	DPCLK6		62	DQS0B
	VREF0B4	GND			63	
	VREF0B4	VCCINT			64	
B4	VREF0B4	GND			65	
B4	VREF0B4	VCCIO4			66	
B4	VREF0B4	IO	LVDS25p		67	DQ1B3
B4	VREF0B4	IO	LVDS25n		68	DQ1B2
B4	VREF0B4	IO	LVDS24p		69	DQ1B1
B4	VREF0B4	IO	LVDS24n		70	DQ1B0
B4	VREF0B4	IO	LVDS23p		71	
B4	VREF0B4	IO	LVDS23n		72	
B3	VREF2B3	IO	LVDS22n		73	
B3	VREF2B3	IO	LVDS22p		74	
B3	VREF2B3	IO	LVDS21n		75	
B3	VREF2B3	IO	LVDS21p		76	
B3	VREF2B3	IO	LVDS20n		77	DQ1R7
B3	VREF2B3	IO	LVDS20p		78	DQ1R6
B3	VREF2B3	IO	VREF2B3		79	
B3	VREF2B3	GND			80	
B3	VREF2B3	VCCIO3			81	
B3	VREF2B3	IO	DPCLK5		82	DQS1R
B3	VREF2B3	IO	LVDS19n		83	DQ1R5
B3	VREF2B3	IO	LVDS19p		84	DQ1R4
B3	VREF2B3	IO			85	DM1R
B3	VREF1B3	CONF_DONE		CONF_DONE	86	
B3	VREF1B3	nSTATUS		nSTATUS	87	
B3	VREF1B3	TCK		TCK	88	
B3	VREF1B3	TMS		TMS	89	
B3	VREF1B3	TDO		TDO	90	
B3	VREF1B3	IO			91	
B3	VREF1B3	CLK3	LVDSCLK2n		92	
B3	VREF1B3	CLK2	LVDSCLK2p		93	
B3	VREF1B3	IO			94	
B3	VREF1B3	TDI		TDI	95	
B3	VREF1B3	IO	VREF1B3		96	
B3	VREF0B3	IO			97	DQ1R3
B3	VREF0B3	IO	LVDS18n		98	DQ1R2
B3	VREF0B3	IO	LVDS18p		99	DQ1R1
B3	VREF0B3	IO	DPCLK4		100	DQS0R
B3	VREF0B3	GND			101	
B3	VREF0B3	VCCIO3			102	
B3	VREF0B3	IO			103	DQ1R0
B3	VREF0B3	IO	VREF0B3		104	
B3	VREF0B3	IO	LVDS17n		105	
B3	VREF0B3	IO	LVDS17p		106	
B3	VREF0B3	IO	LVDS16n		107	
B3	VREF0B3	IO	LVDS16p		108	
B2	VREF0B2	IO	LVDS15n		109	
B2	VREF0B2	IO	LVDS15p		110	
B2	VREF0B2	IO	LVDS14n		111	DQ0T0
B2	VREF0B2	IO	LVDS14p		112	DQ0T1

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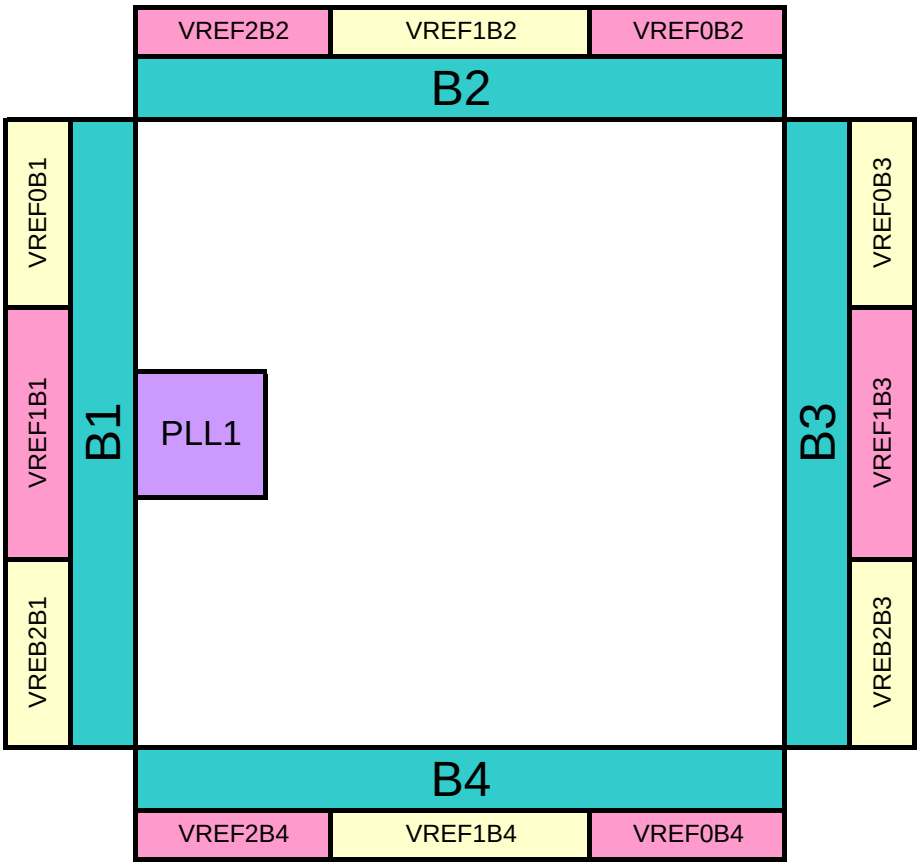
Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T144	DQS for x8 in the T144
B2	VREF0B2	IO	LVDS13n		113	DQ0T2
B2	VREF0B2	IO	LVDS13p		114	DQ0T3
B2	VREF0B2	VCCIO2			115	
B2	VREF0B2	GND			116	
	VREF0B2	VCCINT			117	
	VREF0B2	GND			118	
B2	VREF0B2	IO	DPCLK3		119	DQS0T
B2	VREF0B2	IO	VREF0B2		120	
B2	VREF0B2	IO	LVDS12n		121	
B2	VREF1B2	IO	LVDS12p		122	
B2	VREF1B2	IO	LVDS11n		123	DM0T
B2	VREF1B2	IO	LVDS11p		124	
B2	VREF1B2	IO	VREF1B2		125	
B2	VREF1B2	IO	LVDS10n		126	
B2	VREF1B2	IO	LVDS10p		127	
B2	VREF1B2	IO	LVDS9n		128	
B2	VREF1B2	IO	LVDS9p		129	
B2	VREF2B2	IO	LVDS8n		130	
B2	VREF2B2	IO	LVDS8p		131	
B2	VREF2B2	IO			132	
B2	VREF2B2	IO	VREF2B2		133	
B2	VREF2B2	IO	DPCLK2		134	DQS1T
	VREF2B2	VCCINT			135	
	VREF2B2	GND			136	
B2	VREF2B2	VCCIO2			137	
B2	VREF2B2	GND			138	
B2	VREF2B2	IO	LVDS7n		139	DQ0T4
B2	VREF2B2	IO	LVDS7p		140	DQ0T5
B2	VREF2B2	IO	LVDS6n		141	DQ0T6
B2	VREF2B2	IO	LVDS6p		142	DQ0T7
B2	VREF2B2	IO	LVDS5n	DEV_OE	143	
B2	VREF2B2	IO	LVDS5p	DEV_CLRn	144	

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	No connect pins should not be connected on the board. They should be left floating.
		Configuration and JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
		Clock and PLL Pins
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1. The EP1C3T100 does not support this clock pin.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2. The EP1C3T100 does not support this clock pin.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin. The EP1C3T100 does not support this output pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin. The EP1C3T100 does not support this output pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..33]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 33. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. The EP1C3T100 does not support LVDS I/O interfacing.
LVDS[0..33]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 33. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. The EP1C3T100 does not support LVDS I/O interfacing.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin. The EP1C3T100 does not support this clock pin
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin. The EP1C3T100 does not support this clock pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

Pin Information for the Cyclone™ EP1C3T144 Device, ver 1.4



Notes:

1.This is a top view of the silicon die.

2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

Pin Information for the Cyclone™ EP1C3T144 Device
Version 1.4

Version Number	Date	Changes Made
1.4	3/6/2006	Added CRC_ERROR pin in Pin List and Pin Definitions