PRELIMINARY

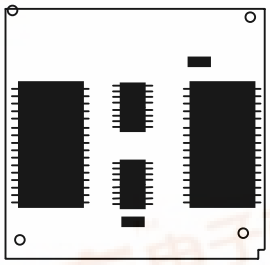
DS1254
2M x 8 NV SRAM with Phantom Clock

www.dalsemi.com

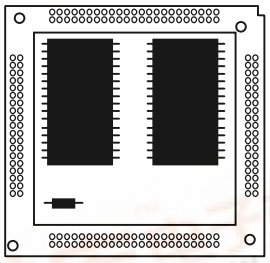
FEATURES

- Real time clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date, months, and years with automatic leap year compensation valid up to the year 2100
- 2M x 8 NV SRAM
- Watch function is transparent to RAM operation
- Automatic data protection during power loss
- Unlimited write cycle endurance
- Surface-mountable BGA module construction
- Over 10 years of data retention in the absence of power
- Battery monitor checks remaining capacity daily
- +3.3V or +5V operation

PACKAGE OUTLINE



(Side -A- Shown)
(For Reference Only Not To Scale)



BGA Module Base
Bottom View

ORDERING INFORMATION

PART #	DESCRIPTION
DS1254X	2M X 8 NV SRAM with Phantom Clock

X: W +3.3V operation; Y +5.0V operation

PIN DESCRIPTION

V_{CC}	- Supply Voltage
A0-A20	- Address Inputs
DQ0-DQ7	- Data I/O
$\overline{CE}$	- Chip Enable Input
$\overline{OE}$	- Output Enable Input
$\overline{WE}$	- Write Enable Input
$\overline{BW}$	- Battery Warning Output (Open Drain)
GND	- Ground

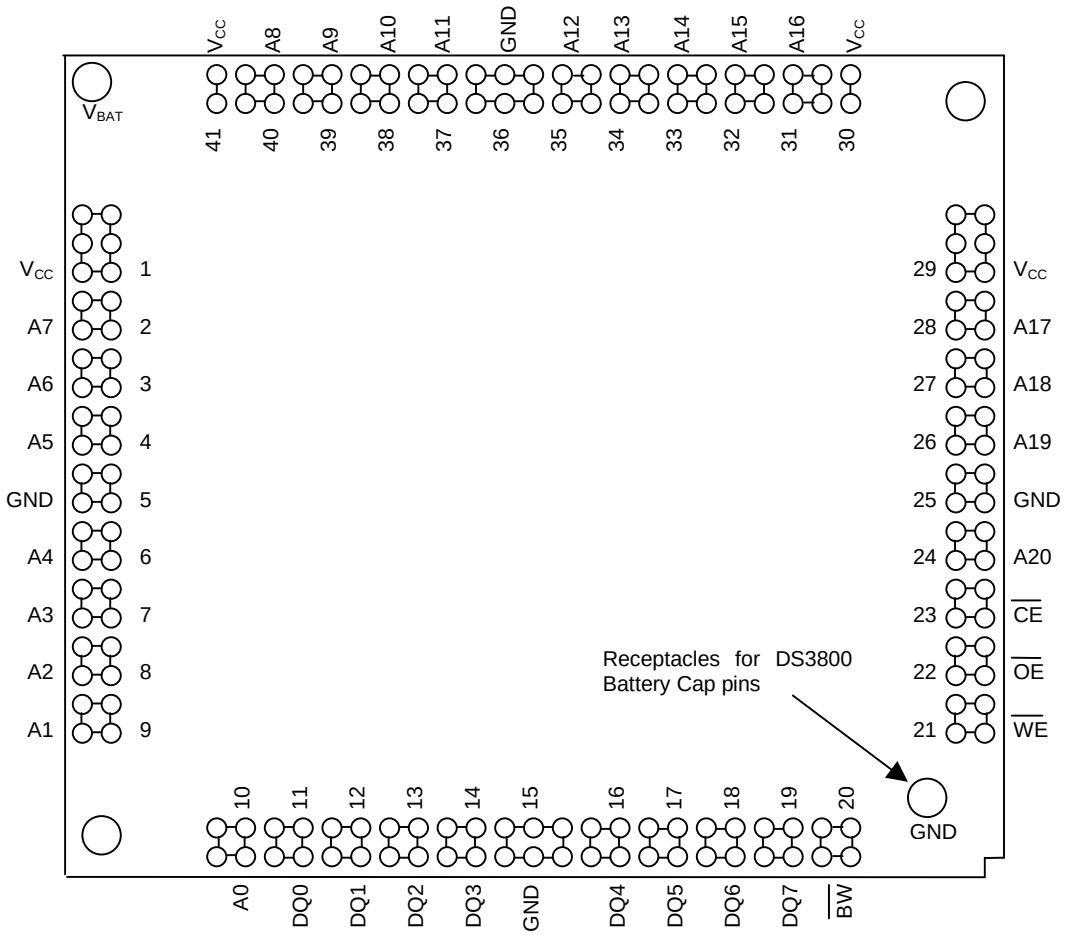
DESCRIPTION

The DS1254 is a fully static nonvolatile RAM (organized as 2M works by 8 bits) with built-in real time clock. The DS1254 has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the DS1254 makes use of an attached DS3800 Battery Cap to maintain clock information and preserve stored data while protecting that data by disallowing all memory accesses. Additionally, the DS1254 has dedicated circuitry for monitoring the status of an attached DS3800 Battery Cap.

The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The phantom clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

Pin Assignment Figure 1

Because the DS1254 has a total of 168 balls and only 35 active signals, balls are wired together into groups, thus providing redundant connections for every signal.



RAM READ MODE

The DS1254 executes a read cycle whenever $\overline{WE}$ is inactive (high) and $\overline{CE}$ is active (low). The unique address specified by the 21 address inputs (A0-A20) defines which of the 2M bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times and states are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1254 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below the power fail point V_{PF} (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. When V_{CC} falls below V_{BAT}, device power is switched from the V_{CC} to V_{BAT}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. All signals must be powered down when V_{CC} is powered down.

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the Phantom Clock, and memory access is inhibited.

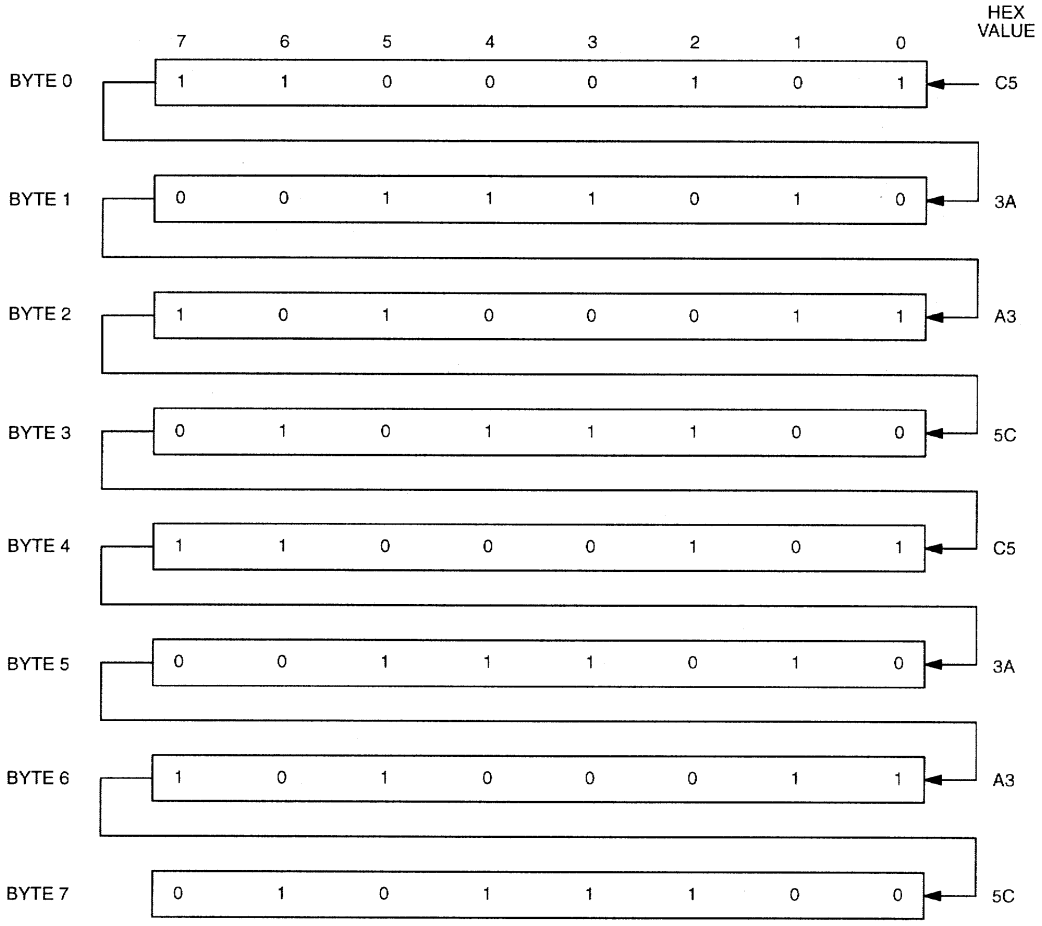
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the Phantom Clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ signals of the device. These 64 write cycles are used only to gain access to the Phantom Clock. Therefore, any address within the first 512 kbytes of memory, (00h to 7FFFFh) is acceptable. However, the write cycles generated to gain access to the Phantom Clock are also writing data to a location in the memory. The preferred way to manage this requirement is to set aside just one address location in memory as a Phantom Clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset.

Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 2). With a correct match for 64-bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

PHANTOM CLOCK REGISTER INFORMATION

The Phantom Clock information is contained in eight registers of 8-bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Phantom Clock registers, each register must be handled in groups of 8-bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 3.

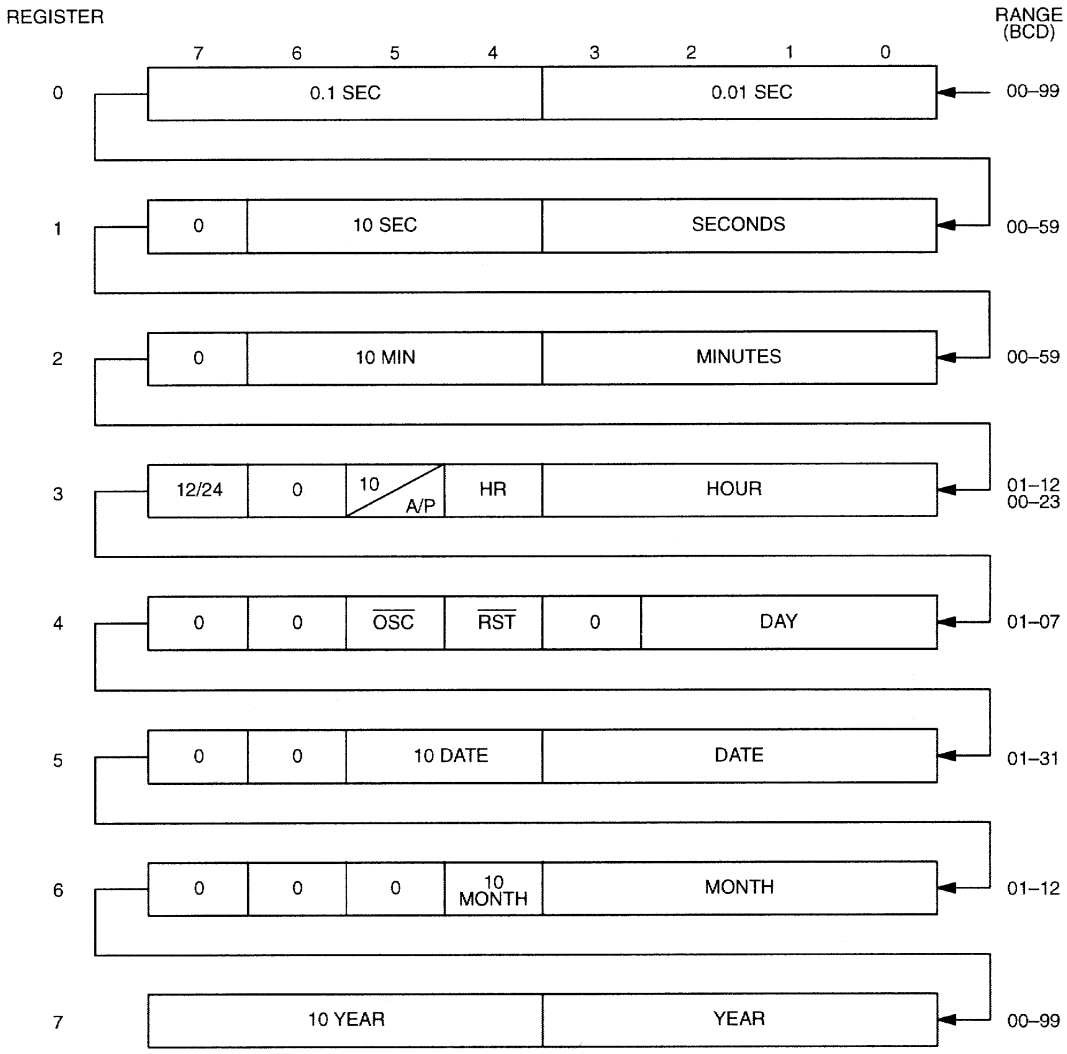
PHANTOM CLOCK PROTOCOL DEFINTION Figure 2



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicate and causing inadvertent entry to the Phantom Clock is less than 1 in 10^{19}. This pattern is sent to the Phantom Clock LSB to MSB.

PHANTOM CLOCK REGISTER DEFINTION Figure 3



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR BIT

Bit 5 of the day register controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

BATTERY MONITORING

The DS1254 automatically monitors the battery in an attached DS3800 Battery Cap on a 24-hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{PF} and is suspended when power failure occurs.

After each 24-hour period has elapsed, the battery is connected to an internal 1 MΩ test resistor for one second. During this one second, if the battery voltage falls below the battery voltage trip point (~2.6V), the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the attached DS3800 Battery Cap is replaced. However, the battery is still re-tested after each V_{CC} power-up, even if was active on power-down. If the battery voltage is found to be higher than ~2.6V during such testing, $\overline{BW}$ is de-asserted and regular testing resumes. $\overline{BW}$ has an open-drain output driver.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage (5V operation)	V_{CC}	4.5	5.0	5.5	V	1
Power Supply Voltage (3.3V operation)	V_{CC}	3.0	3.3	3.7	V	1
Logic 1 Voltage All Inputs V_{CC} = 5V±10%	V_{IH}	2.2		V_{CC}+0.3	V	1
V_{CC} = 3.3V±10%	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Voltage All Inputs V_{CC} = 5V±10%	V_{IL}	-0.3		0.8	V	1
V_{CC} = 3.3V±10%	V_{IL}	-0.3		0.6	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-4.0		+4.0	µA	
I/O Leakage Current	I_{IO}	-4.0		+4.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	3
Output Current @ 0.4V	I_{OL}	2.0			mA	3
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current, t_{CYC} = 100 ns	I_{CCO1}			85	mA	
Write Protection Voltage	V_{PF}	4.25		4.50	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 3.3V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-4.0		+4.0	µA	
I/O Leakage Current	I_{IO}	-4.0		+4.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	3
Output Current @ 0.4V	I_{OL}	2.0			mA	3
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	7	mA	
Standby Current $\overline{CE}$ = V_{CC}-0.5V	I_{CCS2}		2.0	3.0	mA	
Operating Current, t_{CYC} = 100 ns	I_{CCO1}			50	mA	
Write Protection Voltage	V_{PF}	2.8		2.97	V	1

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance: A0-A18, $\overline{OE}$, $\overline{WE}$, $\overline{CE}$	C_{IN}		25	50	pF	
Input Capacitance: A19-A20	C_{IN}		5	10	pF	
I/O Capacitance: DQ0-DQ7	C_{IO}		25	50	pF	
Output Capacitance: $\overline{BW}$	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

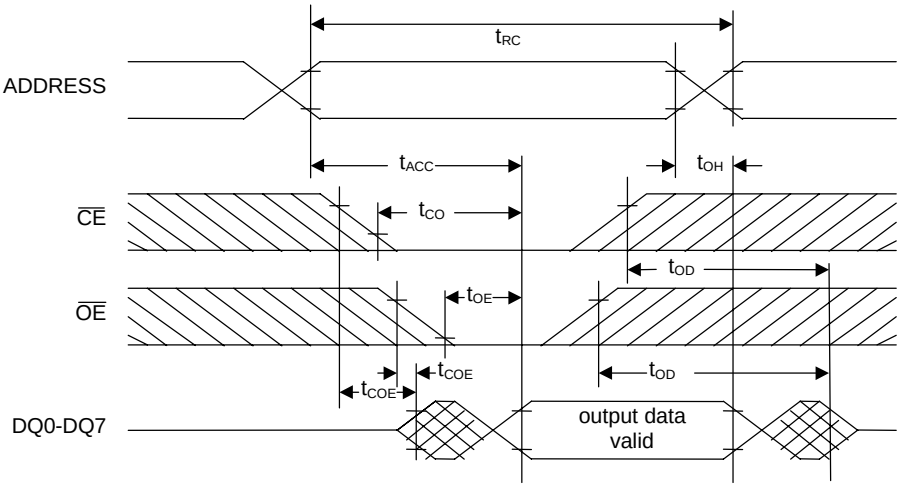
(0°C to 70°C; V_{CC} = 5.0V±10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		nS	
Address Access Time	t_{AAC}		100	nS	
$\overline{OE}$ to Output Valid	t_{OE}		55	nS	
$\overline{CE}$ to Output Valid	t_{CO}		100	nS	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5		nS	2
Output High Z from Deselection	t_{OD}		35	nS	2
Output Hold from Address Change	t_{OH}	5		nS	
Write Cycle Time	t_{WC}	100		nS	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{WP}	70		nS	5
Address Setup Time	t_{AW}	0		nS	
Address Hold Time	t_{AH1}	5		nS	6
	t_{AH2}	25		nS	7
Output High Z from $\overline{WE}$	t_{ODW}		35	nS	2
Output Active from $\overline{WE}$	t_{OEW}	5		nS	2
Data Setup Time	t_{DS}	40		nS	8
Data Hold Time	t_{DH1}	0		nS	6
	t_{DH2}	20		nS	8
Read Recovery (Clock Access Only)	t_{RR}	20		nS	
Write Recovery (Clock Access Only)	t_{WR}	20		nS	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; VCC = 3.3V±10%)

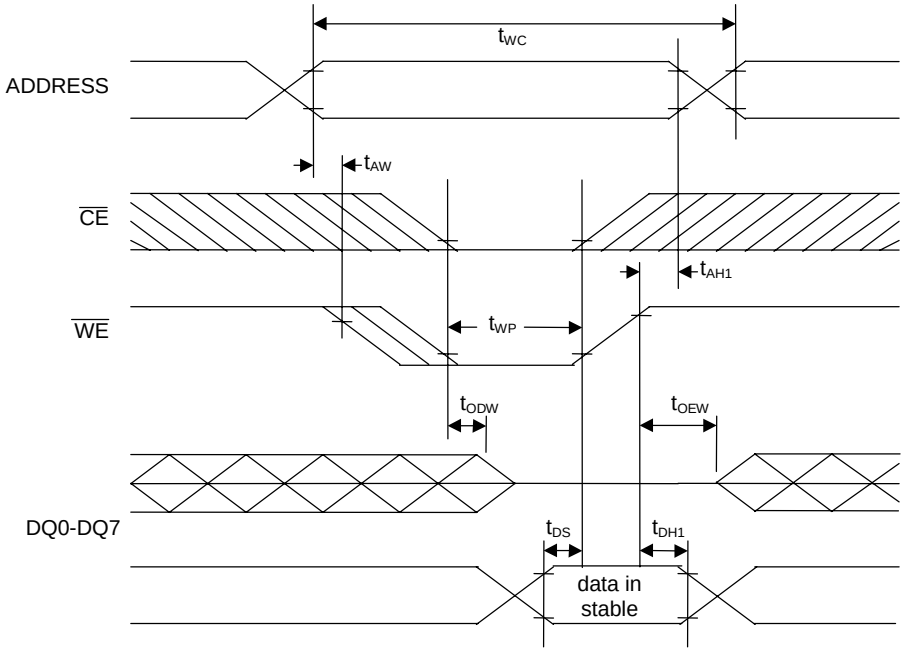
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		nS	
Address Access Time	t_{AAC}		150	nS	
$\overline{OE}$ to Output Valid	t_{OE}		75	nS	
$\overline{CE}$ to Output Valid	t_{CO}		150	nS	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	5		nS	2
Output High Z from Deselection	t_{OD}		70	nS	2
Output Hold from Address Change	t_{OH}	5		nS	
Write Cycle Time	t_{WC}	150		nS	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{WP}	100		nS	5
Address Setup Time	t_{AW}	0		nS	
Address Hold Time	t_{AH1}	5		nS	6
	t_{AH2}	25		nS	7
Output High Z from $\overline{WE}$	t_{ODW}		70	nS	2
Output Active from $\overline{WE}$	t_{OEW}	5		nS	2
Data Setup Time	t_{DS}	60		nS	8
Data Hold Time	t_{DH1}	0		nS	6
	t_{DH2}	20		nS	8
Read Recovery (Clock Access Only)	t_{RR}	20		nS	
Write Recovery (Clock Access Only)	t_{WR}	20		nS	

MEMORY READ CYCLE TIMING Figure 4



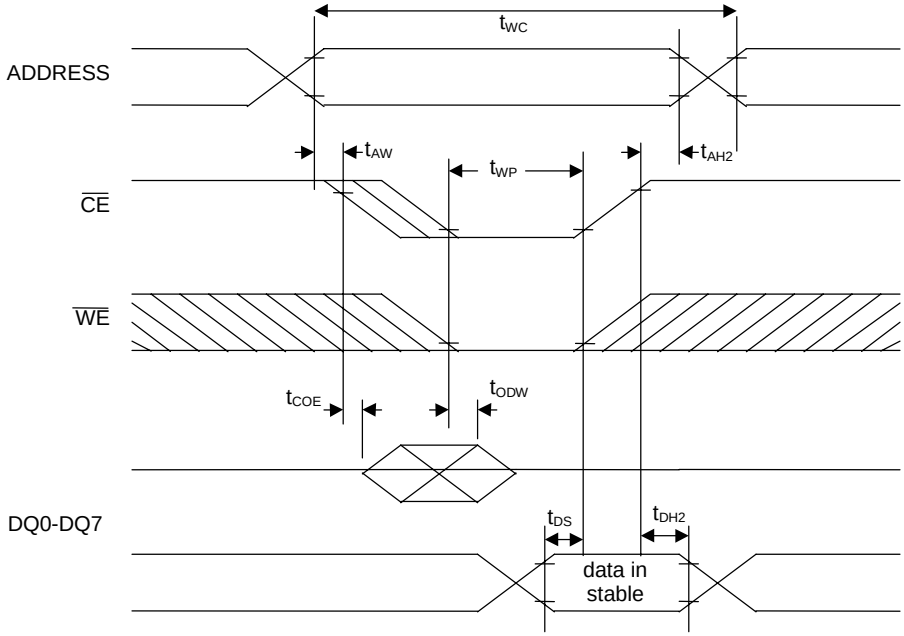
See Note 9

MEMORY WRITE CYCLE TIMING, WRITE ENABLE CONTROLLED Figure 5



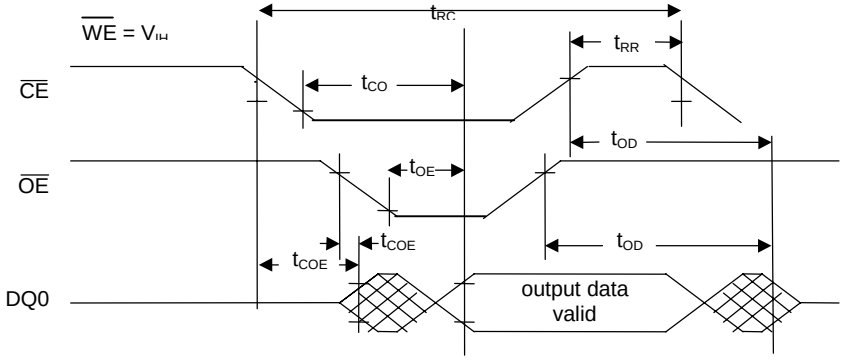
See Notes 5, 6, 8, 10, 11, 12, and 13

MEMORY WRITE CYCLE TIMING, CHIP ENABLE CONTROLLED Figure 6

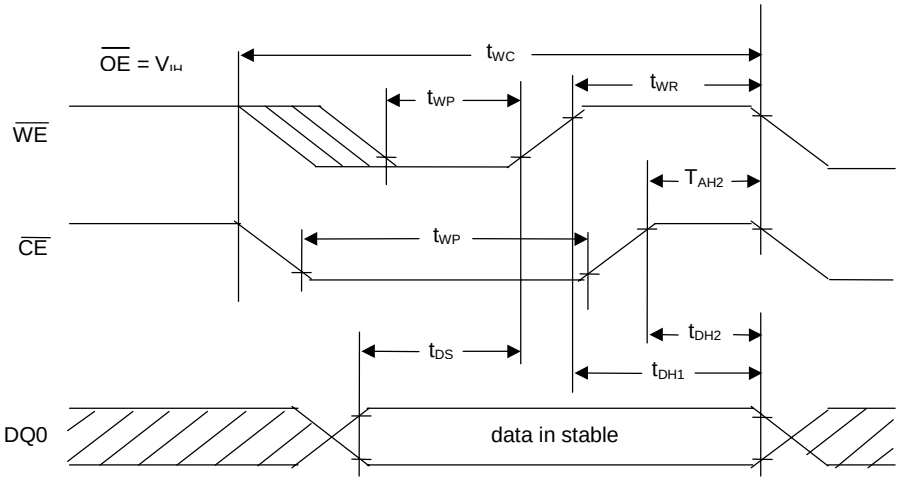


See Notes 5, 7, 8, 10, 11, 12, and 13

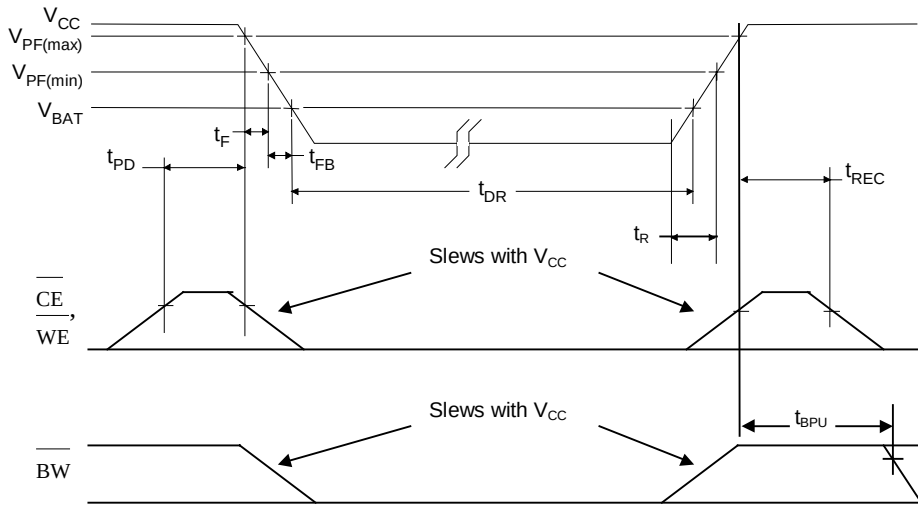
READ CYCLE TO PHANTOM CLOCK Figure 7



WRITE CYCLE TO PHANTOM CLOCK Figure 8



POWER UP/DOWN WAVEFORM TIMING Figure 9



See Note 14

POWER UP/DOWN CHARACTERISTICS (VCC = 5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ and $\overline{WE}$ at V_{IH} Before Power Down	t_{PD}	0			µS	
V_{CC} Fall Time: $V_{PF(max)}$ to $V_{PF(min)}$	t_F	300			µS	
V_{CC} Fall Time: $V_{PF(min)}$ to V_{BAT}	t_{FB}	10			µS	
V_{CC} Rise Time: 0V to $V_{PF(min)}$	t_R	150			µS	
V_{CC} Valid to End of Write Protection	t_{REC}			125	mS	
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	Sec	3

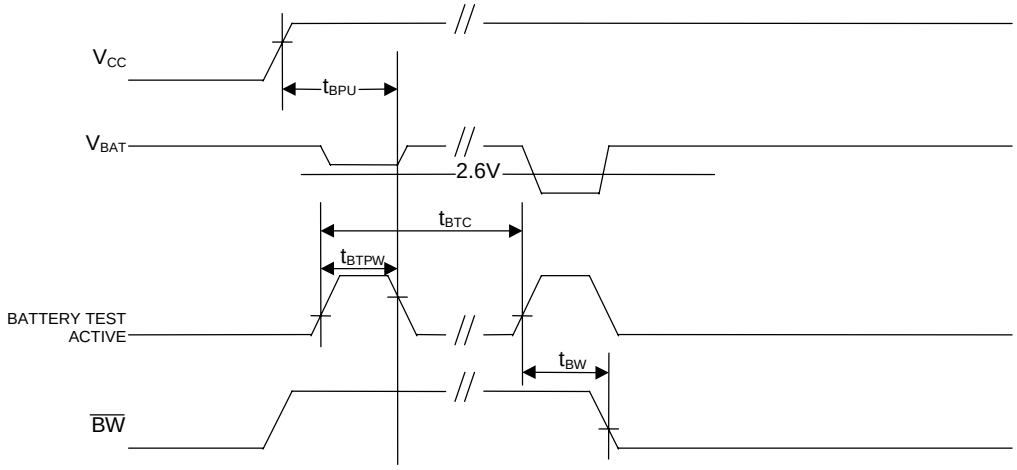
(TA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

BATTERY WARNING DETECTION Figure 10



See Note 3

BATTERY WARNING TIMING (0°C to 70°C; V_{CC} = 5.0V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	Sec	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	Sec	
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	Sec	3

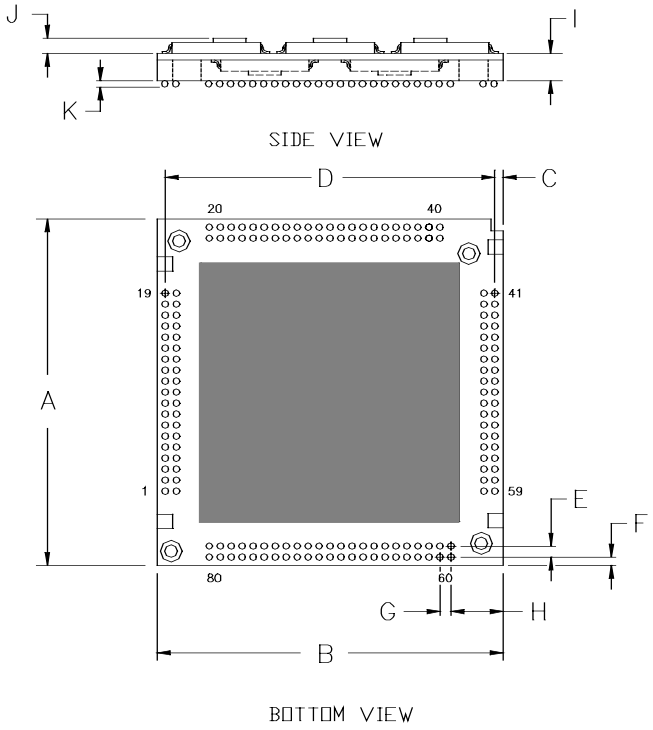
AC TEST CONDITIONS

Output Load: 100 pF + 1 TTL Gate
Input Pulse Levels: 0.0V to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 nS

NOTES:

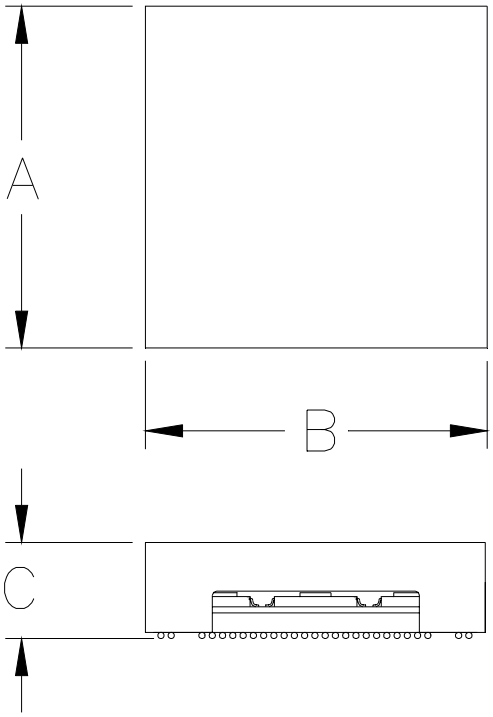
1. Voltage referenced to ground.
2. These parameters are sampled with a 50 pF load and are not 100% tested.
3. $\overline{BW}$ is an open drain output and, as such, cannot source current. An external pullup resistor should be connected to this pin for proper operation. $\overline{BW}$ can sink 10 mA.
4. The DS3800 Battery Cap is a one time use part, but can be removed and replaced. By Design, removal of a DS3800 will mechanically damage the Battery Cap which eliminates the accidental use of a previously attached and possibly low capacity Battery Cap.
5. t_{WP} specified as the logical AND of $\overline{CE}$ and $\overline{WE}$, t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
6. T_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high..
7. T_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
8. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
9. $\overline{WE}$ is high for a read cycle.
10. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
11. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in a write enable controlled write cycle, the output buffers remain in a high impedance state during this period.
12. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
13. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
14. In a power down condition, the voltage on any pin may not exceed the voltage on V_{CC}.

DS1254 PACKAGE DIMENSIONS



		Min	Max
A	in	1.570	1.580
	mm	39.88	40.13
B	in	1.570	1.580
	mm	39.88	40.13
C	in	0.033	0.043
	mm	0.84	1.09
D	in	1.497	1.503
	mm	38.02	38.18
E	in	0.047	0.053
	mm	1.19	1.35
F	in	0.033	0.043
	mm	0.84	1.09
G	in	0.047	0.053
	mm	1.19	1.35
H	in	0.234	0.240
	mm	5.94	6.10
I	in	0.125	0.135
	mm	3.10	3.43
J	in	-	?
	mm	-	?
K	in	0.025	0.030
	mm	0.64	0.76

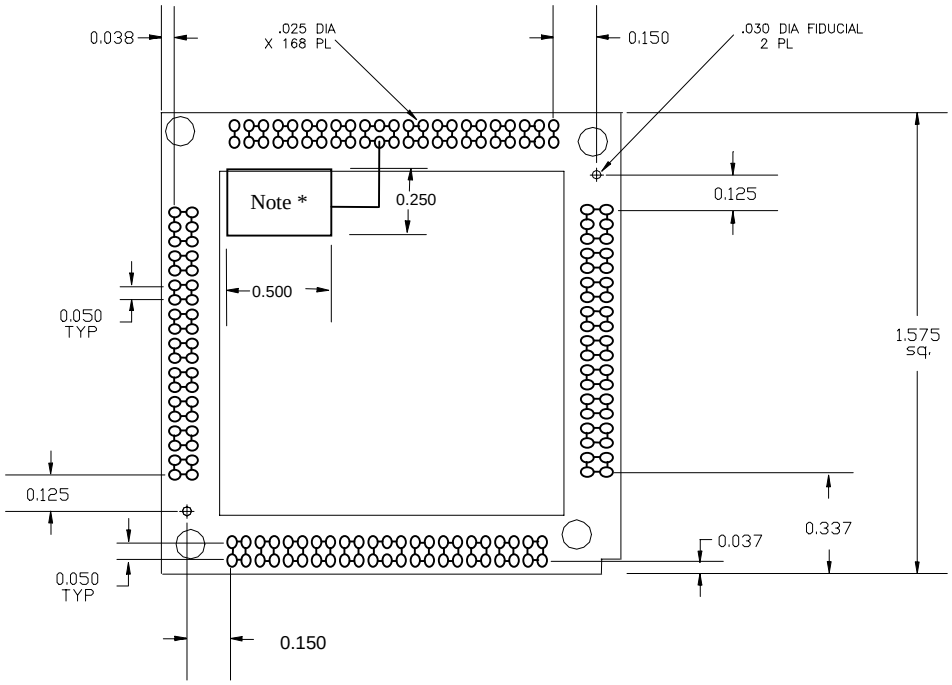
DS1254 PACKAGE DIMENSIONS (WITH ATTACHED DS3800 BATTERY CAP)



		Min	Max
A	in	1.656	1.668
	mm	42.06	42.37
B	in	1.656	1.668
	mm	42.06	42.37
C	in	-	0.485
	mm	-	12.32

DS1254 RECOMMENDED LAND PATTERN (with overlaid Package Outline)

The DS1254 ball grid array is a subset of the industry-standard 40 mm BGA format, with all balls on a 50-mil grid. Corner balls have been removed to provide space for the electrical and mechanical interface features that facilitate attachment of the DS3800 Battery Cap.



* Note: Ground shield to isolate RTC XTAL from EMI