TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B79

COLUMN AND ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The TOSHIBA T6B79 is a driver for a small-or medium-scale dot matrix graphic LCD. It includes the functions of the TOSHIBA T9841B (column driver) and the TOSHIBA T9842B (row driver). It has an 8-bit interface circuit and can be operated with an 80-Series MPU. It generates all the timing signals for the display with an on-chip oscillator. It receives 8-bit data from an MPU, latches the data to an on-chip RAM, and displays the image on the LCD (the data in the display RAM correspond to the dots on the display). The device has 64 column driver outputs and 48 row driver outputs enabling it to drive a 64-dot by 48-dot LCD. In addition, there are resistors to divide the bias voltage, a power supply op-amp, DC-DC converter (doubler, tripler and quadruplexer) and contrast control circuit enabling the LCD to be driven by a single power supply.

Unit: mm

T6B79	LEAD PITCH	
	IN	OUT
(UA)	0.8	0.28

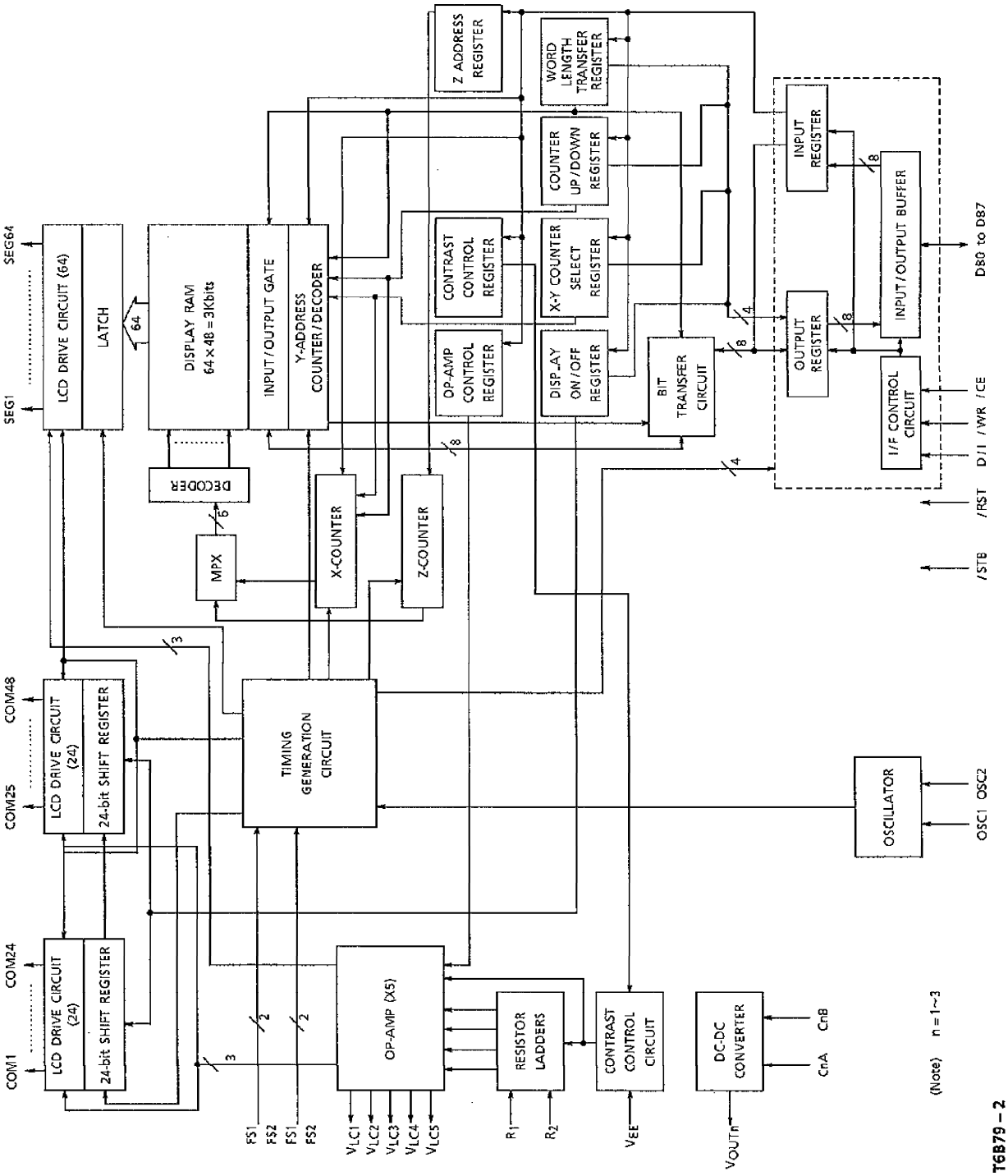
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

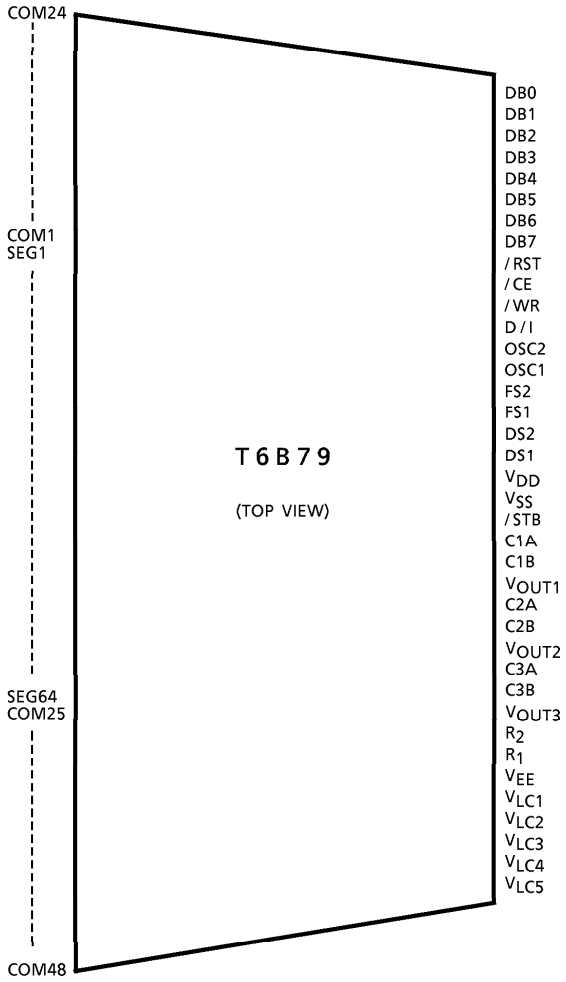
FEATURES

- On-chip display RAM capacity: 64 × 48 = 3072 bits
- Display RAM data
  ① Display data = 1 . . . . . LCD turns on.
  ② Display data = 0 . . . . . LCD turns off.
- 1/16, 1/32 or 1/48 selectable duty cycle
- Word length of display data can be switched between eight bits and six bits according to the character font.
- LCD driver outputs: 64 column driver outputs and 48 row driver outputs
- Interface with 80-Series MPU
- On-chip oscillator with one external resistor
- Low power consumption
- On-chip resistors to divide bias voltage, on-chip operational amplifier for LCD supply, on-chip DC-DC converter (doubler, tripler and quadruplexer), on-chip contrast control circuit
- CMOS process
- Operating voltage: 2.7V to 5.5V
- Operating voltage for LCD drive signal
  $V_{DD} - V_{EE} = 16.0V$ (max)
- Package: TCP (Tape Carrier Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



(*) The above diagram shows the pin configuration of the LSI chip ; it does not show the configuration of the tape carrier package.

PIN FUNCTIONS

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTIONS</th></tr>
<tr><td>SEG1 to SEG64</td><td>Output</td><td>Column driver output</td></tr>
<tr><td>COM1 to COM48</td><td>Output</td><td>Row driver output</td></tr>
<tr><td>DB0 to DB7</td><td>I/O</td><td>Data bus</td></tr>
<tr><td>D/I</td><td>Input</td><td>Input for data/instruction select signal
● D/I = H indicates that the data on DB0 to DB7 is display data.
● D/I = L indicates that the data on DB0 to DB7 is instruction data.</td></tr>
<tr><td>/WR</td><td>Input</td><td>Input for write select signal
● /WR = H → Read selected
● /WR = L → Write selected</td></tr>
<tr><td>/CE</td><td>Input</td><td>Input for chip enable signal
● /WR = L→ Data on DB0 to DB7 is latched on the rising edge of /CE.
● /WR = H→ Data appears at DB0 to DB7 while /CE is Low.</td></tr>
<tr><td>/RST</td><td>Input</td><td>Input for reset signal
● /RST = L → Reset state</td></tr>
<tr><td>/STB</td><td>Input</td><td>Input for standby signal
● Usually connected to V_{DD}
● /STB = L → T6B79 is in standby state and cannot accept any commands or data.
Column driver signal and row driver signal are at the V_{DD} level.</td></tr>
<tr><td>FS1, FS2</td><td>Input</td><td>Inputs for frequency selection
<table>
<tr><th>FS2</th><th>FS1</th><th>f_{OSC} (kHz)</th><th>f_{COM} (Hz)</th></tr>
<tr><td>0</td><td>0</td><td>26.88</td><td>35</td></tr>
<tr><td>0</td><td>1</td><td>53.76</td><td>35</td></tr>
<tr><td>1</td><td>0</td><td>215.00</td><td>35</td></tr>
<tr><td>1</td><td>1</td><td>430.10</td><td>35</td></tr>
</table></td></tr>
<tr><td>DS1, DS2</td><td>Input</td><td>Inputs for duty selection
<table>
<tr><th>DS2</th><th>DS1</th><th>DUTY</th></tr>
<tr><td>0</td><td>0</td><td>1/16</td></tr>
<tr><td>0</td><td>1</td><td>1/32</td></tr>
<tr><td>1</td><td>0</td><td>1/48</td></tr>
<tr><td>1</td><td>1</td><td>1/48</td></tr>
</table></td></tr>
<tr><td>OSC1, OSC2</td><td>—</td><td>When using the internal clock oscillator, connect a resistor between OSC1 and OSC2.
When using an external clock, connect the clock as input to OSC1 and leave OSC2 open.</td></tr>
<tr><td>R_1, R_2</td><td>—</td><td>Inputs for LCD drive bias selection
● LCD drive bias selection is shown in the following table.
<table>
<tr><th>R_2</th><th>R_1</th><th>Bias</th></tr>
<tr><td>0</td><td>0</td><td>1/5</td></tr>
<tr><td>0</td><td>1</td><td>1/6</td></tr>
<tr><td>1</td><td>0</td><td>1/7</td></tr>
<tr><td>1</td><td>1</td><td>1/8</td></tr>
</table></td></tr>
</table>

PIN NAME	I/O	FUNCTIONS
C1A, C1B	—	Connect using a capacitor for ×2 DC-DC converter.
V_{OUT1}	—	DC-DC converter output (×2 output)
C2A, C2B	—	Connect using a capacitor for ×3 DC-DC converter.
V_{OUT2}	—	DC-DC converter output (×3 output)
C3A, C3B	—	Connect using a capacitor for ×4 DC-DC converter.
V_{OUT3}	—	DC-DC converter output (×4 output)
V_{EE}	—	Power supply for LCD driver circuit ● When using on-chip DC-DC converter, connect V_{EE} to V_{OUT}.
V_{LC1} to V_{LC5}	—	Power supply for LCD driver circuit
V_{DD}, V_{SS}	—	Power supply for logic circuit. Reference : Ground

FUNCTION OF EACH BLOCK

- Interface logic

  The T6B79 can be operated with an 80-Series MPU.
  Fig. 1 shows an example of the interface.

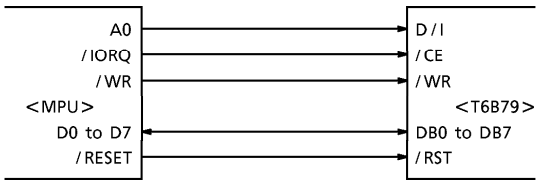


Fig. 1

- Input register

  This register stores 8-bit data from the MPU. The D/I signal distinguishes between command data and display data.

- Output register

  This register stores 8-bit data from the display RAM. When display data is read, the display data specified by the address in the address counter is stored in this register. After that, the address is automatically incremented or decremented. Therefore, when an address is set, the correct data does not appear as the first data item that is read. The data in the specified address location appears as the second data item that is read.

- X-address counter

  The X-address counter is a 48-up/down counter. It holds the row address of a location in the display RAM. Writing data to or reading data from the of display RAM causes the X-address to be automatically incremented or decremented.

- Y-(page) address counter

  The Y-(page) address counter is either an 8-up/down counter, when the word length is eight bits, or an 11-up/down counter, when the word length is six bits. It holds the column address of a location in the display RAM. Writing data to or reading data from the display RAM causes the Y-address to be automatically incremented or decremented.

- Z-address counter

  The Z-address counter is a 48-up counter that provides the display RAM data for the LCD drive circuit. The data stored in the Z-address register is sent to the Z-address counter as the Z start address.
  For instance, when the Z start address is 32, the counter increments as follows: 32, 33, 34···, 46, 47, 0, 1, 2···30, 31, 32. Therefore, the display start line is line 32 of the display RAM.

- Up/down register

  The 1-bit datum stored in this register selects either up or down mode for the X- and Y-(page) address counters.

- Counter select register

  The 1-bit datum stored in this register selects the X-address counter or Y-(page) address counter.

- Display ON/OFF register

  This 1-bit register holds the display ON/OFF state. In the OFF state, the output data from the display RAM is cleared. In the ON state, the display RAM data is displayed. The display ON/OFF state does not affect the data in the display RAM.

- Z-address register

  This 6-bit register holds the data which specifies the display start line. The data is loaded into the Z-address counter on the FRM signal. Using the Z-address register, vertical scrolling is possible.

- Word length register

  The 1-bit datum stored in this register selects the word length: eight bits per word or six bits per word.

- Word length change circuit

  This circuit is controlled by the word length register. When the word length is eight bits, data is transferred eight bits at a time. When the word length is six bits, the data transfer method is as shown in Fig. 2 below.

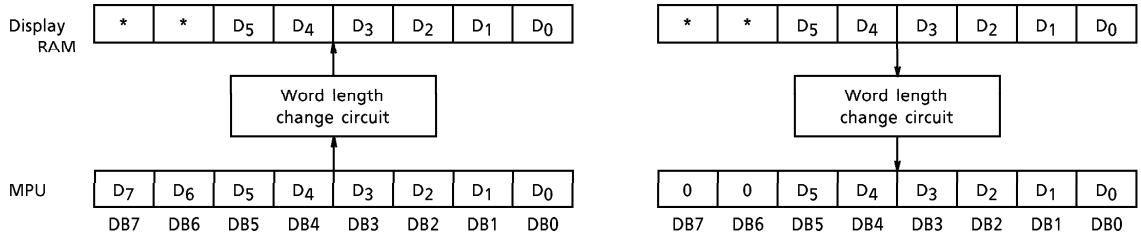


Fig. 2

* : INVALID

- Oscillator

  The T6B79 includes an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2, as shown in Fig. 3. When using an external clock, connect the clock input to OSC1 and leave OSC2 open.

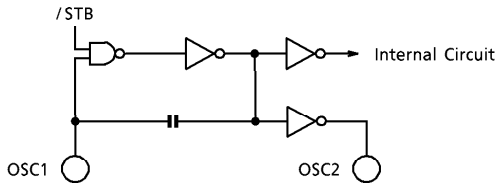


Fig. 3

- Timing generation circuit

  This circuit divides the signals from the oscillator and generates the display timing signals and the operating clock signal.

- Shift register

  The T6B79 has two 24-bit shift registers. These two 24-bit shift registers can be combined to form a 48-bit shift register.

- Latch circuit

  The latch circuit latches data from the display RAM.

- Column driver circuit

  The column driver circuit consists of 64 driver circuits. One of the four LCD driving levels is selected by the combination of the internal M signal and the display data transferred from the latch circuit. Details of the column driver circuit are shown in Fig. 4.

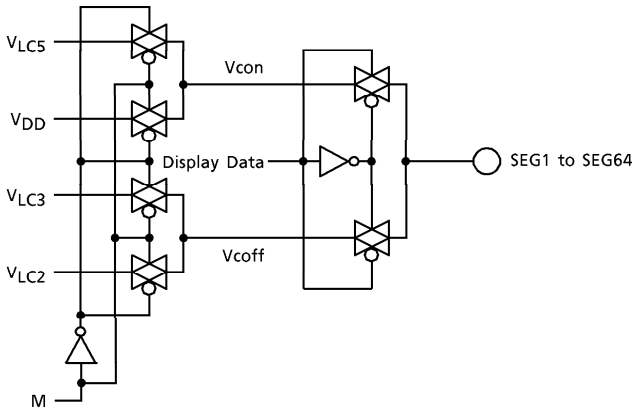


Fig. 4

- Row driver circuit

  The row driver circuit consists of 48 driver circuits. One of the four LCD driving levels is selected by the combination of the internal M signal and the data from the shift register. Details of the row driver circuit are shown in Fig. 5.

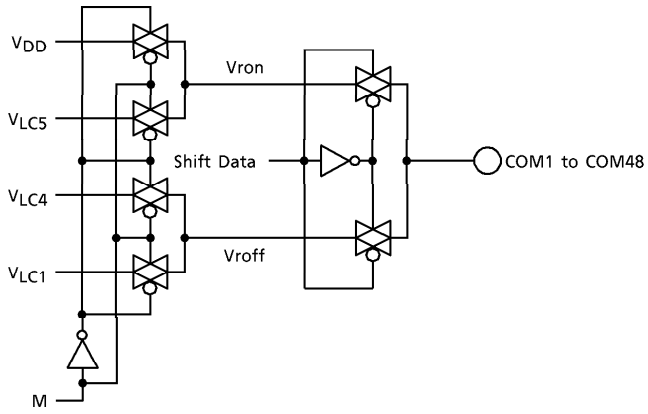


Fig. 5

- DC-DC converter

  The T6B79 has an on-chip DC-DC converter. The DC-DC converter generates a ×2, ×3 or ×4 output level. See Fig. 6.
  When /STB = L, V_{OUT1}, V_{OUT2} and V_{OUT3} = 0 (V). The recommended value for the capacitor is 2.2μF.

  (1) Doubler (×2) mode

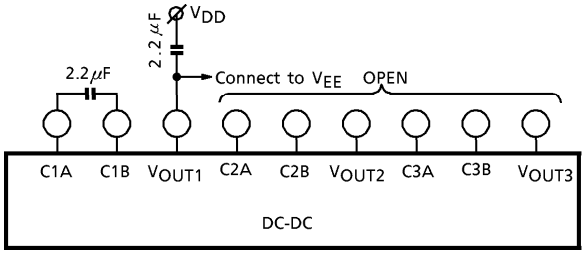


Fig. 6-1

  (2) Tripler (×3) mode

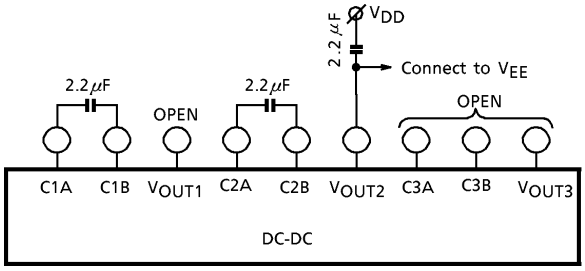


Fig. 6-2

(3) Quadruplexer (×4) mode

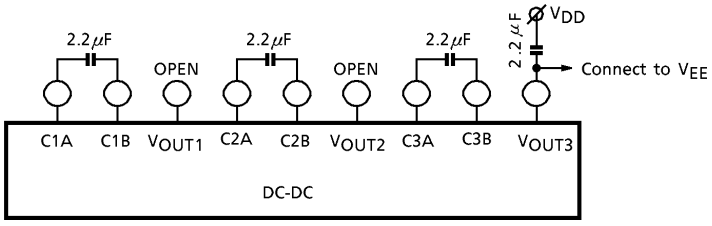


Fig. 6-3

When using an external power supply, input the voltage to V_{EE} and do not connect the capacitors.

- Voltage divider resistors, contrast control circuit

The T6B79 has on-chip resistors which include op-amps, that divide the bias voltage, and a contrast control circuit.
The voltage bias is modified by the values of R_1 and R_2. One of four biases can be selected.
These resistors and the contrast control circuit are shown in Fig. 7 below.

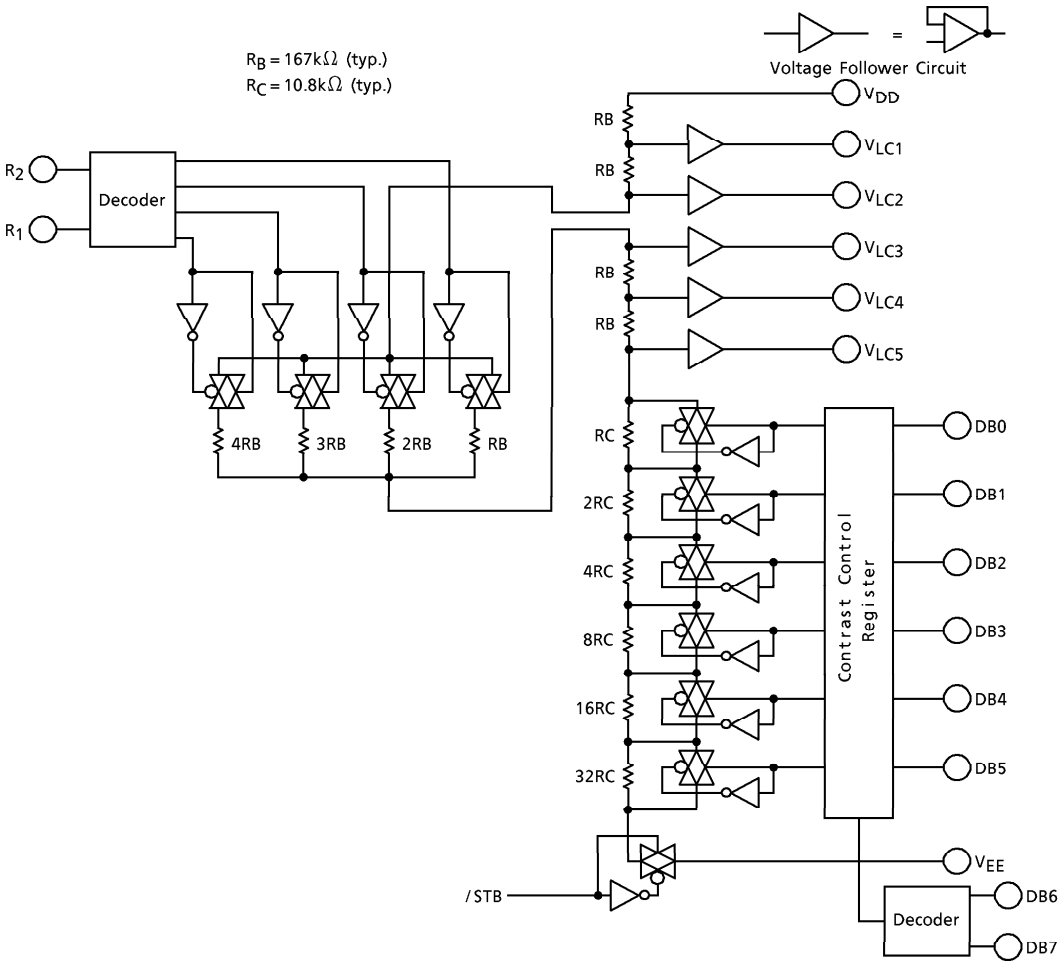


Fig. 7

- Op-amp, op-amp control register

  The T6B79 has five operational amplifiers which determine the LCD driving level. The power supplied by these op-amps is modified by the contents of the op-amp control register to match the LCD panel. The op-amp can also be controlled in such a way that it supplies full current on the rising edge of SEG and a reduced current otherwise.
  To maintain good LCD contrast, connect a capacitor between the op-amp output and V_{DD}. The value of the capacitor should normally be in range 0.1 to 1.0μF.

- Display RAM

  The display RAM consists of 48 rows × 64 columns for a total of 3072 cells. It is directly bit-mapped to the LCD. The relation between the display RAM and LCD is shown in Fig. 8.
  When the word length is set to eight bits, the display RAM is arranged in eight pages and each page contains 48 words. When the word length is set to six bits, the display RAM is arranged in 11 pages and each page contains 48 words. See Fig. 9.

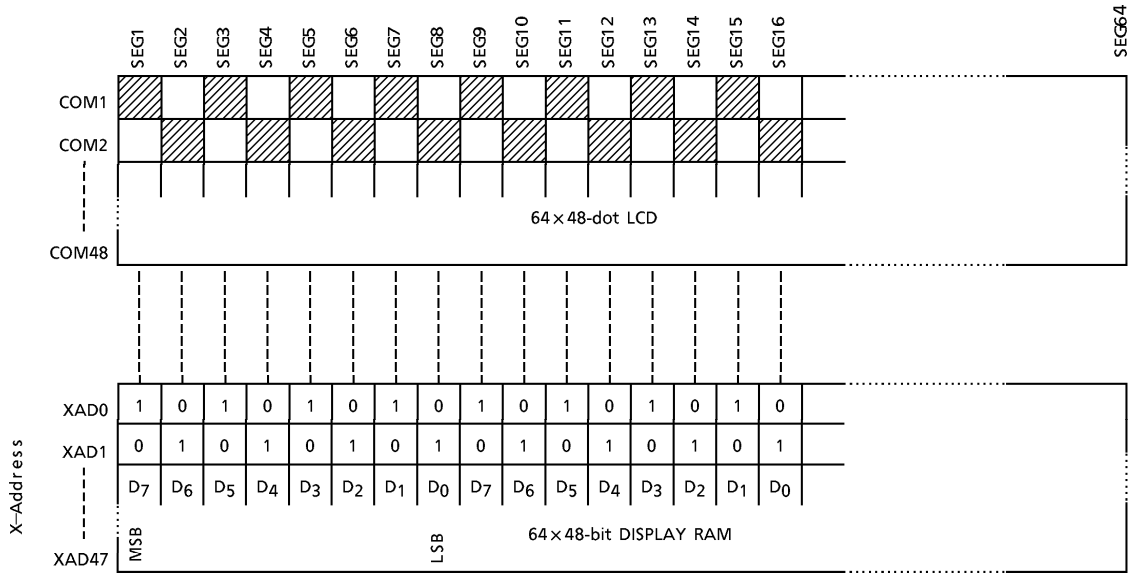
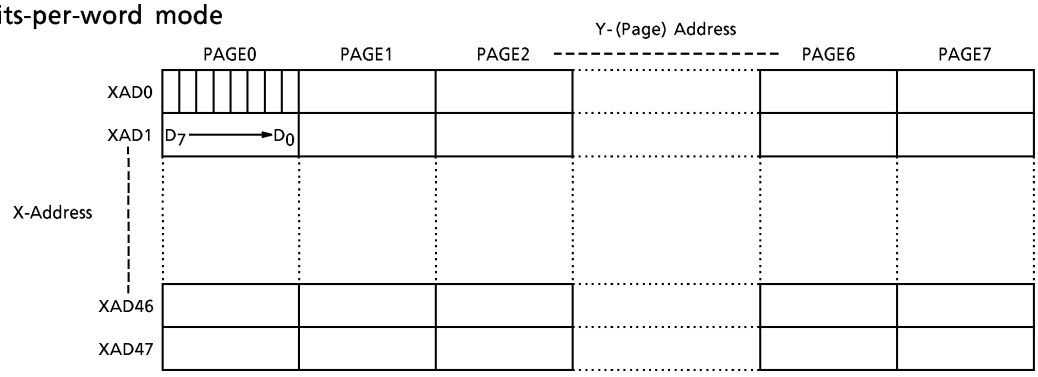


Fig. 8

(1) 8-bits-per-word mode



(2) 6-bits-per-word mode

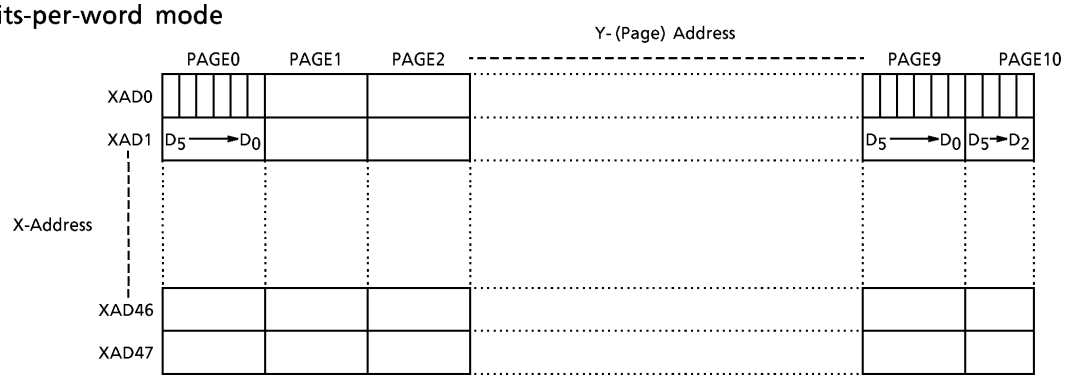


Fig. 9

COMMAND DEFINITIONS

COMMAND NAME	D / I	/ WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	FUNCTION
DPE	0	0	0	0	0	0	0	0	1	1 / 0	Display ON (1) / OFF (0)
86E	0	0	0	0	0	0	0	0	0	1 / 0	Word Length : 8 bits (1) / 6 bits (0)
UDE	0	0	0	0	0	0	0	1	1 / 0	1 / 0	Counter Select : DB1 Y (1) / X (0) Mode Select : DB0 UP (1) / DOWN (0)
CHE	0	0	0	0	0	1	1	*	*	*	Test Mode Select
OPA1	0	0	0	0	0	1	0	*	1 / 0	1 / 0	Op-Amp Power Control 1
OPA2	0	0	0	0	0	0	1	*	1 / 0	1 / 0	Op-Amp Power Control 2
SYE	0	0	0	0	1	*	Y-(Page) Address (0 to 10)				Y-(Page) Address Set
SZE	0	0	0	1	Z-Address (0 to 47)						Z-Address Set
SXE	0	0	1	0	X-Address (0 to 47)						X-Address Set
SCE	0	0	1	1	CONTRAST CONTROL (0 to 63)						Contrast Set
STRD	0	1	B	8 / 6	D	R	0	0	Y / X	U / D	Status Read
DAWR	1	0	Write Data								Display Data Write
DARD	1	1	Read Data								Display Data Read

* : INVALID

- Display ON / OFF select (DPE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	1	1	Display ON (03H)
0	0	0	0	0	0	0	0	1	0	Display OFF (02H)

This command turns display ON / OFF. It does not affect the data in the display RAM.
When the command "Display OFF" is selected, all column display and row display waveforms revert to the V_{DD} level.

(Note) An L input on /RST turns display OFF.

- Word length 8 bits / 6 bits select (86E)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	0	1	8-bit word mode (01H)
0	0	0	0	0	0	0	0	0	0	6-bit word mode (00H)

This command sets the word length for display RAM data to either six bits or eight bits.

(Note) An L input on /RST sets the word length to eight bits per word.

- X / Y (page) counter, up / down mode select (UDE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	0	0	X-Counter / Down Mode (04H)
0	0	0	0	0	0	0	1	0	1	X-Counter / Up Mode (05H)
0	0	0	0	0	0	0	1	1	0	Y-Counter / Down Mode (06H)
0	0	0	0	0	0	0	1	1	1	Y-Counter / Up Mode (07H)

This command selects the counter and the up / down mode. For instance, when X-counter / up mode is selected, the X-address is incremented in response to every data read and write. However, when X-Counter / up mode is selected, the address in the Y-(page) counter will not change. Hence the Y-address must be set (with the SYE command) before it can be changed.

(Note) An L input on /RST sets the Y-counter to up mode.

- Test mode select (CHE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	1	*	*	*	* : INVALID

This command selects the test mode. Do not use this command.

- Set Y-(page) address (SYE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	*	A	A	A	A

* : INVALID

Range: 8-bit/Word : 20H to 27H (Page 0 to Page 7)
6-bit/Word : 20H to 2AH (Page 0 to Page 10)

When operating in 8-bits-per-word mode, this command selects one of the eight pages in the display RAM. (Do not try to select a page outside this range.) When operating in 6-bits-per-word mode, this command selects one of the 11 pages in the display RAM.

(Note) An L input on /RST sets the Y-address to page 0.

- Set Z-address (SZE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	A	A	A	A	A	A

Range: 40H to 6FH (ZAD0 to ZAD47)

This command sets the top row of the LCD screen, irrespective of the current X-address.
For instance, when the Z-address is 32, the top row of the LCD screen is address 32 of the display RAM, and the bottom row of the LCD screen is address 31 of the display RAM.

(Note) An L input on /RST sets the Z-address to 0.

- Set X-address (SXE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	A	A	A	A	A	A

Range: 80H to AFH (XAD0 to XAD47)

This command sets the X-address (in the range 0 to 47). An L input on /RST sets the X-address to page 0.

- Set contrast (SCE)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	A	A	A	A	A	A

Range: C0H to FFH

This command sets the contrast for the LCD. The LED contrast can be set in 64 steps. The command C0H selects the brightest level; the command FFH selects the darkest.

- Op-amp control 1 (OPA1)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	*	A	A

* : INVALID

Range: 10H to 13H (when DB2 = 0)

This command sets the power supply strength for the operational amplifier. This command selects one of four levels. The command 10H selects the lowest power supply strength and the command 13H selects the maximum power supply strength.

(Note) An L input to /RST sets the op-amp power supply strength to the lowest level.

- Op-amp control 2 (OPA2)

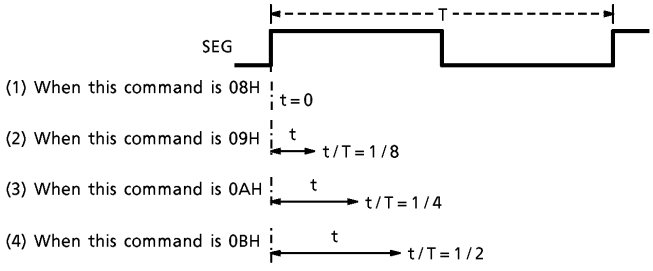
/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	*	A	A

* : INVALID

Range: 08H to 0BH (when DB2 = 0)

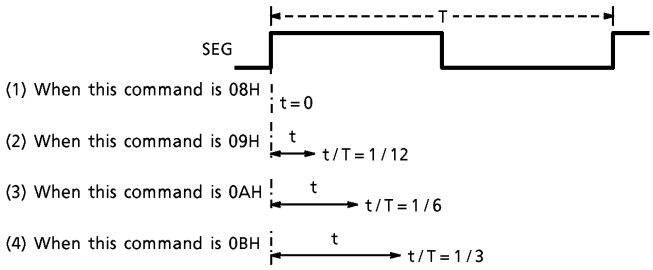
This command enhances the power supply strength of the operational amplifier over a short period from the rising edge of SEG. This command selects one of four levels of strength.

(Note) An L input to /RST sets t to 0 for the op-amp. See Figs. 10-1 and 10-2.
It is not possible to select the combination OPA1 = 10H and OPA2 = 08H.
After a Reset, set OPA1 and OPA2 according to the application.



The amplifier's strength is enhanced over the period denoted by ↔, starting on the rising edge of SEG.

Fig. 10-1 (1/48 duty)



The amplifier's strength is enhanced over the period denoted by ↔, starting on the rising edge of SEG.

Fig. 10-2 (1/6 or 1/32 duty)

- Status read (STRD)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	B	8/6	D	R	0	0	Y/X	U/D

B (Busy) : When B = 1 the T6B79 is executing an internal operation and no instruction can be accepted except STRD.
When B = 0 the T6B79 can accept an instruction.

8/6 (Word Length) : When 8/6 = 1 the word length of the display data is eight bits per word.
When 8/6 = 0 the word length of the display data is six bits per word.

D (Display) : When D = 1 display is ON.
When D = 0 display is OFF.

R (Reset) : When R = 1 the T6B79 is in reset state.
When R = 0 the T6B79 is in operating state.

Y/X (Counter) : When Y/X = 1 the Y counter is selected.
When Y/X = 0 the X counter is selected.

U/D (Up/down) : When U/D = 1 the X and Y counters are in up mode.
When U/D = 0 the X and Y counters are in down mode.

- Write/read display data (DAWR/DARD)

/WR	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D	D	D	D	D	D	D	D
1	1	D	D	D	D	D	D	D	D

DAWR : Display Data Write
DARD : Display Data Read

The command DAWR writes the display data to the display RAM. The command DARD outputs the display data from the display RAM. However, when a data read is executed, the correct data does not appear on the first data reading. Therefore, ensure that the T6B79 performs a dummy data read before reading the actual data.

FUNCTION DESCRIPTION

- X-address counter and Y-(page) address counter

Fig. 11 shows a sample operation involving the X-address counter.
After Reset is executed, the X-address (XAD) becomes 0, then X-counter / up mode is selected.
Next, the X-address is set to 46 using the SXE command.
After data has been written or read, the X-address is automatically incremented by 1.
After X-counter / down mode has been selected and data has been written or read, the X-address is automatically decremented by 1.
When the X-counter is selected, the Y-counter is not incremented or decremented.

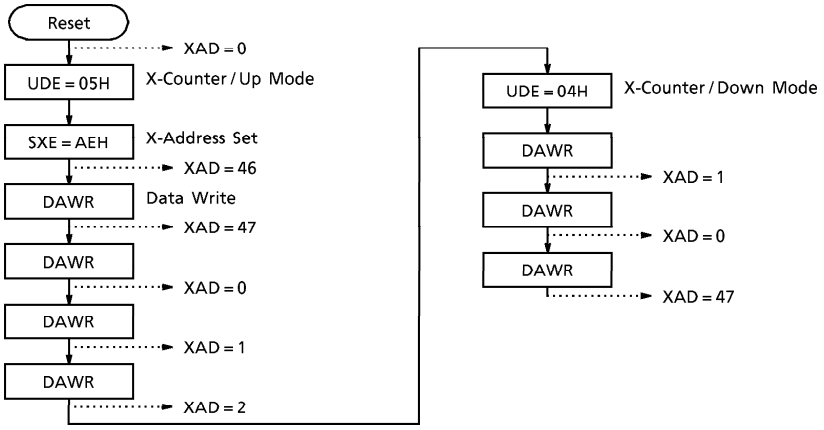


Fig. 11

Fig. 12 shows a sample operation involving the Y-address counter in 8-bit word length mode.
After Reset is executed, the Y-(page) address (Page) becomes 0, then Y-(page) counter / up mode and 8-bit word length mode are selected. After data has been written or read, the Y-(page) address counter is automatically incremented by 1.
After Y-(page) counter / down mode has been selected and data has been written or read, the Y-(page) address is automatically decremented by 1.
When the Y-(page) counter is selected, the X-counter is not incremented or decremented.

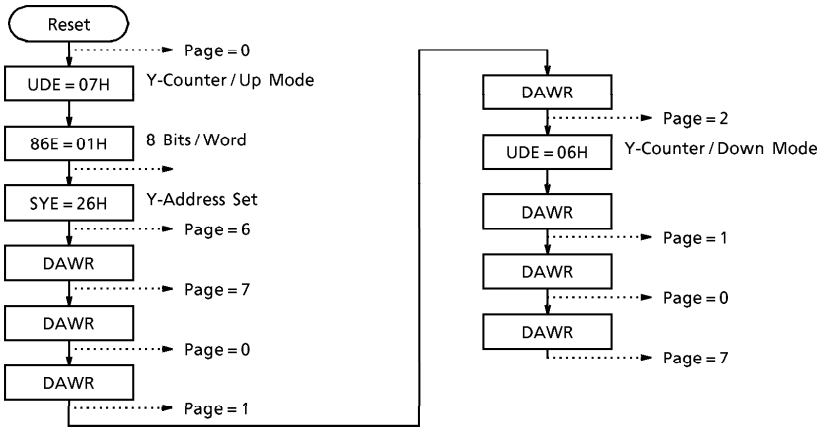


Fig. 12

When operating in 6-bit word length mode, the Y-(page) address counter can count up to 10. If Page = 10 in up mode, after data has been written or read, the Y-(page) address (Page) becomes 0.
If Page = 0 in down mode, after data has been written or read, the Y-(page) address (Page) becomes 10.

- Data read

When reading data, there are some cases when dummy data must be read. This is because when the data read command is invoked, the data pointed to by the address counter is transferred to the output register; the contents of the output register are then transferred by the next data read command.
Therefore when reading data straight after power-on or straight after an address-setting command, such as SYE or SXE, a dummy data read must be performed. See Fig. 13.

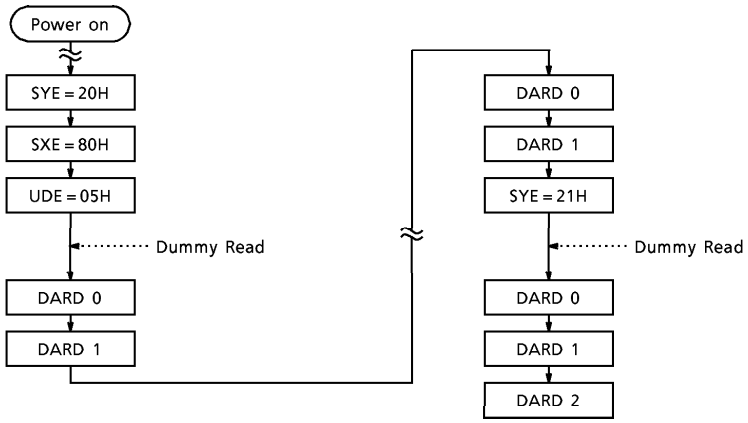


Fig. 13

- Reset function

When /RST = L, the reset function is executed and the following settings are made.

(1) Display ..... OFF
(2) Word length ..... 8 bits / word
(3) Counter mode ..... Y-counter / up mode
(4) Y-(page) address ..... Page = 0
(5) X-address ..... XAD = 0
(6) Z-address ..... ZAD = 0
(7) Op-amp1 (OPA1) ..... min
(8) Op-amp2 (OPA2) ..... min

- Standby function

When /STB = L, the T6B79 is in standby state. The internal oscillator is stopped, power consumption is reduced, and the power supply level for the LCD (V_{LC1} to V_{LC5}) becomes V_{DD}.

- Busy flag

When the T6B79 is executing an internal operation (other than the STRD command), the busy flag is set to logical H. The state of the busy flag is output in response to the STRD command. While the busy flag is H, no instruction can be accepted (except the STRD command). The busy state period (T) is as follows.

$2 / f_{OSC} \leqq T \leqq 4 / f_{OSC}$ [seconds] f_{OSC} : Frequency of OSC1

- Oscillation frequency

  The frequency select pins (FS1 and FS2) are used to set the relation between the oscillation frequency (f_{OSC}) and the frequency of the internal M signal (f_M), as shown in the table below.

R_f (kΩ)	f_{OSC} (kHz)	f_M (Hz)	FS1	FS2
1200	26.88	35	0	0
570	53.76	35	1	0
130	215.00	35	0	1
61	430.10	35	1	1

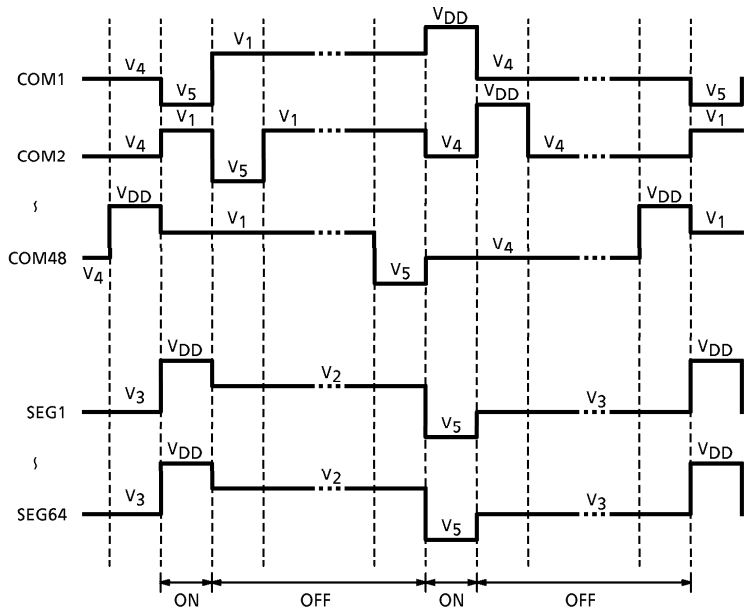
(Note) The resistance values are typical values (V_{DD} = 5.0V).
The oscillation frequency depends on how the device is mounted. It is necessary to adjust the oscillation frequency to a target value.

- Duty select

  The table below shows the relation between the values on the DS1 and DS2 pins and the duty cycle.

DS1	DS2	DUTY
0	0	1 / 16
1	0	1 / 32
0	1	1 / 48
1	1	1 / 48

LCD DRIVER WAVEFORM



LCD driver timing chart (1/48 duty)

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	− 0.3 to 7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{EE} (Note 3)	V_{DD} − 18.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1, 2)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

(Note 1) Referenced to $V_{SS} = 0V$

(Note 2) Applies to all data bus pins and input pins except V_{EE}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4} and V_{LC5}.

(Note 3) Ensure that the following condition is always maintained.
$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5} \geqq V_{EE}$

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITIONS (1) (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 3.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM		SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)		V_{LC5} V_{EE}	—	—	V_{DD} − 16.0	—	V_{DD} − 4.0	V	V_{EE}, V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	R_1, R_2, FS1, FS2, DS1, DS2, DB0~DB7, D / I, / WR, / CE, / RST, / STB
	L Level	V_{IL}	—	—	0	—	0.2 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = − 400μA	V_{DD} − 0.2	—	V_{DD}	V	D / I, / WR, / CE, DB0~DB7, / RST, / STB
	L Level	V_{OL}	—	I_{OL} = 400μA	0	—	0.2	V	
Column Driver Output Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0V Load current = ± 100μA	—	—	7.5	kΩ	SEG1 to SEG64
Row Driver Output Resistance		Rrow	—	VDD − VLC5 = 11.0V Load current = ± 100μA	—	—	1.5	kΩ	COM1 to COM48
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	− 1	—	1	μA	R_1, R_2, D / I, / WR, / CE, DB0~DB7, / STB, / RST, FS1, FS2, DS1, DS2
Operating Freq.		f_{osc}	—	—	20	—	500	kHz	OSC1
External Clock Freq.		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	270	300	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	300	350	μA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	− 1	—	1	μA	V_{DD}
Output Voltage (Quadruplexer Mode)		VO3	3	(Note 4)	− 6.40	− 7.00	—	V	V_{OUT3}

(Note 1) V_{DD} = 3.0 ± 10%, V_{EE} = V_{OUT} (from DC-DC converter), no data access
R_f = 47kΩ, no load, 1 / 8 bias, FS1, 2 = H, op-amp strength at minimum level

(Note 2) V_{DD} = 3.0 ± 10%, V_{EE} = V_{OUT} (from DC-DC converter), data access cycle $f_{/CE}$ = 1MHz,
R_f = 47kΩ, no load, 1 / 8 bias, FS1, 2 = H, op-amp strength at minimum level

(Note 3) V_{DD} = 3.0 ± 10%, V_{DD} − V_{EE} = 16.0V, / STB = L

(Note 4) V_{DD} = 3.0V, I_{Load} = 500μA, V_{EE} = − 9.0V (external power supply)
CnA − CnB = 2.2μF, V_{DD} − V_{OUT3} = 2.2μF, R_f = 47kΩ, Ta = 25°C

DC CHARACTERISTICS

TEST CONDITIONS (2) (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 5.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM		SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)		V_{DD}	—	—	4.5	—	5.5	V	V_{DD}
Operating Supply (2)		V_{LC5} V_{EE}	—	—	V_{DD} − 16.0	—	V_{DD} − 4.0	V	V_{EE}, V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	R_1, R_2, FS1, FS2, DS1, DS2, DB0 to DB7, D / I, / WR, / CE, / RST, / STB
	L Level	V_{IL}	—	—	0	—	0.3 VDD	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = − 400μA	V_{DD} − 0.2	—	V_{DD}	V	D / I, / WR, / CE, DB0 to DB7, / RST, / STB
	L Level	V_{OL}	—	I_{OL} = 400μA	0	—	0.2	V	
Column Driver Output Resistance		Rcol	—	V_{DD} − V_{LC5} = 11.0V Load current = ± 100μA	—	—	7.5	kΩ	SEG1 to SEG64
Row Driver Output Resistance		Rrow	—	V_{DD} − V_{LC5} = 11.0V Load current = ± 100μA	—	—	1.5	kΩ	COM1 to COM48
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	− 1	—	1	μA	R_1, R_2, D / I, / WR, / CE, DB0 to DB7, / STB, / RST, FS1, FS2, DS1, DS2
Operating Freq.		f_{osc}	—	—	20	—	500	kHz	OSC1
External Clock Freq.		f_{ex}	—	—	20	—	500	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	470	650	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	500	700	μA	V_{DD}
Current Consumption (3)		I_{DDSTB}	—	(Note 3)	− 1	—	1	μA	V_{DD}
Output Voltage (Doubler Mode)		VO1	1	(Note 4)	− 4.25	− 4.50	—	V	V_{OUT1}
Output Voltage (Tripler Mode)		VO2	2	(Note 5)	− 8.50	− 9.00	—	V	V_{OUT2}

(Note 1) V_{DD} = 5.0 ± 10%, V_{EE} = V_{OUT} (from DC-DC converter), no data access
R_f = 47kΩ, no load, 1 / 8 bias, FS1, 2 = H, op-amp strength at minimum level

(Note 2) V_{DD} = 5.0 ± 10%, V_{EE} = V_{OUT} (from DC-DC converter), data access cycle $f_{/CE}$ = 1MHz,
R_f = 47kΩ, no load, 1 / 8 bias, FS1, 2 = H, op-amp strength at minimum level

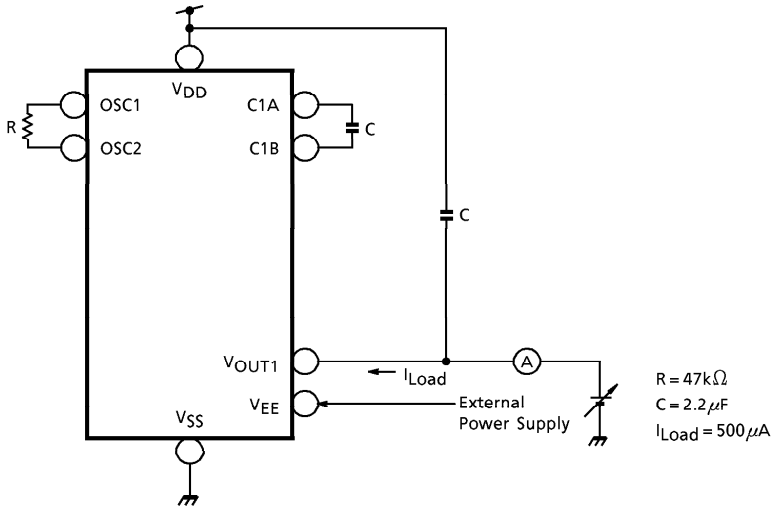
(Note 3) V_{DD} = 5.0 ± 10%, V_{DD} − V_{EE} = 16.0V, / STB = L

(Note 4) V_{DD} = 5.0V, I_{Load} = 500μA, V_{EE} = − 5.0V (external power supply)
CnA − CnB = 2.2μF, V_{DD} − V_{OUT1} = 2.2μF, R_f = 47kΩ, Ta = 25°C

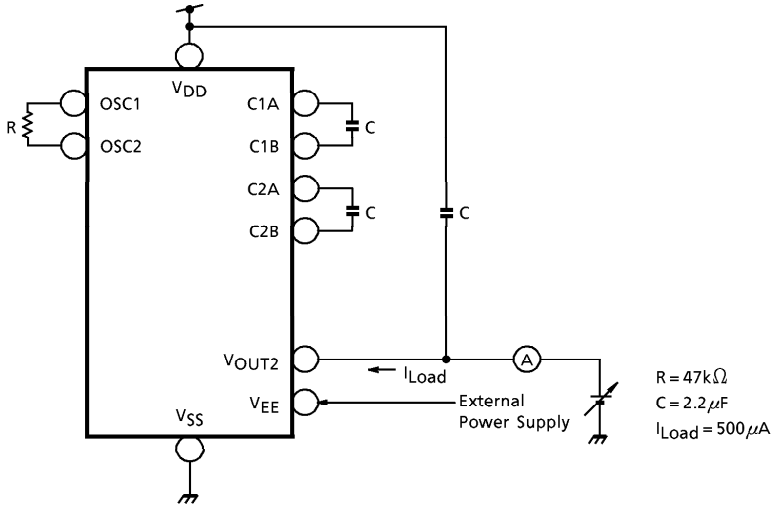
(Note 5) V_{DD} = 5.0V, I_{Load} = 500μA, V_{EE} = − 10.0V (external power supply)
CnA − CnB = 2.2μF, V_{DD} − V_{OUT2} = 2.2μF, R_f = 47kΩ, Ta = 25°C

TEST CIRCUIT

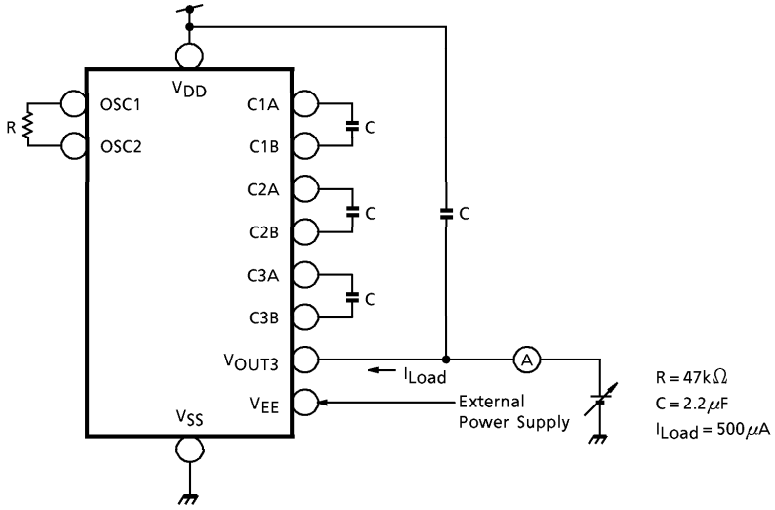
1. Doubler mode



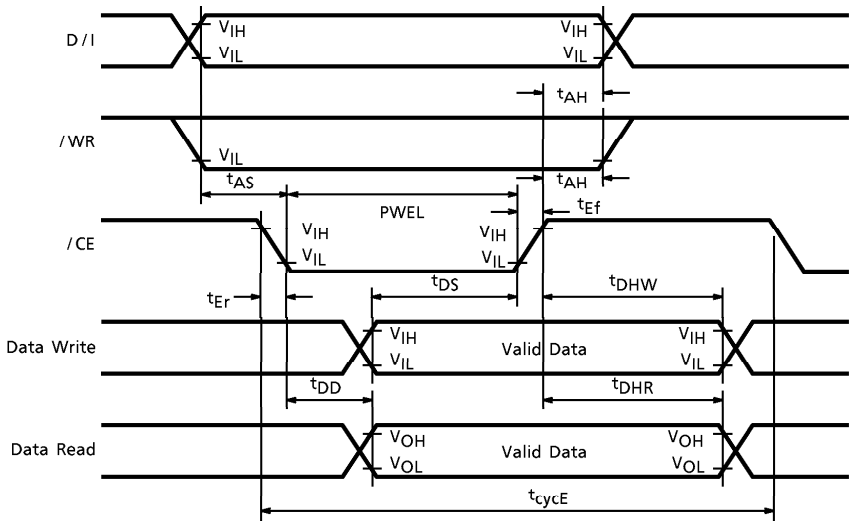
2. Tripler mode



3. Quadruplexer mode



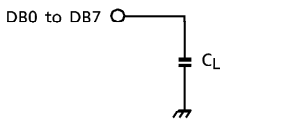
AC CHARACTERISTICS



TEST CONDITIONS (1)
(V_{SS} = 0V, V_{DD} = 3.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM	SYMBOL	MIN	MAX	UNIT
Enable Cycle Time	t_{cycE}	1000	—	ns
Enable Pulse Width	PWEL	450	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	25	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	280	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD} (Note)	—	300	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

LOAD CIRCUIT



C_L = 100pF
(including wiring capacitance)

TEST CONDITIONS (2)
(V_{SS} = 0V, V_{DD} = 5.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM	SYMBOL	MIN	MAX	UNIT
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEL	220	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	0	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD} (Note)	—	120	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

(Note) With load circuit connected

APPLICATION CIRCUIT

- Oscillation frequency is at a minimum.
- LCD drive bias is 1/8.
- DC-DC converter in doubler mode is used.