

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

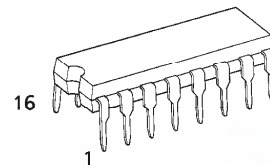
TC4521BP

TC4521BP 24 – STAGE FREQUENCY DIVIDER

TC4521BP is frequency divider consisting of 24 stages of flip-flop. The input section is equipped with an inverter to enable to use either RC oscillator circuit or crystal oscillator circuit and to accept pulse from external clock source.

Each flip-flop is inverted by the falling edge of the output of previous stage flip-flop and this can count up to the maximum of $2^{24} = 16,777,216$.

Since six outputs, 2^{18} , 2^{19} , 2^{20} , 2^{21} , 2^{22} , and 2^{23} are available besides of 2^{24} , adjustment of frequency divided output can be achieved.

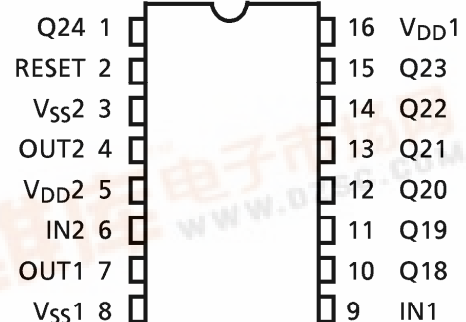


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

MAXIMUM RATINGS

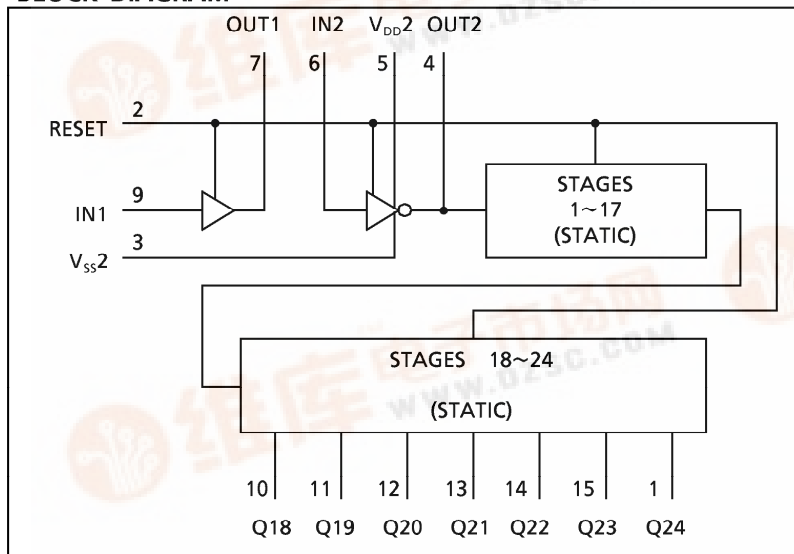
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD1}	$V_{SS1} - 0.5 \sim V_{SS1} + 20$	V
	V_{DD2}	$V_{SS1} - 0.5 \sim V_{DD1} + 0.5$	
Input Voltage	V_{IN}	$V_{SS1} - 0.5 \sim V_{DD1} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS1} - 0.5 \sim V_{DD1} + 0.5$	
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

PIN ASSIGNMENT



(TOP VIEW)

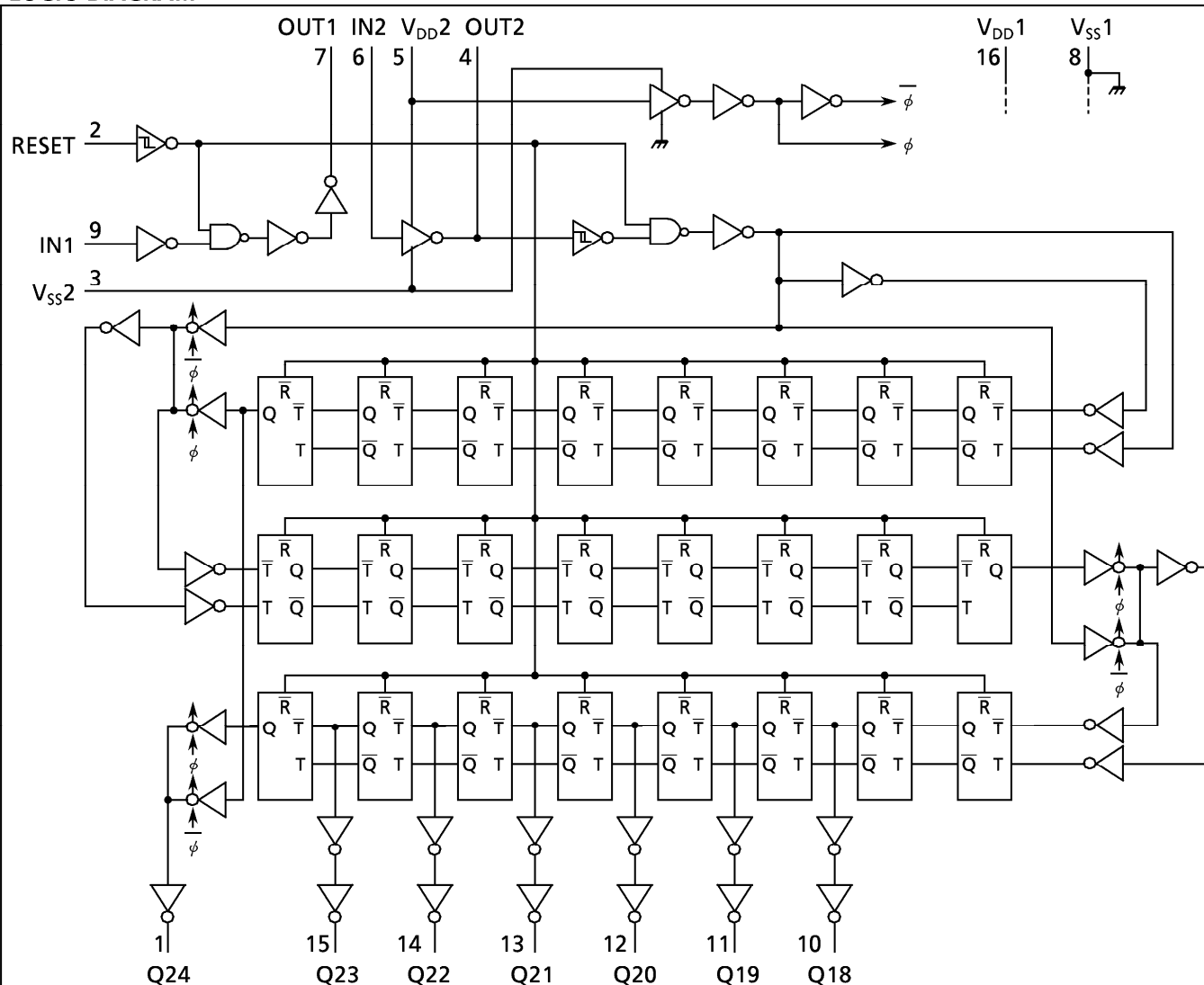
BLOCK DIAGRAM



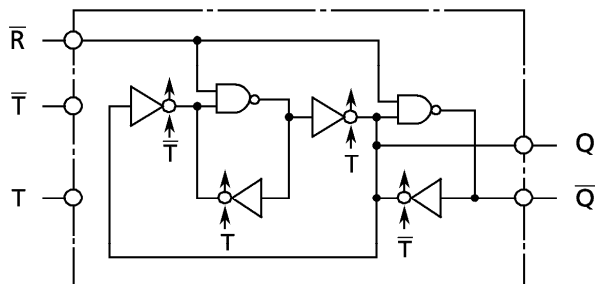
COUNT CAPACITY

OUTPUT	COUNT CAPACITY
Q18	$2^{18} = 262,144$
Q19	$2^{19} = 524,288$
Q20	$2^{20} = 1,048,576$
Q21	$2^{21} = 2,097,152$
Q22	$2^{22} = 4,194,304$
Q23	$2^{23} = 8,388,608$
Q24	$2^{24} = 16,777,216$

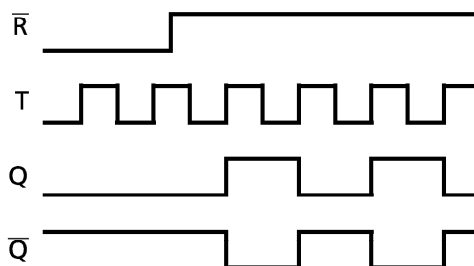
LOGIC DIAGRAM



INTERNAL FLIP FLOP LOGIC DIAGRAM



FLIP FLOP TIMING CHART



961001EBA2'

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RECOMMENDED OPERATING CONDITIONS ($V_{SS1} = V_{SS2} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD1}, V_{DD2}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD1}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS1} = V_{SS2} = 0V, V_{DD1} = V_{DD2}$)

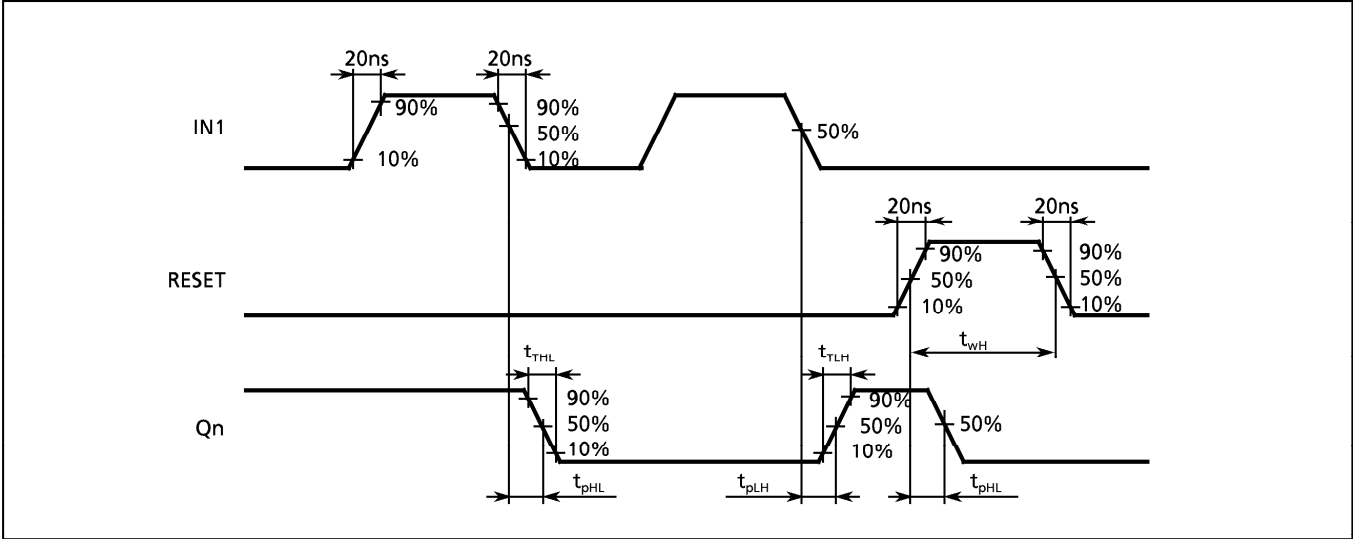
CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5V$	5	-2.5	—	-2.1	-4.0	—	-1.7	—	
		$V_{OH} = 9.5V$	10	-1.5	—	-1.3	-2.2	—	-1.1	—	
		$V_{OH} = 13.5V$	15	-4.0	—	-3.4	-9.0	—	-2.8	—	
Output Low Current	I_{OL}	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.2	—	0.42	—	mA
		$V_{OL} = 0.5V$	10	1.5	—	1.3	3.2	—	1.1	—	
		$V_{OL} = 1.5V$	15	4.0	—	3.4	12.0	—	2.8	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0V, 9.0V$	10	7.0	—	7.0	5.5	—	7.0	—	
		$V_{OUT} = 1.5V, 13.5V$	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT} < 1\mu A$									
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0V, 9.0V$	10	—	3.0	—	4.5	3.0	—	3.0	
		$V_{OUT} = 1.5V, 13.5V$	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT} < 1\mu A$									
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5	—	5	—	0.005	5	—	150	μA
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{SS}1 = V_{SS}2 = 0V, V_{DD}1 = V_{DD}2, C_L = 50pF)

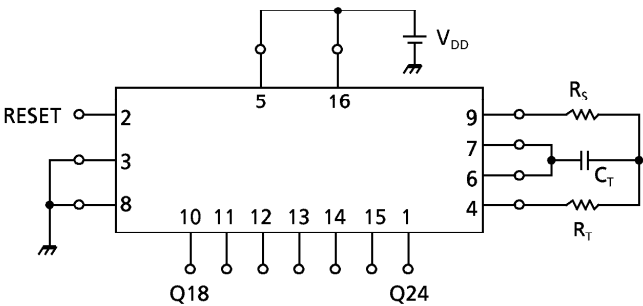
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5 10 15	— — —	70 35 30	200 100 80	ns
Output Transition Time (High to Low)	t _{THL}		5 10 15	— — —	70 35 30	200 100 80	
Propagation Delay Time (IN2 - Q18)	t _{pLH} t _{pHL}		5 10 15	— — —	1.1 0.5 0.3	9.0 3.5 2.7	μs
Propagation Delay Time (IN2 - Q24)	t _{pLH} t _{pHL}		5 10 15	— — —	1.4 0.6 0.4	12 4.5 3.5	
Propagation Delay Time (RESET - Qn)	t _{pHL}		5 10 15	— — —	220 100 70	2600 1000 750	ns
Max. Clock Frequency	f _{CL}		5 10 15	3 6 8	9.5 17.5 23.5	— — —	MHz
Max. Clock Input Rise Time Max. Clock Input Fall Time	t _{rCL} t _{fCL}		5 10 15	No Limit			μs
Min. Clock Pulse Width	t _W		5 10 15	— — —	55 25 16	385 150 120	ns
Min. Pulse Width (RESET)	t _{WH}		5 10 15	— — —	60 26 20	385 150 120	
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



APPLICATION CIRCUIT

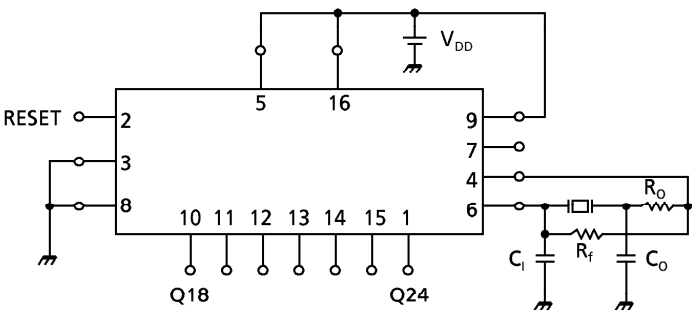
* When CR oscillation is used as time reference



$R_s \geq 2R_T$

$f_{osc} \approx \frac{1}{2.2R_T C_T}$

* When crystal oscillation circuit is used as the time reference



Typical data

X'tal (Hz)	C _i , C _o (pF)	R _o (Ω)
32.768k	23	500k
100k	60	100k
1M	45~50	100
4.194304M	12~15	0

$R_f = 10M\Omega$

Unit in mm

