INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

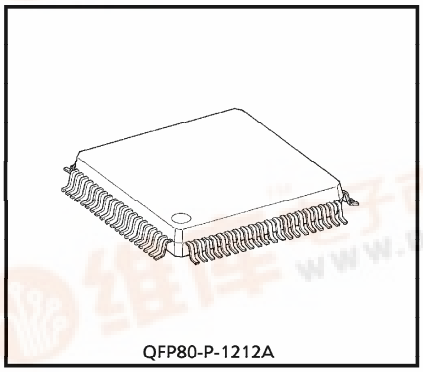
TOSHIBA CCD AREA IMAGE SENSOR

TC6134AF

CCD(Charge Coupled Device)

OUTLINE

The CMOS LSI of TC6134AF was developed to drive the TCD5340C, TCD5280D, TCD5120AC and TCD5130AC. TC6134AF can be combined with a vertical clock driver to constitute the CCD area image sensor driving circuit.



QFP80-P-1212A

Weight : 0.33g (Typ.)

FEATURES

- Generation of all timing pulses required to drive TCD5340C, TCD5280D, TCD5120AC and TCD5130AC.
- Correspondence with electronic shutter from 1/50, 1/60 to 1/10000 s.
  (TCD5120AC, TCD5130AC : 1/50~1/2000 s)
- Generation of sampling pulses for CDS signal processing.

MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Input Current	I_{IN}	± 10	mA
Storage Temperature	T_{stg}	−40~125	°C

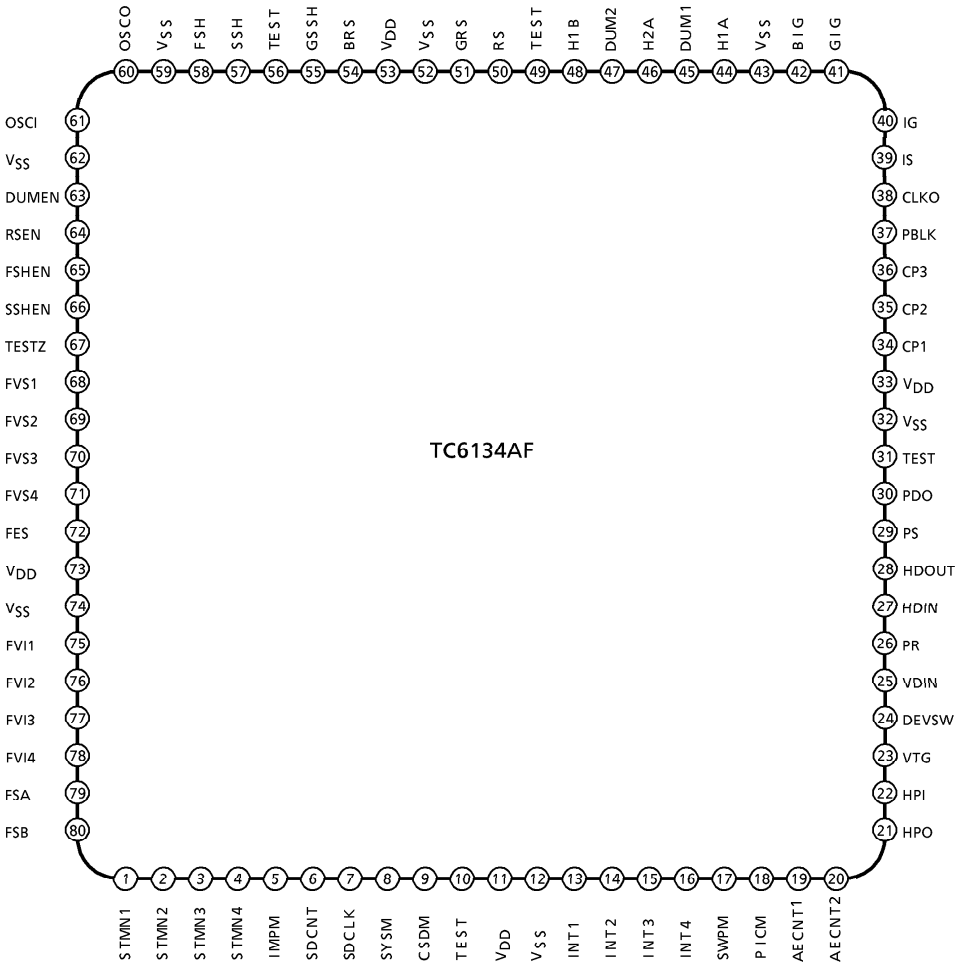
RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.50 ~ 5.50	V
Operating Temperature	T_{opr}	−20 ~ 70	°C

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.75~5.25V, Ta = 0~70°C)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}		3.5	—	—	V
	"L" Level	V_{IL}		—	—	1.5	
Input Current	"H" Level	I_{IH}	$V_{IN} = V_{DD}$	– 10	—	10	μA
			$V_{IN} = V_{DD}$, (included PULL-DOWN)	10	—	200	
	"L" Level	I_{IL}	$V_{IN} = V_{SS}$	– 10	—	10	
			$V_{IN} = V_{SS}$, (included PULL-UP)	– 200	—	– 10	
Output Voltage	"H" Level	V_{OH}	I_{OH} = – 8mA, H1A, H2A	2.4	—	—	V
			I_{OH} = – 4mA except H1A, H2A				
	"L" Level	V_{OL}	I_{OL} = 8mA, H1A, H2A	—	—	0.4	
			I_{OL} = 4mA except H1A, H2A				
Static Consumption Current		I_{DD}	C_L = 0pF, V_{DD} = 5V, Ta = 25°C	—	—	200	μA

PIN CONNECTION



PIN FUNCTION

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION
1	STM1	I	—	Shutter period setting terminal. (See the attached table for the shutter period)
2	STM2	I		
3	STM3	I		
4	STM4	I		
5	INPM	I	—	Terminal for switching shutter speed setting mode. - serial input mode in H level - parallel input mode in L level
6	SDCNT	I	—	Serial data control input connected to VD of synchronization generator IC.
7	SDCLK	I	—	Serial data clock input.
8	SYSM	I	—	Terminal for switching PAL or NTSC mode. - NTSC mode in L level - PAL mode in H level
9	CSDM	I	—	Input terminal for CDS mode.
10	TEST	I	—	Test terminal is opened for normal use.
11	V_{DD}	—	—	Connected to power supply 5V ± 0.25V
12	V_{SS}	—	—	Electronic shutter (Substrate sweep mode) is available on high resolution mode.
13	INT1	I	—	Resolution mode switching input.
14	INT2	I	—	※ Electronic shutter (Substrate sweep mode) is available on high resolution mode. ※ TCD5120AC, TCD5130AC : high resolution mode is available only in normal speed.
15	INT3	I	—	Input terminal for switching electronic shutter sweep mode. -Substrate sweep mode in L level. (TCD5120AC, TCD5130AC : this mode is not available.) -FIT sweep mode in H level.
16	INT4	I	—	Input terminal for switching storage mode. - 2 – 4 storage in L level. (Recommend) - 1 – 4 storage in H level.

INT1	INT2	INT3	
L	L	H L	Field storage mode
H	L		High resolution mode 50%
L	H		High resolution mode 25%
H	H	H L	Frame storage mode

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION
17	SWPM	I	—	Input terminal for switching storage mode. - reversible transfer in L level. - sequencial transfer in H level (Recommend) ※ Sweep mode is fixed to sequencial transfer mode on normal speed mode.
18	PICM	I	—	Input terminal for switching number of horizontal pixels. - 400K TCD5120AC, TCD5130AC, TCD5280D in H level. - 600K TCD5340C in L level.
19	AECNT1	I	—	Input terminal for controlling MNCSD mode, AECNT mode and electronic shutter speed.
20	AECNT2	I	—	
21	HPO	O	⎍	Horizontal transfer control pulse. This pulse is output within horizontal flyback time to indicate that horizontal CCD transfer period has stopped.
22	HPI	I	—	Connected to HPO for normal use.
23	VTG	O	—	Output terminal for standard pulse of AE mode is opened for normal use.
24	DEVSW	I	—	Input terminal for controlling 1H divider - stop working in L level. - work in H level.
25	VDIN	I	—	Input terminal for VD of synchronization generator IC.
26	PR	I	—	Input terminal for phase comparator.
27	HDIN	I	—	Input terminal for HD of synchronization generator IC.
28	HDOUT	O	⎍	Horizontal drive pulse is output when 1H divider works.
29	PS	I	—	Input terminal for phase comparator.
30	PDO	O	—	Output terminal for phase comparator.
31	TEST	I	—	Test terminal is opened for normal use.
32	V_{SS}	—	—	GND
33	V_{DD}	—	—	Connected to power supply 5V ± 0.25V.
34	CP1	O	⎍	Clamp pulse output for clamping the OB portion of CCD signal output.
35	CP2	O	⎍	Clamp pulse output for signal processing.
36	CP3	O	⎍	Clamp pulse output for signal processing.
37	PBLK	O	⎍	Pre-blanking pulse output. H level indicates the erase piriod.
38	CLKO	O	⎍	Master clock output for synchronization generator IC. (fck)

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION
39	IS	O	—	Test terminal is opened for normal use.
40	IG	O	—	Test terminal is opened for normal use.
41	GIG	I	—	Test terminal is opened for normal use.
42	BIG	O		
43	V_{SS}	—	—	GND
44	H1A	O	⊔⊓	Horizontal CCD drive pulse to be connected to the H1A gate of the CCD image sensor.
45	DUM1	O	—	Dummy output 1.
46	H2A	O	⊔⊓	Horizontal CCD drive pulse to be connected to the H2A gate of the CCD image sensor.
47	DUM2	O	—	Dummy output 2.
48	H1B	O	⊔⊓	Horizontal CCD drive pulse to be connected to the H1B gate of the CCD image sensor.
49	TEST	—	—	Test terminal is opened for normal use.
50	RS	O	⊓⊔	Reset gate pulse to be connected to the RS gate of the CCD image sensor.
51	GRS	I	—	Input and output terminal for adjusting RSO and SSH phase. The BRS output is delayed with a capacitor and resistor connected to the GRS, GSSH input.
52	V_{SS}	—	—	GND
53	V_{DD}	—	—	Connected to power supply 5.0V ± 0.25V.
54	BRS	O	⊔⊓	Input and output terminal for adjusting RSO and SSH phase. The BRS output is delayed with a capacitor and resistor connected to the GRS, GSSH input.
55	GSSH	I	—	
56	TEST	I	—	Test terminal is opened for normal use.
57	SSH	O	⊓⊔	Signal sampling pulse output.
58	FSH	O	⊓⊔	Feed through sampling pulse output.
59	V_{SS}	—	—	GND
60	OSCO	O	⊔⊓	Master clock output. (2 fck)
61	OSCI	I	—	Master clock input (2 fck)
62	V_{SS}	—	—	GND
63	DUMEN	I	—	Test terminal is opened for normal use. When L level puts on this terminal, dummy output is enable.
64	RSEN	I	—	Test terminal is opened for normal use. When L level puts on this terminal, RS output is enable.

PIN No.	SYMBOL	I/O	POLARITY	FUNCTION
65	FSHEN	I	—	Test terminal is opened for normal use. When L level puts on this terminal, FSH output is enable.
66	SSHEN	I	—	Test terminal is opened for normal use. When L level puts on this terminal, SSH output is enable.
67	TESTZ	I	—	Test terminal is opened for normal use.
68	FVS1	O		Vertical CCD drive pulse ϕS1, ϕS2, ϕS3 and ϕS4 connected to the inversion type vertical clock driver.
69	FVS2	O		
70	FVS3	O		
71	FVS4	O		
72	FES	O		Electronic shutter pulse connected to the inversion type drive.
73	V_{DD}	—	—	Connected to power supply 5V ± 0.25V.
74	V_{SS}	—	—	GND
75	FVI1	O		Vertical CCD drive pulse ϕI1, ϕI2, ϕI3 and ϕI4 connected to the inversion type vertical clock driver.
76	FVI2	O		
77	FVI3	O		
78	FVI4	O		
79	FSA	O		Field shift drive pulse ϕI1 and ϕI3 connected to the inversion type vertical clock driver.
80	FSB	O		

SETTING FOR ELECTRONIC SHUTTER SPEED

INPM (setting mode)	*3 CSDM (CSD mode)	Electronic shutter						Storage mode			
		STM1	STM2	STM3	STM4	function NTSC	function PAL	sub-strate	FIT shutter	*6 high resolution	
L (Parallel setting)	H or L	L	L	L	L	1/60 (1/30)*	1/50 (1/25)*	×	×	×*1	×*1
		H	L	L	L	1 / 100	1 / 60	○	○	○	○
		L	H	L	L	1 / 120		○	○	○	○
		H	H	L	L	1 / 250		○	○	○	○
		L	L	H	L	1 / 500		○	○	○	○*2
		H	L	H	L	1/1000,1/56	1 / 1000	○	○	○*2	×
		L	H	H	L	1 / 2000		○	○*2	×	×
		H	H	H	L	1 / 4000		○	×	×	×
		L	L	L	H	1 / 8000		○	×	×	×
		H	L	L	H	1 / 10000		○	×	×	×
		L	H	L	H	test mode		—	—	—	—
		H	H	L	H	test mode		—	—	—	—
		L	L	H	H	1 / 51		○	○	○	○
		H	L	H	H	1 / 61		○	○	○	○
	H	L	H	H	H	*4 MNCSD mode. The data about change vector on AECNT1 and AECNT2 increases or decreases shutter speed gradually.		○	○	×	×
								prohibitted from setting on frame storage mode.			
	L	H	H	H	H	*5 AECNT mode Timing pulse on AECNT1 and AECNT2 controls shutter speed.					
H *7 (serial setting)	H or L	Serial binary data on SDCLK and STM4 can set the shutter speed in 1H (partially in 1.5H).						○	○	○	○

☆ shutter speed on frame storage mode

○ available
× disable

*1 When normal mode is set on high resolution mode, there is different storage time in between 1 st and 2 nd field.

*2 When this mode is set, blooming margin of CCD area image sensor decrease.

*3 CSD mode

CSDM:L — When a shutter speed is on normal mode, the shutter speed is changed on the next field.

CSDM:H (CSD mode) — When a shutter speed is set, the shutter speed is changed gradually. The change slope shows as follows;

Storage time	Change slope
1.5H~8H	1H / 4 per field
~262.5 (312.5) H	3 percents of the storage time

*4 MNCSD mode

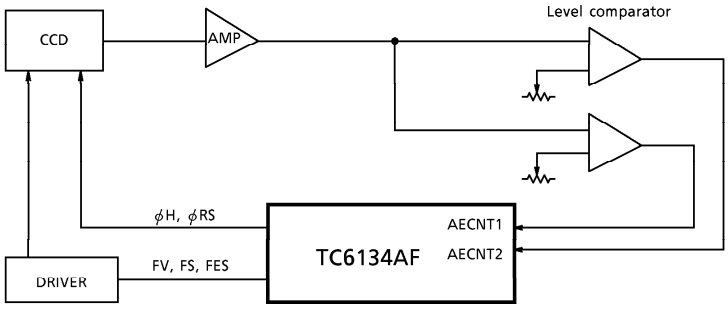
On MNCSO mode (CSDM:H) linputs on AECNT1 and AECNT2 increase or decrease the shutter speed. This mode is prohibitted on the frame storage mode.

CSDM	AECNT1	AECNT2	Function
H	L	L	Lengthen the storage time
	H	L	Not change
	L	H	
	H	H	Shorten the storage time

In this mode the highest shutter speed is limitted as follows:

INT1	INT2	INT3	Mode	Highest shutter speed
L	L	L	Substrate sweep, field storage	~1 / 4000
L	L	H	FIT sweep, frame storage	~1 / 1000
H	L	—	High resolution mode 50%	Prohibition
L	H	—	High resolution mode 25%	Prohibition
H	H	L	Substrate sweep, frame storage	Prohibition
H	H	H	FIT sweep, frame storage	Prohibition

Electronic shutter iris is realized in this mode.

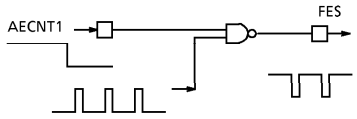


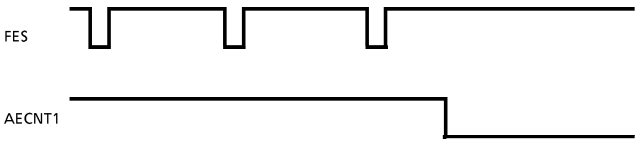
*5 AECNT mode

In this mode timing pulse on AECNT1 and AECNT2 can control the shutter speed.

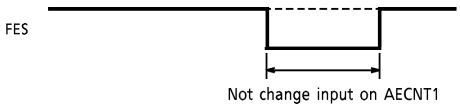
Input on AECNT1 controls FES pulse. The available range of setting the substrate shutter is until 1 / 10000 s.

AECNT1	FES
H	Generation
L	No generation



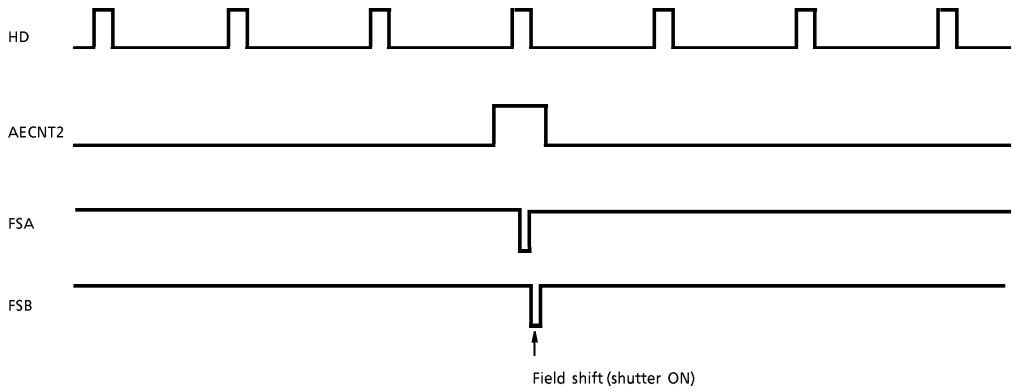


AECNT is not allowed to change while FES pulse is L level. Because AECNT1 gates FES pulse.

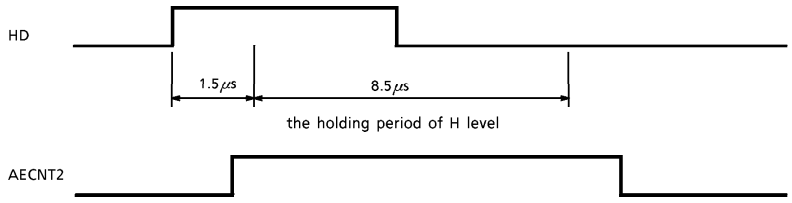


Input on AECNT2 controls FSA and FSB pulses. (FIT shutter).

AECNT2	FSA, FSB, FI1~4
H	Field shift
L	Line shift

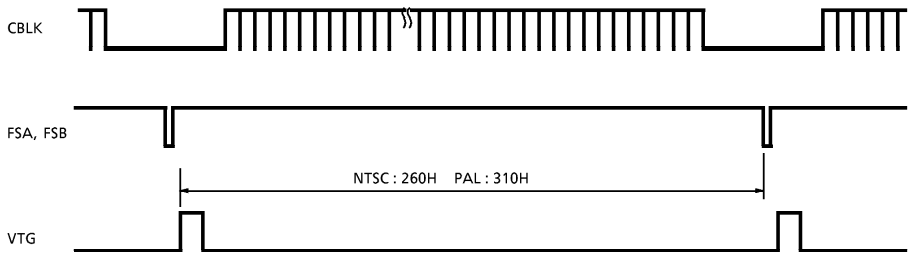


The period of H level on AECNT2 should be longer than the holding period of H level as follows.



On AECNT mode, generation of trigger pulse needs external counter circuits. And VTG pulse is used for the standard pulse resetting the external counter circuits. The time difference of VTG and field shift (shutter OFF) in the next field are set as follows;

260H (NTSC)
310H (PAL)



*6 High resolution mode

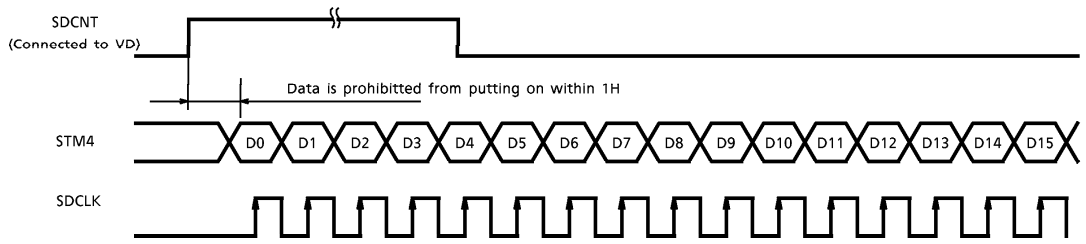
On high resolution mode, substrate and FIT shutter adds and reads out signal of two vertical pixels each field as pixels having different storaged signal. This mode realized high resolution.

For example:

When the shutter speed is set 1 / 100 s on high resolution (50%) mode, 1 / 100 s storaged signal and 1 / 200 s (1 / 100 s × 50%) storaged signal are added and read out. But substrate shutter is not available for TCD5120AC and TCD5130AC, so 1 field storaged (1 / 60 s or 1 / 50 s) signal and 1 / 200 s storaged signal are added and read out.

*7 • Serial setting mode

INPM : H level
STM4 : Serial data
SDCLK : Clock for serial data
SDCNT : Serial data control connected to VD of synchronization generator IC.



SDCNT is connected to VD of synchronization generator IC.
Data is prohibitted from putting on within 1H after VD pulse raises. The data set on STM4 is fed into shutter speed controller when SDCLK pulse raises. The data is organizad 16 bits.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	SS0	S0	S1	S2	S3	S4	S5	S6	S7	S8	×				
Put "0" on D0	9bits binary data put on S0 – 8 can set the shutter speed in 1H. And the data on SS0 can set the shutter speed in 0.5H below 10H on NTSC mode or 14H on PAL mode.										Not concerned				

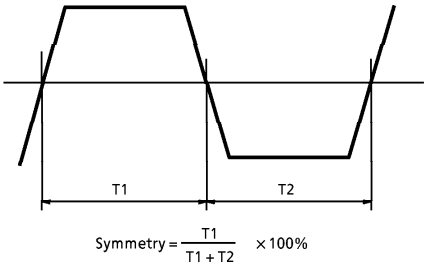
TC6134AF has shift resistor (clock : SDCLK). When data above 16 bits puts on, last 16 bits is available.
Input on SDCNT always connect to VD.

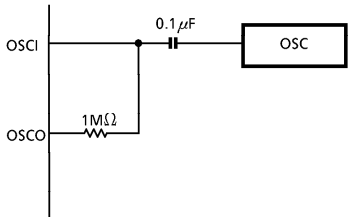
Allowance range of input shows as follows.

System	Storage mode			
	Substrate shutter	FIT shutter	High resolution	
			50%	25%
NTSC	1H~256H	11H~256H	22H~256H	44H~256H
PAL	1H~306H	11H~306H	22H~306H	44H~306H

INPUT OF MASTER CLOCK

- It is necessary the symmetry of master clock put on OSCI is within 50 ± 10%.





- Clock frequency

CCD type No.	TV system	Nominal pixel number	Clock frequency
TCD5120AC	NTSC	400k	1820fH = 28.63636MHz
TCD5130AC	PAL	470k	1816fH = 28.37500MHz
TCD5340C	NTSC	600k	2730fH = 42.95454MHz
TCD5280D	NTSC	400k	1820fH = 28.63636MHz

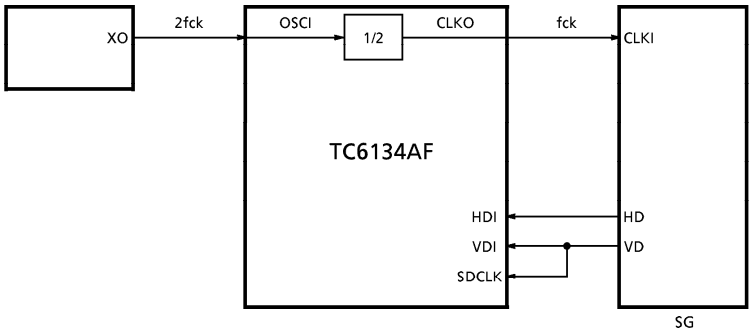
LOW SPEED SHUTTER MODE

TESTZ	SYSM	INPM	CSD	INT1	INT2	INT3	STM1	STM2	STM3	STM4	Storage time
H	L (NTSC)	L	L	H	H	H	H	L	H	L	1/56 s (279H)
H	H (PAL)	L	L	H	H	X	L	L	H	H	1/56 s (277H)
				L	L						

In the case of NTSC mode, this mode is available only in the frame storage and FIT sweep mode.

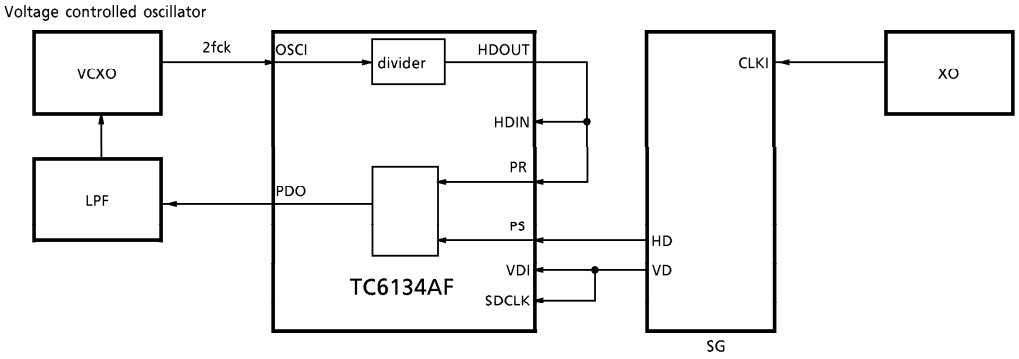
CONNECTION TO SYNCHRONIZATION GENERATOR IC

- Connection to synchronization generator IC
  (master clock is fck)



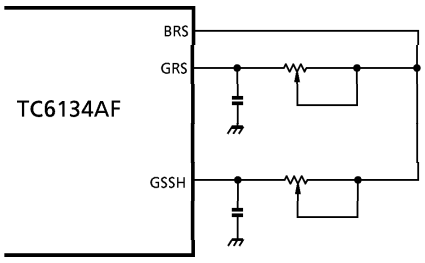
- Connection to synchronization generator IC
  (master clock is except fck)

  If master clock of SG is except fck, it is necessary to lock the phase of an oscillator of SG and TC6134AF.
  Therefore TC6134AF has a divider dividing 2 fck into 1H and an internal phase comparator.

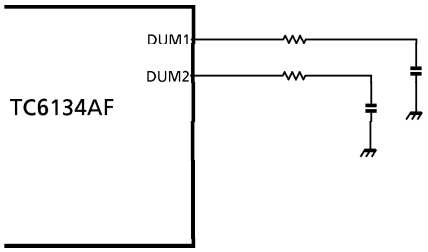


ADJUSTING PHASE OF THE PULSE

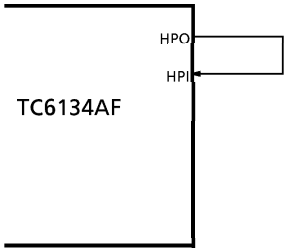
SSH, RS



DEALING WITH DUM1 AND DUM2



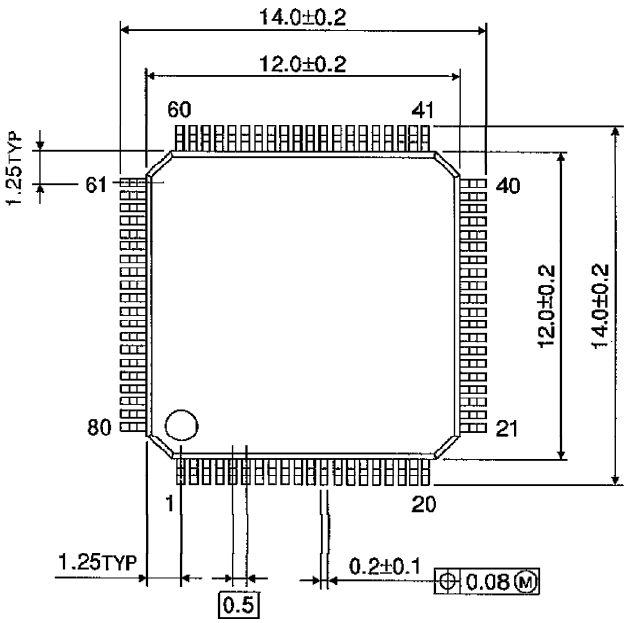
CONNECTING HPO AND HPI

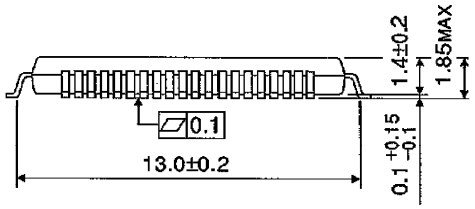


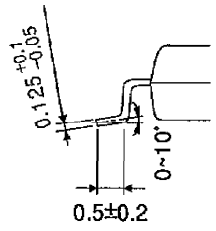
OUTLINE DRAWING

QFP80-P-1212A

Unit : mm







Weight : 0.33g (Typ.)

TC6134AF – 17*
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