

TOSHIBA

TC74AC164P/F/FN/FT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC164P, TC74AC164F, TC74AC164FN, TC74AC164FT

8 - BIT SHIFT REGISTER (S - IN, P - OUT)

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74AC164 is an advanced high speed CMOS 8 - BIT SERIAL - IN PARALLEL - OUT SHIFT REGISTER fabricated with silicon gate and double - layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

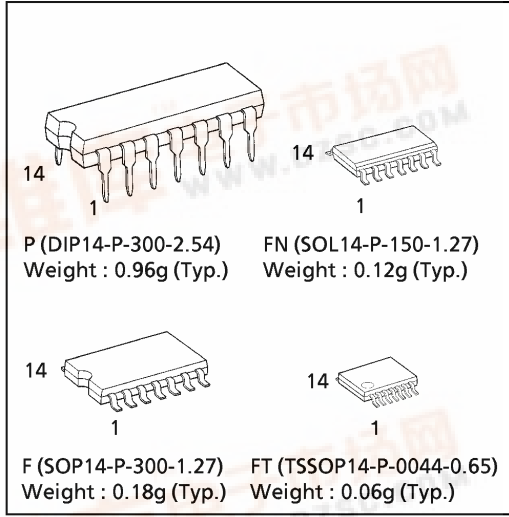
It consists of a serial - in, parallel - out 8 - bit shift register with a CLOCK input and an overriding CLEAR input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

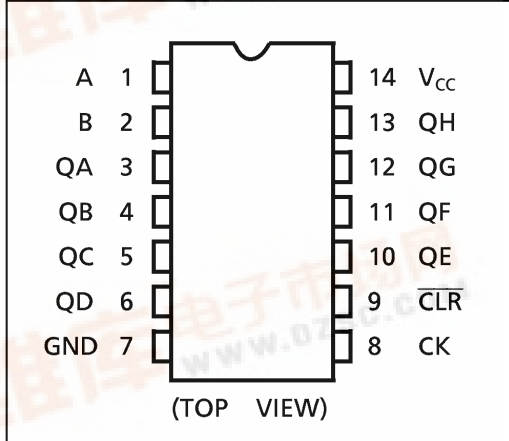
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $f_{MAX} = 170\text{MHz}$ (typ.) at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... V_{CC} (opr) = 2V~5.5V
- Pin and Function Compatible with 74F164



PIN ASSIGNMENT

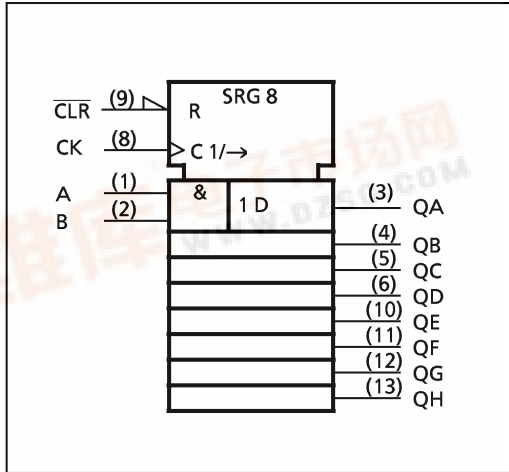


TRUTH TABLE

INPUTS				OUTPUTS			
CLR	CK	SERIAL IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H		X	X	NO CHANGE			
H		L	X	L	QA _n	...	QG _n
H		X	L	L	QA _n	...	QG _n
H		H	H	H	QA _n	...	QG _n

X : Don't Care
 QA_n ~ QG_n : The level of QA ~ QG, respectively, before the most recent positive edge of the clock.

IEC LOGIC SYMBOL

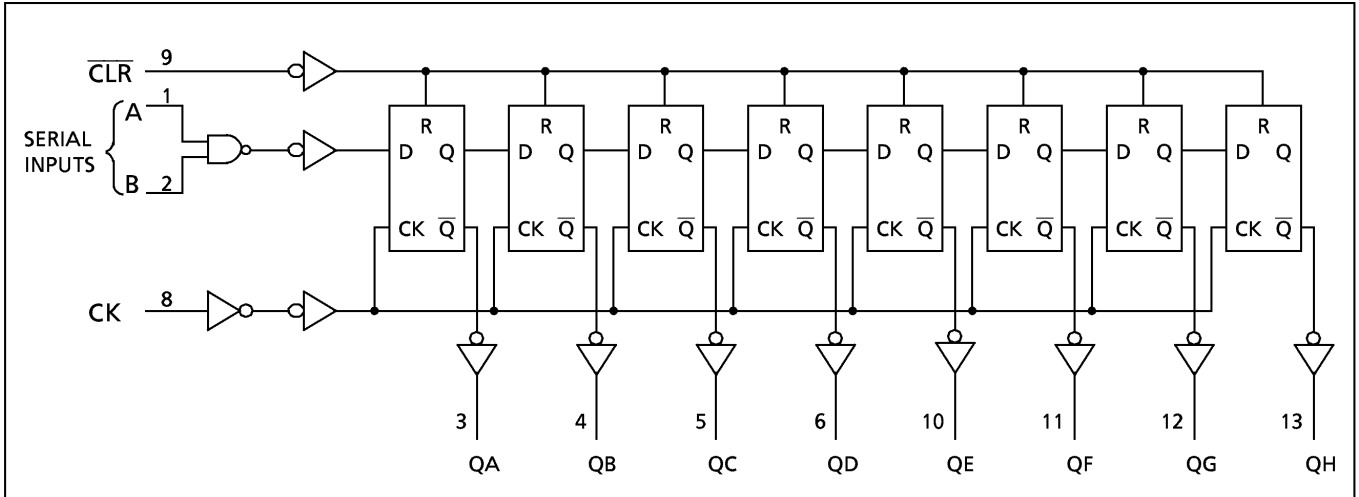


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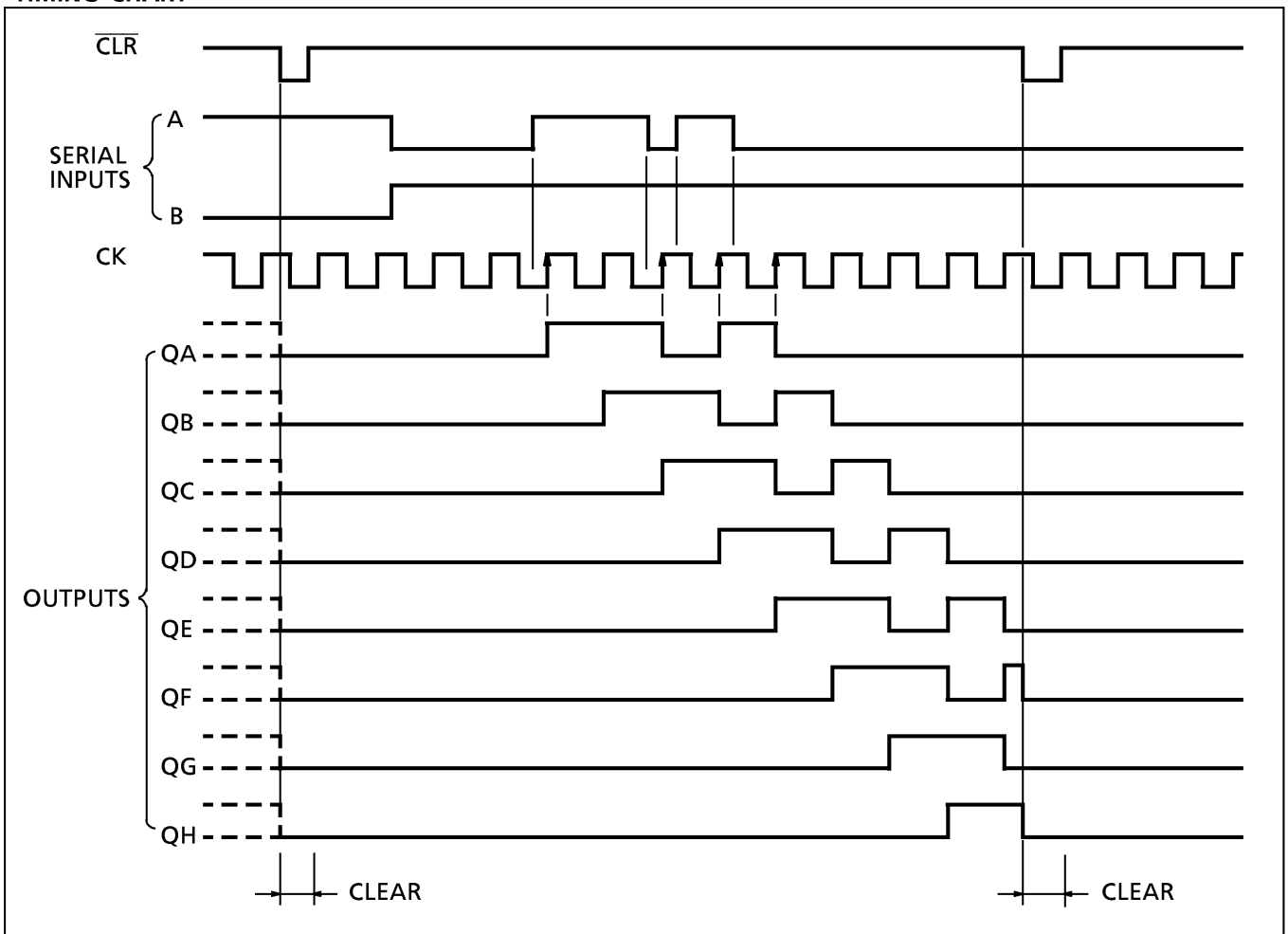
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SYSTEM DIAGRAM



TIMING CHART



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dV	0~ 100 ($V_{CC} = 3.3 \pm 0.3\text{V}$) 0~ 20 ($V_{CC} = 5 \pm 0.5\text{V}$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			3.0	2.10	—	—	2.10	—		
			5.5	3.85	—	—	3.85	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			3.0	—	—	0.90	—	0.90		
			5.5	—	—	1.65	—	1.65		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4\text{mA}$ $I_{OH} = -24\text{mA}$ $I_{OH} = -75\text{mA}^*$	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
5.5	—	—	—	3.85	—					
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 12\text{mA}$ $I_{OL} = 24\text{mA}$ $I_{OL} = 75\text{mA}^*$	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
5.5	—	—	—	—	1.65	—				
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0		

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _W (L) t _W (H)		3.3 ± 0.3	9.0	10.0	ns	
			5.0 ± 0.5	5.0	6.0		
Minimum Pulse Width (\overline{CLR})	t _W (L)		3.3 ± 0.3	9.0	10.0		
			5.0 ± 0.5	5.0	6.0		
Minimum Set-up Time	t _s		3.3 ± 0.3	7.0	7.0		
			5.0 ± 0.5	4.0	4.0		
Minimum Hold Time	t _h		3.3 ± 0.3	1.0	1.0		
			5.0 ± 0.5	1.0	1.0		
Minimum Removal Time (\overline{CLR})	t _{rem}		3.3 ± 0.3	8.5	8.5		
			5.0 ± 0.5	5.0	5.0		

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500 Ω, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	9.6	16.3	1.0	18.6	ns
			5.0 ± 0.5	—	6.6	9.8	1.0	11.2	
Propagation Delay Time (\overline{CLR} -Q)	t _{pHL}		3.3 ± 0.3	—	8.0	15.4	1.0	17.5	ns
			5.0 ± 0.5	—	6.0	11.0	1.0	12.5	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	45	100	—	45	—	MHz
			5.0 ± 0.5	80	150	—	80	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	110	—	—	—	

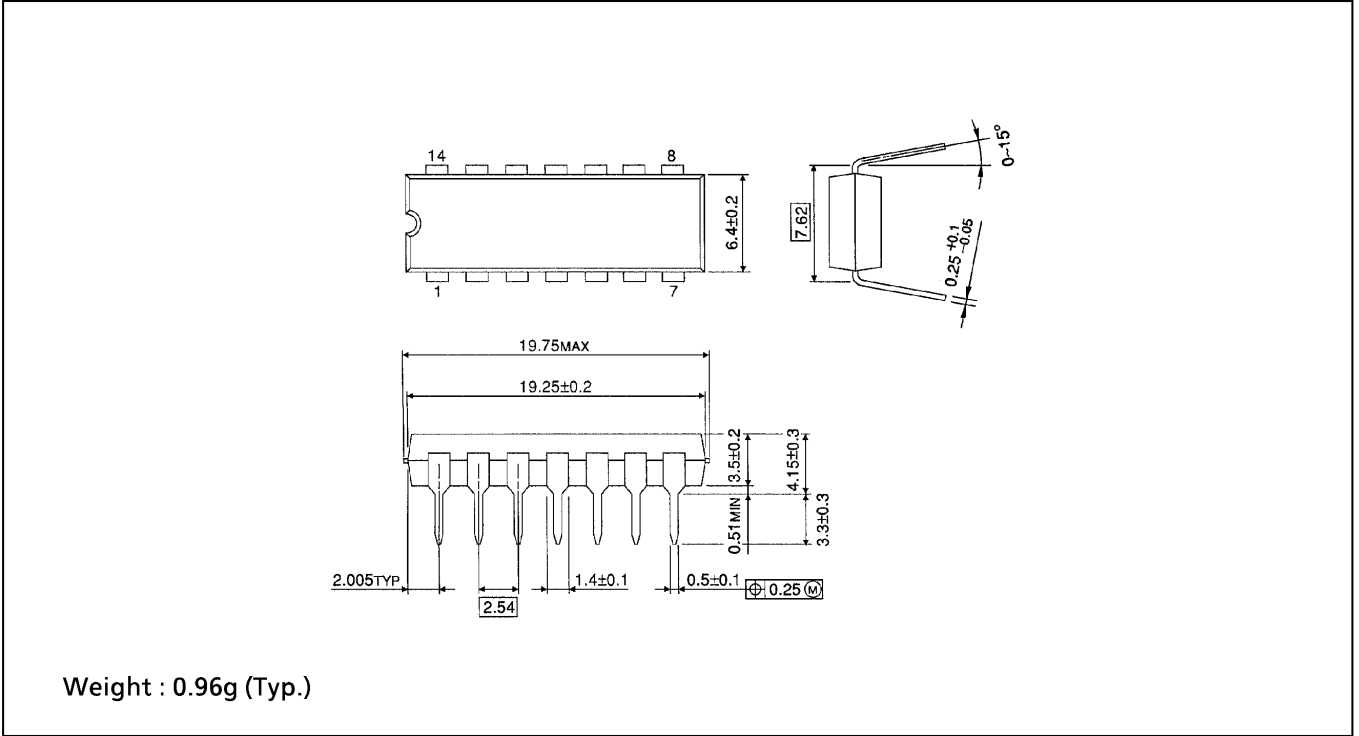
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

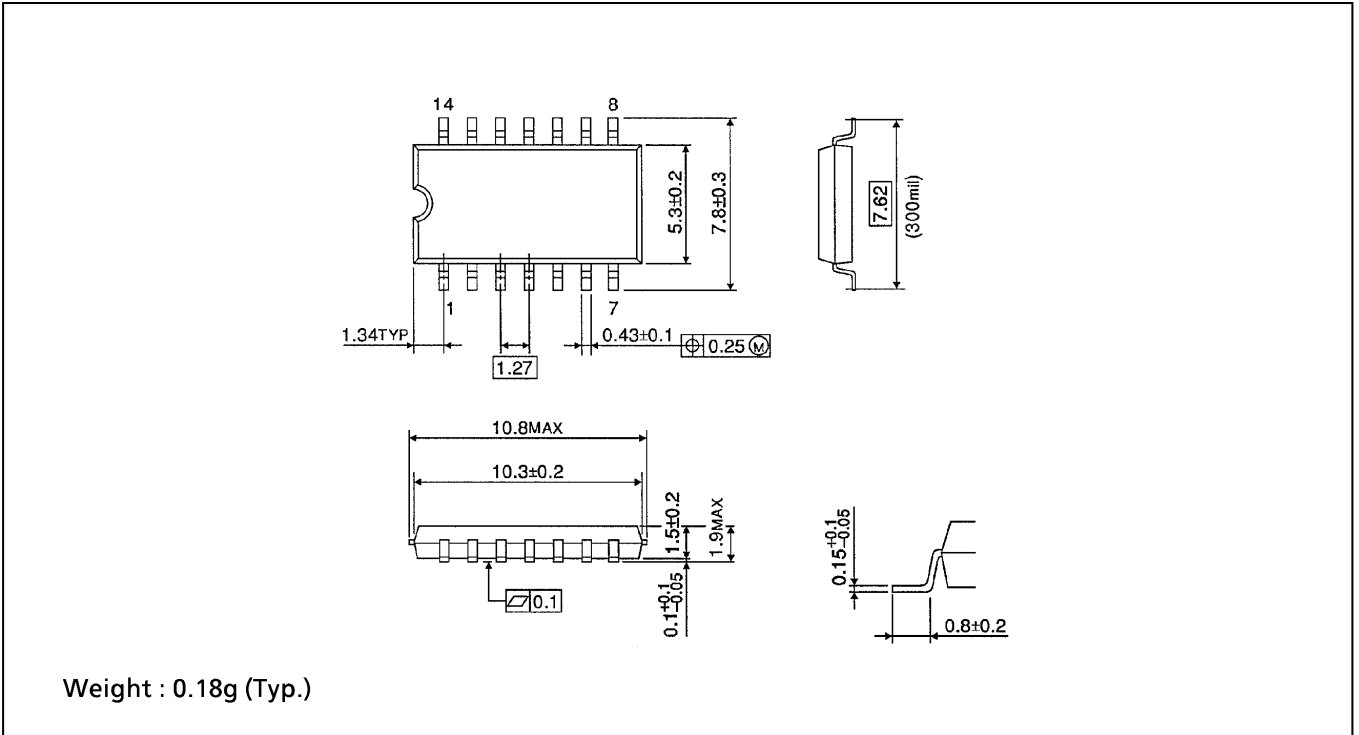
DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

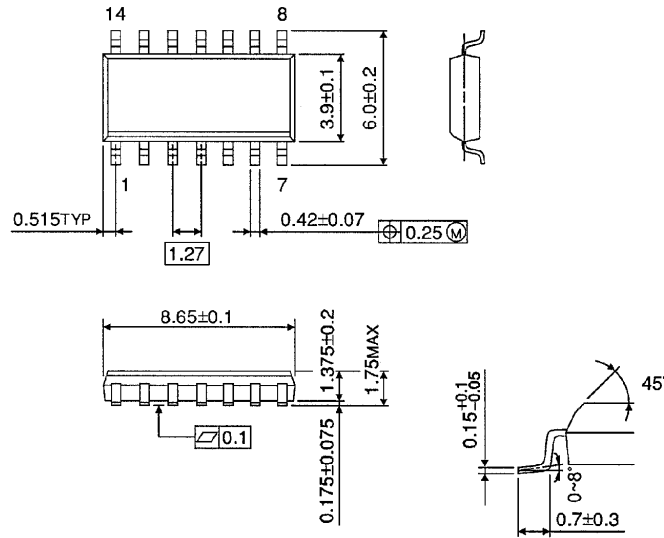
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

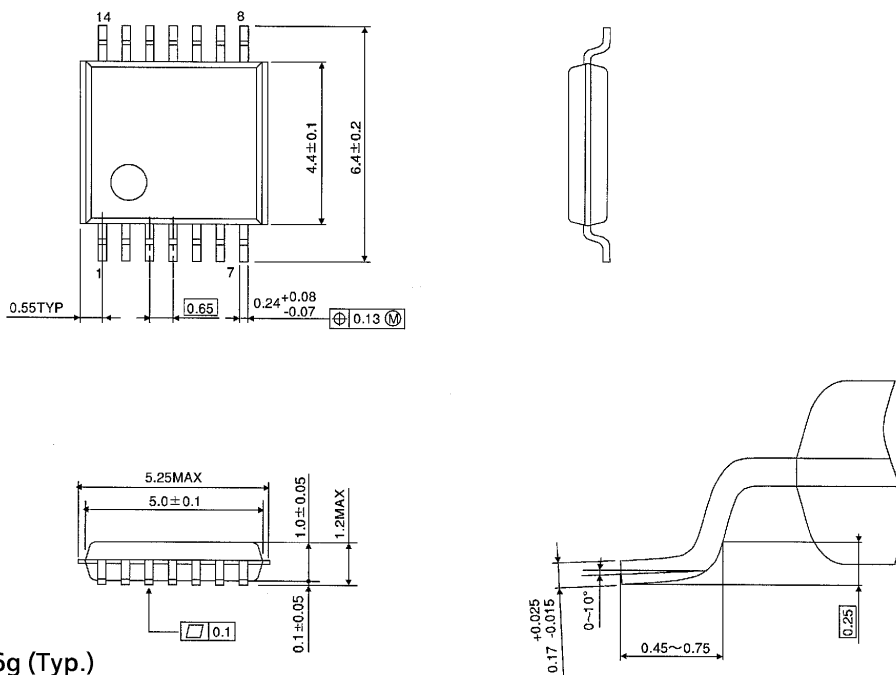
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) OUTLINE DRAWING (TSSOP14-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)