

**TOSHIBA****TC74AC377P/F/FW**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74AC377P, TC74AC377F, TC74AC377FW****OCTAL D - TYPE FLIP - FLOP**

The TC74AC377 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an enable input ( $\bar{G}$ )

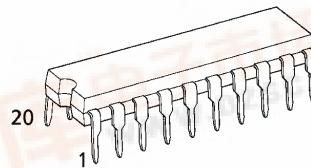
The signal level applied to the D inputs are transferred to Q outputs during the positive going transition of CK.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

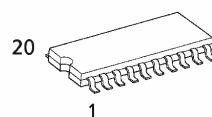
**FEATURES :**

- High Speed .....  $f_{MAX} = 140\text{MHz}(\text{typ.})$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation .....  $I_{CC} = 8\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity .....  $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Symmetrical Output Impedance .....  $|I_{OH}| = |I_{OL}| = 24\text{mA}(\text{Min.})$  Capability of driving  $50\Omega$  transmission lines.
- Balanced Propagation Delays .....  $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range .....  $V_{CC}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F377

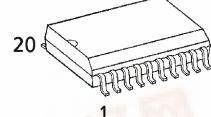
(Note) The JEDEC SOP (FW) is not available in Japan.



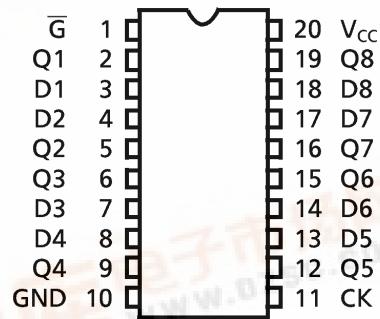
P (DIP20-P-300-2.54A)  
Weight : 1.30g (Typ.)



F (SOP20-P-300-1.27)  
Weight : 0.22g (Typ.)



FW (SOL20-P-300-1.27)  
Weight : 0.46g (Typ.)

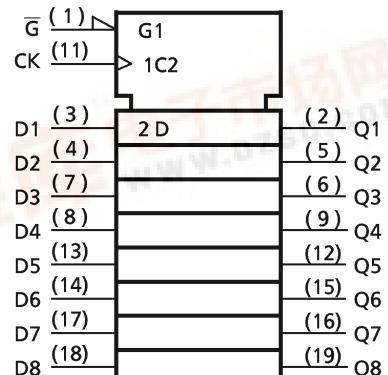
**PIN ASSIGNMENT**

(TOP VIEW)

**TRUTH TABLE**

INPUTS			OUTPUTS
$\bar{G}$	CK	D	Q
H	X	X	NO CHANGE
L	↑	L	L
L	↓	H	H
X	↓	X	NO CHANGE

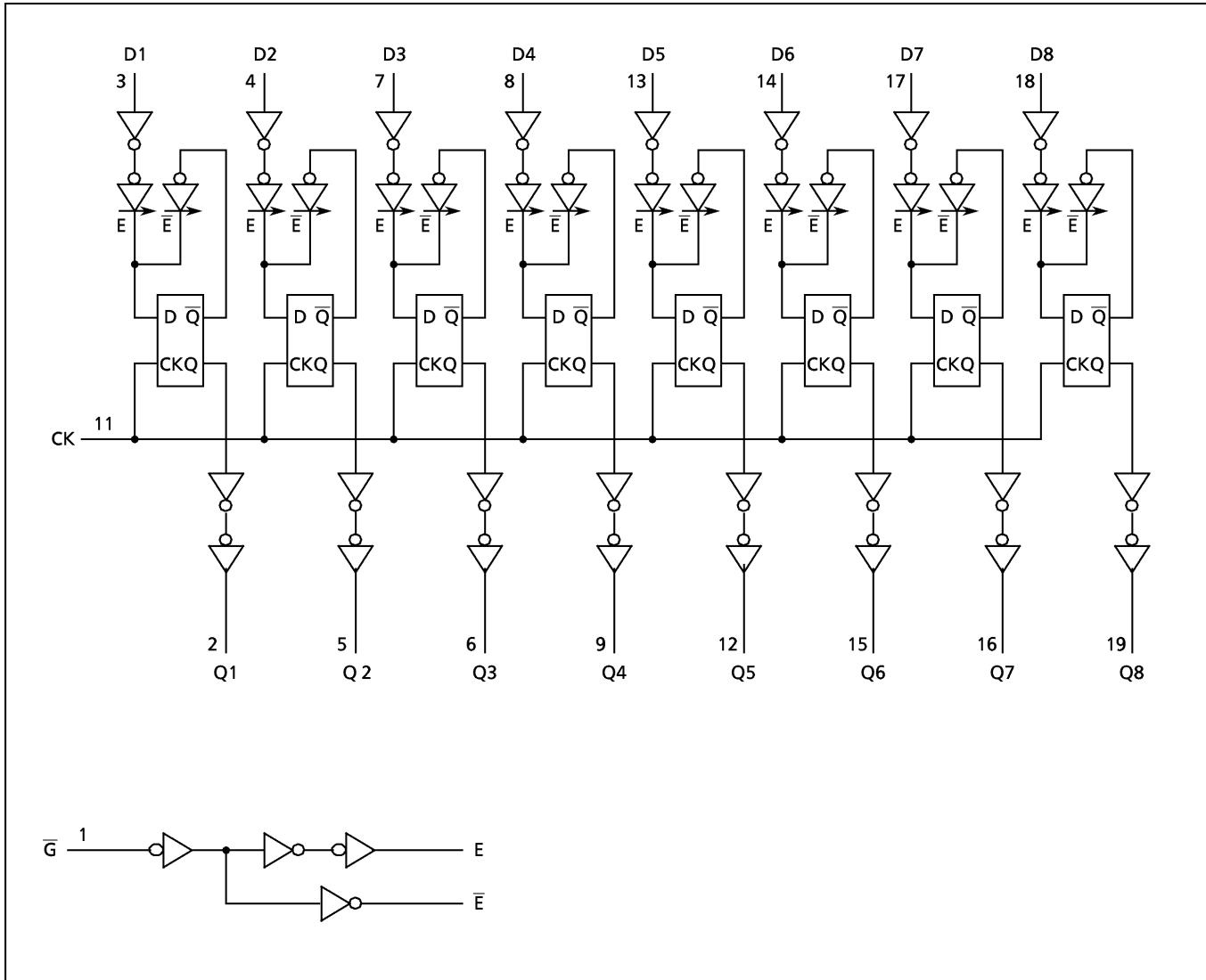
X : Don't Care

**IEC LOGIC SYMBOL**

961001EBA2

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## SYSTEM DIAGRAM



961001EBA2'

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- The information contained herein is subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 50$	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 200$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{STG}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied up to 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{Opr}$	-40~85	°C
Input Rise and Fall Time	$dt/dV$	0~ 100 ( $V_{CC} = 3.3 \pm 0.3\text{V}$ ) 0~ 20 ( $V_{CC} = 5 \pm 0.5\text{V}$ )	ns/V

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V
			3.0	2.10	—	—	2.10	—	
			5.5	3.85	—	—	3.85	—	
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V
			3.0	—	—	0.90	—	0.90	
			5.5	—	—	1.65	—	1.65	
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	—	1.9	V
			$I_{OH} = -4\text{mA}$	3.0	2.9	3.0	—	2.9	
			$I_{OH} = -24\text{mA}$	4.5	4.4	4.5	—	4.4	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0	—	0.0	0.1	—	V
			$I_{OL} = 12\text{mA}$	3.0	—	0.0	0.1	—	
			$I_{OL} = 24\text{mA}$	4.5	—	0.0	0.1	—	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0	

\* : This spec indicates the capability of driving  $50\Omega$  transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS ( Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION		$T_a = 25^\circ\text{C}$	$T_a = -40\text{--}85^\circ\text{C}$	UNIT
			$V_{CC}(\text{V})$	LIMIT	LIMIT	
Minimum Pulse Width ( CK )	$t_W(\text{L})$ $t_W(\text{H})$		$3.3 \pm 0.3$	8.0	8.0	ns
			$5.0 \pm 0.5$	5.0	5.0	
Minimum Set - up Time ( D - CK )	$t_s$		$3.3 \pm 0.3$	8.0	8.0	
			$5.0 \pm 0.5$	4.0	4.0	
Minimum Set - up Time ( $\bar{G}$ - CK )	$t_s$		$3.3 \pm 0.3$	9.0	9.0	
			$5.0 \pm 0.5$	4.0	4.0	
Minimum Hold Time	$t_h$		$3.3 \pm 0.3$	1.0	1.0	
			$5.0 \pm 0.5$	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ , Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION		$T_a = 25^\circ\text{C}$			$T_a = -40\text{--}85^\circ\text{C}$		UNIT
			$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ( CK - Q )	$t_{pLH}$ $t_{pHL}$		$3.3 \pm 0.3$	—	10.6	17.6	1.0	20.0	ns
			$5.0 \pm 0.5$	—	7.4	10.6	1.0	12.0	
Maximum Clock Frequency	$f_{MAX}$		$3.3 \pm 0.3$	50	95	—	50	—	MHz
Input Capacitance	$C_{IN}$			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			—	30	—	—	—	

Note(1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

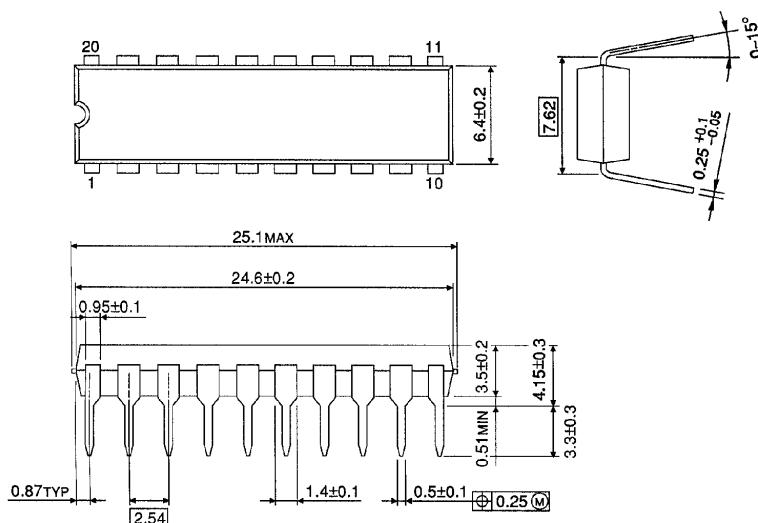
$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total  $C_{PD}$  when n pcs. of Flip Flop operate can be gained by the following equation :

$$C_{PD(\text{total})} = 20 + 10 \cdot n$$

**DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)**

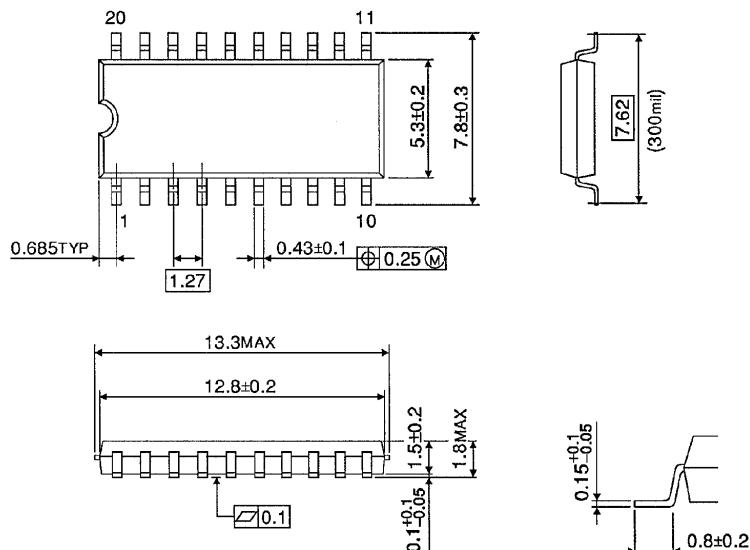
Unit in mm



Weight : 1.30g (Typ.)

**SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)**

Unit in mm

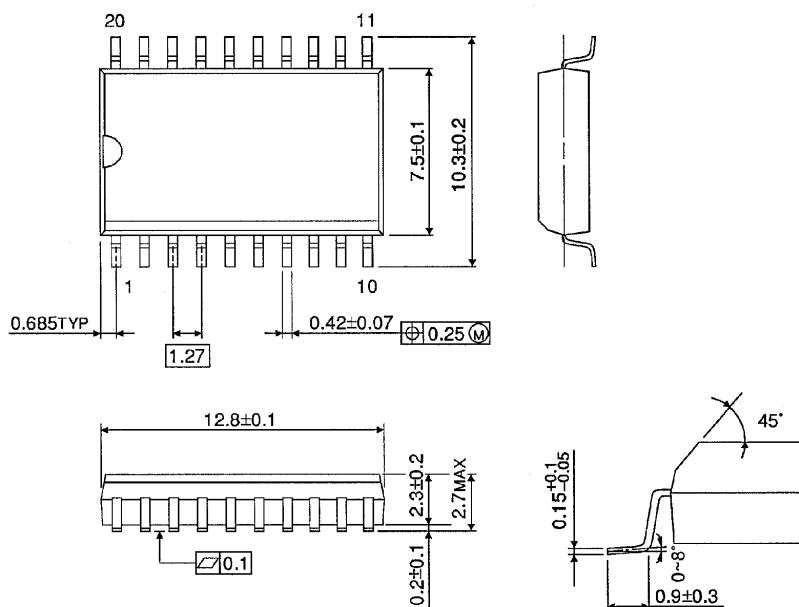


Weight : 0.22g (Typ.)

**SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)